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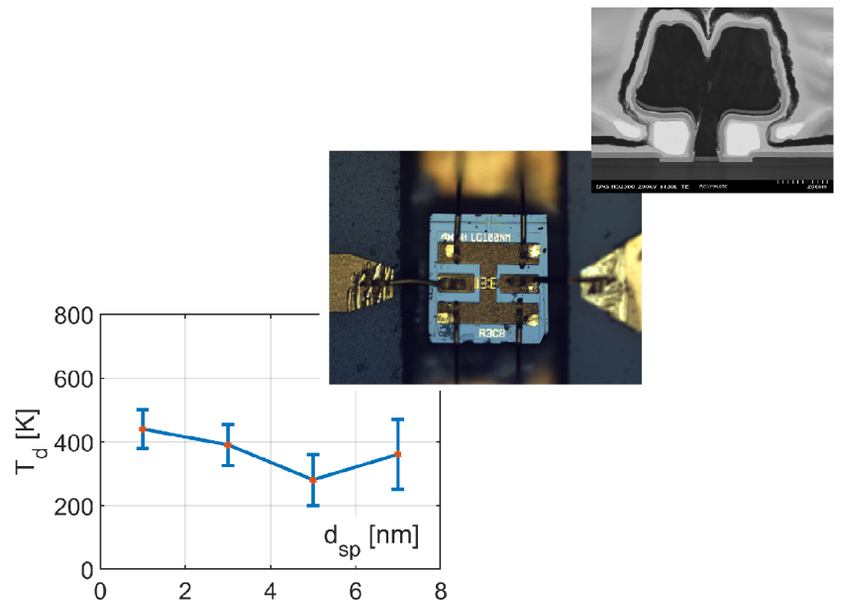
JUNJIE LI • Design and Fabrication ofInP High Electron Mobility Transistors for Cryogenic Low-Noise Amplifiers • 2022



Design and Fabrication of InP High Electron Mobility Transistors for Cryogenic Low-Noise Amplifiers

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CHALMERS UNIVERSITY OF TECHNOLOGY
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THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Design and Fabrication of InP High Electron Mobility Transistors for Cryogenic Low-Noise Amplifiers

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Chalmers University of Technology
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Cover picture: Bottom: The T_d as function of spacer thickness extracted at optimum noise bias for the InP HEMT at 5 K. Middle: InP HEMT mounted in the 4-8 GHz hybrid cryogenic LNA via bond-wires. Top: STEM cross-section of a 100 nm gate-length InP HEMT.

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'If I have seen further it is by standing on the shoulders of giants' - Isaac Newton

'Don't Panic!'
-The Hitchhiker's Guide to the Galaxy

Abstract

High electron mobility transistor (InP HEMT) cryogenic low noise amplifiers (LNAs) have made significant improvements in noise and gain following decades of development. Applications are found from radio astronomy to quantum computing. The noise figure for the best InP HEMT cryogenic LNA, however, is still almost one order of magnitude higher than for a quantum-noise limited amplifier. This motivates further studies to understand the physical mechanisms limiting noise reduction in the InP HEMT. In this thesis, 100-nm gate-length InP HEMTs were developed for probing the intrinsic channel noise in the transistor. Electrochemical etching was found to strongly deteriorate the gate recess etch. This was mitigated by modifying the InP HEMT fabrication scheme to a recess-first process. A comparison of two different device passivation methods, atomic layer deposition of Al_2O_3 and plasma enhanced chemical vapor deposition of Si_xN_y, did not reveal any significant difference in neither gain nor noise for the InP HEMT cryogenic LNA. Channel noise of the InP HEMT was investigated by varying the spacer thickness from 1 to 7 nm in the InAlAs-InGaAs heterostructure. It was found that the optimum spacer thickness was 5 nm for lowest noise temperature in a 4-8 GHz three-stage hybrid LNA at 5 K. This was 2 nm thicker than previously reported spacer thickness used for a similar state-of-the-art InP HEMT cryogenic LNA. The 5 nm spacer InP HEMT LNA minimum average noise temperature was determined to 1.4 K. The channel noise dependence on spacer thickness for the cryogenic InP HEMT was explained by a real-space transfer mechanism associated with the injection of a minor fraction of hot electrons from channel to barrier. Finally, the subthreshold swing of the InP HEMT at 5 K was observed to exhibit a correlation with the noise temperature in the cryogenic LNA. This suggests that the subthreshold swing serves as an indicator of the amount of carrier fluctuations in the InP HEMT channel giving rise to noise.

Keywords: Channel noise, cryogenic, InP HEMT, low-noise amplifier, noise temperature, spacer thickness, subthreshold swing.

List of Publications

This licentiate thesis is based on the following appended publications:

[A] **J. Li**, A. Pourkabirian, J. Bergsten, E. Cha, A. Alexei Kalaboukhov, N. Wadefalk and J. Grahn, "Reduction of Noise Temperature in Cryogenic InP HEMT Low Noise Amplifiers with Increased Spacer Thickness in InAlAs-InGaAs-InP Heterostructures," *Compound Semiconductor Week 2021*, Online, May 9–13, 2021.

[B] **J. Li**, A. Pourkabirian, J. Bergsten, N. Wadefalk and J. Grahn, "Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs", *IEEE Electron Device Letters*, vol. 43, no. 7, pp. 1029-1032, July 2022, DOI: 10.1109/LED.2022.3178613.

[C] **J. Li**, A. Pourkabirian, J. Bergsten, N. Wadefalk and J. Grahn, "On the Relation between rf Noise and Subthreshold Swing in InP HEMTs for cryogenic LNAs," in Proceedings of the *34th Asia-Pacific Microwave Conference*, Yokohama, Japan, November 29 - December 2, 2022.

Other publication not appended in the licentiate thesis:

[D] E. Cha, N. Wadefalk, G. Moschetti, A. Pourkabirian, J Stenarson, **J. Li**, D-H. Kim, and J. Grahn, "InP HEMT Channel Design for Ultra-Low Power Cryogenic Low-Noise Amplifiers", submitted to *IEEE Trans. Electron Devices*, 2022.

Symbols

c	Speed of light in vacuum
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
C_{ds}	Drain-source capacitance
C_{pg}	Gate pad capacitance
C_{pd}	Drain pad capacitance
d_{sp}	Spacer thickness
f	Frequency
f_T	Cut-off frequency
g_m	Transconductance
G_{ds}	Output conductance
G	Gain
k_B	Boltzmann's constant
I_d	Drain current
I_D	Drain current applied to LNA
I_g	Gate current
n_s	Sheet carrier concentration
P_{LNA}	Power consumption
q	Elementary charge
R_c	Contact resistance
R_d	Drain resistance
R_g	Gate resistance
R_i	Intrinsic gate-source resistance
R_j	Intrinsic gate-drain resistance
R_s	Source resistance
R_{sh}	Sheet resistance
SS_{avg}	Average subthreshold swing
T_e	Electron channel temperature
T_d	Drain noise temperature
$T_{e,avg}$	Minimum average noise temperature
T_g	Gate noise temperature
T_{min}	Minimum noise temperature

V_{ds}	Drain voltage
V_{DS}	Drain voltage applied to LNA
V_{gs}	Gate voltage
Φ_{Bn}	Schottky Barrier height
ψ_{bi}	Built-in potential
ΔE_c	Conduction band offset
η	Hot electron fraction
ϵ_s	Dielectric permittivity
μ	Hall electron mobility
ϵ_0	Permittivity of free space
h	Planck's constant

Contents

CHAPTER 1

Introduction

The InP high electron mobility transistor (InP HEMT) has proven to provide the lowest noise figure among all field effect transistors (FETs) at microwave frequencies under 120 GHz [1], [2]. As a result, cryogenic low noise amplifiers (LNAs) equipped with InP HEMTs have been developed and used in the most sensitive detectors such as receivers for radio astronomy, space communication and readout of microwave qubits in quantum computing systems [3]–[5]. Recently, a 4-8 GHz InP HEMT cryogenic LNA with a state-of-the-art minimum average noise temperature $T_{e,avg}$ of 1.3 K was reported [6]. This is nine times higher than the noise temperature for a quantum-noise limited amplifier [7]. Therefore, it appears that there is a potential to reduce the noise in the InP HEMT even further.

The cryogenic InP HEMT is an excellent vehicle for exploring the intrinsic noise properties of the FET. This is due to the small contributions from device parasitic noise sources in the InP HEMT at low temperature. The channel noise in the cryogenic InP HEMT probes the fluctuations of charge carriers in the two-dimensional electron gas (2DEG) for the InAlAs-InGaAs quantum well. Previous work demonstrated that the carrier concentration and the scattering of electrons in the HEMT channel were highly dependent on the

location of the planar doping layer in relation to the heterojunction [8], [9]. Hence by changing the spacer thickness in the InP HEMT, the band diagram and 2DEG are expected to be modified which in turn is essential for the HEMT noise performance. Moreover, to further improve the noise performance of the HEMT, a physical understanding of the noise origin is desirable. The interpretation of the drain noise temperature in the widely used Pospieszalski noise model is often interpreted as a channel noise term [10]. However, the true physical origin of the drain noise temperature is not fully clear.

This thesis is on the design and fabrication of InP HEMTs for cryogenic LNAs. The thesis is organized as follows. The development of the InP HEMT process technology for a high quality gate recess including low gate current is presented in Chapter 2. The improved process allowed the experiment of different epitaxial designs for InP HEMTs to be carried out as reported in Chapter 3. A study has been performed with respect to the spacer thickness in the transistor which controls the location of the doping plane in relation to the quantum well. The key result, *i.e.* the channel noise as a function of spacer thickness, is discussed in detail. It is suggested that the transistor noise is limited by the injection of free electrons from the channel to the barrier in the heterojunction. The subthreshold swing was found to exhibit a correlation with $T_{e,avg}$ in the InP HEMT cryogenic LNAs. Finally, Chapter 4 summarizes the results of this thesis and gives a future outlook.

CHAPTER 2

Process development of InP HEMTs for cryogenic LNAs

2.1 InP HEMT technology

Since the first HEMT was realized by T. Mimura in 1980 [11], the HEMT LNA has found many applications in space communication, sensors and radio astronomy. In 1985, S. Weinreb discovered that the noise temperature of the GaAs HEMT LNA was drastically reduced when cooling the amplifier from room temperature down to a cryogenic temperature around 10 K [12]. The cryogenic HEMT LNA was quickly adopted in receivers requiring highest signal-to-noise ratio [13]. Shortly after introduction, the InAlAs/InGaAs/InP HEMT (*i.e.* the InP HEMT) was demonstrated with excellent microwave noise performance at room temperature [14], and was soon found to perform exceptionally well in cryogenic temperatures as well [15]. The extremely low noise of the InP HEMT can be attributed to the improved transport properties of charge carriers and the reduction of the parasitic resistances in the transistor. However, reported record results for cryogenic LNAs are normally based on InP HEMTs developed for room-temperature applications. In this Chapter, development of the process technology for the InP HEMT targeted specifically for cryogenic LNAs is described.

In this thesis, the InP HEMT was based on an epitaxial stack presented in Fig. 2.1. The layers were grown by an external vendor using molecular beam epitaxy on 3-inch diameter InP substrates [16]. The structure, starting from the InP substrate, consisted of a 500 nm $In_{0.52}Al_{0.48}As$ buffer, an $In_xGa_{1-x}As$ channel and an $In_{0.52}Al_{0.48}As$ layer separated by a Si δ-doped plane. The $In_{0.52}Al_{0.48}As$ spacer layer sandwiched between the doping plane and $In_xGa_{1-x}As$ channel separated the Si dopants from the free electrons in the 2DEG. The thicknesses of the barrier and spacer were adjusted in these investigations, see Section 3.1 for numbers. On top of the barrier, a 4 nm thick InP etch stop layer and a 20 nm n^+ $In_{0.53}Ga_{0.47}As$ cap layer were grown. The InP etch stop layer was introduced to improve etch selectivity between the cap and the barrier, as well as to passivate the traps on the $In_{0.52}Al_{0.48}As$ barrier surface [17].

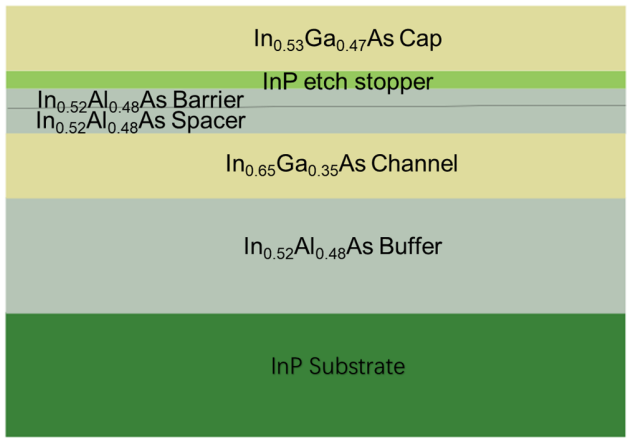

Figure 2.1: Schematic of the epitaxial stack used in InP HEMT fabrication. The Si δ-doping plane is between the InAlAs barrier and spacer layers.

Fig. 2.2 (a) illustrates a schematic of the T-shaped gate InP HEMT. The cross-section scanning transmission electron microscopy (STEM) image in Fig. 2.2 (b) shows a homogeneous lateral gate recess for an InP HEMT with a gate length of 100 nm. The main processing steps were mesa etch, source and drain contact formation, gate contact formation, passivation, pad metallization, air-bridge formation, thinning and dicing [18].

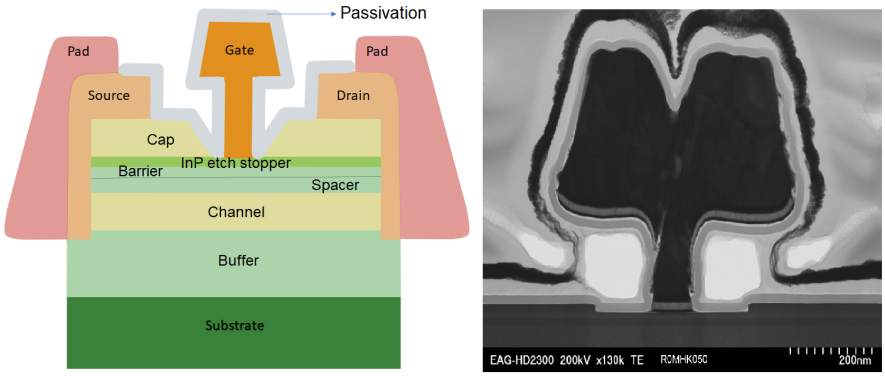

Figure 2.2: (a) Schematic of the processed InP HEMT. (b) Cross-section STEM image of the 100-nm gate-length InP HEMT in the gate region.

2.2 Gate recess formation

The most critical step in HEMT fabrication is the gate recess formation. The reason why the gate recess is critical is that HEMTs are surface-controlled devices: All types of electrical active defects associated with a surface etch process such as the gate recess may end up as non-ideal electrical characteristics for the transistor. This becomes even more severe under cryogenic device operation. The main purpose of the recess etch is to remove the cap layer and create a well-defined gate-to-channel distance. The InP layer here serves as an etch stop layer for the gate recess. In addition, InP electrically passivates the underlying InAlAs barrier surface prone to oxidation and thus creation of surface defects. Another critical dimension is the recess width. It must be wider than the gate foot to ensure that the gate has no contact with the drain and source regions. Moreover, the gate width must be sufficiently large to avoid elevated parasitic capacitances. However, a too wide recess will increase the access resistance of the InP HEMT. In summary, the gate recess formation must be able to provide a constant recess width and depth with low density of surface defects, regardless of HEMT position on the wafer and the material structure in the epitaxial stack.

A traditional wet etch process was here employed in the gate recess formation. The width of the recess was determined by electron beam lithography, etch solution and etch time. The citric acid/H_2O_2 etch solution has been reported to have a high selectivity between InGaAs and InP [19]. The etch mixing ratio and etch time are determined by the relative concentration of acid and oxidizer in the solution. Since H_2O_2 rapidly decomposes into water [20], it is essential to keep track of the H_2O_2 with respect to aging and exposure in air. In this work, best standard practices were established for mixing citric acid and H_2O_2 etch solutions meaning that the gate recess etch conditions were almost identical from run to run.

2.2.1 Recess-first InP HEMT process

In the standard InP HEMT process, the source and drain ohmic contact formation is defined prior to the gate recess etch, see Fig. 2.3(a). This process flow is here denoted as the recess-last method. After a homogeneous gate recess is formed, the gate metal stack of Pt/Ti/Pt/Au can be deposited to form the T-shaped gate contact.

During inspection of the InP HEMTs fabricated in this thesis work, it was observed that the recess surface ended up very uneven for many devices. An example is given in Fig. 2.4. In Fig. 2.4(a), a top-view scanning electron microscopy (SEM) photo illustrates that the recess in the center is different from the recess at the edge. This will cause a poor Schottky contact as demonstrated in the cross-section in Fig. 2.4(b).

A similar gate recess etch problem was noted for HEMTs based on variations in the underlying epitaxial stack. Fig. 2.5(a) presents top-view SEM images of the recess region using an identical recess etch procedure for HEMTs with In channel content varying from 53% to 70%. The recess width measured by SEM is plotted in Fig. 2.6 (blue line). The recess width exhibits an unexpected variation of more than a factor of two as a function of In channel content. This observation together with the unexpected erosion shown in Fig. 2.5 indicated an abnormal etching occurring for the traditional recess-last method.

A plausible explanation of the abnormal gate recess etch behavior is electrochemical etching in the semiconductor layers adjacent to the pre-deposited metal [21]. An electrochemical potential is established between two different materials exposed to an electrolytic solution. The electrochemical reaction accelerates the oxidation of the semiconductor surface in the periphery of metals

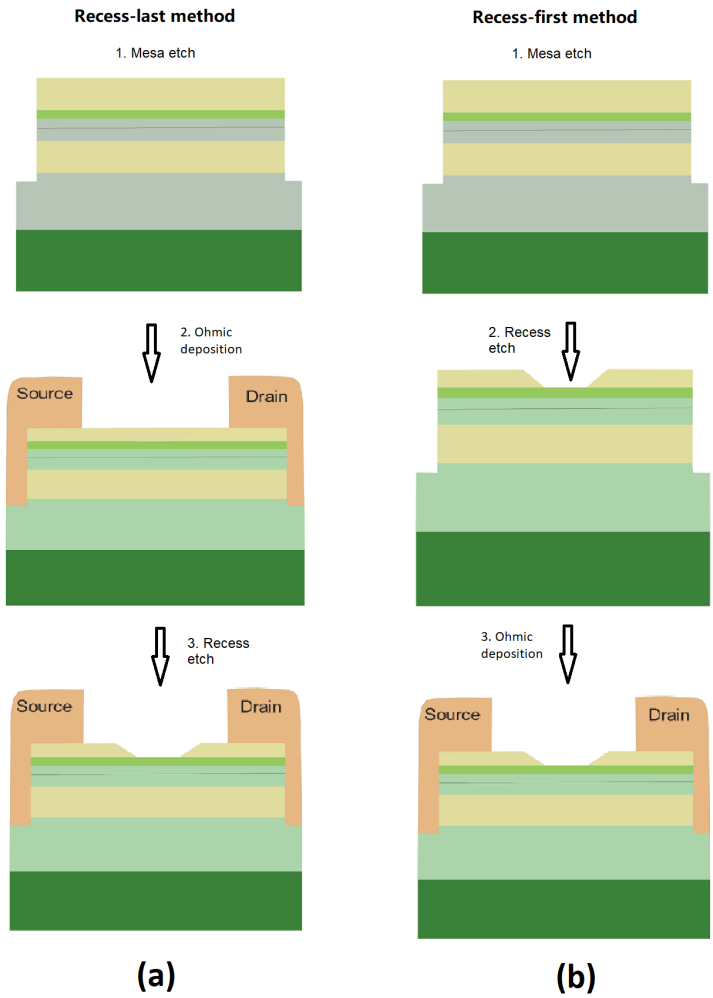

Figure 2.3: (a) Recess-last and (b) recess-first process flow schematically illustrating the order of the ohmic deposition and the gate recess.

even in the presence of deionized water [22]. Evidence has been presented in the literature that electrochemical etching affects the wet-chemical processing of GaAs and related compound semiconductors [23]. The different work func-

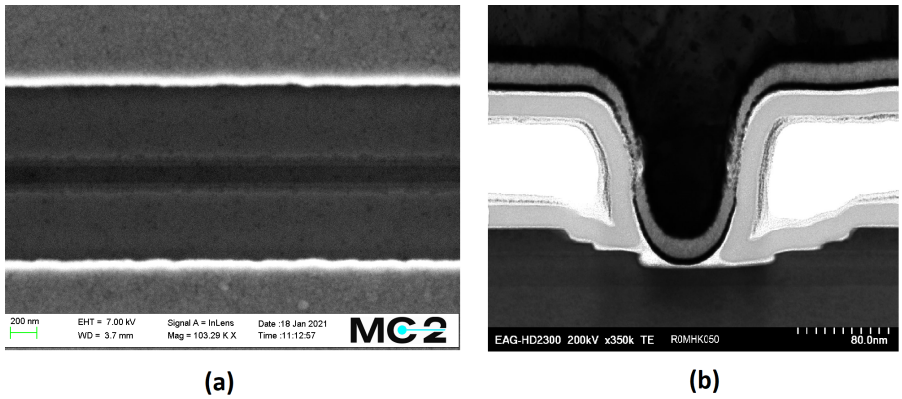

Figure 2.4: (a) Top-view SEM and (b) cross-section STEM image of the abnormal gate recess.

tion between the metal and semiconductor will result in different etch rates and selectivities of the semiconductors [24]. The lateral and vertical etch rates of InAlAs and InGaAs with Ni/Pt surface metal in a non-alloyed ohmic electrode was reported to strongly deviate from the etch rate of the bulk without metal. The deviation was attributed to electrochemical etching [23]. This also seems to apply for the InP HEMTs here using alloyed metal deposition immersed in citric acid etch solution. Therefore, it will be difficult to adjust the etch solution to achieve the required control of lateral and vertical gate recess distances by the recess-last method. In particular, this becomes problematic when processing different epitaxial layers in the same InP HEMT batch.

To alleviate the detrimental effect from electrochemical etching, the InP HEMT fabrication was modified according to the process flow shown in Fig. 2.3(b). The gate recess was etched prior to the ohmic deposition and annealing. The method is here denoted recess-first as opposed to the standard recess-last method illustrated in Fig. 2.3(a). The SEM images for the recess-first method using different In channel content are shown in Fig. 2.5(b). In Fig. 2.6, it is observed that the measured recess width (red line) is substantially more stable for the recess-first method compared with the recess-last process (blue line). However, the recess-first method will sacrifice the accurate alignment between the gate recess and gate metal. This can be compensated by using more alignment marks for the electron beam lithography step. Since

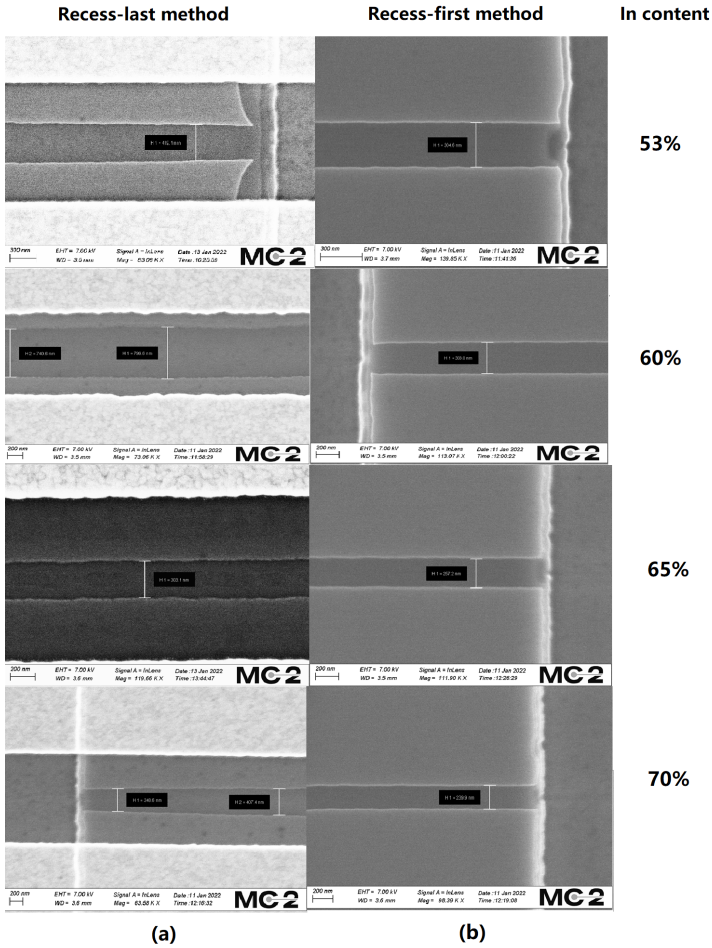

Figure 2.5: Top-view SEM images after gate recess etch using (a) recess-last and (b) recess-first method. In channel content from top to bottom is 53%, 60%, 65% and 70%. Gate recess etch process identical for all samples.

stability in device dimensions between different InP HEMT chips was very important in this research work, the recess-first method was used for device fabrication.

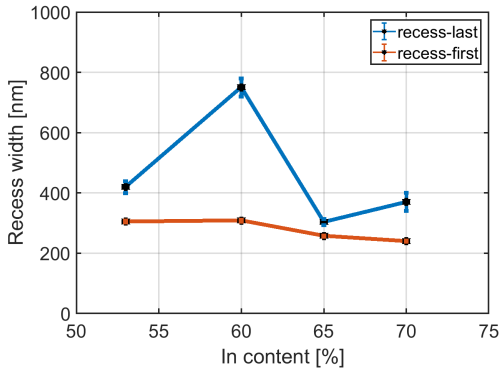

Figure 2.6: The measured gate recess width from Fig. 2.5 versus In channel content for recess-last (blue) and recess-first (red) method.

2.3 Influence of the passivation

After the gate recess etch, the exposed surface contains many defects which may affect the electric performance of the InP HEMT. The InP etch stop layer serves as the passivation for InAlAs barrier layer which helps to eliminate the well-known kink effect in the output drain current when measured under cryogenic conditions [17]. InP is much less reactive than InAlAs. Nonetheless, defects and contaminants may still exist on the surface after processing the InP HEMT. This makes passivation using a dielectric thin film deposition necessary for long-term stability and to prevent contamination of the recess surface. The conventional passivation is either Si_xN_y by plasma enhanced chemical vapor deposition (PECVD) or Al_2O_3 by atomic layer deposition (ALD). However, the passivation itself may introduce problems. Fig. 2.7 shows the undesirable increase in gate current I_g caused by passivation using either PECVD Si_xN_y or ALD Al_2O_3. Such enhancement in I_g is detrimental for the noise of the InP HEMT LNA, in particular for lower frequencies of a few GHz [25], [26].

The increase of the I_g by a factor of ten following passivation appeared for both PECVD and ALD regardless of dielectric; See Fig. 2.7. Gate leakage related to the thermal nature by the depositions was excluded. Experimentally, this was confirmed by exposing the devices in the PECVD chamber at 300°C without depositing Si_xN_y. No increase in I_g was recorded. Al_2O_3 can

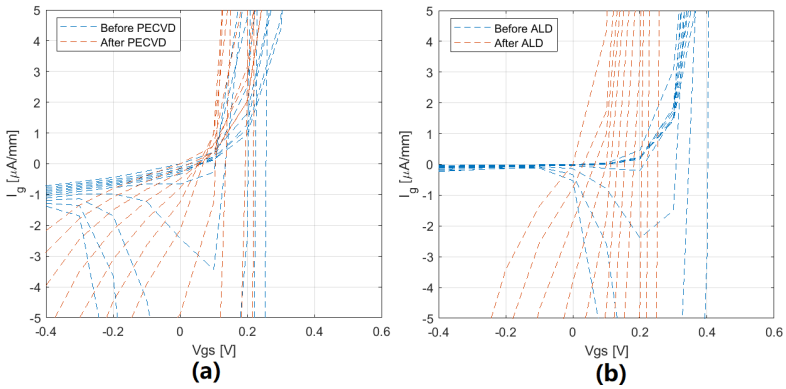

Figure 2.7: Gate current versus gate voltage at 300 K for 2 x 100 μm-width, 100 nm-length InP HEMTs before (blue) and after (red) passivation of (a) PECVD Si_xN_y and (b) ALD Al_2O_3. Drain voltage is 0 - 1 V with steps of 0.1 V.

be easily removed by hydrofluoric acid (HF). The I_g for Al_2O_3 passivated InP HEMTs recovered to the same low level as before passivation after removing the Al_2O_3.

Based on these observations, the I_g increase was deduced to unwanted residuals on the surface prior to the passivation. This could potentially aggravate electrically-active defects and create current paths between gate and channel during passivation. Indeed, it has previously been observed by photoluminescence that interfacial defects are induced on the InP surface by the dielectric depending on the surface treatment before the deposition [27]. Therefore, an oxygen plasma cleaning with 50 W power for 20 s at room temperature was introduced before the passivation. Fig. 2.8(a) confirms that the I_g decreased more than ten times for both Al_2O_3 and Si_xN_y passivation compared with no plasma cleaning at 300 K (Fig. 2.7). The I_g will be even lower at 5 K as depicted in Fig. 2.9(a). The atomic force microscopy (AFM) inspection shown in Fig. 2.10 provides further evidence of the cleaner recess surface following oxygen plasma cleaning.

However, the plasma ashing will create surface traps in the recess area. This can be seen from the kink effect in the output curves at cryogenic temperature as shown in Fig. 2.9(b). The kink effect occurs only at high gate bias (above $V_{gs} = 0.6$ V) which is far from the low-noise bias used for the LNA (around

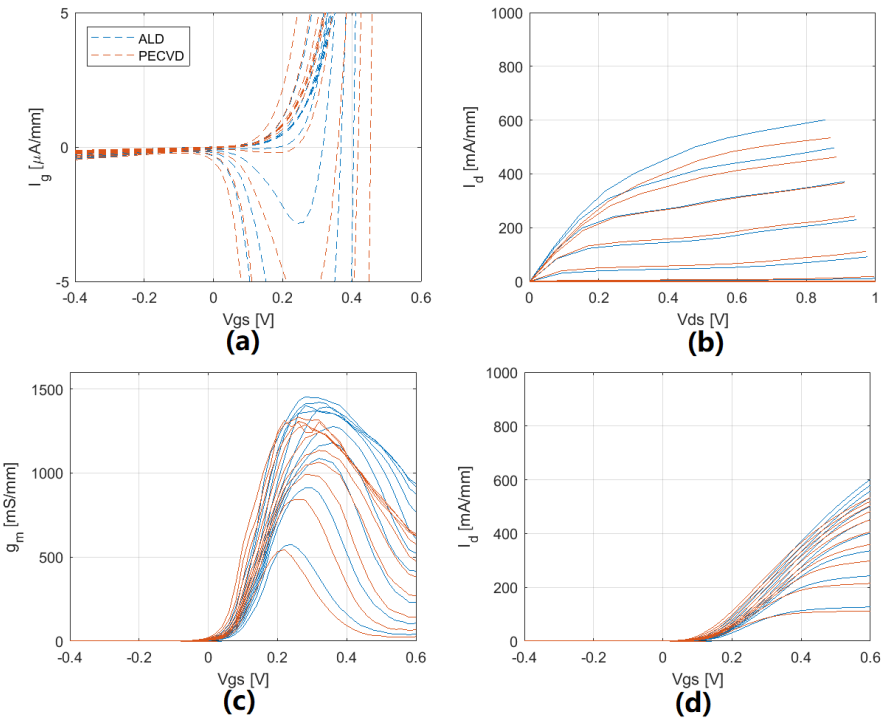

Figure 2.8: dc characterization of 4 x 50 μm InP HEMTs at 300 K using passivation of PECVD Si_xN_y (red) and ALD Al_2O_3 (blue) with a plasma cleaning process. (a) Gate current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (b) Drain current versus drain voltage, with gate voltage -0.4 - 0.6 V in steps of 0.1 V. (c) Transconductance versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (d) Drain current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V.

$V_{gs} = 0.2$ V). In order to mitigate the undesired kink phenomenon, the oxygen plasma process can be replaced by a wet cleaning step using a remover solution.

Figs. 2.8(b) and (c) show slightly higher current driving ability and transconductance g_m for the InP HEMTs with ALD Al_2O_3 at 300 K than for the InP HEMT with PECVD Si_xN_y. In contrast, the current driving ability and g_m become very similar at 5 K; See Figs. 2.9(b) and (c). The threshold voltage V_{th} is almost identical for both passivations at 300 K and 5 K as demonstrated

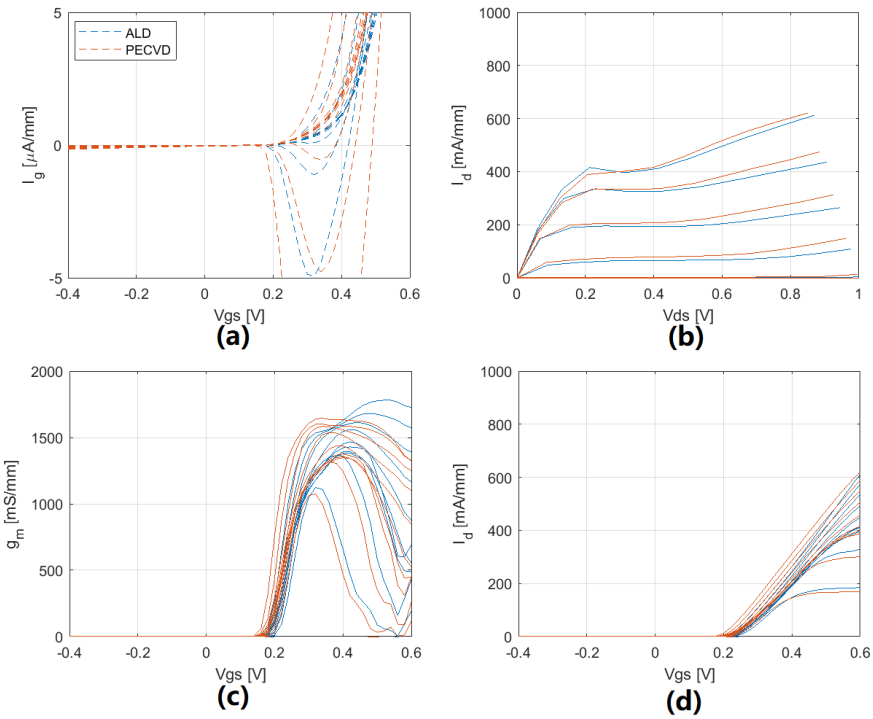

Figure 2.9: dc characterisation of 4 x 50 μm InP HEMTs at 5 K using passivation of PECVD Si_xN_y (blue) and ALD Al_2O_3 (red). (a) Gate current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (b) Drain current versus drain voltage, with gate voltage -0.4 - 0.6 V in steps of 0.1 V. (c) Transconductance versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (d) Drain current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V.

in Fig. 2.8(d) and Fig. 2.9(d). Fig. 2.11 presents the noise and gain of 4-8 GHz LNAs at 5 K equipped with the transistors using either ALD Al_2O_3 or PECVD Si_xN_y. The average gain is 46 dB for both LNAs. The $T_{e,avg}$ is 1.2 K for ALD Al_2O_3-based LNA and 1.3 K for the PECVD Si_xN_y-based LNA. It is concluded that no significant difference with respect to noise and gain in the cryogenic LNA is seen for the two investigated methods used in passivation of the InP HEMT. The better suppression of the kink effect by ALD Al_2O_3 than

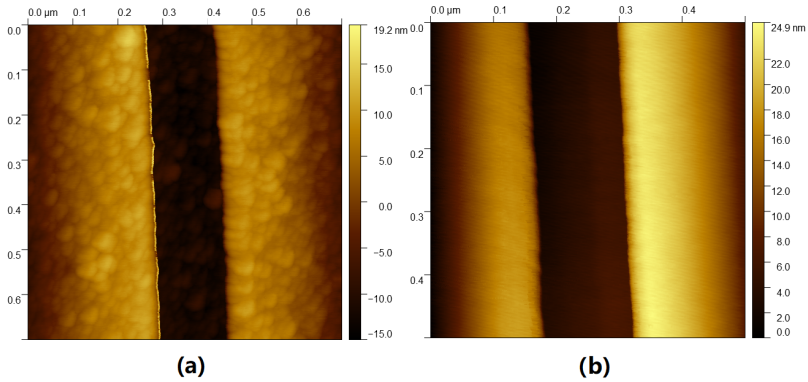

Figure 2.10: AFM images of the gate recess (a) before and (b) after oxygen plasma cleaning. Courtesy of Johan Bergsten.

for the PECVD Si_xN_y reported previously was not observed here [28]. This may be due to the usage of an InP etch stop layer in this thesis work. Such an InP layer will serve as a strong passivation for the InAlAs surface and thus change the conditions for the subsequent dielectric deposition.

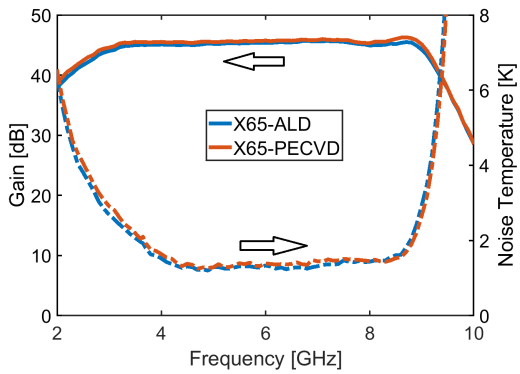

Figure 2.11: The measured gain (solid) and noise temperature (dashed) of a three-stage 4-8 GHz hybrid LNAs integrated with InP HEMT passivated by PECVD Si_xN_y (red) and ALD Al_2O_3 (blue). $V_D = 0.7$ V, $I_D = 15$ mA at 5 K.

CHAPTER 3

Investigation of InP HEMT Spacer Thickness

This thesis aims to gain a better understanding of how small changes in the 2DEG of the InP HEMT channel correlates with its high-frequency noise properties. In the case of a cryogenic InP HEMT, the intrinsic channel noise dominates the total noise contribution. This channel noise can be indirectly measured by using an InP HEMT cryogenic LNA. Since the channel noise is expected to vary with the heterostructure of the InP HEMT [29], the dc properties (associated with the 2DEG) of the device can be coupled with its intrinsic noise behavior.

The spacer is one of the key features that makes the InP HEMT superior with respect to the transport of charge carriers, *i.e.* the free electrons in the channel. The spacer separates the doping impurities from the 2DEG. For a given quantum well heterostructure, the spacer thickness and the amount of dopants determine the number of free electrons forming the 2DEG in the HEMT. The carrier concentration and associated scattering of electrons have been reported to depend on the choice of spacer thickness [8], [9]. It is therefore evident that optimization of spacer thickness is also needed for the InP HEMT noise performance. Prior to this licentiate thesis, such an optimization had not been carried out for InP HEMTs aimed for cryogenic LNAs.

Since variation in the spacer thickness introduces a minimum amount of modifications in the heterostructure, the optimization of the spacer thickness may provide information on the impact of device noise from the 2DEG itself without taking material imperfections such as increased lattice strain or defect density into account. Moreover, for the InP HEMT at cryogenic temperature, a proper noise measurement will mainly record the intrinsic nature of electron fluctuations in the transistor and not by the parasitic noise sources. This may reveal new insights into the noise mechanisms in the channel of the InP HEMT.

In this chapter, the optimization of the spacer thickness in the InP HEMT with respect to noise in a cryogenic LNA is described. The LNA was designed in 4-8 GHz based on 4×50-μm InP HEMT. The transistor technology was a 100-nm gate-length InP HEMT with 15 nm 65% In channel using the recess-last process and ALD Al_2O_3 passivation described in Chapter 2. The results suggest that the noise in the channel is limited by injection of a small fraction of electrons from channel to barrier. Finally, the observed correspondence between the subthreshold swing and the noise temperature in the InP HEMT cryogenic LNA is described.

3.1 Epitaxial design

The experiment was based on variations in the epitaxial structure for the InP HEMTs. Four epitaxial structures with variation of spacer thickness d_{sp} of 1, 3, 5 and 7 nm were designed; See epitaxial structure in Fig. 2.1 and descriptions in Chapter 2. A one-dimensional self-consistent Poisson-Schrödinger solver was used to simulate the heterostructures at 300 K and 5 K [30]. The simulation showed that the 2DEG could be made very similar in the structures where the total thickness of the barrier and spacer layer was kept constant at a value of 9 nm as illustrated in Table. 3.1. The δ doping level was adjusted with the intention to keep the sheet carrier concentration n_s constant for all samples, 2.5×10^{12} cm^{-2} at 300 K.

Table 3.1: The spacer and barrier thickness of the investigated structures.

Spacer (nm)	*Barrier* (nm)
1	8
3	6
5	4
7	2

3.2 Hall measurements

To evaluate the transport properties of the channel electrons, Hall bars were fabricated for the various epitaxial structures shown in Fig. 3.1. The heavily doped cap layer was absent in these measurements. Hall measurements were conducted in a magnetic field of 1 T from 300 K to 5 K. The Hall electron mobility μ, sheet resistivity R_{sh}, and n_s are plotted in Fig. 3.2. In Fig. 3.2(a), μ is observed to increase steeply with reduced temperature and flatten out below 50 K. In this region, the difference in mobility between $d_{sp} = 5$ (and 7) nm and $d_{sp} = 1$ nm is almost a factor of 3. The strong dependence of mobility on the spacer thickness at 5 K is due to various degree of scattering in the channel electrons caused by different d_{sp}. In contrast, at 300 K, the mobility was almost similar showing typical μ between 9,500 and 14,000 cm^2/Vs. The difference in mobility is reflected in R_{sh} behavior with temperature plotted in Fig. 3.2(b). Finally, it is seen in Fig. 3.2(c) that n_s showed only a $\pm 10\%$ dependence on spacer thickness with no temperature variation. The data in Fig. 3.2 demonstrated that the epitaxial materials used for InP HEMT experiments in this thesis was of high quality and showed expected differences with respect to d_{sp}.

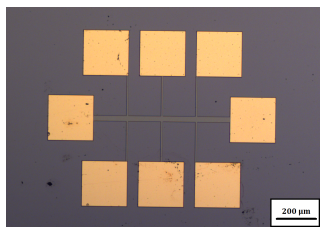

Figure 3.1: Picture of the Hall bar structure.

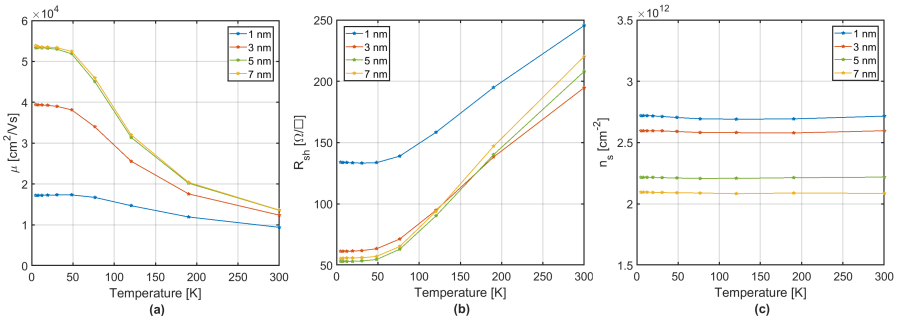

Figure 3.2: The (a) μ, (b) R_{sh} and (c) n_s of the epitaxial structures with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow).

3.3 dc and rf characterization

The dc and rf properties of InP HEMTs with epitaxial structures described in Section 3.1 were characterized on-wafer at 5 K. In Fig. 3.3, the output $I - V$ curves are presented for different overdrive voltages $V_{OV} = V_{gs} - V_{th}$ [6]. The maximum drain current level at $V_{ds} = 0.8$ V with an V_{OV} of 0.7 V is around 900 mA/mm at 5 K for all InP HEMTs but for $d_{sp} = 1$ nm. The latter was due to its lower μ; See Fig. 3.2(a).

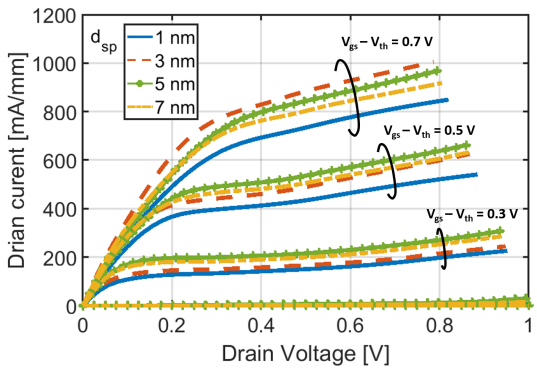

Figure 3.3: Drain current of the InP HEMTs with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. [From Paper B]

The g_m of the InP HEMTs with different d_{sp} in Fig. 3.4 illustrates that the InP HEMT with $d_{sp} = 3$ nm possesses the highest peak transconductance at 5 K. This is consistent with its higher current driving capability at elevated drain and gate bias as shown in Fig. 3.3. The variation in V_{th} can be seen in Fig. 3.4. V_{th} is known to depend both on the barrier thickness x_d and doping concentration n_D [8]:

$$V_{th} \approx \phi_{Bn} - \frac{qn_D x_b}{\varepsilon_s} - \frac{\Delta E_c}{q}, \tag{3.1}$$

where q is the electron charge, ε_s is the dielectric permittivity for InAlAs, ϕ_{Bn} is the Schottky barrier height and ΔE_c is the conduction band offset. The decrease of the barrier shifts the V_{th} positively whereas the increase of the doping concentration shifts the V_{th} negatively [31]. As a result, V_{th} as a function of d_{sp}, plotted in Fig. 3.5, experiences a maximum around 0.1 V at 5 nm. This makes the cryogenic InP HEMT an enhancement mode (normally-off) FET for $d_{sp} = 5$ nm.

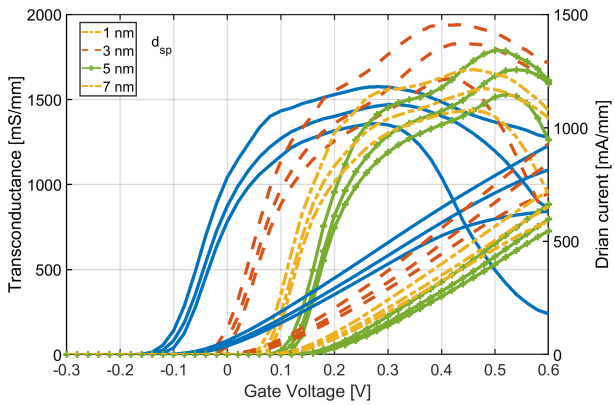

Figure 3.4: The transconductance (left) and drain current (right) of the InP HEMT with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. $V_{ds} = 0.4$ - 0.8 V with step of 0.2 V.

Elevated I_g in the InP HEMT will increase the noise level and obscure the intrinsic channel fluctuations, in particular when using a low-frequency LNA design. The gate current plotted in Fig. 3.6 indicates that the I_g for all the InP HEMTs was below 0.1 μA/mm at the expected gate voltage for lowest noise

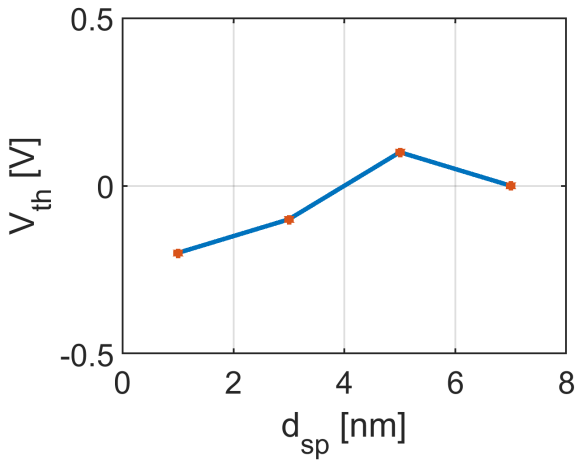

Figure 3.5: Threshold voltage V_{th} as a function of d_{sp} at 5 K.

[32]. Such a very low gate current level confirmed the successful development of the low-noise cryogenic InP HEMT given in Chapter 2. Hence the I_g of the devices is not expected to present problems in the noise extraction procedures described in next section.

The comparison of S-parameters up to 50 GHz for the InP HEMTs with different d_{sp} is demonstrated in Figs. 3.7 and 3.8. The S-parameters are measured at 5 K at a bias of I_d=5 mA and V_{ds}=0.475 V which is the estimated optimum noise bias using the indicator $\sqrt{I_{ds}}/g_m$ [13]. The input and output reflection coefficients S_{11} and S_{22} are very similar for all the devices. The gain S_{21} of InP HEMTs with $d_{sp} = 5$ and 7 nm are slightly higher than $d_{sp} = 1$ and 3 nm due to their higher intrinsic g_m. Overall, the rf measurements indicated that all InP HEMTs did not show signs of any oscillation behavior at their optimum noise bias points.

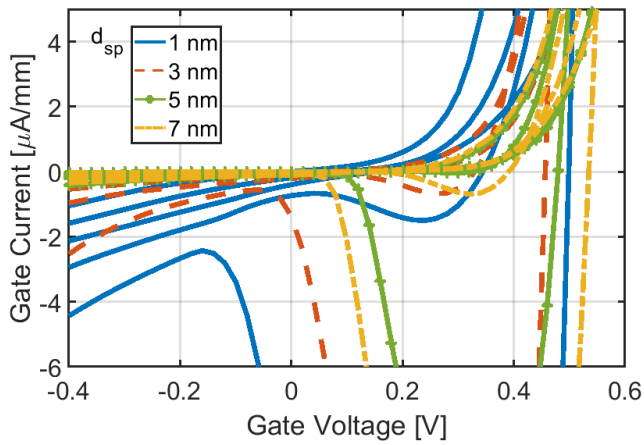

Figure 3.6: Gate current of the InP HEMTs with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. $V_{ds} = 0 - 1$ V in steps of 0.25 V.

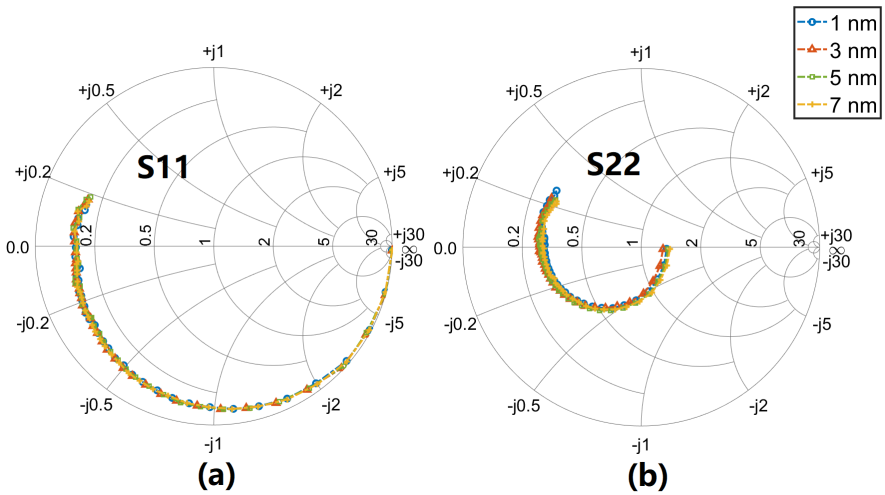

Figure 3.7: The (a) S_{11} and (b) S_{22} measurements at 5 K of the InP HEMTs with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow) all at the bias points of $I_d = 5$ mA and $V_{ds} = 0.475$ V.

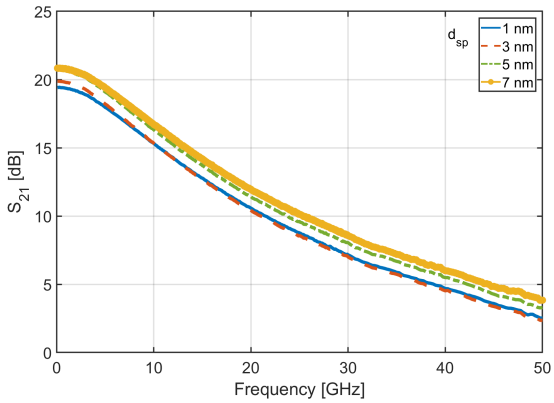

Figure 3.8: The S_{21} measurements at 5 K of the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) all at the bias points of I_d = 5 mA and V_{ds} = 0.475 V.

3.4 Noise characterization of 4-8 GHz cryogenic LNAs

The noise at cryogenic temperature for the InP HEMT is too small to be estimated with high accuracy using an on-wafer measurement. The most reliable method requires the insertion of discrete devices in a hybrid LNA designed for lowest noise [33]. As a result, the noise difference between the cryogenic LNAs can be attributed to the noise difference between the InP HEMTs. As illustrated in Fig. 3.9, diced individual transistors were mounted by wire-bounding in three-stage 4–8 GHz hybrid LNAs. To find the optimum bias conditions for lowest $T_{e,avg}$, the noise temperature was measured by sweeping the LNA drain current I_D. The optimum noise biases V_{DS} and I_D for the LNA and the corresponding biases (V_{ds}, I_d) for the InP HEMT are stated in Table 3.2 for various d_{sp}. Also the dc power consumption P_{LNA} for the LNA is given. In Fig. 3.10, the minimum noise regions are indicated by the boxes.

The noise and gain of the LNAs based on InP HEMTs with varying spacer thickness at their optimum noise biases are plotted in Fig. 3.11. The $T_{e,avg}$ and average gain G_{avg} of the LNAs are listed in Table 3.3. All LNAs reveals similar gain of around 40 dB which is indicative of the accuracy in the noise

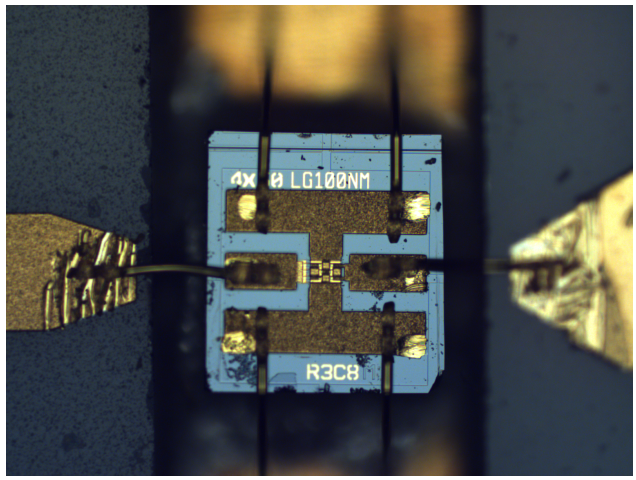

Figure 3.9: InP HEMT mounted by bond-wires in the 4–8 GHz hybrid LNA.

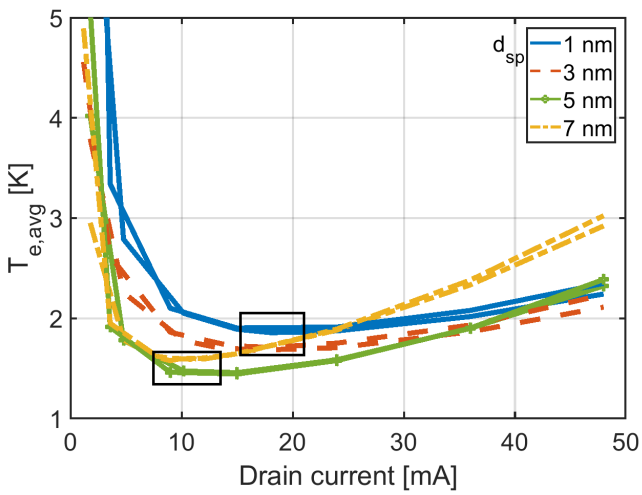

Figure 3.10: The $T_{e,avg}$ for InP HEMT LNAs with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow) versus I_D at 5 K and the drain biases of V_{ds}=0.325 V and 0.475 V. Black boxes indicate the minimum noise regions.

Table 3.2: The optimum noise bias and power consumption for the 4-8 GHz cryogenic LNAs based on InP HEMTs with different spacer thickness at 5 K.

d_{sp} (nm)	V_{DS} (V)	I_D (mA)	V_{ds} (V)	I_d (mA/ mm)	P_{LNA} (mW)
1	0.75	18.0	0.475	30	13.5
3	0.73	16.8	0.475	28	12.3
5	0.51	12.0	0.325	20	6.1
7	0.61	9.0	0.475	15	5.5

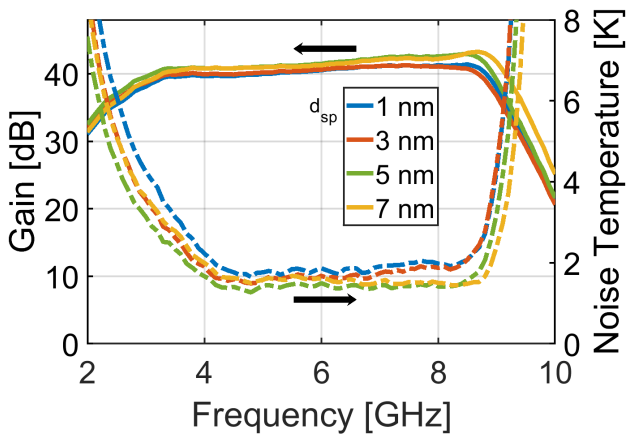

Figure 3.11: The measured gain (solid) and noise (dashed) temperature of three-stage 4-8 GHz hybrid LNAs integrated with the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) at 5 K and the optimum noise bias of each LNA.

measurements. The $T_{e,avg}$ shows a minimum of 1.4 K for d_{sp} = 5 nm. This is 36% lower than the $T_{e,avg}$ of InP HEMT with d_{sp} = 1 nm. In comparison with d_{sp} = 3 nm, which previously reported the lowest noise in this frequency range [25], the InP HEMT cryogenic LNA with d_{sp} = 5 nm exhibits a 20% lower noise level.

In addition to being superior in noise performance, InP HEMTs cryogenic LNAs with d_{sp} = 5 and 7 nm dissipate around 50% P_{LNA} less than the LNAs

Table 3.3: The average noise temperature and gain for the 4-8 GHz LNAs based on InP HEMTs with different spacer thickness at 5 K.

d_{sp} (nm)	1	3	5	7
$T_{e,avg}$ (k)	1.9	1.7	1.4	1.6
G_{avg} (dB)	40	41	42	41

with d_{sp} = 1 and 3 nm; See Table 3.2. In summary, Tables 3.2 and 3.3 present convincing evidence that the d_{sp} is an essential parameter in noise and dc power reduction for the InP HEMT cryogenic LNA, here investigated for 4-8 GHz.

3.5 InP HEMT noise temperature

To understand the difference in noise level between the investigated InP HEMTs, the Pospieszalski noise model (neglecting the low gate current) can be used [13]. This model expresses the minimum noise temperature $T_{\min}$ for the HEMT as:

$$T_{\min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g G_{ds} T_d}, \tag{3.2}$$

where $R_t = R_s + R_g + R_i$. R_s and R_g are the parasitic source and gate resistances, R_i is the intrinsic gate-to-source resistance, G_{ds} is the output conductance, f is the frequency, and f_T is the cutoff frequency. T_d and T_g are the equivalent drain and gate noise temperatures, respectively. Since contributions from the extrinsic parasitic noise elements are largely reduced at cryogenic temperature, the dependence of $T_{\min}$ on T_d is very strong for the cryogenic InP HEMT.

T_d for the InP HEMTs was extracted from the noise temperature of the LNA circuit using a small-signal model described in Ref. [34]. The de-embedded intrinsic circuit is outlined in Fig. 3.12. The intrinsic small-signal parameters for the investigated InP HEMTs are presented in Table 3.4. The values are similar for all devices which is reasonable since they have identical geometries. The relatively low R_i and gate-source capacitance C_{gs} indicate a promising low-noise performance of the devices[32], [35]. The T_d of the InP HEMTs extracted at their optimum noise bias are plotted in Fig. 3.13. The error bars

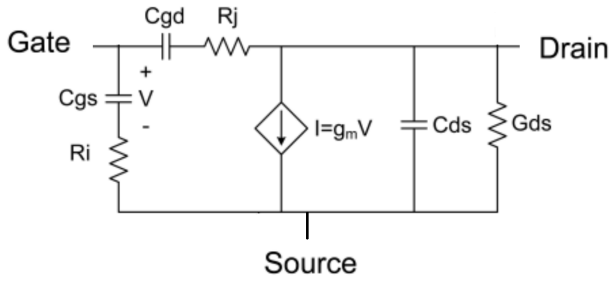

Figure 3.12: Equivalent intrinsic circuit of the InP HEMT [34].

Table 3.4: Intrinsic small-signal modeling parameters at the optimum noise bias for the InP HEMTs at 5 K.

d_{sp} (nm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	G_{ds} (mS)	g_m (mS)	R_j (Ω)	R_i (Ω)
1	115	44	60	19	210	21	1
3	119	47	56	19	213	22	1.2
5	114	47	56	18	199	21	1.3
7	112	39	52	13	174	22	1.2

in T_d are estimated from the noise simulations covering the frequency band 4-8 GHz [36]. In Fig. 3.13, the T_d exhibits a clear variation with d_{sp} for the InP HEMT at 5 K. It is observed that the T_d shows a minimum for $d_{sp} = 5$ nm.

The Pospieszalski noise model assigns all the resistive elements of the intrinsic circuit to T_g and T_d. T_g is generally accepted to present the thermal noise of the gate metal whereas T_d normally is interpreted as the amount of channel carrier fluctuations. The T_d can therefore be regarded as the channel noise in the cryogenic InP HEMT. Normally, a high electron mobility for the channel material in the InP HEMT is targeted for low-noise applications according to the well-known semi-empirical noise expressions such as the Fukui equation [37]. Dopants serve as efficient scattering for electrons at spacer thicknesses below 5 nm as seen in the reduction of mobility. While the scattering mechanism of the 2DEG can be of several physical origins, the impurity scattering is supposed to be significant at cryogenic temperature [38] which is consistent with the measured Hall electron mobility. However, the channel electrons in

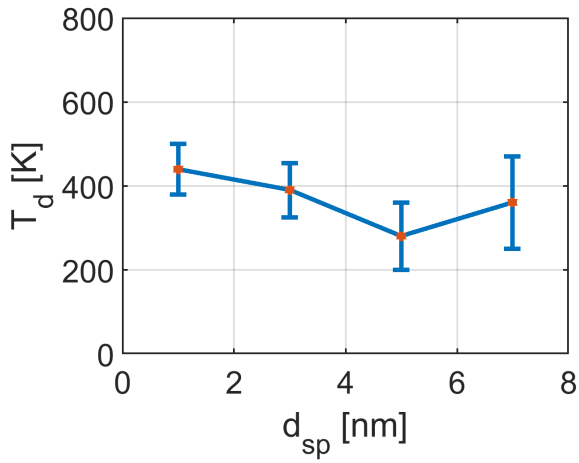

Figure 3.13: The T_d of the InP HEMT as function of spacer thickness extracted at optimal noise bias at 5 K. [From paper B]

the investigated InP HEMTs are expected to move at saturated velocity [39]. The Hall mobility reflects the average transport of the 2DEG at low electrical field and thus gives limited information on the expected noise level in the intrinsic InP HEMT at low temperature.

A recent theoretical study predicts that real-space transfer (RST) in the InP HEMTs is important for microwave drain noise [40]. RST is the emission of 2DEG carriers from the channel into the barrier. RST noise has earlier been proposed to occur in the GaAs HEMT [41] and InAlAs/InGaAs/InAlAs/InP quantum well [42].

The RST can be experimentally confirmed by the occurrence of negative differential resistance (NDR) in the $I - V$ output curves at elevated gate voltage [43]. It has been proven that prior to the valley transfer, hot electrons experience RST via channel carrier emission into the barrier in the III-V heterostructure of a HEMT [44]. In Fig. 3.14, drain current versus drain voltage at 5 K is plotted beyond $V_{gs} = 1$ V. It is observed that the NDR is weak yet observable for InP HEMTs with $d_{sp} = 1$ and 3 nm at $V_{gs} > 1$ V. The absence of NDR in Fig. 3.14 for $d_{sp} = 5$ and 7 nm is probably due to their more positive V_{th} of the InP HEMTs which means they would have required a higher V_{gs} for the RST to be detectable. However, this voltage is

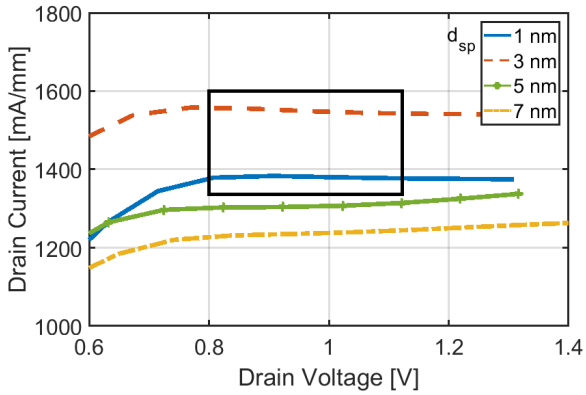

Figure 3.14: The drain current of the InP HEMT with d_{sp} = 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K, V_{gs} = 1.14 V. The box in the diagram shows the NDR region.

far beyond the optimum noise bias range listed in Table 3.2. Nevertheless, RST noise in the InP HEMT may occur before it is detectable by NDR in $I-V$ measurements. It is therefore plausible that even a small fraction of channel electrons suffering from RST may lead to a reduced confinement of the 2DEG meaning increased T_d for the transistor [40].

In Ref. [40], it is proposed that the fraction of hot electron transfer from the channel to barrier in a HEMT is determined by ΔE_c and V_{gs}. However, a HEMT at a gate bias below V_{th} cannot experience RST. When comparing different devices, it is V_{OV} which controls the fraction of transferred electrons via RST. Therefore, compared to Ref. [40], a modified equation is proposed to describe the hot electron fraction η taking the varying threshold voltage into account:

$$\eta = \exp(-\frac{\Delta E_c - (V_{gs} - V_{th})}{k_B T_e}) = \exp(-\frac{\Delta E_c - V_{OV}}{k_B T_e}), \tag{3.3}$$

where k_B is the Boltzmann constant and T_e is the electron channel temperature. If RST is responsible for noise in the HEMTs, with ΔE_c the same for all the structures, the noise must be minimized for the lowest V_{OV} at optimum noise bias. This is confirmed in Fig. 3.15 where the V_{OV} shows a clear minimum for d_{sp} = 5 nm. V_{OV} illustrates a better correlation with T_d (Fig.

3.13) compared with μ as a function of d_{sp}. Therefore, it is suggested that the observed difference in the channel noise probed by T_d is due to RST in the intrinsic InP HEMT at low temperature.

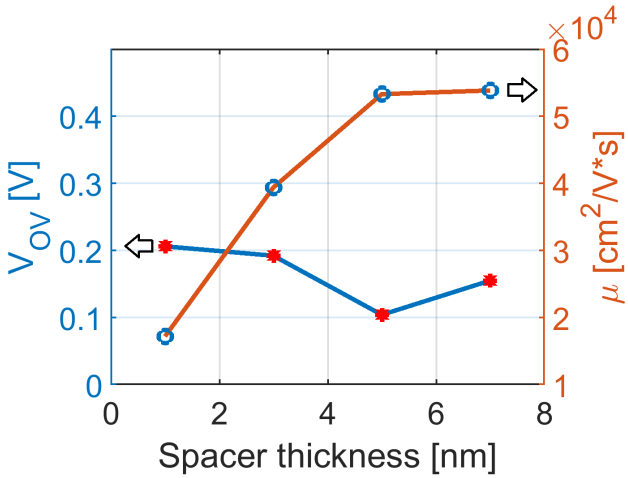

Figure 3.15: The V_{OV} at optimum noise gate bias and μ for the InP HEMT versus d_{sp} at 5 K.

3.6 InP HEMT noise and the subthreshold swing

In the mapping of noise properties for the InP HEMT and its corresponding dc properties, all measured at 5 K, an interesting correlation was observed between $T_{e,avg}$ and the subthreshold swing [45]. The average subthreshold swing SS_{avg} was calculated from the average drain current with V_{ds} from 0.025 to 1 V versus gate voltage shown in Fig. 3.16. From the curves, the SS_{avg} was determined to be 25, 23, 14 and 15 mV/dec for d_{sp} = 1, 3, 5 and 7 nm, respectively. The latter values of SS are among the lowest reported for cryogenic FETs yet still much beyond the theoretical Boltzmann limit SS, *i.e.* $(k_BT/q)ln10$ [8]. The deviation from the Boltzmann limit occurs at 80 K for InP HEMTs with d_{sp} = 1 and 3 nm and 60 K for d_{sp} = 5 and 7 nm. $T_{e,avg}$, $\sqrt{I_{ds}}/g_m$ and SS_{avg} versus d_{sp} for InP HEMTs measured at 5 K are plotted in Fig. 3.17. $T_{e,avg}$ reflects the rf properties of the transistor as depicted in

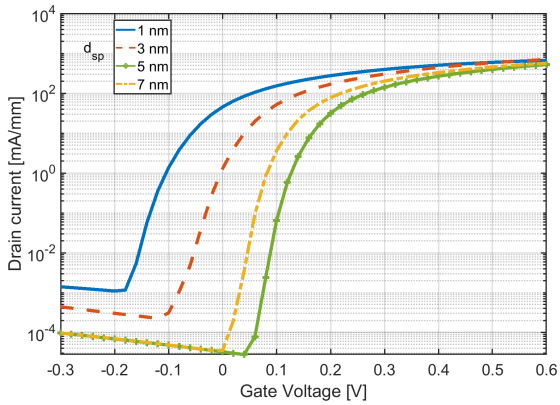

Figure 3.16: The average drain current (V_{ds} = 0.025 - 1 V) in the subthreshold region versus gate voltage of the InP HEMT at 5 K with d_{sp} = 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot).

Fig. 3.17 (a). The widely used noise indicator $\sqrt{I_{ds}}/g_m$ plotted in Fig. 3.17 (b) does not show a fully consistent relation with $T_{e,avg}$ as a function of d_{sp} at the optimum noise bias. Finally, SS_{avg} in Fig. 3.17 (c) is another dc property which monitors the I_d/g_m ratio. This is similar to the $\sqrt{I_{ds}}/g_m$ but at a lower bias [46].

Out of the two dc parameters $\sqrt{I_{ds}}/g_m$ and SS_{avg}, it appears that the latter better reflects the difference in noise between the cryogenic InP HEMTs. The saturation of the SS at low temperature is indicative for intrinsic mechanisms related to electron scattering in the 2DEG when approaching 0 K [47]. According to the model in ref. [47], the higher saturation SS_{avg} in InP HEMTs at cryogenic temperature indicates a large band-tail extension. As a result, the 2DEG in the channel will be affected by the increase of the electron density in the conduction-band tail. This may explain the better correspondence between SS_{avg} and $T_{e,avg}$ than for $\sqrt{I_{ds}}/g_m$ and $T_{e,avg}$. Since the noise performance of the InP HEMT at low temperature cannot be measured directly on-wafer with high accuracy, this suggests that SS for the InP HEMT (measured at the same low temperature) may serve as a useful and swift indicator for the expected rf noise in the cryogenic LNA.

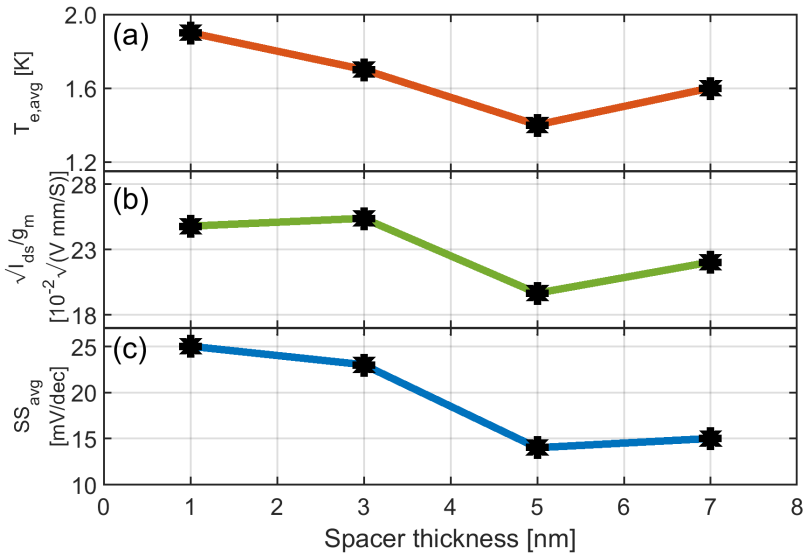

Figure 3.17: (a) The $T_{e,avg}$ (red) of the InP HEMT LNAs extracted at optimum noise bias. (b) $\sqrt{I_{ds}}/g_m$ (green) at optimum noise bias of the InP HEMTs. (c) The SS_{avg} (blue) of the InP HEMTs extracted at V_{ds}=0.1 V. All data points were based on measurements at 5 K. [From paper C]

CHAPTER 4

Conclusions and Future Work

4.1 Conclusions

This licentiate thesis has presented three achievements in the design and fabrication of low noise InP HEMTs for cryogenic LNAs.

The traditional gate recess-last method (with respect to metallization) was found to suffer from electrochemical etching making the targeted HEMT fabrication unstable. This was solved by modifying the process to a recess-first variant yielding stable InP HEMTs regardless of the epitaxial structure. A plasma cleaning procedure prior to passivation was added to solve the problem of enhanced gate leakage at 300 K following dielectric deposition. Furthermore, no significant difference in dc or noise of InP HEMT performance at 5 K was discovered for ALD and PECVD passivated devices. The HEMT process development made it possible to fabricate InP HEMTs with high uniformity required for the noise characterization in hybrid 4-8 GHz LNAs at cryogenic temperature.

The channel noise estimated by T_d for the cryogenic InP HEMTs was determined from noise measurements of the LNA at low temperature. Different LNAs, each one equipped with InP HEMTs with a spacer thickness in the

InAlAs-InGaAs heterojunction ranging from 1 to 7 nm, were investigated. It was found that the T_d exhibited a clear minimum with $d_{sp} = 5$ nm. In comparison with previous state-of-the-art results for InP HEMT cryogenic LNAs, this value was 2 nm thicker. The electron mobility in the channel was found to be a poor noise indicator for the HEMT at low temperature. The correlation between T_d and V_{OV} at the optimum noise bias with d_{sp} suggested the limiting factor for noise reduction in the cryogenic HEMT is related to RST involving injection of hot electrons from channel to barrier.

Finally, a correlation between the noise and the SS of the InP HEMT, both measured at low temperature, was observed and interpreted in relation to the traditional dc parameter $\sqrt{I_{ds}}/g_m$. It is proposed that the SS for the InP HEMT measured at low temperature may serve as an efficient dc indicator for the noise in the cryogenic LNA.

The results in this study show the significance for epitaxial optimization of the InP HEMT in cryogenic LNAs. This will lead to better understanding of the noise mechanisms in the HEMT and will help us to reduce the minimum noise temperature in the cryogenic LNA even further.

4.2 Future work

As the SS showed a clear correlation with noise at cryogenic temperature, it would be interesting to investigate the connection between channel noise and the SS at varying ambient temperatures. The temperature dependence of the channel noise will provide further understanding of the physical origin of the high-frequency channel noise in InP HEMTs.

In addition, measuring T_d for various ambient temperature is of interest. The temperature dependence of T_d is still under debate [48]. Another way to test the RST theory is to change the Al content in the barrier [40]. This will modify the ΔE_c and control the hot electron fraction emitted from the channel into the barrier. If the theory is correct, a higher Al content barrier should result in reduced RST noise. In practice, however, a higher Al content in the barrier risks to introduce more defects in the heterostructure.

This licentiate thesis has only reported on the spacer thickness influence for the noise in the T_d. Evidently, there are numerous material parameters in the epitaxial structure of the low-noise InP HEMT to be investigated. A previous study claimed that 80% In channel InP HEMT has significantly higher noise

than a 65% In channel InP HEMT [6]. However, it is still not clear how the In content affects the noise. Therefore, a systematic study with variation of the In channel content and the channel thickness is motivated to gain better understanding of the noise properties in the cryogenic InP HEMT.

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Junjie Li
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Paper A

Reduction of Noise Temperature in Cryogenic InP HEMT Low Noise Amplifiers with Increased Spacer Thickness in InAlAs-InGaAs-InP Heterostructures

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Reduction of Noise Temperature in Cryogenic InP HEMT Low Noise Amplifiers with Increased Spacer Thickness in InAlAs-InGaAs-InP Heterostructures

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***Abstract*—The impact of InP HEMT spacer thickness on cryogenic performance in low noise amplifiers (LNAs) has been investigated. 100 nm gate-length InP HEMTs based on InAlAs-InGaAs-InP heterostructures with different spacer thickness (1 nm, 3 nm and 5 nm) were fabricated. The Hall measurements, simulated band structures and dc characteristics of InP HEMTs were compared for all the three different epitaxial structures at 5 K. The noise performance of the InP HEMT was studied using a three-stage 4–8 GHz hybrid LNA at 5 K. All LNAs yielded an average gain above 30 dB across the whole band. When biased for optimal low noise operation, the LNA with 5 nm spacer thickness InP HEMTs achieved an average noise temperature of 1.3 K. The LNAs with spacer thickness of 1 nm and 3 nm InP HEMTs exhibited a higher average noise temperature of 1.9 K and 1.7 K, respectively. The reduction in LNA noise temperature with increased spacer thickness was observed to correlate with a strongly enhanced electron mobility in the InP HEMT structure at 5 K.**

Keywords—Cryogenic; low noise amplifier; InP HEMT; spacer thickness; noise

C-band (4-8 GHz) cryogenic InP HEMT low noise amplifiers (LNAs) are highly demanded in quantum computing systems for the readout of qubits at the 4 K stage [1]. The thermal noise which originates from the kinetic energy of the charge carriers in the 2DEG channel constitutes one of the dominating noise sources in the HEMT [2]. It is well known that engineering of the InP HEMT epitaxial structure plays a decisive role for the HEMT performance [3]. From photoluminescence investigations on HEMT epitaxial structures, it was demonstrated that the scattering of carriers in the channel was dependent upon spacer thickness [4]. This suggests that the spacer design plays a role in the HEMT LNA noise performance. Here we report the noise temperature of cryogenic C-band LNAs based on InP HEMTs with different spacer thickness.

Fig. 1 shows the schematic of InP HEMT epitaxial layers with three different spacer thicknesses of 1, 3 and 5 nm. The InAlAs barrier thickness above the spacer was adjusted correspondingly to keep the total gate-to-channel distance constant. In Fig.2, Hall measurements revealed a strong dependence on the electron mobility as a function of spacer thickness at 5 K compared to 300 K. In contrast, sheet carrier concentration was relatively insensitive to spacer thicknesses. The band structure and electron density at 5 K has been simulated using the measured electron mobilities, see Fig.3. The energy barriers of the channel are almost the same for all three structures. The main difference is the distance between delta doping energy well and the 2DEG channel.

4×50 μm,gate-width 100 nm gate-length InP HEMTs were fabricated using the method described in Ref. [5]. The output dc characteristics at 5 K of the InP HEMTs with different spacer thickness are plotted in Fig. 4. The 1 nm spacer InP HEMT exhibited the lowest current driving capability whereas the 3 nm and 5 nm spacer InP HEMTs were similar. The threshold voltage shifted toward more positive values with increased spacer thickness. The gate leakage bell shape seen in Fig. 5 suggests that the 5 nm spacer InP HEMT has the lowest impact ionization [6]. All devices exhibited relatively low gate current leakage (< 0.1 μA/mm) at their optimum low-noise bias, which implies that the gate leakage will not degrade the noise temperature in the C-band LNA [5].

The noise performance of InP HEMTs was investigated in a three-stage 4–8 GHz hybrid LNA employing the measurement method described in [7,8]. The noise of the LNA at 300 K was comparable for all three spacers with an average noise temperature (Te,avg) of about 28 K. The gain of the LNAs at 300 K was similar to that of 5 K and increased with spacer thickness. The noise of the LNAs biased at the optimum point at 5 K decreased with the spacer thickness in the frequency band as shown in Fig. 6 where the LNA with 5 nm spacer InP HEMTs exhibited the lowest Te,avg of 1.3 K. The reduction of noise is correlated with an observed increase in electron mobilities, indicating that 2DEG charge carriers experience less scattering from the delta doping plane with thicker spacer.

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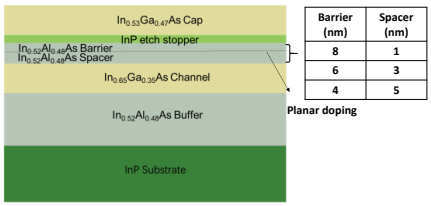

Barrier (nm)	Spacer (nm)
8	1
6	3
4	5

Fig. 1. Schematic of InP HEMT epitaxial layers with three different spacer thickness used in this work.

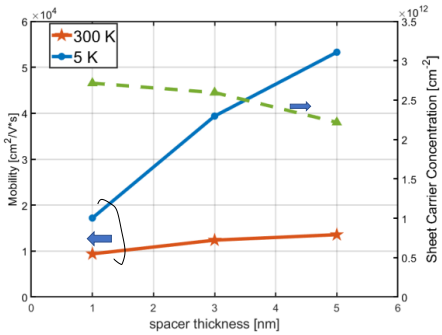

Fig. 2. The measurement data of the three structures without cap layers. The sheet carrier concentration at 300 K (green dashed line) and electron mobility at both 5 K (blue circle solid line) and 300 K (red star solid line) versus spacer thickness.

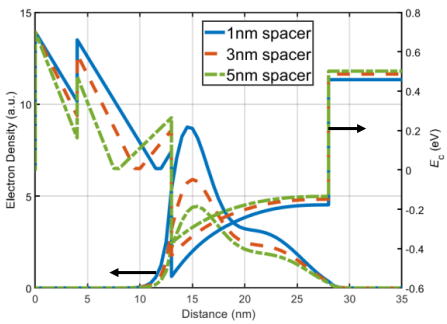

Fig. 3. Simulated band structure and 2DEG electron density for spacer thickness of 1nm (blue solid), 3 nm (red dashed) and 5 nm (green dash-dot). The δ doping was adjusted according to the measured Hall mobility at 5 K.

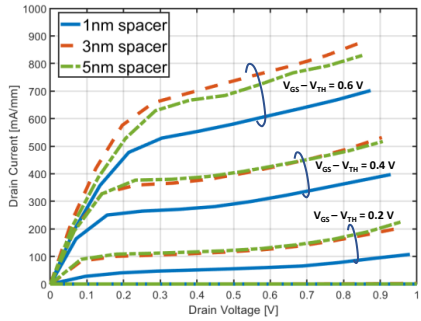

Fig. 4. The *I-V* characteristics of the 100 nm gate length InP HEMT using 4 × 50 μm gate-width layout with spacer thickness of 1 nm (blue solid), 3 nm (red dashed) and 5 nm (green dash-dot) at 5 K. V_{TH} was -0.3 V, -0.2 V and 0 V for 1 nm, 3 nm and 5 nm spacer, respectively.

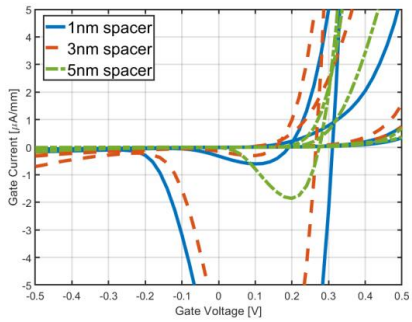

Fig. 5. Gate current of the 100 nm gate-length InP HEMT with spacer thickness of 1 nm (blue solid), 3 nm (red dashed) and 5 nm (green dash-dot) at 5 K. V_{DS} = 0.1 – 0.9 V in steps of 0.2 V.

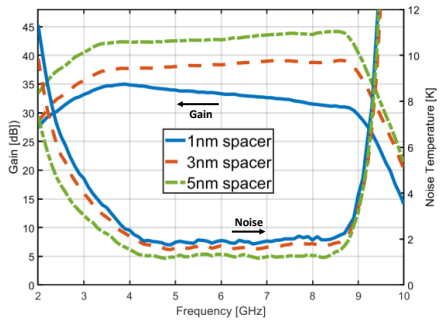

Fig. 6. The measured gain and noise temperature of three-stage 4-8 GHz hybrid LNAs integrated with the 100 nm InP HEMT with spacer thickness of 1 nm (blue solid), 3 nm (red dashed) and 5 nm (green dash-dot) at the ambient temperature of 5 K. The optimum noise bias for all LNAs was V_D = 0.7 V and I_D = 18 mA.

Paper B

Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs

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Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs

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***Abstract*— InP high electron mobility transistors (InP HEMTs) with different spacer thickness 1 to 7 nm in the InAlAs-InGaAs heterostructure have been fabricated and characterized at 5 K with respect to electrical dc and rf properties. The InP HEMT noise performance was extracted from gain and noise measurements of a hybrid low-noise amplifier (LNA) at 5 K equipped with discrete transistors. When biased for optimal noise operation, the LNA using 5 nm spacer thickness InP HEMTs achieved the lowest average noise temperature of 1.4 K at 4-8 GHz. The InP HEMT channel noise was estimated from the drain noise temperature which confirmed the minimum in noise temperature for the 5 nm spacer thickness InP HEMT. It is suggested that the spacer thickness acts to control the degree of real-space transfer of electrons from the channel to the barrier responsible for the observed noise variation in the cryogenic InP HEMTs.**

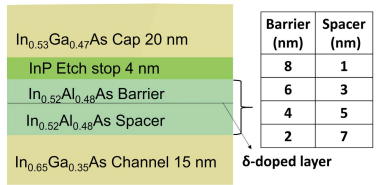
***Index Terms*— Cryogenic, InP HEMT, low-noise amplifier, noise, spacer thickness.**

I. Introduction

THE InP high electron mobility transistor (InP HEMT) is the workhorse device for the design of the cryogenic low noise amplifier (LNA) which offers the lowest noise temperature among all semiconductor-based circuits [1]. Applications are found in microwave and mm-wave receivers for radio astronomy and space communication [2]. At present, there is a rapid development of electronic devices used in quantum computing systems [3]. The cryogenic InP HEMT LNA has here become instrumental for the readout of microwave qubits at the 4 K stage [4], [5]. To further improve the qubit readout, the noise properties at low temperature for the InP HEMT are crucial.

It is well known that engineering of the InP HEMT epitaxial structure plays a decisive role for the device electrical performance [6] and this becomes even more critical under cryogenic operation [5]. Previous work demonstrated that the carrier concentration and the scattering of carriers in the HEMT channel were highly dependent on the location of the planar doping layer in relation to the heterojunction [7], [8]. Hence the choice of spacer thickness is expected to modify the properties of the two-dimensional electron gas (2DEG) which in turn is essential for the HEMT noise performance. To the authors knowledge, this has not been reported for the HEMT operating under the temperature conditions used in cryogenic LNAs.

In this study, we report on the optimum spacer thickness in the InAlAs-InGaAs heterojunction for lowest channel noise in the cryogenic InP HEMT LNA. The results suggest that the noise can be related to the amount of real-space transfer of electrons between channel and barrier in the InP HEMT.



Barrier (nm)	Spacer (nm)
8	1
6	3
4	5
2	7

Fig. 1. Schematic of epitaxial stack used in HEMT fabrication. The table shows the investigated variation in spacer (and barrier) thickness.

II. Device Technology

The epitaxial layers were grown by molecular beam epitaxy on 3-inch diameter InP substrates. Starting from the bottom, the epitaxial stack consisted of a 500 nm thick $In_{0.52}Al_{0.48}As$ buffer and a 15 nm pseudomorphic $In_{0.65}Ga_{0.35}As$ channel layer. Fig. 1 shows a schematic of the InP HEMT epitaxial layers above the buffer. By growing an $In_{0.52}Al_{0.48}As$ layer with a Si δ-doped plane on top of the channel, a heterojunction with a 2DEG was formed. The spacer thickness was the distance between the top of the channel and the δ-doped layer. Four different samples with spacer thickness d_{sp} of 1, 3, 5 and 7 nm were grown. The δ doping level was calibrated to keep the sheet carrier concentration at a constant value of 2.5×10^{12} cm^{-2} for all four structures. The $In_{0.52}Al_{0.48}As$ barrier thickness above the δ-doped layer was adjusted accordingly so

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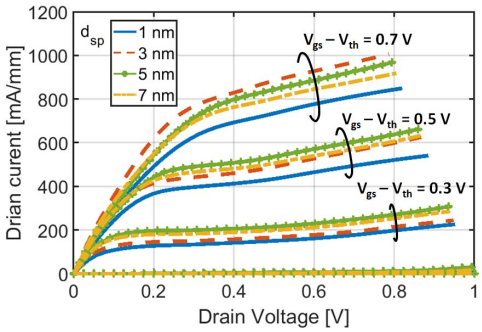

Fig. 2. Drain current versus drain voltage of InP HEMT with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K.

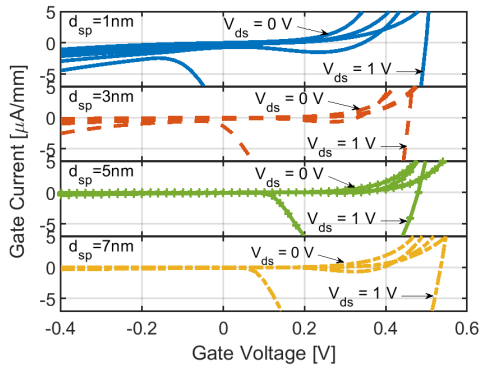

Fig. 3. Gate current versus gate voltage of InP HEMT with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. V_{ds} = 0 – 1 V in steps of 0.25 V.

that the total thickness of the barrier and spacer layer was 9 nm for all four structures, see table insert in Fig. 1(a). To improve etching selectivity for the subsequent cap layer, a 4 nm thick InP etch stop layer was grown on the barrier [9]. The InP etch stop layer also served to passivate material-related defects in the gate recess region [10]. The epitaxial stack was finalized by growing a 20 nm thick n^+ $In_{0.53}Ga_{0.47}As$ cap layer.

The measured Hall electron mobility at 5 K for epitaxial structures without cap layer was 17,000, 39,000, 53,000 and 54,000 cm^2/Vs for structures with d_{sp} = 1, 3, 5 and 7 nm, respectively. The sheet carrier concentration at 5 K showed only a ±10% dependence on spacer thickness.

InP HEMTs using epitaxial structures with different d_{sp} were fabricated simultaneously employing the technology described in [2]. The transistor gate length and gate width were 100 nm and 4×50 μm, respectively.

III. Results

InP HEMTs with different spacer thicknesses were electrically characterized on-wafer at 5 K. The drain current versus drain voltage curves in Fig. 2 showed expected output behavior with no obvious kink effect previously reported for cryogenic InP HEMTs [2]. This is attributed to the efficient suppression of surface traps in the gate-recess region by the InP etch stop layer [9]. In saturation, all transistors displayed similar current driving ability except for InP HEMTs with d_{sp} = 1 nm where the drain current was lower. This was expected due to the relatively low Hall electron mobility and high sheet resistance at 5 K for d_{sp} = 1 nm.

The gate current I_g of the InP HEMTs with different spacer thickness is plotted in Fig. 3. All devices exhibited low gate current leakage <1 μA/mm with no impact ionization in the gate bias range between 0 and +0.2 V and drain-source bias lower than 0.5 V. Under such bias conditions, the InP HEMT is close to its optimum low-noise region. The amount of gate leakage shown in Fig. 3 is not expected to degrade the noise temperature in the LNA [11]. From the drain current versus gate voltage characteristics, the subthreshold swing (SS) at V_{ds} = 0.1 V was calculated to be 24, 20, 12 and 13 mV/dec for d_{sp} = 1, 3, 5 and 7 nm, respectively. The SS levels for d_{sp} = 5 nm is among the lowest reported for a field-effect transistor yet beyond the theoretical Boltzmann limit [12].

It was observed from the drain current versus gate voltage that the threshold voltage V_{th} varied with d_{sp}. For d_{sp} = 1, 3, 5 and 7 nm, the V_{th} was −0.2, −0.1, 0.1 V and 0 V, respectively. This was expected because V_{th} depends on the location of the δ-doped layer and the doping concentration [13]. With increased d_{sp} and decreased δ doping level, the V_{th} will show a positive shift and vice versa. Hence, there will be a maximum in V_{th}, here at 5 nm, when the spacer thickness was increased from 1 to 7 nm and the δ doping concentration was increased to keep the sheet carrier concentration in the channel constant.

Since the noise level of the InP HEMT at cryogenic temperature is too low to be accurately estimated from probed measurements [14], chips were diced into discrete InP HEMTs which were mounted in three-stage 4–8 GHz hybrid LNAs. By measuring the gain and noise of the amplifier at 5 K, the cryogenic transistor noise was possible to extract employing a methodology described in [14], [15]. All measurements were performed at the bias point for lowest amplifier noise using the same attenuator. As a result, the noise difference between the LNAs could be attributed to the noise difference for the InP HEMTs with different spacer thickness.

As seen in Fig. 4(a), the amplifier experimental data at 5 K revealed differences between the LNAs based on InP HEMTs with varying spacer thickness. All LNAs exhibited similar gain of around 40 dB which in turn meant high accuracy for the noise measurements. The noise temperature of the LNAs decreased with increased d_{sp} from 1 to 5 nm for InP HEMTs. Considering the relative differences in noise in Fig. 4(a), the LNA with 5 nm spacer InP HEMTs exhibited the lowest average noise temperature $T_{e,avg}$ of 1.4 K at 4-8 GHz. The noise level is on a par with the best result previously reported for this frequency band [2]. The $T_{e,avg}$ of LNAs with d_{sp} = 1, 3 and 7 nm was 1.9, 1.7 and 1.6 K, respectively. The optimum noise bias for the LNA was V_{DS} = 0.51 V, I_D = 12.0 mA for d_{sp} = 5 nm and V_{DS} = 0.61 V, I_D = 9.0 mA for d_{sp} = 7 nm. These biases were smaller

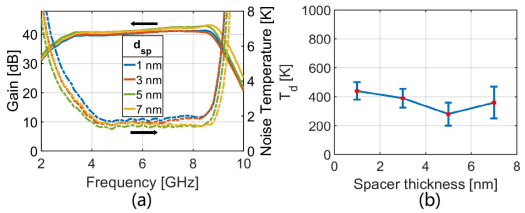

Fig. 4. (a) The measured gain (solid) and noise temperature (dashed) of three-stage 4-8 GHz hybrid LNAs integrated with the InP HEMT with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow) at the optimum noise bias of each LNA at 5 K. (b) The T_d as function of spacer thickness extracted at optimum noise bias for the InP HEMT at 5 K.

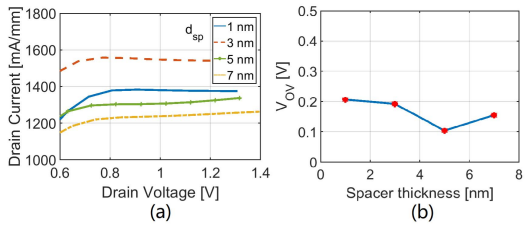

Fig. 5. (a) The drain current at 5 K for InP HEMT with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot), V_{gs} = 1.14 V. (b) The overdrive voltage $V_{OV} = V_{gs} - V_{th}$ at optimum noise gate bias for the InP HEMT versus d_{sp} at 5 K.

than $V_{DS} = 0.75$ V, $I_D = 18.0$ mA for $d_{sp} = 1$ nm and $V_{DS} = 0.73$ V, $I_D = 16.8$ mA for $d_{sp} = 3$ nm. The corresponding optimum noise bias for the InP HEMTs was $V_{ds} = 0.475$ V, $I_d = 30$ mA/mm for $d_{sp} = 1$ nm, $V_{ds} = 0.475$ V, $I_d = 28$ mA/mm for $d_{sp} = 3$ nm, $V_{ds} = 0.325$ V, $I_d = 20$ mA/mm for $d_{sp} = 5$ nm and $V_{ds} = 0.475$ V, $I_d = 15$ mA/mm for $d_{sp} = 7$ nm.

The noise generated in the HEMT was quantified by the drain noise temperature T_d [16]. The T_d was extracted by comparing the measured gain and noise of the LNA with simulations [2] based on an equivalent small-signal HEMT model using the measured S-parameters [17]. The intrinsic small-signal parameters for the investigated InP HEMTs displayed similar values which is reasonable since they had identical geometries. The T_d of the InP HEMT extracted at its optimal noise bias are presented in Fig. 4(b). The error bars in T_d were estimated from the noise simulations through the frequency band 4-8 GHz. It is observed that T_d shows a minimum for InP HEMT with 5 nm spacer thickness. Even though the error bars in Fig. 4(b) are large in absolute numbers, the relative change in T_d suggests that noise in the transistor channel depends upon the spacer thickness of the cryogenic InP HEMT.

IV. Discussion

The high-frequency noise in the InP HEMT is connected to the degree of carrier fluctuations in the 2DEG channel. This will lead to a distribution in electrons velocities related to the noise spectrum of the InP HEMT [18]. The cryogenic InP HEMT is here well suited to probe the amount of noise since the intrinsic channel constitutes the dominant noise source in the full device [2]. Dopants serve as efficient scattering for electrons at spacer thicknesses below 5 nm as seen in the reduction of mobility. While the scattering mechanism of the 2DEG can be of several physical origins, impurities scattering is supposed to be significant at cryogenic temperature [19] which is consistent with the measured Hall mobility. Normally, one strives for a high-mobility channel for reducing noise in the HEMT as guided by well-known semi-empirical noise expressions such as the Fukui equation [20]. However, the channel electrons in the investigated InP HEMTs are expected to move at saturated velocity [21]. The Hall mobility reflects the average transport of the 2DEG at low electrical field and thus gives limited information on the expected noise level in the intrinsic InP HEMT at low temperature.

A recent theoretical study predicts that real-space transfer (RST) in the InP HEMTs is an important source for microwave drain noise [23]. RST is the emission of 2DEG carriers from the channel into the barrier prior to valley transfer [24]. RST noise has earlier been proposed for GaAs HEMTs [26] and InAlAs/InGaAs/InAlAs/InP quantum wells [27]. A well-known manifestation of RST in HEMTs is negative differential resistance (NDR) in the $I - V$ output curves at elevated gate voltage [25]. This is indeed observed (Fig. 5(a)) for our InP HEMTs at 5 K for d_{sp} = 1 and 3 nm. The absence of NDR for d_{sp} = 5 and 7 nm is due to the higher V_{th} of the InP HEMTs. Note that the NDR in Fig. 5(a) is far beyond the low-noise bias of the InP HEMT. RST may however also occur at low-bias operation and be detectable as increased noise in the HEMT [23], [26]. In Reference [23], it is proposed that the fraction of the electron transfer from the channel to barrier in a HEMT is determined by the conduction band offset ΔE_c and gate bias V_{gs}. However, a HEMT at a gate bias below V_{th} cannot have any RST. When comparing different devices, it is the overdrive voltage $V_{OV} = V_{gs} - V_{th}$ which controls the fraction of transferred electrons. If RST is responsible for noise in the HEMTs, with ΔE_c the same for all the structures, the noise must be minimized for the lowest V_{OV} at the optimum noise bias. This is confirmed in Fig. 5(b) where the V_{OV} shows a clear minimum for $d_{sp} = 5$ nm which is the InP HEMT with lowest T_d (Fig. 4). We therefore hypothesize that the channel noise probed by T_d is due to RST in the intrinsic InP HEMT at low temperature.

V. Conclusion

The channel noise estimated by T_d of the cryogenic InP HEMTs has been studied using a spacer thickness variation from 1 to 7 nm in the InAlAs-InGaAs heterostructure. It was found that the T_d versus d_{sp} exhibited a clear minimum at 5 nm. The electron mobility was a poor noise indicator. The correlation between T_d and V_{OV} at the optimum noise bias with d_{sp} suggests that RST noise can be important in cryogenic InP HEMTs. The result in this study shows the significance for epitaxial optimization of the HEMT for use in LNAs for quantum computing and will help to reduce the minimum noise temperature in the 4 K readout even further.

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Paper C

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On the relation between rf noise and subthreshold swing in InP HEMTs for cryogenic LNAs

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***Abstract* — 4 - 8 GHz low-noise amplifiers (LNAs) based on InP high electron mobility transistors (InP HEMTs) with different spacer thickness in the InAlAs-InGaAs heterostructure were fabricated and characterized at 5 K. A variation in the lowest average noise temperature of the LNA was observed with spacer thickness. We here report that the subthreshold swing (*SS*) at 5 K for the HEMT exhibited similar dependence with spacer thickness as the lowest average noise temperature of the LNA. This suggests that low-temperature characterization of *SS* for the HEMT can be used as a rapid assessment of anticipated noise performance in the cryogenic HEMT LNA.**

Index Terms — Cryogenic, InP HEMT, low-noise amplifier, noise, subthreshold swing

I. Introduction

The InP high electron mobility transistor (InP HEMT) offering the lowest noise temperature for the cryogenic low noise amplifier (LNA) are highly demanded in applications of microwave and mm-wave receivers for radio astronomy, space communication, and, more recently, in quantum computing [1]. Since the noise performance of the HEMT at low temperature cannot be measured directly on-wafer with high accuracy, the dc parameter $\sqrt{I_{ds}}/g_m$ is often used as a guide for predicting the optimum noise bias between various devices [2]. The $\sqrt{I_{ds}}/g_m$ originates from the Pospieszalski empirical model for the HEMT and is particularly useful for noise assessment of cryogenic transistors. Here we report on the subthreshold swing (*SS*) of the InP HEMT as an alternative rapid indicator of its rf noise performance at cryogenic temperature. We have fabricated cryogenic 4-8 GHz InP HEMTs LNAs with different spacer thickness in the InAlAs-InGaAs heterostructure. The measured differences in average noise temperature between the cryogenic HEMT LNAs were found to correlate well with the measured *SS* of the HEMTs at the same temperature.

II. Device Technology

The InP HEMTs were made from epitaxial structures described in Ref. [3] which is shown in the inset of Fig.1. The spacer thickness d_{sp}, *i.e.* the distance between the top of the InGaAs channel and the δ-doped plane in the InAlAs, varied between 1, 3, 5 and 7 nm. The total thickness of the barrier (the InAlAs layer above the δ-doped layer) and the spacer layer was 9 nm for all structures.

InP HEMTs using epitaxial layers with different d_{sp} were fabricated simultaneously employing the device process described in Ref. [4]. The transistor gate length and gate width were 100 nm and 4×50 µm, respectively. Fig. 1 shows a cross-sectional scanning transmission electron microscopy (STEM) image of the gate region for a finalized InP HEMT (d_{sp} = 3 nm). The STEM image reveals a well-controlled symmetric recess with 125 nm distance at each side of the 100 nm long T-shaped gate. Furthermore, the in-diffusion of Pt beneath the gate, defining the gate-to-channel distance, is clearly observed [4].

III. Results

The dc characteristics of the InP HEMTs were characterized on-wafer at 5 K. The drain current I_d and gate current I_g of the InP HEMTs with different spacer thickness all showed expected behavior [3]. The drain current versus gate voltage in

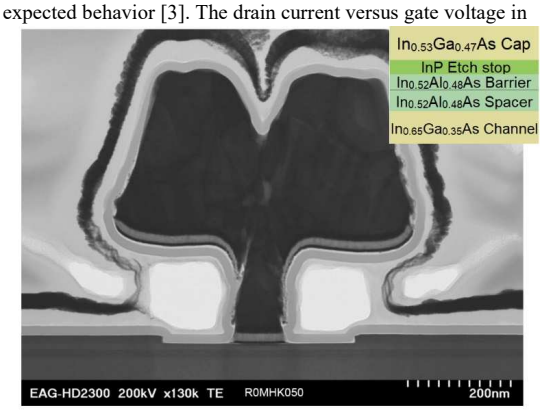

Fig. 1. STEM image of the 100 nm-length gate of the InP HEMT with d_{sp} = 3 nm. The inset: epitaxial stack of the InP HEMT.

TABLE I

INTRINSIC SMALL-SIGNAL MODELLING PARAMETERS AT THE OPTIMUM NOISE BIAS FOR THE INP HEMTS AT 5 K

d_{sp} (nm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	g_{ds} (mS)	g_{mi} (mS)	R_j (Ω)	R_i (Ω)
1	115	44	60	19	210	21	1
3	119	47	56	19	213	22	1.2
5	114	47	56	18	199	21	1.3
7	112	39	52	13	174	22	1.2

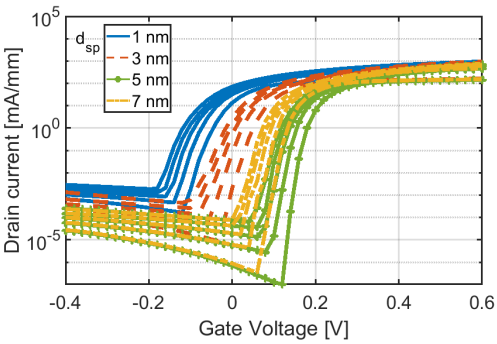

Fig. 2. Drain current versus gate voltage. V_{ds} = 0.1 – 0.9 V in steps of 0.2 V. Temperature was 5 K.

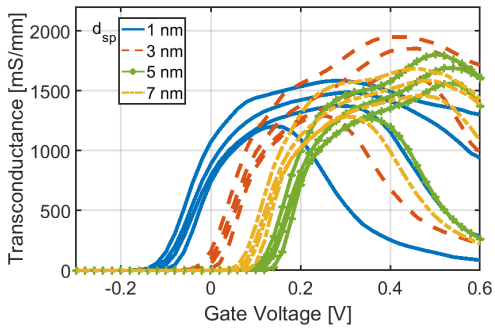

Fig. 3. The transconductance versus gate voltage. V_{ds} = 0.2 – 0.8 V in steps of 0.2 V. Temperature was 5 K.

log scale is plotted in Fig. 2. The *SS* at V_{ds} = 0.1 V showed that InP HEMTs with d_{sp} = 1 and 3 nm have higher *SS* of 24 and 20 mV/dec compared with d_{sp} = 5 and 7 nm with *SS* of 12 and 13 mV/dec, respectively. The latter values of *SS* are among the lowest reported for a field-effect transistor yet still much beyond the theoretical Boltzmann limit $(k_BT/q)\ln 10$ at these low temperatures [5].

Fig. 3 presents the transconductance of the InP HEMTs with different spacer thickness at V_{ds} = 0.2 – 0.8 V in steps of 0.2 V. The InP HEMT with d_{sp} = 3 nm exhibited the highest peak transconductance at 5 K which is consistent with its higher current driving capacity at elevated drain and gate [3]. Fig. 3 also demonstrates the variation in threshold voltage V_{th} [3]. The intrinsic small-signal parameters for the investigated InP HEMTs at the optimum noise bias were extracted and are presented in Table I. The extraction was based on an equivalent small-signal HEMT model using the measured S-parameters [6]. It is observed that the various InP HEMTs displayed similar small-signal values which was reasonable since they had identical geometries.

Four three-stage 4–8 GHz hybrid LNAs were assembled using the InP HEMTs with different spacer thickness [7]. The gain and noise of the amplifiers were measured at 5 K [8]. When biased at V_{DS} = 0.7 V, I_D = 15.0 mA, LNAs with d_{sp} = 5 and 7 nm of the InP HEMTs exhibited higher gain and lower noise than LNAs with d_{sp} = 1 and 3 nm as shown in Fig. 4. To find the lowest noise for each LNA, we measured the noise with sweeping drain current and voltage. Fig. 5 depicts the average noise temperature T_{avg} of the LNAs at different biases. The

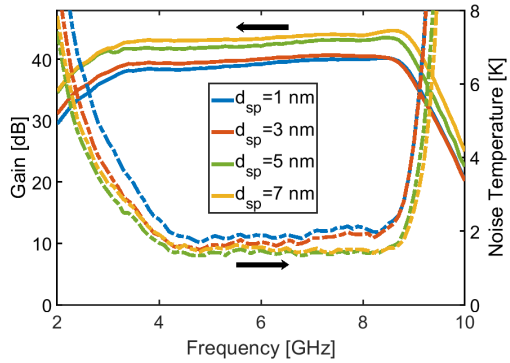

Fig. 4. The measured gain (solid) and noise temperature (dashed) of three-stage 4-8 GHz hybrid LNAs integrated with the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) at bias of V_{DS}=0.7 V, I_D=15.0 mA. Temperature was 5 K.

lowest T_{avg} of LNA with d_{sp} = 1, 3, 5 and 7 nm were 1.9, 1.7, 1.4 and 1.6 K, respectively. The optimum noise biases for the LNA were V_{DS} =0.75 V, I_D =18.0 mA for d_{sp} = 1 nm, V_{DS} =0.73 V, I_D=16.8 mA for d_{sp} = 3 nm, V_{DS}=0.51 V, I_D=12.0 mA for d_{sp} = 5 and V_{DS} =0.61 V, I_D =9.0 mA for d_{sp} = 7 nm, respectively [3].

In Fig. 6, the HEMT LNA average noise temperature, $\sqrt{I_{ds}}/g_m$, and SS are plotted versus spacer thickness, all measured at 5 K. The $\sqrt{I_{ds}}/g_m$ in Fig. 6(b) does not show a fully consistent relation with the average noise temperature in

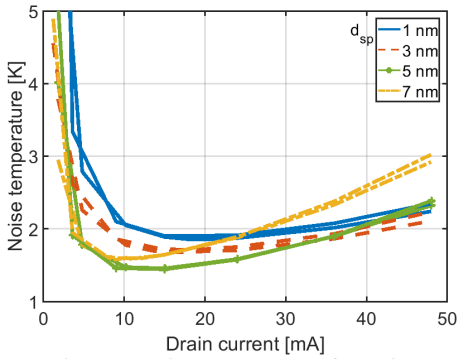

Fig. 5. The average noise temperature T_{avg} of LNAs integrated with the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) versus LNA drain current I_D at drain bias of V_{ds}=0.325 V and 0.475 V.

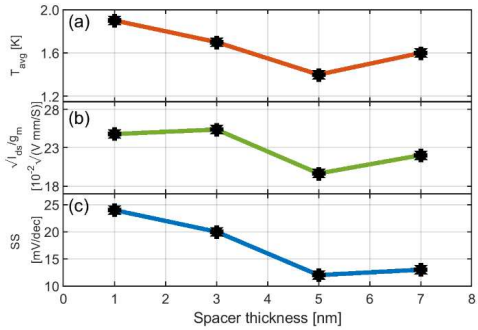

Fig. 6. (a) The T_{avg} (red) of the LNAs extracted at optimum noise bias. (b) $\sqrt{I_{ds}/g_m}$ (green) at optimum noise bias of the InP HEMTs. (c) *SS* (blue) of the InP HEMTs extracted at V_{ds}=0.1 V. All curves in (a), (b) and (c) as a function of spacer thickness at 5 K.

Fig. 6(a). In contrast, the SS in Fig. 6(c) demonstrates an excellent correspondence with the measured noise in the HEMT LNAs. *SS* reflects the ability to switch off the transistor. A lower *SS* means a higher g_m/I_d ratio which is important for the noise properties. At this low temperature, it is expected that *SS* is independent of temperature and depends on a band tail energy parameter and a body-effect coefficient [5]. One explanation of our data is that the *SS* in Fig. 6(c) captures the amount of scattering for the 2DEG carriers as a function of position of the δ-doped plane in the HEMT reflecting the rf noise performance of the LNA. Hence the *SS* measurement at low temperature might be able to serve as an efficient tool to identify the best InP HEMT for the cryogenic LNA.

IV. Conclusion

The T_{avg} of the cryogenic LNAs has been studied using InP HEMTs with a spacer thickness variation from 1 to 7 nm in the InAlAs-InGaAs heterostructure. It was found that the LNA with 5 nm spacer InP HEMT exhibited a clear minimum in noise with T_{avg} = 1.4 K. The similarity between the dependance of T_{avg} (at optimum noise bias) and *SS* (at low drain voltage) with d_{sp} suggests that *SS* serves as an indicator for the expected rf noise variation in the cryogenic HEMT LNA.

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