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RF PA Predistortion using Non-Linear RF-DACs

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Abstract—Analog and/or digital predistortion may be used to linearize power amplifiers (PAs) at the cost of additional hardware. We present a novel scheme which uses segmented non-linear RF-DACs to linearize PAs at no additional hardware cost. An expanding segmented scaling chosen at design time may be adjusted using DAC bias, allowing linearization to be adapted. Simulations demonstrate the robustness and flexibility of the approach, achieving excellent overall linearity over a large range of DAC and PA bias conditions.

Index Terms—Linearization, Non-linear scaling, Power amplifier (PA), Predistortion, RF-DAC.

I. INTRODUCTION

Wireless networks increasingly use millimeter-wave (mmW) frequencies, where broad and continuous spectrum is available. The 5G mmW-bands, for example, are around 3 GHz wide [1]. Also, spectrum-efficient modulation schemes require highly linear transmitters. Additionally, with massive multiple-input-multiple-output (mMIMO) transmitters at mm wavelengths, a large number of antennas and transmitters are combined in densely packed arrays, resulting in strict energy and thermal budgets [2].

RF-DACs are an alternative for CMOS mmW transmitter realizations with implementations demonstrating a peak saturated output power of around 19 dBm [3], [4]. However, overall system efficiency may be degraded by the large cost of generating and buffering the quadrature LO signals. Hence, for higher overall system efficiency and/or higher output power, RF-DACs cascaded with power amplifiers (PAs) are of interest.

Transmitter PAs follow an inverse relationship between output power and linearity. To fulfil the linearity requirements, either the PAs need to operate at significant power back-off, and/or a predistorter (PD) is required to compensate for the non-linear PA characteristic. Predistorters may be implemented in the analog or the digital domain. Analog PDs (APDs) may approximate the inverse of the PA non-linearities using diodes [5], couplers [6], [7], or cold-mode transistors [8]; but they often present significant power losses in addition to large footprints [6]. Digital PDs (DPDs) perform the linearization in the digital domain, before conversion to the analog domain, to allow for linearization of the entire transmitter. Although digital processing is highly flexible, computations need to be performed at the full modulator sample rate, i.e., several times larger than the signal bandwidth [9], potentially reaching beyond 10 GS/s [10]. Parallel implementations are possible, but the computational cost is at best the same [2]. Hybrid linearization approaches have also been proposed as a way to reduce the DPD complexity by performing coarse linearization in the analog domain [11]–[13]. Although the constituent APD and DPD circuits can be simplified compared with the “pure” cases, this approach requires both additional analog hardware and digital computations at the full sample rate.

In this work, we present a novel linearization approach that utilizes a non-linearly scaled RF-DAC to compensate for the non-linearities of the combination of the RF-DAC with a PA driven by it. For the evaluation, a moderate output power CMOS PA is used, but the concept is also applicable for

Fig. 1. (a) A schematic showing the transmitter concept used as base for the evaluation. (b) A schematic of the unit cell topology used in the RF-DACs, parts in gray are modelled using a high-level model. (c) A schematic of the PA used to evaluate the linearization. Segments S1–S8 are scaled as in Fig. 3.
higher-power PAs in other technologies. Segmented non-linear RF-DACs have been previously demonstrated to linearize the compression effects in the RF-DACs themselves, both in the low gigahertz range [14] and for a complete Cartesian IQ-modulator at mmW frequencies [10]. Simulations show that excellent overall linearization of the DAC/PA combination can be achieved over a large range of DAC and PA parameters, without modifying the RF-DAC segment scaling. Furthermore, the new concept needs no additional analog hardware, nor any additional computations in the digital domain. The approach is therefore highly attractive in wideband mMIMO applications.

II. SYSTEM ILLUSTRATION

An illustration of the targeted transmitter topology is shown in Fig. 1a. Non-overlapping quadrature LO signals are generated and fed to two segmented non-linear RF-DACs, followed by a gain stage and finally the PA. The RF-DACs are based on the topology presented in [10] and are modelled using a 22 nm FDSOI CMOS process. The unit cell topology, used to realize the RF-DACs, is shown in Fig. 1b. The gain stage $G$ is introduced to model PAs with similar non-linear characteristics but different input power requirements. In an actual implementation, this gain stage may be omitted.

A PA prototype, designed for 16–32 GHz in the same process, is employed to verify the proposed linearization concept. A schematic of the PA is shown in Fig. 1c. The PA uses a stacked configuration to achieve higher output power. The NMOS transistors have 64 fingers, with a gate length and width of 18 nm and 2 µm, respectively. The PA is biased in class-AB mode, with a gate bias ($V_{G1}$) of 350 mV and a nominal $V_{DD}$ of 1.8 V. The PA is used at several supply voltages and bias points, which significantly affects its AM/AM and AM/PM characteristics, as shown in Fig. 2.

III. LINEARIZATION

A. Static PA linearization

The AM/AM and AM/PM characteristics describe the PA static non-linear input/output behavior. A static predistorter aims to invert the PA AM/AM and AM/PM characteristics [15] and must therefore provide an expanding AM/AM mapping to counter PA compression. Since the AM/AM characteristic only changes slightly within the PA operating bandwidth, linearization can be realized for a range of frequencies. For the AM/PM distortion, it is sufficient to approach a constant phase for a range of input magnitudes, as a non-zero absolute value corresponds to a simple delay. In Fig. 2b, the phase is normalized to the value at a low input power level; in the following, we evaluate the maximum range of the corresponding functions for each bias case.

The PA characteristic, its inverse, the segmented DAC scaling, the output resulting from combining the segmented DAC with the PA, and the normalized cumulative DAC width, plotted versus DAC input code. The inset shows the error between the segmented DAC output magnitude and the inverse of the PA characteristic in LSB. These curves overlap in the main plot.
B. Linearization concept

The core design task for the proposed linearization scheme is to select a non-linear scaling for the RF-DAC segments. As a starting point, we have used the inverse of the PA characteristic when driven by a uniform RF-DAC. Fig. 3 shows the PA characteristic versus the DAC input code. The inverse of this characteristic is then used to compute the scaling of the 8 segments. Since the DAC itself will exacerbate the compression, as seen in Fig. 3, iterative improvements will be required to find a scaling that inverts the joint DAC and PA compression to approach a linear transfer. The resulting expanding function will be more pronounced than when compensating only for compression in the RF-DAC itself.

The selected non-linear segment scaling is chosen at design time, making it fixed in hardware. However, the RF-DAC bias enables adjustment of its transfer characteristic. Its compression is set by the supply voltage and the LO magnitude. Since DAC compression will counteract the expanding non-linear scaling, the overall transfer characteristic of the DAC may thus be adapted to approximate the inverse of the PA non-linearity. Figure 4 shows the output magnitude normalized (using the highest code) to the design point (the blue curve) versus input code for both DAC and DAC plus PA. The effect of an increased supply voltage is shown in Figs. 4a and 4b, for a fixed LO magnitude. The effect of an increased LO magnitude is shown in Figs. 4c and 4d for a fixed supply voltage. While the DAC in almost all cases provides an expanding non-linear output characteristic, the output from DAC plus PA can be made to show either expanding or compressing behaviour, depending on bias. The DAC AM/PM characteristic changes little with bias settings, so the overall AM/PM behavior cannot be tuned much with this approach.

IV. Evaluation

The proposed linearization concept has been evaluated through individual schematic-level circuit simulations of the key components: RF-DACs (excluding the LO generation) and PA. For the RF-DACs, the analog parts of the unit cells, shown in black in Fig. 1b, and the output matching network, realized using the balun and shunt capacitors, were included. The function performed by the gray parts was realized using a high-level model. For the PA, the entire circuit was included. The static AM/AM and AM/PM characteristics were simulated for both circuits; for the RF-DACs, this was done for all magnitude codes, while for the PA, an input range exceeding the RF-DAC output dynamic range was used. These results were then used to evaluate the linearization performance of the combined circuit. As simulations are based on the dominating quasi-static behaviour, the signal bandwidth has no effect.

The PA was simulated at its center frequency. With non-overlapping LO signals, I/Q cross-modulation distortion can be kept very small [10], making it possible to use individually-simulated RF-DACs. The quadrature LO signals were generated by ideal voltage sources, representing the non-overlapping pulses up to the third harmonic. For modulated signals, two DACs were combined to form a Cartesian IQ-modulator. We used 256QAM single-carrier signals, up-sampled 4 times using an RRC-filter (factor 0.2), to evaluate the linearization performance for modulated signals.

For the evaluation, all simulations used 8-segment 10 bit signed RF-DACs, with a size ratio of 2.685 between the largest and smallest segments. The normalized cumulative DAC width relative to input code is shown in Fig. 3; the slope gives the segment scale factor. Relative to a uniform DAC with the same minimum unit cell, this scaling increases the total DAC transistor width by 62 %. This is the only potential change in hardware cost brought by this linearization method. The segment scaling may be realized using the same total DAC transistor width as used for the uniform DAC, forcing the use of a smaller minimal unit cell size. However, this would, as for an APD, result in a reduced overall gain.

A. Linearization at nominal bias condition

The nominal bias settings used to derive the DAC scaling were an LO magnitude of 250 mVpk-pk and a DAC supply voltage of 0.9 V. Fig. 5 shows output signal spectra when driving the PA ($V_{DD} = 1.8$ V), at equal output powers with segmented and uniform DACs. Spectra for the outputs of the segmented and uniform DACs are also shown for identical digital inputs. The segmented-DAC output shows bandwidth expansion due to the non-linearity; yet, out-of-band emissions after the PA are clearly reduced with the segmented DAC.

In Table I, the error-vector magnitude (EVM) and adjacent-channel power ratio (ACPR) achieved with the uniform and segmented scaling are presented at two different operating points: the design point used to derive the scaling.
(that also gives optimum static performance), and the point resulting in the best modulated performance at a fixed supply voltage. From the table, we can observe that the EVM and ACPR improvement increases with increased PA compression. With the uniform DAC, the reduced PA compression is a result of higher code density for the upper range, giving a reduced peak-to-average power ratio. The segmented DAC provides a uniform code-to-magnitude spacing across the full range.

B. Linearization across DAC bias settings

Based on Fig. 4, it is clear that the DAC supply voltage and LO magnitude allow us to adapt the non-linear characteristics of the segmented DAC. Figures 6a and 6b shows static and modulated performance for various combinations of LO magnitude and DAC supply voltage. The nominal design point is marked with a white marker. The red overlaid contours show the PA compression, calculated as the small-signal gain minus the gain achieved using the highest DAC code.

The performance was also evaluated with modulated signals to analyse the influence of magnitude and phase non-linearities. EVM and ACPR is shown in Figs. 6c and 6d. As the DAC output power depends on the bias conditions, we can achieve good linearization across a range of output power levels. The phase dependence is however weak, as seen in Fig. 6b. Finally, note that modulated performance is less sensitive to bias settings than static performance is; in the following, we focus on the latter.

C. Linearization across DAC output power

From a system-design perspective, it may be desirable to re-use a certain RF-DAC component across a family of PAs for different requirements. To model this situation, the transmitter concept (Fig. 1a) includes a gain parameter G which changes the PA input power requirement. The static performance for G = ±5 dB is shown in Fig. 7. With a reduced gain, a larger DAC output power is required; thus, the optimum is shifted toward larger LO magnitudes, as seen in Figs. 7a and 7b. Correspondingly, with an increased gain, a lower DAC output power is required, shifting the optimum towards using lower LO magnitudes, as shown in Figs. 7c and 7d. Since the nominal DAC compression contribution depends on the LO magnitude, the amount of PA compression that can be compensated for is also affected. Importantly, still good linearization performance.

D. Linearization at different PA bias conditions

For efficient operation, also at reduced peak output power, it is desirable to reduce PA supply voltage, which however changes the PA characteristics as seen in Fig. 2. Fig. 8 shows the static performance for PA supply voltages of 1.2 V and 0.8 V (significant reductions from the nominal 1.8 V). We can...
observe that the changed non-linear PA characteristic does not have a significant impact on the achieved linearization, even though the PA AM/AM behavior at the lower supply voltages is quite different compared to the nominal design point. Since a reduced PA supply voltage results in slightly increased compression for a given input level, it is expected that optimum linearization is achieved at reduced LO magnitudes.

Reducing the PA supply voltage to 0.8 V results in a 5.3 dB output power reduction when a constant input power is provided. When also accounting for the changes in DAC output power resulting from adapting the linearization, a 7.1 dB peak power back-off can be achieved while keeping the DAC supply voltage at 0.9 V. By reducing the DAC supply voltage, an even larger back-off range can be achieved.

Throughout our evaluation, we have observed a similar relationship between the static and modulated performance as shown in Fig. 6 also for the other cases; but figures are omitted for clarity reasons, as we believe they will not add anything to the discussion. Figures showing the modulated performance are available in [16].

V. DISCUSSION

The proposed linearization concept enables operation of an RF PA deeper in compression while retaining usable performance in terms of ACPR and EVM, without any additional components on either side of the analog/digital interface. In comparison, a DPD may require a higher DAC resolution in addition to the high computational effort. This is since digitally expanding a quantized signal before compressing it in the analog domain results in a higher code density for the upper range, at the cost of a reduced code density in the lower range, where the majority of the samples will be for a modulated signal with a high peak-to-average power ratio (PAPR). In contrast, the segmented expanding non-linear DAC combined with a non-linear PA provides a uniform code density throughout the entire range.

The evaluation is based on two RF-DACs in a Cartesian configuration, where cross-modulation is minimized through the use of non-overlapping LO signals. This is important, since the linearization does not address cross-modulation as it is applied separately to the two signal paths. An output power combiner would allow sinusoidal LO signals, which could extend the applicability of the principle to higher frequencies. The linearization performance for modulated signals using the Cartesian topology is limited by the 1D linearization that brings in slightly degraded linearization performance for symbols in the constellation corners. The shallow optimum observed for modulated signals in Figs. 6c and 6d is a result of this limited linearization performance. A polar configuration would avoid both the cross-modulation problem and the degraded linearization performance; the linearization concept should be readily applicable also in this case.

The presented linearization approach is capable of linearizing the static non-linearity. It cannot be used to compensate for any fast dynamic non-linearities. Although no simulations have been performed using wideband signals, we expect that memory effects in the RF-DACs and/or PA will limit the achievable bandwidth.

This publication includes investigations only for a CMOS PA of moderate output power, but we believe the concept can be useful also with a higher-power PA (with adaptations).

VI. CONCLUSION

In this paper, we present a novel linearization concept that is capable of linearizing PAs at no additional hardware cost, neither in the analog domain nor in the digital domain. Through simulations, we have demonstrated excellent linearization over a large range of bias conditions, both for the RF-DACs and for the PA, thus showing the robustness and flexibility of this approach. Although modulated performance has been evaluated using a Cartesian IQ-modulator, the principles can also be applied to a system using a polar IQ-modulator. In addition, the concept also relaxes the requirement for the modulator resolution as no additional resolution is needed for the DPD.

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