THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

GaN-based HEMTs for Cryogenic Low-Noise Applications

Mohamed Aniss Mebarki

Department of Space, Earth and Environment

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Mohamed Aniss Mebarki

Department of Space, Earth and Environment
Chalmers University of Technology
SE-412 96 Gothenburg
Sweden
Telephone + 46 (0)31-772 1000

Cover description

Top left: photo of the cryogenic setup used for the microwave noise characterization, with illustrated indication of the reflection coefficient from the input network allowing to reach the best noise performance. A magnification of a fixture with a GaN HEMT is shown below.

Bottom left: photo of the GaN HEMT under the microscope, while being characterized using the probe station.

Top right: Calculated constant noise figure circles around the optimum impedance allowing the best performance of different GaN HEMTs at the cryogenic temperature of ~10 K, all plotted in the Smith chart.

Bottom right: calculated optimum noise temperature and optimum power dissipation at the cryogenic temperature of ~10 K of different GaN HEMTs with varied gate width.

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MOHAMED ANISS MEBARKI

Group for Advanced Receiver Development - GARD
Department of Space, Earth, and Environment
Chalmers University of Technology

Abstract

Radio-astronomy deals with signals and radiations of extremely weak intensity. Also, it requires robust and rugged technologies able to sustain and prevent the Radio Frequency Interferences (RFI). Complying with the required high sensitivity, Low Noise Amplifiers (LNAs) operating at cryogenic temperatures are key elements in radio astronomy instrumentation. Thus far, advanced semiconductor technologies but with limited power-handling capabilities have been traditionally employed as LNAs. Over the past decades, Gallium Nitride (GaN)-based high electron mobility transistors (HEMTs) were demonstrated at room temperature to offer a combination of both excellent low-noise operation and a superior high-power handling performance compared to other materials. In addition, a number of studies indicated a promising potential for the GaN technology to operate at cryogenic temperatures. However, the cryogenic noise performance of the GaN-HEMTs remained unexplored so far.

This thesis investigates the potential of GaN–based HEMTs for low-noise operation at these cryogenic temperatures. Established characterization and modeling approaches were employed for this purpose. As a main result, this work reveals a first estimation of the noise performance of GaN-HEMTs at cryogenic temperatures of ~10 K which compares to other more advanced technologies in this field. This was achieved through the extraction of a model, based on experimental noise measurements, describing the microwave noise behavior at cryogenic temperatures at the device level. The model predicts the noise contribution of GaN-HEMTs at cryogenic temperatures with respect to the frequency of operation, the dissipated power, and the total periphery of the device. Hence, it constitutes the basis for the design of future GaN-based LNAs which fulfill the different requirements set by the demanding cryogenic applications.

The extracted cryogenic noise model was used to identify and analyze the role of the different physical parameters of the device, over which a technological control might be possible in the future in order to improve the assessed noise performance of the cryogenic GaN-HEMTs. From that perspective, GaN-HEMTs featuring superconducting Niobium (Nb)-gates were demonstrated for the first time. The successful integration of superconducting Nb-gates into AlGaN/GaN HEMTs was demonstrated on different samples, showing a suppression of the gate resistance independently of the width and length of the gate below a critical temperature T_c < 9.2 K. The superconductivity of the gate leads to the cancellation of the associated noise contribution. Comparing the noise performance of the resulting devices to that of the conventional Gold (Au)-gated GaN-HEMTs, it was concluded that further management of the device's self-heating is required to enable the full potential of the Nb-gate by maintaining its superconductivity while operating at optimum-noise bias conditions.

Key words: *Gallium Nitride (GaN), High Electron Mobility Transistor (HEMT), superconductivity, Niobium (Nb), Cryogenic temperatures, high frequency, Low Noise Amplifier (LNA), Radio-astronomy, RFI.*

List of Publications

Appended Papers:

This thesis is based on the following papers:

[A] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "Noise Modeling of AlGaN/GaN HEMT at Cryogenic Temperatures, *IEEE Transactions for Transactions on Microwave Theory and Techniques*, 2022. Accepted for publication.

[B] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Pavolotsky, A., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "GaN HEMT with superconducting Nb gates for low noise cryogenic applications", *Physica Status Solidi A*, 2022. Accepted for publication.

[C] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "A Cryogenic Scalable Small-Signal & Noise Model of GaN HEMTs", *Proceedings of the 32nd IEEE International Symposium on Space Terahertz Technology (ISSTT)*, 2022.

Other Papers:

The following publications are not appended at the end of the thesis due to overlapping content or due to content not related to the thesis:

[I] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Pavolotsky, A., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "GaN HEMTs with superconducting Nb gates for cryogenic Low Noise applications", *Compound Semiconductor Week (CSW)*, 2022, pp. 1-2.

[II] López, C.D., Mebarki, M.A., Desmaris, V., Meledin, D., Pavolotsky, A.B. and Belitsky, V., "Wideband Slotline-to-Microstrip Transition for 210–375 GHz Based on Marchand Baluns" *IEEE Transactions on Terahertz Science and Technology*, vol. 12, no. 3, pp. 307-316, 2022.

List of Abbreviations

DC	Direct Current
DSB	Double Side Band
GHz	Giga Hertz
THz	Terahertz
FET	Field Effect Transistor
HEMT	High Electron Mobility Transistor
2DEG	2-Dimensional Electron Gas
ENR	Excess Noise Ratio
IF	Intermediate Frequency
MIC	Microwave Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
Al	Aluminium
Cu	Copper
Au	Gold
Nb	Niobium
HEB	Hot Electron Bolometer
SIS	Superconductor Insulator Superconductor
IF	Intermediate Frequency
RF	Radio Frequency
RFI	Radio Frequency Interference
SEM	Scanning Electron Microscope
Si	Silicon
SiGe	Silicon Germanium
GaAs	Gallium Arsenide
GaN	Gallium Nitride
AlGaN	Aluminium Gallium Nitride
InP	Indium Phosphide
LNA	Low Noise Amplifier
RT	Room Temperature
VNA	Vector Network Analyzer
TCAD	Technology Computer Aided Design

Contents

1. Introduction

The progress in science relies most often on the achievements in instrumentation technology. This is particularly valid for the radio-astronomy. In this field, the observation of objects and matter located far-away from the planet Earth and beyond is of interest. Using radio-telescopes, the information on which are based such studies are presented in the form of electrical signals. Because these signals travel a long distance before reaching the observation point, and due to the presence of different attenuation factors along the way, the detected intensity is typically very weak. Hence, an instrumentation of extreme sensitivity is required by the scientists in this field. The sensitivity can be defined as the minimum signal variation that can be detected by a radio-astronomy receiver. Noise is a major limitation of the sensitivity of the radio-astronomy receivers. The environment itself with which deals the instrumentation in radio-astronomy introduces a limitation to the detection of signals due to the surrounding noise, usually referred to as the "sky-noise limit" [1]. While the latter form of noise is undistinguishable from the signal and could not be reduced, the electronic noise inherent to the operation of the system can be influenced by technology developments.

Electronic noise refers to the spontaneous fluctuations of voltages or currents in a circuit. At a microscopic level, it corresponds to random motions and processes involving the charge carriers. One common metric to quantify the noise is the noise temperature, given in Kelvins [K]. The concept of noise temperature derives from the consideration that a source of noise within a certain frequency-band can be presented as a radiation of a black body at such an equivalent temperature, T_e, that it radiates the same amount of noise-power within the same bandwidth. Hence, the definition of the equivalent noise temperature, T_e:

$$T_e = \frac{P_n}{k_B B} \tag{1}$$

Where P_n is the noise power, k_B is the Boltzmann constant and B the frequency-bandwidth. A lumped resistor presents an equivalent noise temperature equals to its physical temperature. In the case of an amplifier, the prior consideration implies that it can be seen as a noiseless device matched to an equivalent source of noise at its input. The source delivers the same noise power that would be measured at the output of the noisy amplifier. Hence, the source of noise can be seen as a resistor at an equivalent temperature T_e which characterizes the noise contribution of the amplifier.

Another common metric is the noise figure, noted NF and given in decibels [dB]. The noise figure relates to the noise temperature by:

$$NF = 10 \log_{10} \frac{T_e}{T_0} \tag{2}$$

Where T_0 = 290 K, a reference noise temperature. The linear form of NF is called the noise factor, and is equivalent to the ratio of the signal-to-noise levels at the output and input of the element.

In order to assess the limitation introduced by the electronic noise, it can be illustrative to consider a common figure of merit evaluating the sensitivity of a radio receiver, noted S and given by [2]:

$$S \propto \frac{A_{eff}}{T_{sys}} \tag{3}$$

Where T_{sys} is the equivalent noise temperature of the system, A_{eff} is the effective signal-collection area determined by the telescope dish antenna. From equation (1), reducing the noise temperature of the system allows to improve its sensitivity. The effective collection area can be optimized by either increasing the size of the antenna or by forming arrays of receivers which outcomes can be analytically combined to form a single output. Ultimately, the development of any radio-astronomy receiver is conditioned by that of the low-noise technologies.

Figures 1-a and 1-b show schematic illustrations of the receivers in radio-astronomy. Two common configurations of the receivers are presented. In both configurations, two main parts can be distinguished: the front-end and the back-end. The latter is dedicated for the processing and the detection of the information of interest from the received signal. It is the front-end part which deals first with the radiation, or the signal. Thus, equation 3 mainly applies to this part to assess the performance of the system.

Figure 1: Illustration of typical radio-astronomy receivers. a) configuration used for frequencies up to around 100 GHz b) configuration used for above 100 GHz.

It is seen from Figures 1-a and 1-b that the front-end receiver is constituted of a chain of cascaded elements. The overall noise contribution of such a system is calculated using the Friis equation, which is expressed for any system of n cascaded elements as:

$$T_{sys} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \cdots + \frac{T_n}{G_1 G_2 \ldots G_{n-1}} \tag{4}$$

Where the indices $(1 - n)$ refer to the position of each element with respect to the direction of the signal-incidence. Hence, the noise contribution of an element is further impactful when placed prior to a Low Noise Amplifier (LNA), as the amplification of the latter reduces the contributions of the subsequent elements in the chain. Together with equation (3), equation (4) motivates the efforts towards the optimization of the noise performance of the LNAs and the quest for a better understanding of their physical origins and limitations.

For the detection of signals of frequencies up to around 100 GHz, the receivers presenting the configuration in Figure 1-a are usually preferred. In this configuration, the overall noise performance of the system is dominated by that of the first LNA since it occupies the frontmost position after the antenna. The influence of the subsequent elements is, according to equation (4), reduced by the factor of gain. The

state-of-the art of LNAs nowadays present a factor of 3 to 5 times the fundamental quantum limit of noise, defined as: $\frac{hf}{k_B}$ [3] [4]. The quantum-noise limitation applies to the overall noise performance of the receiver. However, depending on the operation of the mixing element its definition differs. The latter definition ($\frac{hf}{k_B}$) applies when the mixer is in a Single Side-Band mode of operation, i.e. when the frequency-image of the Radio Frequency (RF) signal presented at the input of the mixer is filtered-out. Otherwise, in Double Side-Band (DSB) mode, the quantum limit of noise becomes $\frac{hf}{2k_B}$.

The use of the receiver configuration in Figure 1-b is prevalent for the detection of ultra-high frequency signals, typically around the sub-THz range and beyond. This is because electronic amplifiers that might be capable to efficiently process such high-frequency signals, without noise penalty, are so far not available. Instead, a mixer is placed directly after the antenna in order to down-covert the upcoming signal to lower frequencies, referred to as Intermediate Frequencies (IF). At these frequencies, the signal is then treated by a dedicated amplifier while ensuring the lowest possible noise contribution. The development of superconductor-based mixers allowed the noise performance of these elements to further approach the fundamental quantum limit of noise. Two superconducting-technologies are predominant for the mixers with the lowest-noise requirement: the Superconductor–Insulator–Superconductor (SIS) mixers and the Hot Electron Bolometers (HEBs). While the SIS based mixers offer a superior noise-performance compared to HEB, it is limited by a material property that prevents it from operating above a gap frequency which is specific for the particular superconductor material. In the case of SIS based on Niobium (Nb), for instance, this frequency limit is typically about 0.7 THz [5] [6]. On the other hand, the HEB, being based on a fundamentally different mode of operation than SIS, does not present any theoretical limitation on the maximum frequency of operation. However, it does present a physical limitation on the IF bandwidth that can be delivered to the subsequent amplifier. Nevertheless, most recently, the GaN-material properties were demonstrated to offer new possibilities to improve the IF bandwidth of the HEBs [7].

Aside to a required high sensitivity, another concern for the radio-astronomy applications is the dynamic range of the signal's detection. Since the saturation power-level of the mixers is usually limited, when the LNA is at the frontmost position of the system (Figure 1-a) a larger dynamic range and a wider IF bandwidth can be obtained compared to the configuration in Figure 1-b [4]. In fact, while efforts are continuously focused towards increasing the RF and IF bandwidths of the receivers, certain unwanted signals may interfere within the frequency-bands of interest. This phenomenon is usually referred to as Radio-Frequency Interferences (RFI) [2]. Also, either intentionally or unintentionally, signals of relatively high power may be detected by the receivers. While the LNAs with the lowest noise contributions are so far predominantly obtained using III-V materials, these materials are known to present relatively low-power handling capabilities linked to their inherent properties [8]. Thus, these unwanted interfering signals might be harmful, and even destructive, for the LNAs based on these materials. Hence, it is required a technology that ensures both high sensitivity and reliability of the system to release the challenges imposed by the RFI. Such a technology might be simultaneously competitive in terms of low-noise performance while still offering higher-power capabilities.

Besides, other modern applications operating at cryogenic temperatures are also increasingly requiring wideband LNAs with decent power performance. Typically, these applications deal with discrete signals

that might be of relatively large power. Such applications concern the readout of microwave kinetic inductance arrays [9] and the readouts used in quantum-computing systems [10].

1.1. The HEMT technologies for low noise applications

The electronic low-noise amplification was historically relying on the parametric amplifiers and the Field-Effect Transistors (FETs), until the late 1970s. A major technological breakthrough in this field occurred during that latter period, coinciding with the advent of the high electron mobility transistors (HEMTs) [11]. The electrical operation of the HEMTs relies on the same principle as that of the FETs, as will further detailed in chapter 2. In contrast to the conventional transistors available at that time, the HEMTs offer a remarkably higher-speed microscopic transport of the charge carriers which translates into an optimized high-frequency operation and most notably a reduction of the noise temperature. This performance is owing to the spatial separation of the electrons flow from the ionized dopants in the structure, which yields a confinement of a high density of carriers in a thin channel-layer where they can benefit from a largely improved mobility. The channel obtained from the confinement of the carriers can be seen as a triangular quantum well, or a 2-Dimensional Gas of Electrons (2DEG). This was achieved through the engineering of the materials' energy-bands, involving heterojunctions of the III-V type of compound semiconductors. The material properties on which are based these devices, as well as their physical geometry, are the most determinants of their overall performance. The first HEMT was based on the Gallium Arsenide (GaAs) material. Another III-V material, the Indium Phosphide (InP), was later incorporated into the same type of structures. The InP devices presented even better performance compared to their GaAs counterparts.

It is only in 1993, that a Gallium Nitride (GaN)-based HEMT was proposed and its practical operation demonstrated [12]. The first motivation behind the development of the GaN technology was the fact that the breakdown voltage, or the maximum electrical biasing that maintains the safe operation of the device, is related to the characteristic energy bandgap of the material on which it is based. Presenting a bandgap energy typically around 3 times larger than that of both InP and GaAs bulk materials, the GaN inherently offers a superior high-power performance. As will be further discussed in chapter 2, the GaN-HEMTs formation presents a technological difference compared to the other semiconductor devices which is that it does not require any intentional doping of the material.

Table 1: Summary of the physical properties of Si, GaAs, InP and GaN bulk materials, at room temperature. The data were compiled from [8] [13]:

	SiGe	SiC	GaAs	InP	GaN
Electron mobility $[\mathrm{cm}^{-2}/\mathrm{Vs}]$	1500 – 2800	700	8500	5400	900 – 1100
Electron saturation velocity $[\times 10^7\ cm/s\ ]$	0.1 – 1	2	1 - 1.3	1.9	1.5 – 2.3
Dielectric constant	14	9.7	12.9	12.5 – 14	8.9
Bandgap energy [eV]	0.94	0.945	1.41	1.35	3.49
Thermal conductivity $[\mathrm{W/cm-K}]$	1.5	3.5 - 4.5	0.5	0.7	1.3 – 1.5

In terms of the microwave and low-noise operation, from the material aspect, any HEMT's performance is determined by both i) a high channel conductivity and ii) a high electron velocity. The channel conductivity is proportional to both the electron mobility and the 2DEG density. Both the bulk GaAs and InP materials present a higher electron mobility compared to GaN. However, the HEMT technology based on the latter show a larger electron density. Typically, an electron density of $2 - 4 \times 10^{12} cm^{-3}$ is obtained in GaAs and InP devices against $1 - 1.9 \times 10^{13} cm^{-3}$ in GaN-HEMTs. Hence, the resulting sheet conductivity in the GaN devices is to some extent compensated by the larger 2DEG density and is comparable to that in other technologies. The electron's saturation velocities are of the same order of magnitude for all these materials. Table 1 summarizes and compares the physical parameters, at room temperature, of the materials on which are based the main semiconductor technologies.

Taking advantage of the physical properties reviewed above, the GaN technology evolved quite rapidly after its invention. Its superior power-handling potential qualified it nowadays as the application of choice for power applications. On the other hand, its excellent high-frequency and low-noise performance makes it suitable to build extremely reliable and robust low-noise amplifiers (LNAs). For room temperature operation, as recently reviewed in [14], the performance of GaN-based LNAs are now competitive with other technologies up to the sub-THz range. Simultaneously, they offer superior high-power capability which releases the need for additional protective or power-limitation devices.

1.2. Cryogenically cooled HEMTs for low noise applications

The operation of the HEMT technologies at cryogenic temperatures was rapidly demonstrated of remarkable interest for low-noise applications right after its advent. The first cryogenic LNA based on the HEMT technology was specifically developed for a radio-astronomy receiver in 1985 [11]. A year after, using the same receiver, this successful integration led to the discovery of new interstellar molecules located 400 light-years away [15].

The improvement of the HEMTs' performance when cooled-down can be explained by the fact that, with respect to RT, the mobility of the electrons becomes significantly larger. This leads to enhanced and higher-speed electrical transport. Also, the electrical conductivity of the materials increases. A reduced contribution of the parasitic resistances and that of the interconnects is then obtained. Moreover, the phenomenon of superconductivity that features certain materials used in the application-systems implies an interest in the cooling of the entire chain including the LNAs. This is due to the fact that the enabling of the resistance-less state inherent to these materials is conditioned by a specific critical physical temperature. The latter is, for instance, around 9.2 K for Niobium (Nb). Besides, the thermal conductivity of the materials usually increases at low temperatures allowing a larger integration of the different components and reduces the self-heating effects inherent to the active devices.

Thus far, Indium Phosphide (InP)-based devices are the technology of choice for ultra-low noise applications at cryogenic temperatures [3]. The GaAs-based cryogenic HEMTs usually present a slightly higher noise temperature, but are still costs-effective and competitive at relatively high-frequency and wide-bandwidth conditions. Besides, Silicon-Germanium (SiGe)-based also present a potential for cryogenic low-noise operation. The noise temperature of SiGe-based LNAs is usually relatively higher than those based on III-V materials, but are competitive in terms of low-power dissipation requirements [16].

However, to date, the noise performance of the GaN-based LNA technology at cryogenic temperatures remain nearly unexplored. Indeed, so far, only few studies investigated the static and microwave characteristics of the GaN technology at cryogenic temperatures [17] [18]. The conclusions from these works converge towards an overall improvement of the performance of GaN HEMTs when cooled down. In particular, it has been experimentally verified for different GaN heterostructures that both the electron mobility and the sheet conductivity in the 2DEG substantially increase at cryogenic temperatures compared to room temperature [19] [20] [21]. However, in order to know the best noise performance that can be achieved by the GaN-HEMTs, it is required to perform a study and develop a model that describes the microwave noise behavior of the GaN device at the targeted temperature of operation. It is one of the main purposes of this thesis to address this so far lacking information in the literature, as will be further introduced in the next section.

1.3. Motivations and outline of the thesis

Based on the discussion above, the development of cryogenic GaN-based LNAs can be of benefit to address the requirements set by modern and next-generation of cryogenic low-noise applications, and radio-astronomy receivers in particular. This is considering both configurations represented in Figure 1-a and 1-b. First, as it was shown in [22], the noise in HEMTs remain nearly constant below a certain temperature of around 15 - 10 K since no further improvement of the mobility might be expected. Thus, using a HEMT as a first stage for the detection of relatively low-frequency signals may release the requirement imposed by using superconductor materials to reach lower temperatures, e.g. 4K. This is of interest especially knowing that the cooling power is usually limited at these low temperatures. From that perspective, using a GaN-based LNA at the first stage of the receiver (Figure 1-a) would offer an advantage compared to the InP and GaAs technologies knowing the superior power-handling capability of GaN. Indeed, a larger power dynamic range could be obtained in this case. This may address and prevent the limitations related to the RFI and the unwanted high-power signals. On the other hand, considering the configuration in Figure 1-b, the promising HEBs' performance resulting from the incorporation of the GaN material offer the possibility for a monolithic integration with GaN-based LNAs. This would be of interest from the technological perspective, improving the manufacturing repeatability and the yield of the receivers.

The assessment of the GaN technology integration into radio-astronomy instrumentation applications is still conditioned by an effective modeling and estimation of its minimum noise contribution at the different physical temperatures, frequency and power dissipation. Hence, a main objective of this thesis is to provide a first estimation of the minimum noise temperature of GaN-HEMTs at around 10 K.

Such an estimation requires the retrieval of a model parameters able to describe the cryogenic noise behavior of the device. Also, when this model is related to the physical parameters of the device, it may also provide novel insights on the possibilities to optimize the GaN technology for the targeted applications.

Furthermore, as the radio-astronomy receivers already include superconducting materials operating below their critical temperatures, the integration of superconducting electrodes of GaN HEMTs would minimize the associated thermal noise.

After the first introductive chapter, this thesis is structured as follows:

- Chapter 2: Deals with the general physical principles defining the operation of the GaN devices. The cryogenic static and microwave characteristics of the technology are presented and analyzed.
- Chapter 3: Provides an overview of the existing technologies for cryogenic low-noise applications, their state of the art and the added value of the GaN technology in this field. After showing the necessity for an accurate modeling of the cryogenic noise behavior, the approaches from both the physical and analytical standpoints to proceed with that task are presented.
- Chapter 4: Presents the general procedure to measure and extract the noise characteristics of the device at cryogenic temperatures.
- Chapter 5: Presents a summary and analysis of the cryogenic noise model extracted through this thesis. Putting into perspective the possibility for further technological improvements, the extracted noise model is used to study the possible added values from the improvements of the different sources of noise in the device. Finally, from the same perspective, the results and discussion of the attempted development of GaN-HEMTs with superconducting-Nb gates are presented.
- Chapter 6: summarizes the conclusion from this thesis and discusses the works that can be completed in the future.

2. The GaN-Based Technology

In this section the physical properties of the devices are presented. Focused on their cryogenic behaviour, the typical characteristics of the static and microwave operation are presented. From the perspective of future adjustments of the technology for improved cryogenic low-noise operation, the effects of different physical aspects on the intrinsic small-signal parameters of the device are studied.

2.1. Physical principles

GaN HEMTs are obtained by the heterojunction of a GaN layer with a barrier layer made of an alloy of a group-III and nitrides (III-nitrides) material. As any FET, a fundamental feature in the GaN HEMTs is the presence of a lateral path where the electrical current can flow further referred to as the channel [23].

The formation of the channel of electrons occurs in the GaN side of the barrier/GaN heterojunction. It results from the discontinuity in the energy-band diagram, which arises at the interface. Anderson's rules, introduced in 1962 [24], can be used to describe the corresponding energy-bands profile. It states that the difference of the two materials' electronic affinities determines an offset of the conduction-band. The electronic affinity, defined as the difference between the bottom energy-level of the conduction band and the vacuum level, is a material constant. Knowing the conduction band-offset, a valence band-offset is derived from the difference in the materials' bandgaps. The GaN material presenting a lower electronic affinity compared to that of the barrier, the conduction band falls below the Fermi level in the GaN side of the heterojunction. This gives rise to a quantum well, i.e., quantized sub-bands, where the carriers could be confined close to the interface. Hence, the term of two-dimensional gas of electrons (2DEG) to refer to the channel as in this case the carriers would be able to move within only 2 directions.

While in other technologies, the carriers are introduced by doping, the presence of the latter at the barrier/GaN interface is due to one of the specific material properties: the existence of an inherent polarization. In fact, the net polarization at the interface is a combination of 2 types of polarizations: spontaneous and piezo-electric. First, all the III-nitrides materials present a spontaneous polarization. In the case of GaN, this is due to the larger electronegativity of the Nitrogen (N) compared to that of the Gallium (Ga) atoms. Given the asymmetric nature of the material crystalline structure, an electric dipole moment results along the direction of the growth. The vector of the resulting spontaneous polarization is then pointing either towards the surface or the substrate, respectively depending on whether N or Ga is present at the surface. Thus, referring to these cases as N-polar or Ga-face GaN, the sign of the respective spontaneous polarization (P_{GaN}^{sp}) is either positive or negative. Ga-face GaN is the most common and has so far benefited from relatively more maturity compared to the growth with the second type of polarity [25] [23]. Hence, Ga-face GaN is considered throughout this thesis.

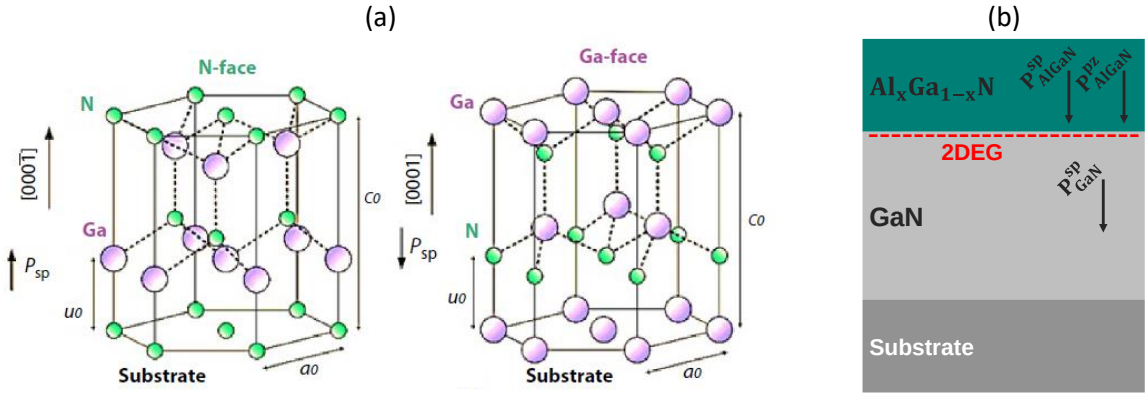

Figure 2: a) illustration of the lattice structure of GaN with Ga-face and N-face polarity – after [26]. b) illustration of ($AlGaN$/Ga-face GaN) heterojunction with the polarization-induced 2DEG in the GaN layer.

In addition, a piezoelectric polarization is present at the barrier side of the heterojunction's interface. This is due to the lattice mismatch between the barrier and the channel layers and given the fact that the barrier undergoes a mechanical strain [8]. The sign of the piezoelectric polarization depends on the nature of the strain; negative when tensile and positive for a compressive one. Considering $Al_xGa_{1-x}N$ barrier, with x the mole fraction of Aluminium (Al), a tensile strain was experimentally assessed in this case resulting in a piezoelectric polarization. Hence, noted respectively P^{pz}_{AlGaN} and P^{sp}_{AlGaN}, the piezoelectric and spontaneous polarizations in the $Al_xGa_{1-x}N$ layer are of the same sign as illustrated in Figure 2. The relatively thick GaN layer is usually considered as free of strain; it does not present a piezoelectric polarization.

Correspondingly, a polarization-induced charge density at the interface of the $Al_xGa_{1-x}N$/GaN heterojunction arises from the difference of the polarizations in both layers. The extraction of the spontaneous and piezoelectric polarization in the III-nitrides materials was proposed in [27] using linear interpolation-based approximated formulas, derived from first-principles analysis and function of the respective mechanical properties of the materials. An analytical description of the polarization-induced sheet carrier (2DEG) concentration in the different III-Nitrides heterostructures, considering their geometrical and physical properties, was provided in [28] and extensively verified against experimental results. Although the presence of the carriers at the heterojunction interface is explained by the inherent net polarization, their primary origin is subject to a theory introduced in [29] which is since then commonly adopted. It suggests that electrons are provided by donor-like states present at the surface of the hetero-structure.

In the following, the physical principles introduced above are illustrated through the structures studied in [A] and [B]. Figure 3 presents an illustration of the cross-sectional view of the epitaxial structure of the device.

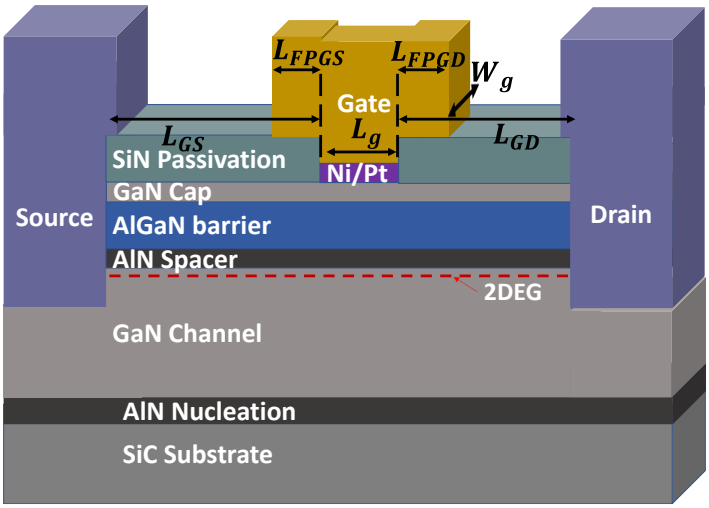

Figure 3: cross-section view of the epitaxial structure of the studied devices

These devices are based on SiC-substrate template, with an AlN nucleation layer facilitating the growth of the GaN buffer layer. The latter is Fe-doped to ensure its electrical insulation [30]. The GaN channel and the AlGaN barrier are separated through an AlN spacer layer. Since the spacer has a larger bandgap than the barrier, it helps limiting the extension of the electrons wave-function towards the opposite side of the GaN-channel layer and supports the 2DEG confinement [31]. The barrier is made of 29 % Al mole-fraction. The structure is capped with a thin (2 nm) GaN layer, which is beneficial for the reliability of the device [32]. The spacer, the barrier and the cap layers are unintentionally doped (u.i.d). On the top surface, a passivation is provided by an SiNx layer. The passivation has a protective function towards the top layers of the device and helps to reduce the surface-related defects and trapping effects [33] [34]. An overview of the latter is introduced in a next section.

2.1.1. Physical simulations

Figure 4 shows the calculated profiles of the energy band-diagrams and electron density at physical temperatures ranging from 300 down to 5 K, through a vertical cutline along the device. The simulations were obtained using Sentaurus TCAD software based on the finite elements method (FEM). The results shown in Figure 4 support the theoretical foundations explaining the formation of the channel in the studied GaN-HEMTs, as described earlier; at the interface. Moreover, from the physical simulations at cryogenic temperatures two fundamental conclusions can be drawn:

1. First, no freeze-out of the carriers is observed. This is, thus, supporting a primary qualification of the GaN technology for cryogenic applications. It also points out their advantage over other semiconductor-doped technologies such as Silicon (Si)-based ones, which typically suffer from a dramatic drop of the carrier density at low temperatures [35] [36].
2. Second, the carrier density remains almost constant with temperature as less than 0.8 % variation on n_s was estimated between 300 and 5 K. This simulation result is in good agreement with the experimental ones reported for other GaN-based heterostructures [37] [38]. It predicts the robustness and stability of the studied device against the extreme variation of physical temperature.

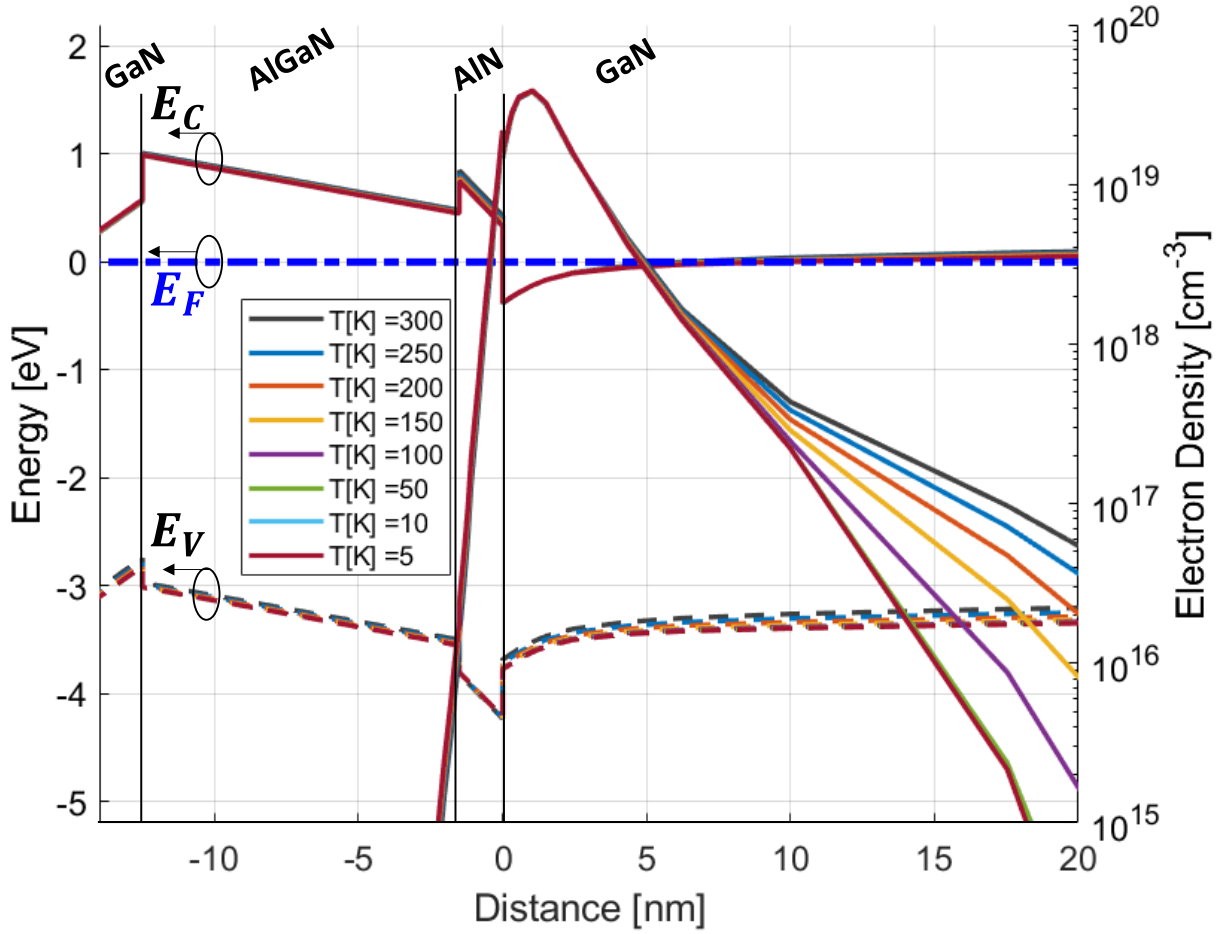

Figure 4: The spatial distribution along a vertical cutline from the cross-sectional view of the device of: the electronic energy bands (left axis); the valence band (dashed lines) and the conduction band (solid lines), E_F indicates the Fermi level (left axis, dot-dashed lines), and the electron density (right axis, solid lines). The results at 8 physical temperatures, T, from 300 down to 5 K are shown.

In the simulations, the polarization at all the different III-Nitrides interfaces were modelled using the formulas from [28]. The buffer layer was assumed to be relaxed, the polarization at its bottom were assumed to be compensated by the interface defects [39]. The values of the bandgap and electron affinity were taken from [28] [40]. The temperature dependence of the bandgap was considered, using the experimental results in [41]. The donor-like surface states, as origin of the 2DEG electrons, were modelled considering a single energy level located at the interface between the GaN cap and the passivation layer. This is a commonly used approach in the literature to model an effective distributed repartition of the surface donors [39] [42]. The sheet density of the surface donors was set to $N_{SD}[cm^{-2}] = 1 \times 10^{14}$, as a threshold of their concentration exists to compensate for the opposite interface polarization and to allow the formation of the 2DEG [42]. Their energy was calibrated at $E_{SD}[eV]$ = 0.2, with respect to the conduction band edge, to fit the Hall measurements of the 2DEG sheet carrier density (n_s) at room temperature (~ 300 K). Both selected N_{SD} and E_{SD} are in close agreement with other works in the literature dealing with similar type of structures [42] [39]. The Fe-doping of the buffer was accounted by setting fixed traps with an initial value of activation energy of 0.5 eV from the conduction band, in line with the findings in [43] [44].

2.1.1. 2DEG characterization

The 2DEG sheet density as well as the electron mobility in the channel can be measured using the Hall-effect measurements. For this purpose, Van der Pauw structures [45] were designed and characterized after fabrication. The sheet carrier density, n_s, and the low-field electron mobility, μ_{LF}, were typically in average 1.09 x 10^{13} cm^{-2} and 2090 cm^2/Vs respectively at room temperature (RT) – from [B]. The sheet resistance, R_{sh}, estimated from the Hall measurement is ~ 274 Ω/square, as it can be shown that [45]:

$$R_{sh} = \frac{1}{q n_s \mu_{LF}} \tag{5}$$

Upon cooling of the device, μ_{LF} is expected to increase based on data from the experimental reports from [20] [19] [38] [37]. Indeed, in different AlGaN/GaN heterostructures, it was found that the suppression of certain scattering mechanisms such as those related to optical and acoustic lattice vibrations lead to the significant improvement of the overall mobility [20]. Compared to RT, a factor of 5 times increase of μ_{LF} was reported in [20], and up to 7 in [38] at around 4 K.

2.2. Electrical Characteristics

Figure 5 shows a top-view image of a typical fabricated 3-terminals device, obtained using Scanning Electron Microscope (SEM) – from [B]. The sample presents a 2 x 25 µm gate periphery. A two gate-fingers design was used. The choice of such a design aims at the reduction of the gate resistance, which affects the microwave and low-noise performance as will be further discussed later in this thesis. Indeed, the resistance due to the gate metallization, R_{g-ee}, can be estimated through the relation [46]:

$$R_{g-ee} = \frac{\rho_g}{3\, A_g N_f^2} W_g \tag{6}$$

Where ρ_g is the sheet resistivity of the gate electrode, W_g and A_g are respectively the width and cross-section of the gate-finger. In the simple case of a gate-finger presenting a rectangular shape, $A_g = t_g/L_g$ where t_g and L_g are respectively the thickness and length of the gate. The factor 1/3 is derived from the distributed nature of the gate with respect to the active area in the device. N_f is the number of gate fingers. Hence, increasing the latter reduces the total gate resistance.

The gate terminal consists of a Nickel (Ni)/Platinum (Pt) Schottky stack of 20/30 nm, followed by the metallization layer on top. Most of the studied devices included field-plate extensions of the gate towards source and drain, which serve to improve the high electrical-field capabilities of the device and its reliability [23]. While the gate-metallization is commonly made of Gold (Au), in [B] the feasibility and impact of a superconducting Niobium (Nb) gate was experimented**.** Further analysis of this experiment is provided in the chapter 5 of this thesis. The sheet resistivity of the gate electrode was characterized using DC end-to-end measurements, at RT and down to the cryogenic temperature (CT) of ~ 4 K. Specific test structures were designed for this purpose. Further details can be found in [B].

The source and drain are recessed (Ta)-ohmic contacts [47]. Transmission Line Measurements (TLM) were used to characterized the ohmic (source and drain) contacts at RT, typically found to range from of 0.32 –

0.36 Ωmm. The electrical isolation of the fabricated devices within the same die was obtained by mesa-etching.

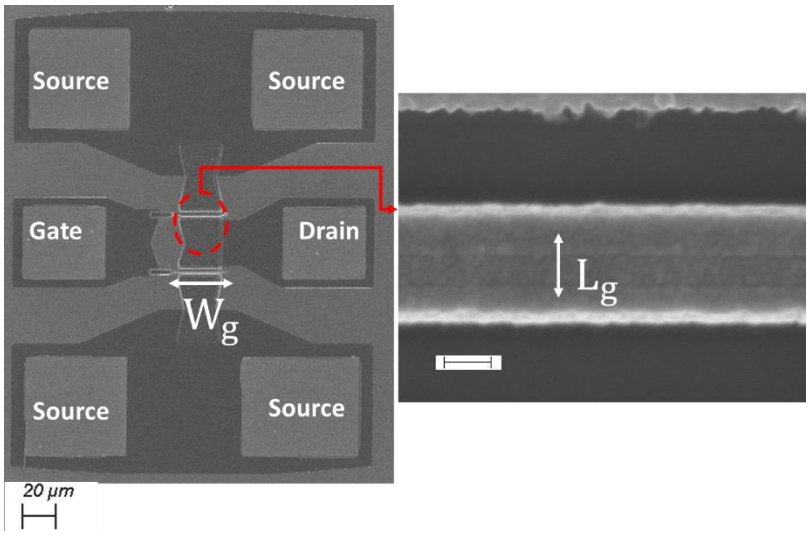

Figure 5: SEM image of a fabricated device, in the inset the gate finger is magnified. W_g and L_g refer respectively to the effective width and length of the gate.

2.2.1. Static operation

The electrical operation of the FETs relies on the combination of a vertical electrical-field, defined by the gate to source voltage V_{GS}, and a lateral field, defined by the drain to source voltage V_{DS}. As described above, in the studied devices, a 2DEG channel exists at the GaN-buffer even when no bias is applied. When sufficiently high level of V_{GS} is applied, the channel is depleted as the electrons are pushed away towards the substrate and no drain-current conduction is possible. The corresponding threshold gate-voltage is also called the pinch-off voltage.

Applying V_{DS}, the electrons laterally flow through the channel which electrical depth depend on V_{GS}. The resulting drain to source current, I_{DS}, increases linearly with the electron's velocity until it reaches its saturation level. The V_{DS} level corresponding to the non-linear variation of $I_{DS} - V_{DS}$ is called the knee voltage, V_K. The carrier mobility in the linear part of the $I_{DS} - V_{DS}$ curve is defined by the ratio of the lateral electric field and the carrier velocity. Its variation at $V_{DS} > V_K$ is described by more complex non-linear models [23] [48] [49]. The slope of the linear part is defined by the on-resistance, R_{on}, which is the sum of the resistances from the contacts resistances of the drain and source, their intrinsic access resistances and the channel resistance.

The transconductance, g_m, quantifies the sensitivity of I_{DS} to the variation of V_{GS} :

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{7}$$

Figure 5 shows a typical static (DC) characteristics at RT and CT, from the devices studied in [B]. Upon cooling of the device, a larger peak of the transconductance and a smaller on-resistance are usually obtained.

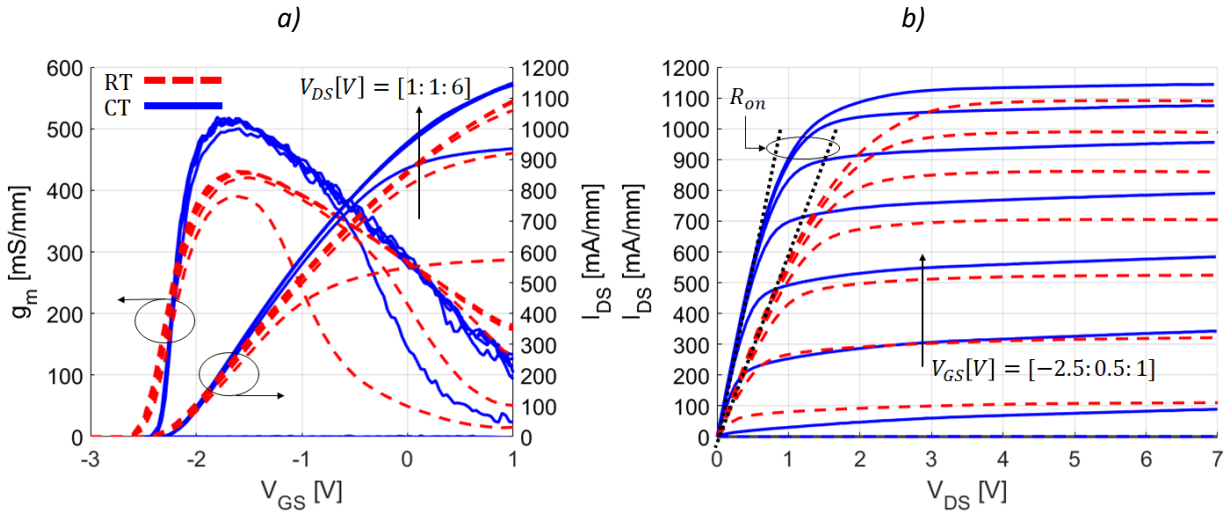

Figure 6: a) Variations of the extrinsic transconductance, g_m, and the drain to source current, I_{DS}, with V_{GS}. b) I_{DS} (V_{DS}) curve at RT (dashed lines) and CT (continuous lines)

The temperature-dependence of the DC characteristics is primarily linked to that of the electron mobility, its velocity, the electrical conductivity of the channel and metallic contacts. The possible prevalence of the electron trapping effects, and their bias and thermal-variations, can also contribute to this dependence by affecting the electron density in the channel. The trapping effects are discussed in the next section.

The substantial reduction of R_{on} when cooling down the device reflects the enhancement of the access resistances and the channel conductivity. The transconductance, which increase by about +20 % in the case of the results in Figure 6, defined in equation (8), relates to the extrinsic device where the voltage drop from the contact and access resistances is not accounted. In fact, the $g_m - V_{GS}$ characteristic is also influenced by the source access -resistance, R_s, as:

$$g_m = \frac{g_{m-int}}{1 + R_s\, g_{m-int}} \tag{8}$$

where g_{m-int} denotes the transconductance of the intrinsic device. R_s is temperature-dependent, and in accordance with the variation of R_{on}, significantly decreases at CT. Thus, it also contributes to the estimated improvement of g_m from RT to CT. In the discussion of the small signal modelling provided below, the distinction between the extrinsic and intrinsic components will be further described and the extraction of the related parasitic resistances will be discussed. Also, the increase of the slope of g_m near the pinch-off manifests the enhanced control of the gate over the channel. This is in line with the results from other cryogenic HEMT technologies [50] [3].

As will be further described, knowing the dominant thermal noise in HEMTs linked to its equivalent resistive elements, the observed DC features predict an improvement of the noise performance at CT.

2.2.2. Trap mechanisms and effects

From a physical standpoint, a trapping effect is defined as the event of the capture or the emission of the carriers at an energy level within the bandgap of the semiconductor. As a consequence, the electrical characteristics of the HEMTs are affected since the 2DEG density is directly altered by the trapping effects. The trapping effects in GaN HEMTs has drawn attention in the literature [51]. Among the major causes leading to the trapping effects is the fact that the channel formation in GaN-HEMTs, as discussed earlier in this thesis, is particularly sensitive to defects, impurities and surface charges. These latter present less impact on the properties of the other HEMT technologies, making them less exposed to the trapping effects. Also, the maturity of the fabrication and growth processes of GaN-HEMTs is relatively less advanced compared to other technologies based on III-V materials due to their earlier development. Hence, aiming at further development of this technology, different technological solutions to identify, eliminate or reduce the trapping effects in GaN-HEMTs were progressively proposed in the literature [23] [51].

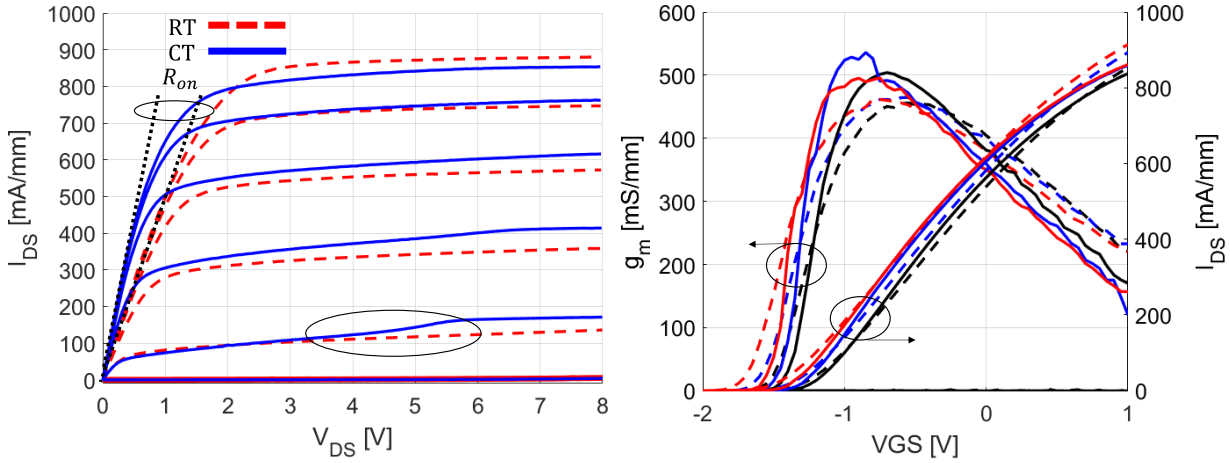

Figure 7: a) $I_{DS}(V_{DS})$ curve of 2x25 µm transistor, for $V_{GS} = [-1.5:0.5:1]$ at RT (red dashed lines) and CT (blue continuous line). The pronounced kink effect at CT is highlighted. b) $I_{DS}(V_{GS})$ and $g_m(V_{GS})$ curves of the same transistor and at the same temperatures at V_{DS} [V] = 3 (black), 6 (blue) and 9 (red). Reproduced from [A].

In [A], it was revealed a prevalence of the trapping effects when cooling-down the tested device through the comparison of its DC characteristics at RT and CT. Figure 7 present the DC characteristics of the device measured at both temperatures. Two major signs of trapping effects are noticed. Firstly, comparatively with the RT characteristic, the maximum drain current was found to decrease by around 5.6 % at CT. While both the on-resistance and maximum transconductance increased at CT, indicating an overall improvement of the channel electrical conductivity and modulation, these conditions were expected to lead to an increase of the maximum current. Therefore, the presence of traps might have counterbalanced the effects of the former features at CT. Secondly, a kink is observed in $I_{DS}(V_{DS})$ curve which is clearly more pronounced at CT at high negative V_{GS}. The kink effect was concluded to be linked to the carrier trapping in GaN HEMTs from several studies [52] [53]. Thus, its prevalence at CT might be an indication of a one or more trapping effects that become more severe at CT. In fact, this can be explained by the slow-down of the emission time of traps at low temperatures [54]. Also, similar DC behavior was previously reported for other GaN-HEMTs at cryogenic temperatures in [54] [55]. Due to the differences in the

qualities of the involved materials and the variety of the growths and processing steps, the manifestation of traps at the same conditions studied herein is not observed in other GaN-based technologies [38] [56]. It should be noted that the devices studied in [A] and [B], although presenting similar epitaxial structures, were fabricated within different dies and involved different processing steps. Thus, this may explain the presence of these effects in [A] and not in [B]

Concerning the origin and the locations of traps, the top surface and the buffer are usually found to be the most recurrent regions for traps. The incorporation of a passivation layer on top of the barrier was proposed in the literature to address the surface-related trapping effects [33] [57]. However, later studies have shown that parallel trapping effects from interfaces or under the gate metal may still be present when a surface passivation is used [58]. In [53], such effects were linked to a specific surface-treatment involving fluorine that precedes the deposition of the gate. The design of the gate field-plates was shown in [59] to play a role in the sensitivity of the device towards the trapping effects. In addition, the barrier can also be the location of deep level of traps [60]. All these effects might be linked to a variety of causes at the microscopic level, such as charges at the surface, defects, threading dislocations and unintentional presence of impurities. In the buffer region, the intentional doping might induce trapping effects. Indeed, while the doping of the buffer with acceptor atoms intends to increase its resistivity to enhance the 2DEG confinement and its modulation, it was shown that these incorporated elements are likely to create defects in which can be trapped the 2DEG electrons [52] [30]. The trapping effects impact the noise performance of the GaN HEMTs at low frequencies and within the 1/f limit [61] [62].

2.3. Small-Signal Operation & Modeling

Although the transistor presents an inherent non-linear behaviour, upon input excitation around a fixed bias point its electrical response could be mathematically approximated to be linear. This principle defines the small-signal operation, and is used to characterize the microwave properties of the device. Lumped electrical elements are used to represent the frequency-dependence of the transistor response. Different approaches exist to extract these representations, or small-signal models (SSM) [63]. The semi-empirical models are commonly used, as they combine a relative simplicity of the extraction procedure and a physical consistency of the results. For the same motivations, all the results presented in this work were based on the approach proposed in [64].

Figure 8 shows the equivalent lumped model of the HEMT [64]. The model includes 17 elements, which subscripts g, s and d denote respectively the gate, source and dr<ain. Arranged in a matrix form, the model is extracted by comparison to the measured S-matrix. The strategy for the extraction of its parameters relies on the distinction of an intrinsic part, which elements are bias-dependent. The remaining parts are assumed bias-independent. These latter are usually referred to as extrinsic elements. Despite this nomination, the series resistances are in reality representative of parts of the epitaxial structure.

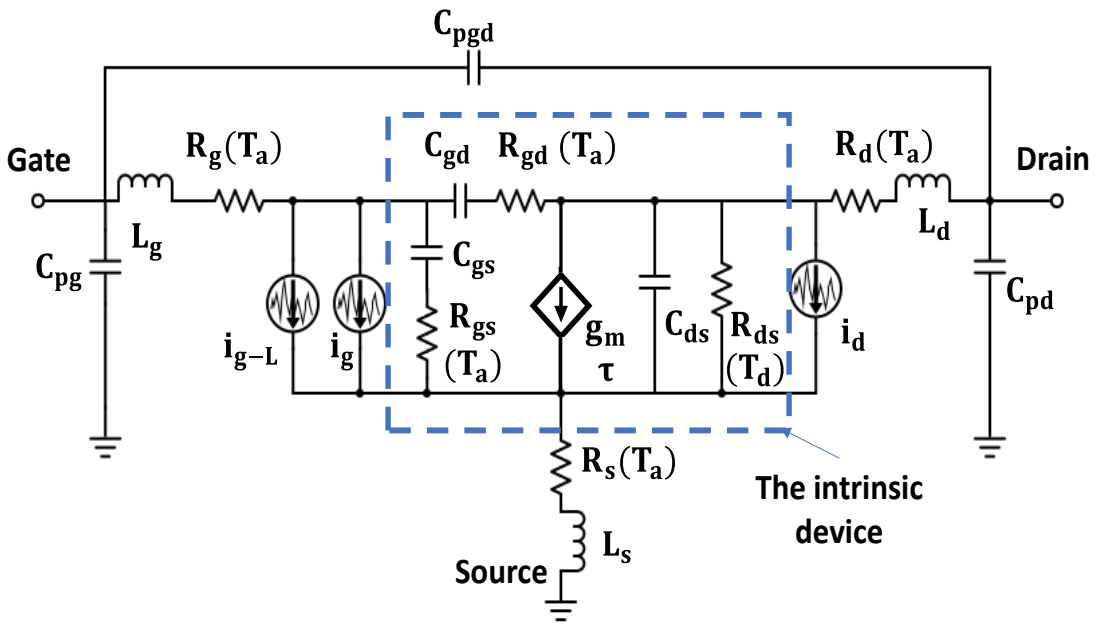

Figure 8: Equivalent small-signal model of the GaN HEMT [64]. The square with dashed-lines highlights the definition of the intrinsic device. The different current noise sources are illustrated; i_g, i_g, i_{g-L}, referring to those associated with the gate, drain and gate leakage.

2.3.1. Extraction of the extrinsic circuit

At V_{DS} = 0 V, the representation in Figure 8 simplifies to that shown in Figure 9-a, referred to as the Cold-FET model. This simplification is due to the suppression of the voltage-current source (g_{m-int}), as no current flows through the channel at this bias condition. A more general representation can be found in [64] – Figure 2. For simplicity, the effect of the drain to source impedance is neglected in Figure 9-a considering full channel and sufficiently high-frequency conditions. The representation in Figure 9-a is useful for the extraction of the bias-independent elements of the model in Figure 8. The parasitic capacitances C_{pg}, C_{pd} and C_{pgd}, accounting for the coupling effects between the transistor and contact pads, must be de-embedded in prior. The equivalent circuit as simplified in Figure 9-b is used for that end. It applies to the bias conditions of $V_{GS} << V_{TH}$ and sufficiently low frequencies (usually <3 – 5 GHz). This is to neglect the channel conductance, the series parasitic elements and the intrinsic resistances with respect to the capacitive elements. The Y-parameters are convenient to proceed with the extraction procedure of the parasitic capacitances, the following set of 3 equations is then obtained:

$$Im(Y_{11}) = j\omega(C_{pg} + C_{gsp} + C_{gdp}) \quad (9)$$

$$Im(Y_{12}) = -j\omega(C_{gdp}) \quad (10)$$

$$Im(Y_{22}) = j\omega(C_{pd} + C_{dsp} + C_{gdp}) \quad (11)$$

Once the extrinsic capacitances de-embedded, the remaining bias-independent elements are conveniently extracted using the Z-matrix representation of the model in Figure 9-b. The parameters of the gate impedance are, first, extracted using an iterative procedure [64]. This was also detailed in [B].

The same applies to the source and drain resistances, which are obtained from the frequency-dependence of the Z-parameters.

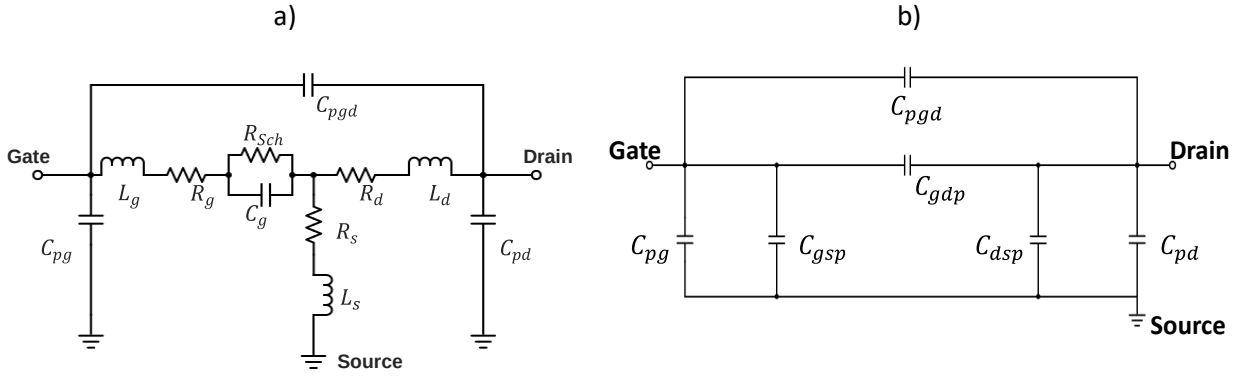

Figure 9: a) Equivalent SSM at V_{DS} = 0 V b) Simplification of the model at $V_{GS} << V_{TH}$ and low frequency

2.3.2. Extraction of the intrinsic circuit

Once the bias-independent element de-embedded from the representation shown in Figure 9-a, the intrinsic parameters from the model in Figure 8 are conveniently described using the Y-matrix as:

$$Y_{tot} = Y_{ext} + Y_{int} \tag{12}$$

Where Y_{tot}, Y_{ext} and Y_{int} are respectively the Y-matrix representations of the total, the extrinsic and intrinsic circuits. Y_{ext} is obtained from the sum of the Y-matrix resulting from equations 9 – 11 and the Y-representation of the model in Figure 9-a. The fit of Y_{tot} to the Y-transform of the measured S-parameters, leads to the determination of the elements of Y_{int} as:

$$Y_{int} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ -Y_{gd} - \dfrac{Im(Y_{gs})}{Y_{gs}^*} Y_{gm} & Y_{ds} + Y_{gd} \end{bmatrix} \tag{13}$$

Where:

$$Y_{gs} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{gs}} \tag{14}$$

$$Y_{gd} = \frac{j\omega C_{gs}}{1 + j\omega C_{gd} R_{gd}} \tag{15}$$

$$Y_{ds} = j\omega C_{ds} + g_{ds} \tag{16}$$

$$Y_{gm} = g_m e^{j(\frac{\pi}{2} - 2\pi F\tau)} \tag{17}$$

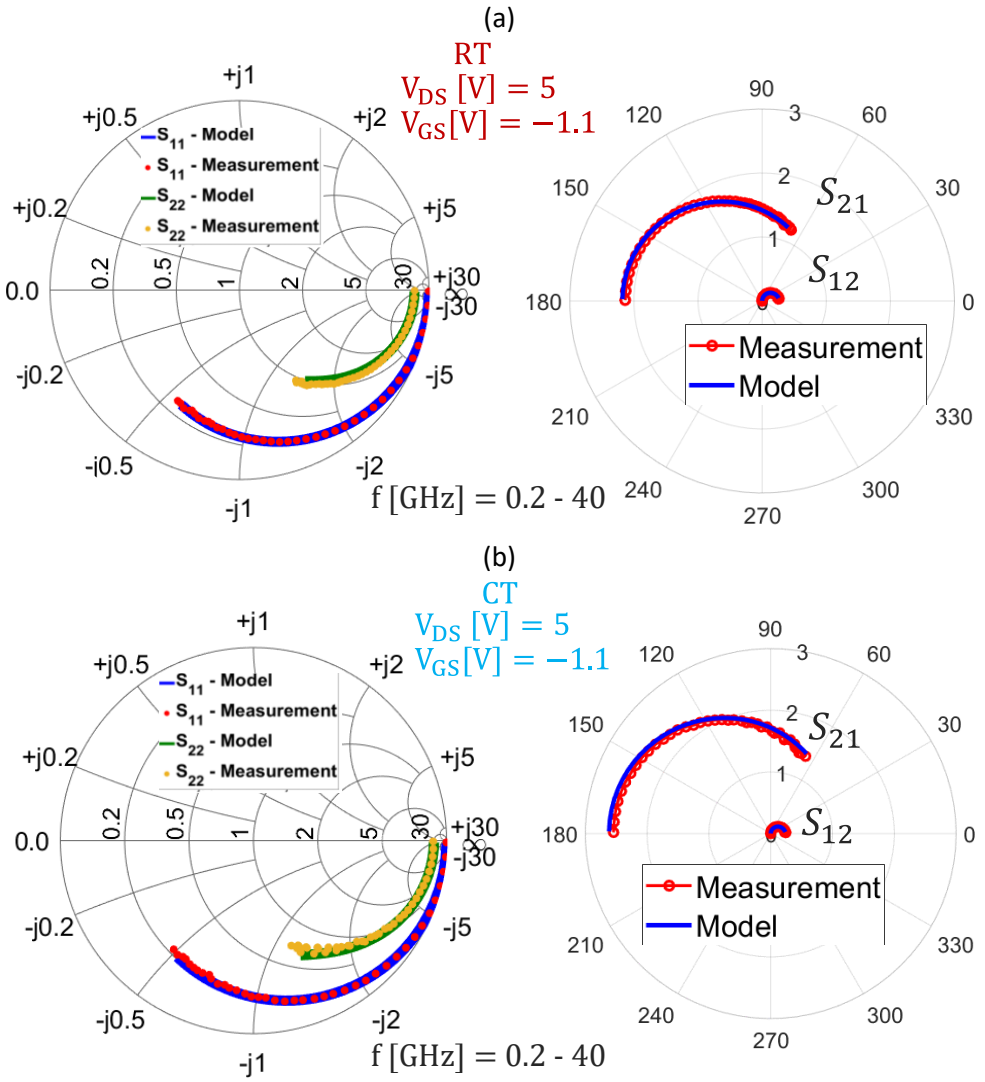

Figure 10: Comparison of typical measured and modelled S-parameters of a 2x25 µm device, at V_{DS} = 5 V and V_{GS} = -1.1 V over the frequency range 0.2 – 40 GHz at a) RT b) CT

Figure 10 presents a comparison of typical measured and modelled S-parameters at a fixed bias point, V_{DS} = 5 V – V_{GS} = -1.1 V, at both RT and CT. This sample presents a total periphery of 2x25 µm. An excellent agreement of the model with the measurements over a large frequency range of 0.2 – 40 GHz is observed at both physical temperatures. Once a fitting of the model against measurements is achieved, the intrinsic parameters can be determined from the frequency-dependence of the Y-transform by solving the equations 13 – 16.

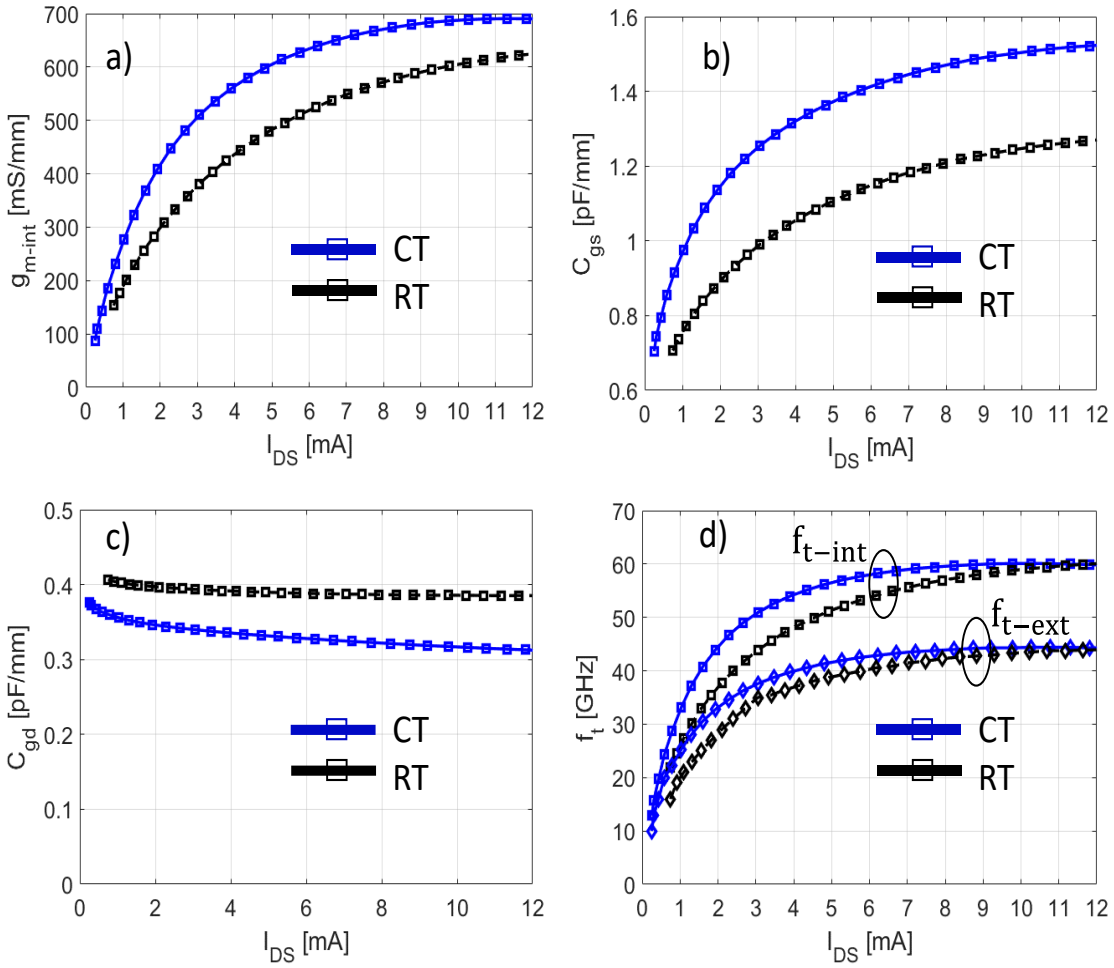

Figure 11: The current dependence at V_{DS}=5 V of the intrinsic small signal parameters at RT (black) and CT (blue). a) g_{m-int} b) C_{gs} c) C_{gd} d) f_t - reproduced from [A].

Being one of the main parameters affecting the noise performance, the intrinsic transconductance, denoted as g_{m-int}, was observed to significantly increase at CT. Also, a steeper slope of g_{m-int} after the pinch-off is noted, reflecting an enhancement of the transport mechanisms in the channel and a better control of the gate over the channel resulting from the cooling-down of the device (Figure 11-a). The gate to source capacitance, C_{gs}, increases at CT as shown in Figure 11-b. The C_{gs}-I_{DS} characteristic is found particularly temperature-sensitive, a faster increase and an earlier saturation at CT are observed. The behaviour of C_{gs} could be related to the variation with the temperature of the material properties and the distribution of the carriers, as was previously observed in other III-V devices [65] [66]. The variation of C_{gd}, plotted in Figure 11-c, is found to be less bias and temperature dependent. This may also indicate its relatively small effect on the noise behaviour of the device. Altogether, these parameters determine the cut-off frequency. The latter is known to be one of the main parameters determining the noise performance vs. frequency. The intrinsic cut-off frequency, shown in Figure 11-d, is defined by the equation:

$$f_{t-int} = \frac{g_{m-int}}{2\pi(C_{gs} + C_{gd})} \tag{18}$$

Indeed, an analytical approximation of the minimum noise temperature that can be achieved by the transistor, noted T_{min} in the following, is given by [67]:

$$T_{min} \sim 2\frac{f}{f_{t-int}}\sqrt{(R_s + R_g)T_g g_{ds} T_d} \quad (19)$$

Where T_d and T_g are respectively the equivalent temperatures of the intrinsic drain- and gate-source resistances. This expression ignores the effects of parasitic elements which are not amplified by the gain-stage of the transistor, represented by g_{m-int}. Equation 19 shows the weight of g_{m-int} and the sum of $(C_{gs} + C_{gd})$, through f_{t-int}, in the noise performance of the device as they present a direct linearity with T_{min}.

The validity of the small-signal model was verified at a larger range of bias points, and quantified using the following error function:

$$\epsilon_{ij}[\%] = 100 \times \frac{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}} - S_{ij_{modeled}}|}{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}}|} \quad (20),$$

where $S_{ij_{measured}}$ and $S_{ij_{modeled}}$ are respectively the measured and modelled S-parameters, i and j denoting the port number, over the frequency range from f_{min} = 0.2 GHz to f_{max} = 40 GHz. Figure 12-a shows the variation of the error function as a dependence on the different bias points ranging from at V_{DS} = 4 - 10 V and V_{GS} = -1.5 – -0.5 V at CT, in the case of a 2x25 µm transistor studied in A. An average error in the range of 2 – 3 % was obtained in this case, which quantifies the accuracy of the model.

Also, the physical consistency of the model can be assessed from the variation of the intrinsic parameters with both V_{DS} and V_{GS}, see Figure 12-b to f. The variation of g_{m-int} is found consistent with the definition provided above. In fact, its variation reflects that of the electron velocity and channel density. Hence, it shows minor variation with V_{DS} in the saturation region (Figure 12-b). C_{gs}, from a physical standpoint, reflects the effect of a parallel-plate capacitance formed between the 2DEG and the gate-metal. Since negatively increasing V_{GS} leads to the depletion of the channel, C_{gs} decreases near the pinch-off voltage as the effective separation between the channel and the gate increases (Figure 12-c). On the other hand, upon existence of the channel, increasing V_{DS} leads to the increase of the velocity of the carriers which probability to get closer to the barrier-interface increases leading to the decrease of the effective gate-channel distance. C_{gd} arises from the extension of the depletion region under the gate to the drain. Hence, increasing the drain-to-source field leads to the decrease of C_{gd} (Figure 12-d). Thus, the sum of C_{gs} and C_{gd} provides the total gate capacitance. In addition, the gate capacitance reflects also the effect of the field plates extension from the gate metallization. g_{ds} reflects the conduction of the drain current, hence it saturates at high V_{DS} (Figure 12-f).

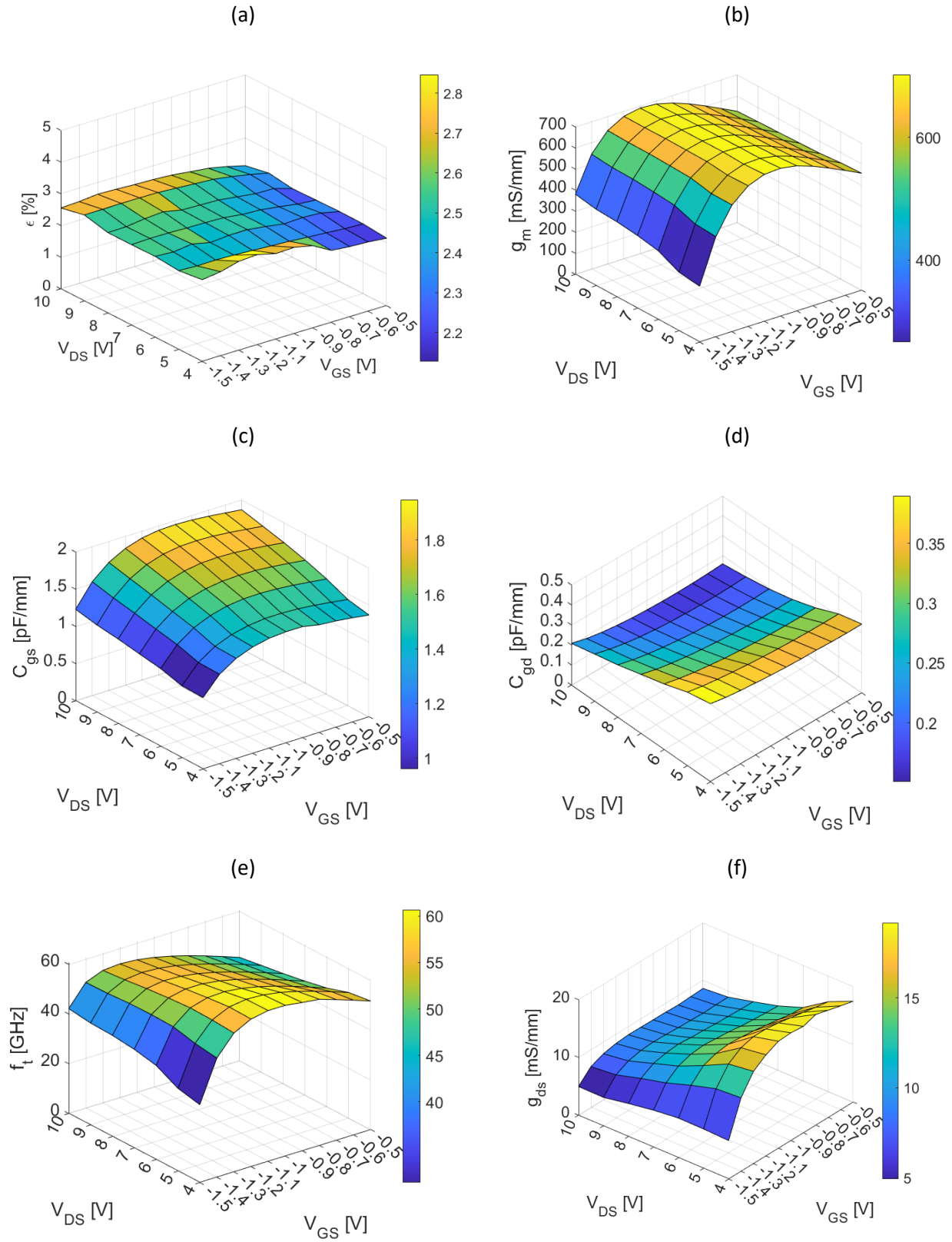

Figure 12: Bias-dependence, with respect to V_{DS} and V_{GS} of the parameters of the small-signal model at CT: a) The model error-function b) g_{m-int} c) C_{gs}d) C_{gd} e) f_{t-int}f) g_{ds}.

2.3.3. Effect of the gate-width dependence

Resulting from this procedure, as of particular interest for the noise modeling, the extracted resistances of the source and drain are presented in Figure 13 with their gate-width dependence at RT and CT – as reproduced from [C]. An excellent consistent dependence of the model with the gate-width is obtained; as expected the drain and source resistance are inversely proportional to W_g due to their dominantly intrinsic nature. Also, a substantial reduction of the access resistances with temperature is observed. This is supporting the results from the DC characterization presented above. It is also predicting a positive impact towards the improvement of the noise performance of the device at CT. However, as will be shown in chapter 5 and based on the study in [B], a larger gate-width leads to a proportional increase of the gate resistance due to its dominantly extrinsic nature related with the gate metallization. Hence, the thermal noise associated with the gate would increase using a larger gate width.

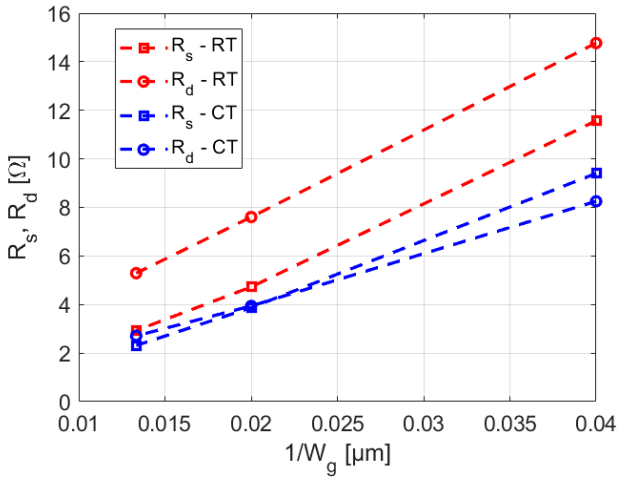

Figure 13: Gate-width dependence of the extracted source and drain resistances at RT (red) and CT (blue).

The trends of the intrinsic parameters presented in the previous subsection were verified from the study of the scalability of the model with the gate width, as reported in Figures 14-a – d, from [C]. The validation of the model against the measurements was confirmed for these different samples with different gate-widths, as an uncertainty in the same order of 2 – 3 % was obtained (Figure 14-a). An expected linear increase of the transconductance with the gate-width is observed (Figure 14-b), due to larger driven drain current. The gate-to-source capacitance was confirmed to increase upon cooling of the device. Also, the total gate capacitance scales linearly and increases with the gate-width (Figure 14-c – d). This feature impacts the input impedance of the device, and will be found of interest for the optimum noise matching in chapter 5 – from [C].

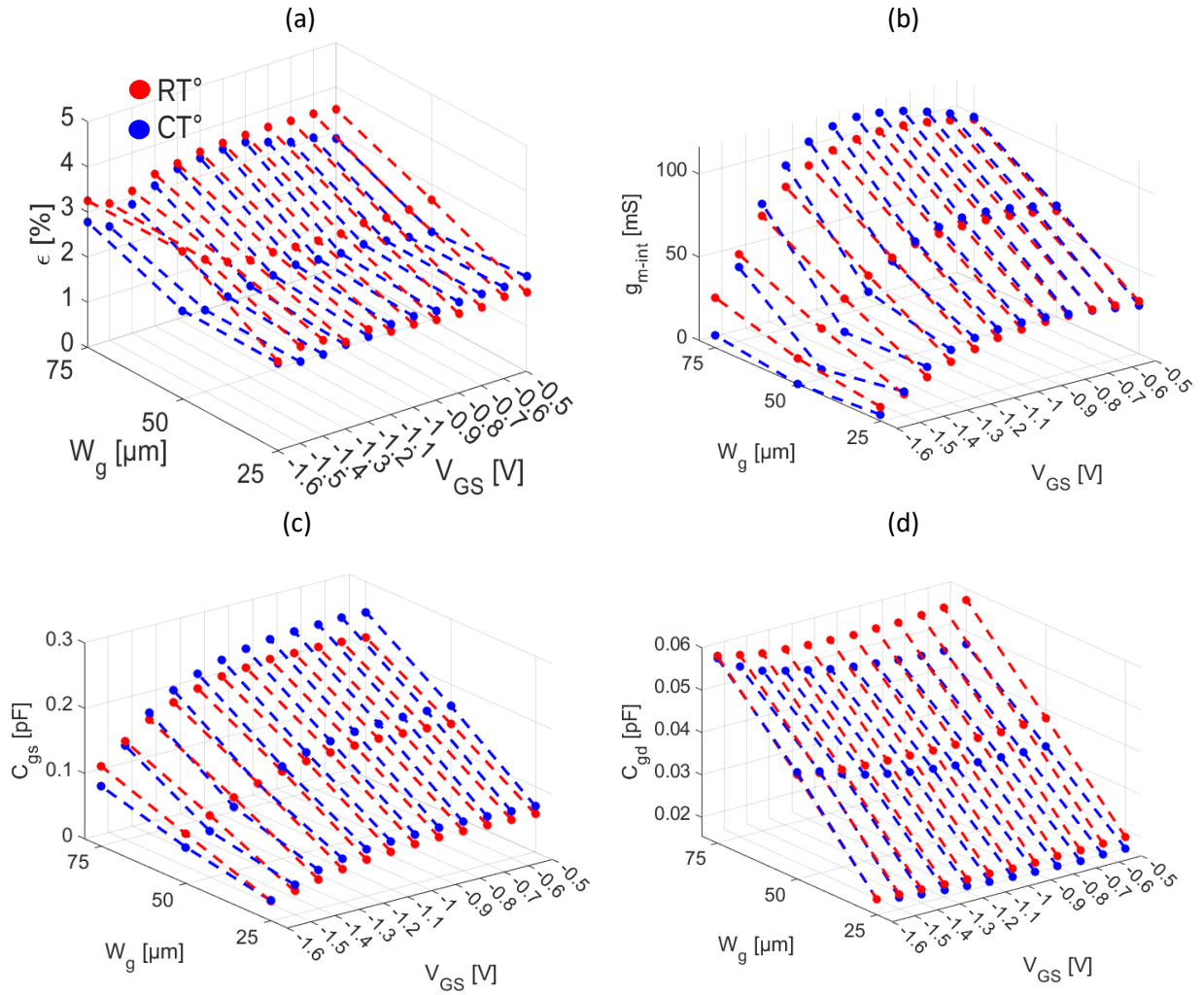

Figure 14: Gate-width dependence at RT (in red) and CT (blue) of the parameters of the small-signal model at V_{DS} = 5 V; a) the model error function b) g_{m-int} c) C_{gs} d) C_{gd}

2.4. Summary

This chapter reviewed the static performance and operation of the GaN HEMTs at cryogenic temperatures. Different physical parameters and their influence on the cryogenic behaviour of the device were presented and discussed. It was shown that the overall microwave and static performance improved upon cooling of the device. A cryogenic small-signal model of the devices was extracted, its validity was verified through the study of both its dependences on the bias and the total gate width. The results further motivate the investigation of the low-noise potential of the GaN HEMTs at the cryogenic temperature conditions. This will be the subject of subsequent chapters.

3. Low Noise Amplification at Cryogenic temperatures: State-of-the-art & Modeling Approaches

The potential and suitability of the GaN-technology for the microwave and low-noise operation at cryogenic temperatures was concluded from the previous chapter. Putting into perspective the different requirements set for the future design of cryogenic GaN-based LNAs, a review of the main existing technologies is introduced in this chapter. The second part of this chapter discusses the necessity for a model that describes and assesses the microwave noise behavior of the GaN-HEMTs, considering the requirements set by the cryogenic low-noise applications. The main existing approaches to achieve this task, the reasoning on which they are based and their physical interpretations are presented.

3.1. General considerations for the design of low-noise amplifiers

As illustrated in Figure 15, a one-stage LNA is constructed from the cascaded input matching network, the transistor device and an output matching network. The matching networks are designed in such a way that the lowest noise temperature should be ensured, while simultaneously allowing the transistor to present a decent microwave gain and a stable operation. The expressions of the gain and stability can be found in [68], equations 3.2.4 and 3.3.13 respectively. These are depending on the scattering parameters of the HEMT and the reflection coefficients with respect to the impedances shown by the matching networks. A larger total gain can be obtained by cascading a number of LNA-stages. By means of equation (4), the noise performance of the 1st stage has the main impact on the total noise temperature. Hence, it is important for the designer to estimate the noise temperature of the HEMT device and the parameters allowing its minimization. The description of the noise performance at both the system and the device levels, and the impact of the different physical parameters of the HEMT are discussed in a later section of this chapter.

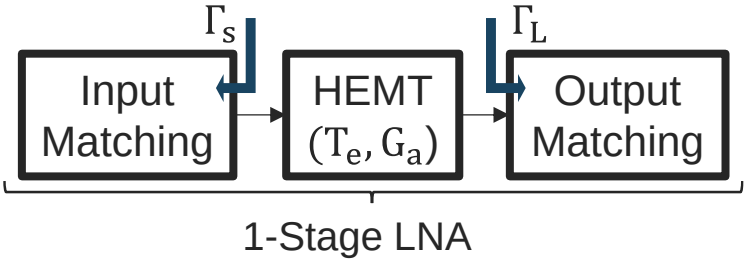

Figure 15: Schematic block illustration of a single stage LNA. Γ_s and Γ_L are respectively the source and load reflection coefficients from the input- and output- networks.

Aside from fulfilling the gain and noise requirements, the LNA is expected to cover a wide frequency-bandwidth. The design of the matching networks has usually a major impact on the bandwidth of a single stage. Cascading multiple stages also aims at increasing the covered frequency-range. Generally, in order to ensure a flat response of the amplifier over the entire targeted frequency band, the design is made for a slightly higher noise temperature than the lowest possible. From that perspective, as studied in [C], the size of the transistor impacts the degree of how critical it is to deviate from the optimum-matching.

While the requirements for larger bandwidths are increasingly demanded for the targeted applications, unwanted and interfering signals (the RFI) may disturb the operation of the LNA within the frequency-

band of interest. Thus, a higher dynamic range is required for modern LNAs at cryogenic temperatures [4]. This way, the saturation and the resulting lost sensitivity towards weak signals of the system can be prevented. Hence, technologies with high-power handling are also required. As discussed in this thesis, the inherent GaN material properties are advantageous to address this challenge.

Cryogenic operation of an amplifier should consider low power consumption. This is especially motivated by the fact that the cooling power at cryogenic temperatures is usually limited and presence of "hot" component would warm up nearby components. One possibility to address that limitation is reducing the size of the transistor to lower the driven current, without affecting the other performance. More profound changes imply the lateral scaling of the transistor, the optimization of the distance between the gate and channel or that of the general vertical epitaxy to ensure a better control of the gate over the channel and an enhanced confinement of the 2DEG.

One additional common challenge in the design of the cryogenic LNAs relates to the input reflections. This is usually resulting from the trade-offs on the wideband and the optimum noise-matching leading to certain restrictions on the input standing-wave-ratios (SWR). For instance, in [69], the LNAs were specifically designed to meet the radio-astronomy receivers' requirements, an average S_{11} as high as -3.7 dB was reported over the 4 – 12 GHz band. A high input return loss may degrade the overall system performance and leads to instabilities in the prior stage of the LNA in the receivers' chain, i.e., the mixer [70]. To address this challenge, one solution implies to use an input isolator but inevitably leads to degradations of the total noise of the receiver and mechanical restrictions due to their size. Another solution would be to rely on a balanced amplifier design, as was demonstrated in [71].

Finally, in terms of the assembly and integration of the LNAs suitable for operation at cryogenic temperatures, two options are usually available. The first relies on surface-mount components, manually assembled and interconnected via bond-wires [72]. This type of circuits is called microwave integrated circuits (MICs). The second, which emerged through the development of advanced fabrication processes, relies on the integration of all the components onto a single substrate [73]. Called Monolithic MICs (MMICs), the assembly of this type of circuits present a high level of integration, repeatability and yield. However, since limited degree of tuning is available for each component, the noise performance is usually difficult to achieve to be optimal in this case. On the other hand, using MICs, the performance of each component can be adapted and selected in such a way that the optimum overall performances are achieved. For this reason, the MICs are the most common for the applications with ultra-low noise requirements [4].

3.2. Low-noise amplification at cryogenic temperatures – State of the art

The noise performance at the device level are controlled by both its dimensions and the properties of its materials. The HEMTs based on the III-V materials dominate so far over the state of the art of the ultra-low noise applications. The first HEMTs were based on InAlAs/GaAs heterojunctions on GaAs substrates. The incorporation of Indium (In) to the channel layer, becoming InGaAs, was after then demonstrated to be beneficial to improve the 2DEG properties and confinement. These HEMTs are referred to as pseudomorphic (pHEMT), in contrast to the metamorphic ones (mHEMT). The latter introduce a transitional layer between the channel and substrate layers to reduce the lattice mismatch between these two, which otherwise negatively impacts the performance of the device. The use of an InP as a substrate and further incorporation of In into the barrier, becoming InAlAs, led to the development of a new

generation of devices; the InP HEMTs. These technologies can operate at extremely low temperatures, and their low-noise performance substantially improve under these conditions.

An average noise temperature as low as 1.4 K in the range of 4 to 8 GHz was reported using InP HEMTs at the physical temperatures of 4 to 15 K [74] [75]. In terms of wide-band operation, fractional bandwidth of up to around 190 % was reported using the InP HEMTs [73]. Most recently, an advanced InP-technology was demonstrated to achieve a state-of-the-art 4 K noise temperature over the entire band of 2 to 18 GHz [72]. The maximum frequency of operation is strongly impacted by the gate length, as the cut-off frequency is inversely proportional to L_g. Hence, the development of the LNA technologies focuses on the scaling of the gate length of the HEMTs. The state of the art in terms of high frequency of operation was recorded using InP-HEMTs with 25 nm gate length, reaching 850 GHz at RT with 11.1 – 13.6 dB gain and ~ 4300 K noise temperature [76]. The LNAs based on the same technology were reported to operate at the physical temperature of 25 K up to 670 GHz with 15 – 25 dB gain and 400 K noise temperature [77].

Due to their earlier development, the GaAs pHEMTs constitute the most mature technology. However, their noise performance is usually worse compared to InP HEMTs [4]. Among the best results, an average noise temperature of 5 K with 25 dB gain over 4 – 8 GHz at the physical temperature of 12 K was reported in [78].

The GaAs mHEMTs are relatively more advanced, and present a noise performance which competes with that of InP HEMTs. In [50], at a physical temperature of 10 K, it was reported an average noise temperature of 5 K over the 4 – 8 GHz band with 37 dB gain being 12 dB higher than the GaAs-pHEMTs cited above. More recently, with a gate length of 50 nm an InGaAs mHEMTs-based LNA was demonstrated to outperform the InP-based technologies within the bandwidth of 67-116 GHz [79].

The Silicon (Si)-based technologies cannot operate at cryogenic temperatures as suffering from the freeze-out of the carriers [35]. However, the incorporation of Germanium (Ge) to Si in Heterojunction-Bipolar-Transistors (HBT) allows the operation at cryogenic temperatures. In terms of low power-dissipation, SiGe transistors were demonstrated in 2016 to consume a record-low 0.3 mW at the 1.8 – 3.6 GHz frequency band [16]. This same power consumption was since then also achieved by InP-LNAs in 2020 [80].

As introduced earlier in this thesis, in addition to the noise performance, modern applications of cryogenic LNAs require a large dynamic range and high power-handling capability. These properties are usually overlooked and not available for cryogenic LNAs but could be found for cryogenic LNAs based on SiGe technology in [81]. These SiGe LNAs cooled to 17K were shown to present a better power performance compared to the III-V - based LNAs. No significant changes were observed on the power performance compared to room temperature (RT). However, while no cryogenic data are available so far, the state of the art of GaN-LNAs at RT by far outperforms the power-handling performance of the latter technologies.

3.3. GaN-based HEMTs for low-noise amplification – State of the art

For low-noise applications, the GaN-technology present a unique combination of high-frequency, low-noise and high-power performance. At room temperature, one of the most illustrative results of such combination were reported in 2008 [82]. These LNAs, based on AlGaN/GaN HEMTs on SiC substrate with 0.2 µm gate length, achieved an average noise temperature of 35 K at RT within a bandwidth of 2 – 8 GHz. Simultaneously, the same LNA exhibited ultra-high-power handling capabilities, with a linear output power of up to 32.9 dBm (~2 W). Also, several reports showcased the superior survivability of the GaN-

HEMTs towards dynamic and high input power levels compared to other technologies [8] [83] [84]. The scaling of the gate lengths allowed the operation of the GaN-HEMTs at higher frequencies. For instance, 0.1 µm GaN-HEMTs were covering a bandwidth of 22-30 GHz with a noise temperature of 28 – 84 K in [83]. Recently, a wideband GaN-LNA based on devices with 70 nm gate length was reported to cover 63 up to 101 GHz with a gain of 21 – 24 dB and an average noise temperature of 259 K [85]. This noise contribution compares by factor of 2 higher than the state of the art based on InP HEMTs within the same band. The GaN-LNAs, however, usually require a power consumption which is up to an order of magnitude larger than their counterparts based on the III-V materials. This is because, as initially designed for high-power operation, the best intrinsic features of the GaN-HEMTs at high frequencies are usually obtained at larger biasing conditions. Nevertheless, some promising efforts towards addressing this challenge were also reported in the literature. In [86], downscaling the lateral dimension of the GaN-HEMTs with 0.15 µm was already shown to improve the noise performance while dissipating less DC-power. Most recently, while the technology gained in maturity over the last decade, aggressive downscaling of GaN-HEMTs by reducing to the sub-100 nm range both the gate length and the total lateral distance were proposed [87] [88]. GaN-HEMTs with 20 nm gate length and 100 nm total lateral distance were then demonstrated in [89], leading to an enhancement of both the noise performance and the DC-power dissipation. Using this advanced technology, it was achieved a power consumption of only 1.6 – 27.3 mW per stage with a noise performance of ~ 101 – 175 K (NF ~ 1.3 – 2 dB) and 24 dB gain within the 30 – 39.2 GHz band. These results compare directly to the state of the art from the other technologies at the same conditions. In fact, these improvements of the technology performance also involved the reduction of the electrical contact resistivities by developing an improved fabrication process and an optimization of the vertical epitaxial structure. Altogether, this is positively impacting the thermal noise and the gain at high frequencies. Simultaneously, these devices maintained their superior high-power potential as their breakdown voltages were still around 2.5 times higher than the GaAs and InP technologies.

In 2008, the same technology previously reported at RT in [82] based on AlGaN/GaN HEMTs on SiC substrate with 0.2 µm gate length, were tested in [90] at the modest lower temperature of 243 K (-30 C°). An impressive reduction of the noise temperature was then reported, showing a maximum of 13.7 K (< 0.2 dB) over the entire bandwidth of 2 – 8 GHz. The difficulty of the noise measurements at these conditions was already visible; a measured point was reported to fall below a physical limit and ripples over the measured band led to relatively large variations of the estimated noise temperature within a range of 3.4 - 10.2 K. Nevertheless, compared with the RT measurements, the average noise performance improved by a factor of ~4. Simultaneously, the high-power handling capabilities remained almost constant with a linear output power of 32.8 dBm (~2 W). In 2019, commercial GaN-LNAs were experimentally tested for the first time at cryogenic temperatures of about 10 K [21]. An improvement of the noise by a factor of almost 10 was then reported. However, these amplifiers were exclusively designed for RT operation and large power handling capacity and, consequently, did not include any noise-matching adapted for such low temperatures. The estimation of the lowest noise temperature that can be achieved using GaN-HEMTs at cryogenic temperatures was still conditioned by the retrieval of a model describing the optimum noise performance. This was addressed for the first time in [A]. The GaN-HEMTs with 200 nm gate length presented an average best noise temperature of 4.1 K within the frequency-band of 4.5 – 6.5 GHz, at the cryogenic temperature of ~10 K. In [B], the same GaN technology but with a design more adapted to power applications and which introduces a penalty on the noise performance, was reported to achieve 8 K average noise temperature at the same frequency and temperature conditions. These latter results will be further discussed in chapter 5. Nevertheless, as shown in Figure 16 presenting

an overview of the state of art of the different technologies of cryogenic HEMTs reviewed in this chapter, the GaN-HEMTs present a noise performance which is comparable to their counterparts based on other materials. Noting the earlier and longer development of the latter, it is reasonable to consider that further optimization of the GaN technology would lead to further improving its noise performance and possibly competing with InP and GaAs devices.

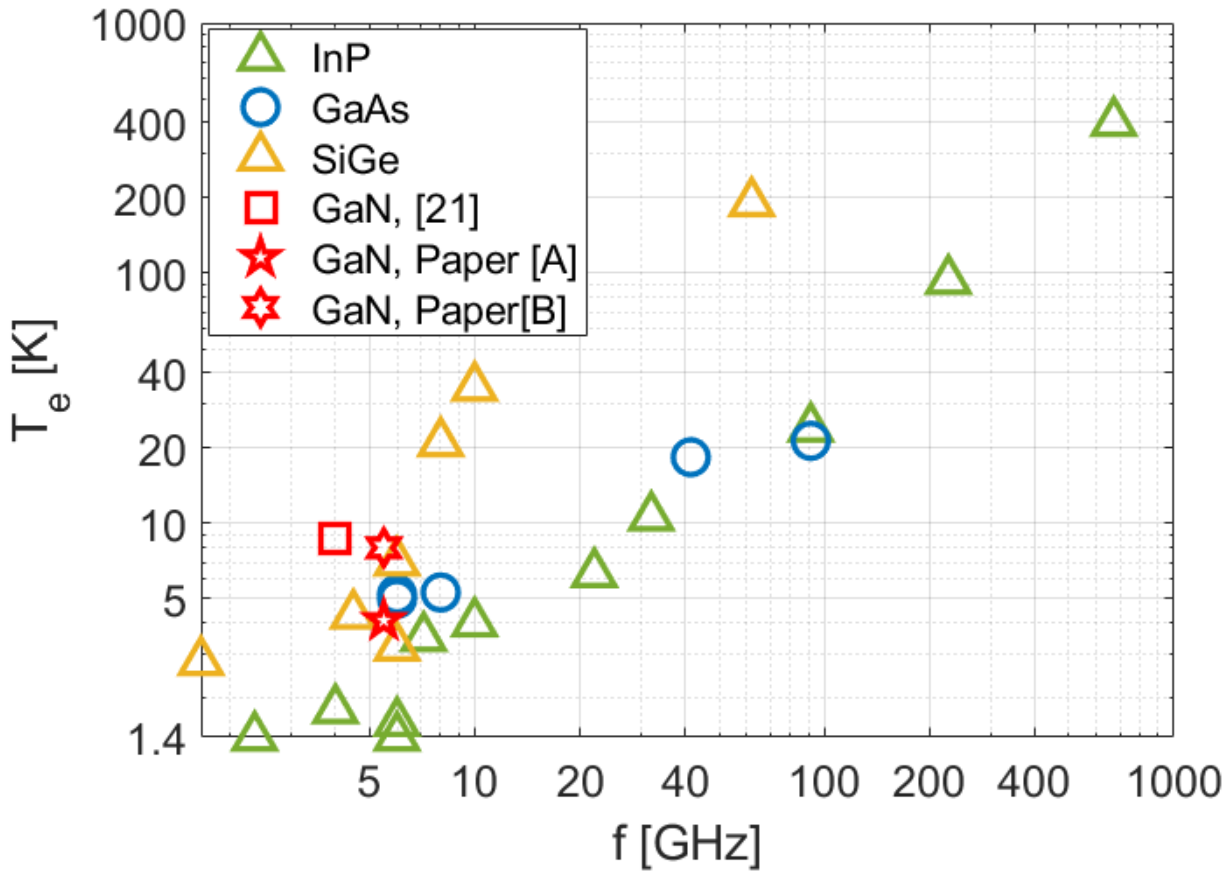

Figure 16: Summary of the state-of-the art of cryogenic HEMTs, the plot shows the average noise temperature at cryogenic temperatures of 4 – 20 K achieved at center frequency from the reviewed literature.

3.4. The Noise modeling from the LNA-design perspective

From the circuit design perspective, the noise temperature of the transistor depends on the source impedance, $Z_s = R_s + \mathrm{j}X_s$, as [91] [67]:

$$T_e = T_{min} + R_n G_{opt} T_0 \frac{\left|Z_S - Z_{opt}\right|^2}{R_s R_{opt}} \tag{21}$$

where T_{min}[K], is the minimum noise temperature; $Z_{opt} = R_{opt}[\Omega] + \mathrm{j}X_{opt}[\Omega]$ is the optimum impedance and its equivalent admittance: $Y_{opt} = G_{opt}[\mathrm{S}] + \mathrm{j}B_{opt}[\mathrm{S}]$, R_n $[\Omega]$ the noise resistance and T_0 = 290 K the standard temperature. From this equation, a set of 4 noise parameters (NPs): $\{R_{opt}, X_{opt}, T_{min}, R_n\}$ that describe the transistor noise contribution to any circuit is defined. The equation (21) provides the key to implementing the best noise performance of the transistor: providing $Z_s = Z_{opt}$ leads to $T_e = T_{min}$. Thus, only the design of the input matching allows using the full low-noise potential of the transistor. R_n reflects the sensitivity towards deviations of the source impedance from the optimum one.

Direct measurements of these 4 noise parameters would logically require at least 4 different noise measurements. As will be discussed in chapter 4, the difficulty of such a task is further emphasized at cryogenic temperatures if not impossible to achieve with a sufficient accuracy. Alternatively, non-direct approaches are usually adopted for the extraction of the cryogenic NPs. These approaches rely on a description of the noise behaviour at the device level, as introduced in the next sections of this chapter.

3.5. Sources of noise in the HEMT

Two main physical origins of the noise in HEMTs can be identified at microwave frequencies: the thermal noise and the shot-noise.

The thermal noise originates in HEMTs from the random scattering of the charge carriers, that is the electrons in the case of the 2DEG. The noise behavior in FETs was for the first time theoretically studied in [92]. Such mechanism of noise results in the random fluctuation of the number of carriers in the channel, due to their scattering with the lattice. In addition, due to the capacitive coupling of the channel to the gate, an induced noise of the same origin appears at the gate. Hence, the gate and channel noises are to some extent correlated. In terms of voltage and current, the thermal noise is by definition of statistical nature. Hence, they are expressed in a form of the square of their variation (variance). At thermal equilibrium, the following formulas are useful to quantify respectively a current- and voltage-noise through an ohmic resistor, R [93]:

$$< i_n^2 > = \frac{4\, k_B T}{R} B \tag{22}$$

$$< v_n^2 > = 4 k_B T R B \tag{23}$$

Where T is the physical temperature. The equivalent lumped elements of the small signal model of the HEMT (Figure 8) are considered to be at the thermal equilibrium. Hence, as will be discussed in a later section, these formulas are important basis for the estimation of the total noise temperature of the device.

The shot noise arises from the discreteness of the charge carriers which participate in the conduction of a current. A condition for the shot noise formation is that the carriers should cross a barrier of potential [93]. Considering the 2DEG as a conductor, this latter condition is believed to be not fulfilled in the channel [92]. However, in [94], it was suggested that for very short gate lengths (< 0.1 µm) the origin of noise in the channel may be ascribed to a suppression of shot noise. On the other hand, the conduction of the leakage current through the Schottky gate leads to an associated shot noise. The expression of a source of a shot noise is related to the DC current, I_{DC}, by:

$$< i_{shot}^2 > = 2\, q\, I_{DC}\, B \tag{24}$$

At low frequencies (< 1 GHz), a noise source called Flicker noise is predominant. It manifests by an inverse proportionality to the frequency of operation (1/f). Also, the generation and recombination of carriers are associated with noise at these low frequencies. This latter type of noise is due to the capture and emission by the traps, which affects the density of carriers [93]. As these phenomena occur at frequencies below the considered microwave range, they are not treated in this thesis.

3.6. The Noise modeling and the noise correlation matrix at the device level

In order to relate the 4NPs introduced above to the intrinsic parameters of the device, and the associated sources of noise, the circuit-theory of noisy linear two-ports can be used. By analogy to the representation of the scattering matrix dealing with the deterministic signals, the noise correlation matrix is introduced to express the random fluctuations of the signals.

Based on the works of [95] [96], a comprehensive way to define the concept of the noise correlation matrix is to rely on the illustration in the Figure 17.

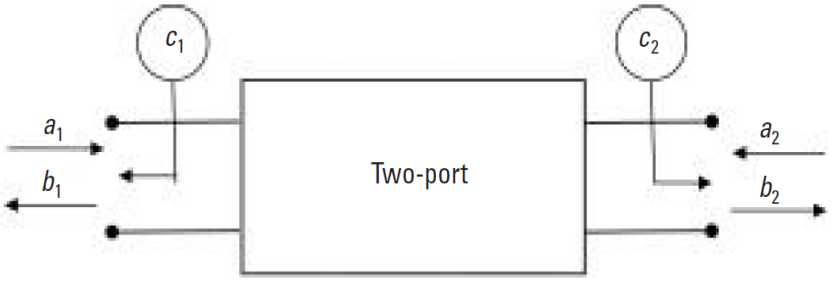

Figure 17: Illustration of the noise waves associated with a linear two-ports device – from [97]

The definition of the S-parameters relates to the input waves, a_1 and a_2, to the output waves, b_1 and b_2. By analogy, the 2-port's noise can be treated as waves, noted c_1 and c_2, emanating from its input and output respectively. This definition combined with that of the S-parameters leads to the linear matrix representation:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} + \begin{bmatrix} c_1 \\ c_2 \end{bmatrix} \quad (25),$$

where c_1 and c_2 are correlated since they are attributed to the same origin: the intrinsic 2-ports. A physical interpretation of this representation in the time domain is to relate the noise sources c_1 and c_2 to the noise self- and cross-power spectral densities. In the frequency-domain, obtained by Fourier transform, these correspond to the auto and cross-correlation functions [95].

Arranging in a matrix form the noise sources, c_1 and c_2, as well as their correlation, one obtains:

$$C_s = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} = \overline{\begin{bmatrix} c_1 \\ c_2 \end{bmatrix} \begin{bmatrix} c_1 \\ c_2 \end{bmatrix}^+} = \begin{bmatrix} \overline{|c_1|^2} & \overline{c_1 c_2^*} \\ \overline{c_1^* c_2} & \overline{|c_2|^2} \end{bmatrix} \quad (26)$$

Here the sign "+" refers to the conjugate transpose operation and "*" is the complex conjugate. Equation (26), then, defines the noise correlation matrix of the 2-ports.

A useful expression for C_s as a function of both the physical temperature and the S-matrix is:

$$C_s = k_B T (I - SS^+) \quad (27)$$

Where I is the identity matrix. Equation (27) allows the extraction of the noise sources, defining the noise contribution of the 2-ports to any electronic circuit, directly from its S-matrix when its physical temperature is known.

From the same analogy introduced above, in addition to the scattering form defined by equation (27), the admittance, impedance and chain representations of the noisy 2-ports can be derived. This can be achieved using the transformations formulas provided in Table 1 in [95]. The Figure 18 illustrates these equivalent 2-port representations, and the resulting respective arrangement of the input and output noise sources.

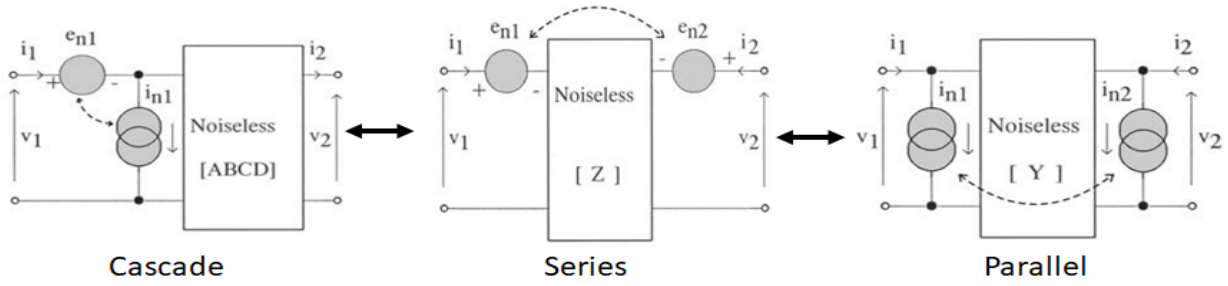

Figure 18: Illustration of the equivalent representations of a linear noisy 2-ports, based on ABCD, Z and Y-matrices – from [98].

From these derived properties, the rules to account for the different types of interconnections of the 2-ports are obtained using equations 5 – 7 in [95] For comprehensive purposes, the chain (ABCD) representation is of particular interest since it complies with the general definition of the equivalent input noise temperature. The noisy 2-ports is in this case seen as a noiseless device to which are connected at its input both correlated noise sources. This representation is, then, convenient to extract the set of 4 NPs introduced earlier as:

$$C_A = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \begin{bmatrix} R_n & \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}^*} \\ \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}} & R_n \left| Y_{opt} \right|^2 \end{bmatrix} \quad (28)$$

Equation (28) is obtained from (27) through the corresponding transformation. Consequently, the 4NPs are also function of the noise sources and the S-parameters of the device.

In the case of the HEMT, however, the effective temperature of the intrinsic device differs from that of the environment due to its active nature. Thus, the temperature in equation (27) cannot be directly predicted. Consequently, semi-empirical methods are the most established way to obtain the 4NPs of a HEMT. Indeed, a most common approach to retrieve the set of 4 NPs relies on i) the assumption of a thermal noise origin, ii) the extraction of the equivalent small signal model from the measured S-parameters, and iii) a single noise measurement of the device. Called the Pospieszalski noise model, this method has been previously implemented for a reliable modelling at cryogenic temperatures of various HEMT technologies [67] [99].

3.7. The Pospiezalski noise model

The Pospieszalski noise model intervenes following a major theoretical work by Van der Ziel in 1962 [92]. The thermal noise attributed to the channel conduction in FETs was then identified as the main noise mechanism, at frequencies beyond which 1/f noise is neglected. Upon the assumption of the thermal noise origin, in the Pospieszalski model, each resistive element in the equivalent electrical model contribute to the total noise temperature of the device. Thus, the full estimation of the device noise contribution depends on the effective temperatures of the resistances in the lumped equivalent model. In addition, the noise temperature values of the equivalent lumped elements which are not part of the intrinsic device are fairly approximated to be at the ambient temperature. The drain-to-source resistance, on other hand, is directly exposed to the self-heating from the drain power dissipation. The equivalent drain noise temperature is then noted T_d. The main originality in the Pospieszalski model is to treat the latter as a fitting parameter. This is together with the intrinsic gate noise temperature, noted T_g. T_g usually tends to the ambient temperature. Also, to comply with the fundamental thermal noise origin, T_d and T_g are frequency-independent.

In order to achieve the fitting against the measured noise temperature of the transistor, the NPs must be expressed as function of T_d and T_g so they can be plugged into equation (21). For this purpose, the circuit-theory of noisy linear two-ports is useful. More specifically, applied to the HEMT the admittance form of equation (27), as depicted in figure 18, leads to the equivalent representation shown in Figure 8. Hence, a noise current source is considered at the gate node, noted $\overline{i_g}$, and a noise current source at the drain node, denoted $\overline{i_d}$, in shunt with the noiseless device. Both current noise sources are correlated through the factor:

$$C = \frac{\langle i_g^* i_d \rangle}{\sqrt{\langle i^2{}_g \rangle \langle i^2{}_d \rangle}} \quad (29)$$

C reflects the capacitive coupling between the gate and the channel. The admittance form of the noise correlation matrix of the intrinsic device, C_{Y-int}, is then expressed [100]:

$$C_{Y-int} = \begin{bmatrix} \langle i_g^2 \rangle & \langle i_g i_d^* \rangle \\ \langle i_g^* i_d \rangle & \langle i_d^2 \rangle \end{bmatrix} \quad (30)$$

Since C_{Y-int} is related to the S-parameters of the devices, by means of equation (27) and the corresponding transformation matrix, it can be expressed as function of the equivalent small signal parameters and their assigned equivalent temperatures:

$$C_{Y-int} = \begin{bmatrix} T_g(R_i|Y_{gs}|^2 + R_{gd}|Y_{gd}|^2) & T_g\left(R_i|Y_{gm}|^* + R_{gd}|Y_{gd}|^2\right) + T_d g_{ds} \\ T_g(R_i|Y_{gm}| + R_{gd}|Y_{gd}|^2) + T_d g_{ds} & T_d g_{ds} + T_g R_i|Y_{gm}|^2 + T_g R_{gd}|Y_{gd}|^2 \end{bmatrix} \quad (31)$$

On the other hand, since the admittance and chain representations are equivalent, the NPs are directly derived from C_{Y-int} through equation (27) after applying the corresponding matrix transformation. Thus, the retrieval of the small signal model, in addition to T_d and T_g, leads to the extraction of the full noise model of the device through its 4NPs.

In fact, one notes that the intrinsic noise behavior of the device can also be fully described using the set of 4 parameters introduced in equation (30): $< i_g >$, $< i_d >$ and the real and imaginary parts of the correlation factor C. These parameters provide a direct insight on the frequency- and bias-dependences of the noise behavior at the discrete level of the device. This is in contrast to the set of 4NPs from equation (20), which are mainly indicative on the noise behavior at the macroscopic or the system level. Thus, the analysis of the parameters in equation (30) is useful from the perspective of the physical interpretation of the device's noise model.

3.7.1. Physical interpretations

Considering the example of the first cryogenic noise model of the GaN-HEMTs, from the experimental data presented in [A], Figures 19-a – d show the frequency- and bias-dependences of $< i_g >$, $< \mathrm{i_d} >$ and C at the physical temperature of T ~ 10 K. A strong dependence of $< i_d >$ with respect to $\mathrm{I_{DS}}$ is observed. $< i_d >$ mostly reflects the bias-dependence of $\mathrm{T_d}$. The latter increases proportionally to the drain power dissipation, leading to the self-heating of the channel – see Figure 19-d. $< i_d >$ is almost frequency-independent. This is consistent with the negligible effect of C_{gd} as observed in the previous chapter. $< i_g >$ presents a weak bias-dependence, it becomes relatively sensitive to I_{DS} for current levels higher than around 20% of the saturation level of the drain current. This might be linked to the increase of the ambient temperature due to the self-heating of the transistor. $< i_g >$ increases linearly with the frequency, resulting from the effect of C_{gs} on the input impedance of the transistor. This is also reflecting the fact that the noise appearing at the gate is induced from the channel through the capacitive effect, represented by C_{gs}. The variation of C tends to be frequency-independent. Also, C shows a negligible effect of its real part with respect to the imaginary one. One can reasonably consider that this correlation factor between the gate and the channel noise sources is purely imaginary. This is in line with the conclusions obtained from the theoretical works [101] [102]. Thus, in this case, the intrinsic noise model can be simplified to three parameters by excluding the real part of C.

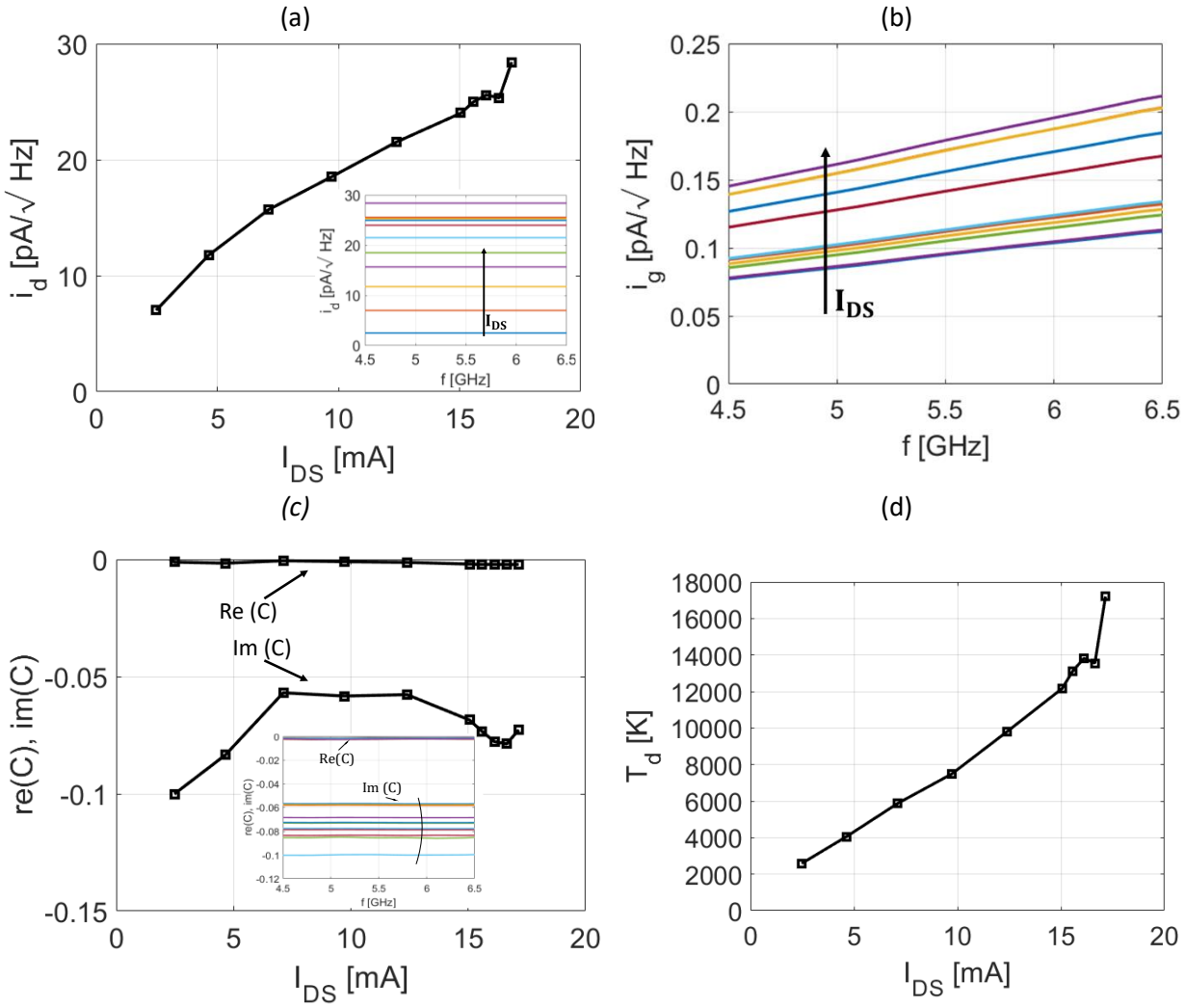

Figure 19: Extraction of the intrinsic noise sources of a GaN-HEMT at a cryogenic temperature of ~10 K, as studied in [A] a) Bias-dependence of $< i_d >$ at f= 6 GHz, the inset shows its frequency-dependence. b) frequency-dependence of $< i_g >$ at I_{DS} within the same range in Figure 19-a. c) Bias-dependence of C at f = 6 GHz, the inset shows the frequency-dependence. e) bias dependence of the frequency-independent parameter T_d.

3.7.2. Physical validation

The physical validity of the extracted Pospieszalski noise model can be verified through the condition on the Lange parameter defied as $N = R_n G_{opt}$, introduced in [103] and [67]:

$$1 \leq \frac{4NT_0}{T_{min}} \leq 2 \tag{32}$$

The left-hand side of the expression is consequence of the non-variant nature of N and T_{min} under lossless impedance transformation, while the second side is a property that was found specific to HEMTs and HBTs

devices [103]. Considering the intrinsic transistor, which noise contribution is denoted $T_{min-int}$, this condition is found to be satisfied over both the entire studied frequency and bias ranges as shown in Figure 20.

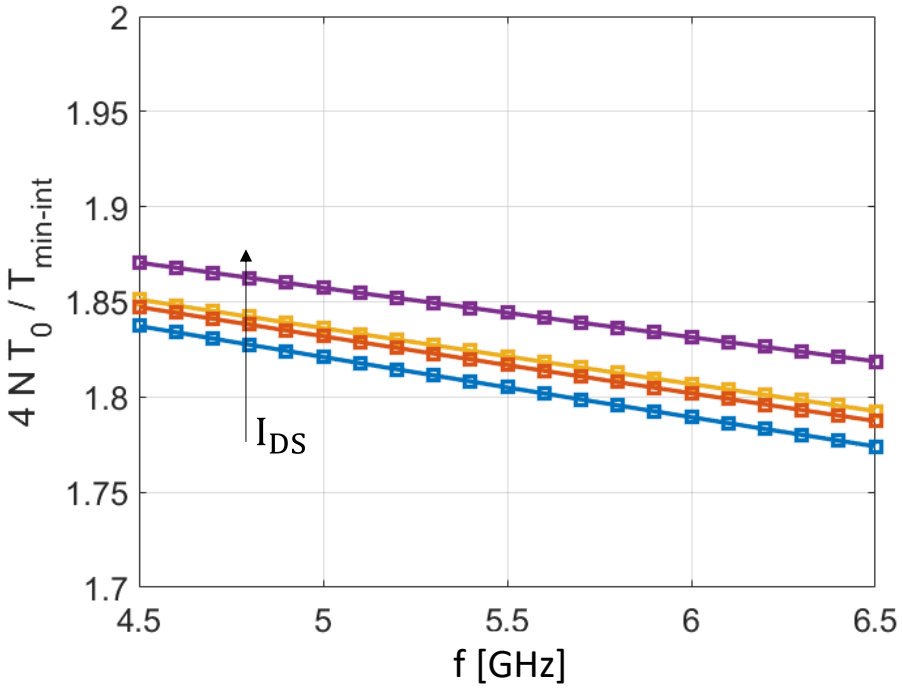

Figure 20: Variation of $\frac{4NT_0}{T_{min-int}}$ with frequency at cryogenic temperatures, at $I_{DS}[mA] = 2.5 - 10$, V_{DS} = 5 V – from [A].

3.8. Summary

In this chapter, the main existing technologies for low-noise amplification and their state of the art were reviewed. Through the analysis of this review, it was shown that the GaN technology may present a strong asset from its unique combination of low-noise and high-power performance. This is also motivated by its excellent low noise performance at room temperature, and its suitable static and microwave behaviors at cryogenic temperatures concluded from the last chapter. However, it was shown that the estimation of its potential for low-noise applications at cryogenic temperatures was still conditioned by the retrieval of a noise model at the same temperatures. Then, to this end, the Pospieszalski noise model was identified as one of the main established and reliable methods. Considering the first extracted cryogenic noise model of the GaN HEMTs presented in [A], an analysis of the parameters of this latter revealed an expected physical consistency.

4. Microwave Noise Measurements & techniques at cryogenic temperatures

This chapter discusses the experimental considerations surrounding the estimation of the noise temperature of devices at cryogenic temperatures, specifically applied to the noise characterization of cryogenic GaN-HEMTs. A general procedure to this end is presented, involving a specific test setup and a de-embedding routine. Finally, the validity and the uncertainty of the measurements and de-embedding processes are verified using a reference LNA.

4.1. The Y-factor method

The noise contribution of a transistor to any electronic circuit is commonly measured using the Y-Factor approach. The basic principle of this test method relies on applying two distinct levels of noise powers, or equivalently two different physical temperatures, at the input of the device under test (DUT). It is assumed that the DUT presents a linear variation of the output power with respect to the input power. It implies that any change in the noise power measured at the device's output constantly relates to the change of the input noise power. Hence two input states are sufficient to define the Y-Factor, Y, as the ratio of the corresponding measured output noise powers. Both the equivalent noise temperature of the transistor and its available gain can be inferred from the Y-Factor, as will be detailed.

Different techniques can be used to deliver the required couple of known input powers [78] [104]. For the following discussion, a noise-diode is considered as the source. From the off-state and on-state of the noise diode, the noise powers P_c and P_h, and their noise temperatures T_c and T_h, are respectively shown at the input of the DUT. The terms cold and hot are also used to refer to the off and on-states of the noise diode respectively, hence the subscripts c and h. The Y-Factor is then defined as:

$$Y = \frac{P_h}{P_c} \tag{33}$$

At the output of the noise source, the noise temperature relates to the noise power through the ratio:

$$T_{h,c} = \frac{P_{h,c}}{B\ k_B} \tag{34}$$

In order to specify T_h with respect to T_c, a parameter called the Excess-Noise-Ratio (ENR) is introduced and expressed in a linear scale as:

$$ENR = \frac{T_h - T_c}{T_0} \tag{35}$$

The DUT presents an available gain, noted G_a. From the general definition of the concept of noise temperature, the noise power at the output of the DUT results from the amplification of its equivalent noise temperature, T_e, and that delivered by the noise diode. It is expressed as:

$$P_{h,c} = Bk_B G_a (T_{h,c} + T_e) \tag{36}$$

Hence, using the Y-factor definition and solving for T_e, the equivalent noise temperature of the DUT is:

$$T_e = \frac{T_h - T_c Y}{Y - 1} \tag{37}$$

Similarly, the available gain derived from (36) is:

$$G_a = \frac{P_h - P_c}{Bk_B (T_h - T_c)} \tag{38}$$

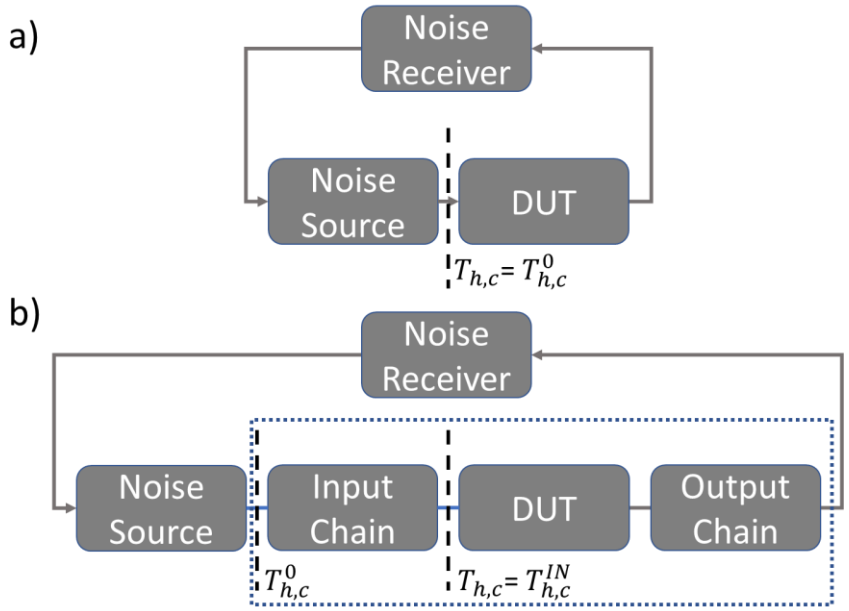

Figure 21: Illustration of the typical setup for the noise measurement in the case; a) a noise source directly connected to the noise receiver b) involving input and chains interfacing the DUT to the noise receiver, corresponding to the cryogenic measurements.

Equations (34) – (38) can be straightforwardly applied in the case of a DUT directly connected to the noise source. However, in practice and especially for the measurements in a cryogenic environment, a chain of components is used to interface the noise source with the DUT as illustrated in Figure 21. These components are usually passive and introduce different losses which, therefore, alter the expressions of T_h and T_c effectively presented at the input of the DUT. In this case, the latter parameters are noted $T^{IN}_{h,c}$. This is in order to distinguish the hot and cold temperatures delivered by the noise-diode which from now on are noted $T^0_{h,c}$.

As to provide a general expression of the resultant extraction in such scheme, it is considered a passive input pad at a known physical temperature T_{a-IN}, presenting insertion losses noted L_{IN} =1/G_{a-IN} , with G_{a-IN} its available power gain. Using the same reasoning as for equation (34), the noise power at the output of the input chain,.i.e., at the input of the DUT is expressed:

$$P_{h,c}^{IN} = kB\left[\frac{T_{h,c}^{0}}{L_{IN}} + \frac{T_{e-IN}}{L_{IN}}\right] \quad (39)$$

$$P_{h,c}^{IN} = kB\left[\frac{T_{h,c}^{0}}{L_{IN}} + T_{a-IN}(1 - \frac{1}{L_{IN}})\right] \quad (40)$$

Here T_{e-IN} is the equivalent noise temperature of the input chain. In equation (40), it was introduced the definition relating the equivalent noise temperature to the physical temperature and the insertion losses:

$$T_{e-IN} = T_{a-IN}(1 - \frac{1}{L_{IN}}) \quad (41)$$

Thus, plugging in equation (34), it is obtained:

$$T_{h,c}^{IN} = \frac{T_{h,c}^{0}}{L_{IN}} + T_{a-IN}(1 - \frac{1}{L_{IN}}) \quad (42)$$

Then, to extract the noise temperature of the DUT, equation (42) must be plugged into equation (37) using $T_{h,c} = T_{h,c}^{IN}$.

4.2. Cryogenic noise measurements – Specifications and challenges

T_e tends to substantially reduce at cryogenic temperatures. Thus, from the analysis of the equations extracted in the previous section, the impact of the input chain ($T_{h,c}$) is further emphasized in such conditions. Thus, in a cryogenic environment, one needs to particularly consider the specific conditions of the input chain from both the microwave and the thermal points of view. In fact, the cryogenic measurements present a number of challenges that condition both the structure of the characterization setups and the procedures to obtain the noise data.

First, compared to the noise measurements at RT, a major difference is the substantial larger time that the cryogenic measurements require. This is mainly due to the time needed for the cooling cycles, which typically take 7 – 8 hours. Second, from the microwave perspective, two main challenges can be identified. The first concerns the noise source impedance which may differ when switching from its off to on states. This impacts the frequency-dependence of the resulting noise temperature [105]. This is because the estimation of the frequency-dependent losses and gains, including that of the DUT, depend on the source impedance. The second concern is the estimation of the S-parameters at the cryogenic temperatures, since the insertion losses are calculated from the scattering parameters (S-parameters). Note that in the case of the cryogenic on-wafer measurements of the HEMT, a cryogenic calibration-substrate is usually available and is used with a coplanar probes-station embedded into a cryogenic system. However, this is not the case for the coaxial-based setups. This may impact, in particular, the estimation of the insertion losses from the input chain. Thus, a calibrated Vector Network Analyzer (VNA) is required to measure the respective S-parameters. A usual calibration at any physical temperature requires the measurements of 3 to 4 known standards. However, at cryogenic temperatures, such a 2-ports' procedure would require at least 42 hours in our conditions. This is because no mechanical manipulation of the setup is possible once

the system is cooled down. Over this required time for such a method of calibration, the possible drifts of the VNA operation may lead to multiple errors from each of the calibration standards' measurements. Besides, a measurement using a RT calibration may no longer be valid at cryogenic temperature (CT). This is due to the variation of the physical properties and geometry of the setup connections with the temperature (thermal contraction and conductivity changes), leading to an equivalent shift in the reference planes and hindering a proper de-embedding of the data.

Finally, a concern from the thermal point of view arises from the fact that not all the elements of the measurement setup are at the same physical temperature. It implies that the interconnects, typically made of coaxial cables, are subjects to a thermal gradient. Consequently, the estimation of the respective noise temperature is affected by the propagated uncertainty of its assigned physical temperature.

Addressing this set of challenges, a variety of non-trivial strategies were proposed in the literature to accurately extract the noise parameters of HEMTs [105] [104]. The choice of an appropriate method should simultaneously serve the practicality, the time consumption and the accuracy of the measurements. For this purpose, the cold-attenuator (CA) method offers several advantages [105]. The practicality of this method at cryogenic temperature is facilitated by the fact that only one noise source and a microwave attenuation are required. This is contrasting with other methods requiring, for instance, the use of input impedances-tuner [106], mechanical switches [107] or adapted heating systems [78] which are difficult and time-consuming to implement in a cryogenic setup. Furthermore, once the S-parameters of the different parts of the setup are available, the noise measurements are obtained over only one cooling cycle using the CA method. This is also advantageous time-wise.

The method primarily addresses the errors related to the input chain. This is achieved by placing an attenuator in front of the DUT. The losses of the attenuator are significantly larger than those of the other elements of the setup. Since the attenuator is placed at a fixed and uniformly distributed cryogenic temperature, which can then be monitored using a thermal sensor, its noise contribution is determined with a higher accuracy than the other input elements. Hence, the accuracy of $T_{h,c}$ is improved since the contribution of the cryogenic attenuator dominates in the expressions of T_{e-IN} and L_{IN}. In fact, considering now the presence of the attenuator, the expression of $T_{h,c}$ =$T_{h,c}^{IN'}$ at the input of the DUT becomes:

$$T_{h,c}^{IN'} = \frac{T_{h,c}^{0}}{L_{IC}L_{CA}} + \frac{T_{a-IC}(L_{IC}-1)}{L_{IC}L_{CA}} + T_{a-CA}(1-\frac{1}{L_{CA}}) \quad (43)$$

Where L_{IC} and L_{CA} refer to the losses of the input cable and the cryogenic attenuator, correspondingly, while T_{a-IC} and T_{a-CA} are their respective physical temperature values. It can be seen from equation (43) that, when L_{CA} is large enough, all the terms tend to be insignificant with respect to the last term which is only dependent on the temperature and losses of the CA. This way, the impact of the thermal gradient over the input cable is reduced proportionally to L_{CA}. The same also applies to the impact of the possible changes in the noise-source impedance when switched from its on to off states.

4.3. Experimental cryogenic setup of the noise characterization

Figure 21 presents a typical schematic overview of a cryogenic setup for the microwave noise measurements. This setup was, for instance, employed in [A], where further description of its different parts is provided.

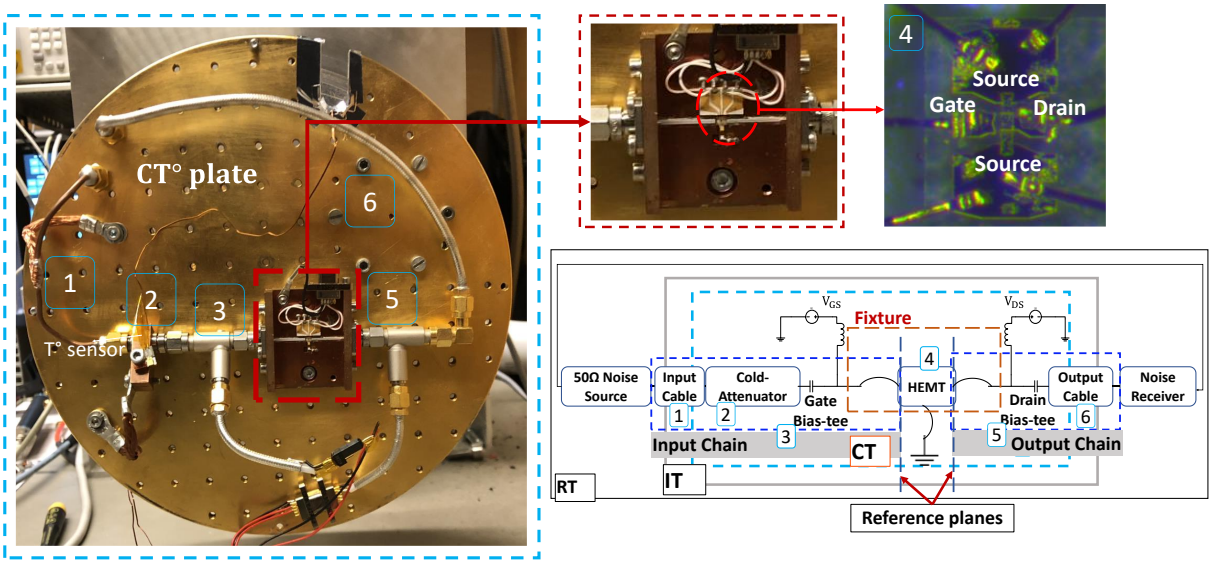

Figure 22: Image of the cryogenic noise measurements setup (left) with the corresponding block schematic (right). The image was mirrored to facilitate the readability of the schematic from left to right. In the top right is shown a microscopic top-view image of the transistor with the interconnecting bond wires, as mounted on fixture for the noise measurements. IT refers to the physical temperature of the cryostat stage interfacing the RT to the CT parts of the system. Reproduced from [A]

Such a setup relies on the implementation of the CA method. The system consists of a commercial 50 Ω noise-diode source placed at RT, the cryostat where the cryogenic system is embedded and includes coaxial cables, the 20 dB cold-attenuator, the bias-circuits and the fixture where the HEMT is mounted. The noise data are collected by the noise receiver, consisting of a spectrum analyzer and preamplifier, via an output coaxial cable. The cryostat has different stages, ensuring the transition from RT to the to the lowest cryogenic physical temperature, noted CT. The latter corresponds to the stage where the DUT is placed. A typical CT is around 10 K [A]. Further cooling can be provided, down to 4 K, as was the case in [B].

As discussed earlier, the CA method addresses the thermal gradient through the coaxial cables. In practice, for accurate implementation of the method, a calibrated thermal sensor is directly clamped to the 20 dB CA. Therefore, knowing the exact temperature of the attenuator helps in the de-embedding of the device noise temperature [108] [A]. In addition, in order to limit the thermal variation between the two ends of the stainless coaxial cables, with relatively low thermal conductivity.

The copper (Cu) fixture (Figure 22) hosting the HEMT acts a thermal sink for the transistor. The fixture, providing good thermal conductivity, consists of the input and output microstrip lines through which the transistor is electrically connected with Gold (Au)-based bond wires. A thin (5 mil) Alumina substrate is used for the microstrip lines.

The noise receiver block (figure 20) includes, for low-gain measurements, a preamplifier LNA in front of the spectrum analyzer to increase the signal-to-noise ratio. An electrical isolator in front can be used to limit the impact of the output impedance shown by the measured system on the noise temperature of the preamplifier [109]. The Friis formula is then used to subtract the noise contribution of the noise receiver block from the total measured noise temperature, before the extraction of the DUT noise temperature.

4.4. De-embedding of the cryogenic noise measurements

The de-embedding procedure of the cryogenic noise measurements addresses the challenges described in section 4.2.

For the following discussion, referring to Figure 22, the input chain includes: the input coaxial cable, the cryogenic attenuator, the gate bias-tee and the input microstrip line placed on the fixture. Also, the output chain is defined as including: the output microstrip line, the drain bias-tee and the output coaxial cable. T_{e-IN} and T_{e-OUT} , G_{a-IN} and G_{a-OUT} are respectively the resultant noise temperature and the available gain of the input and output chains. Hence, T_{e-DUT}, the noise temperature of the DUT is expressed:

$$T_{e-DUT} = G_{a-IN}\,[T_{e-sys} - \left(T_{e-IN} + \frac{T_{e-OUT}}{G_{a-IN}G_{a-DUT}}\right)] \tag{44}$$

To solve the equation (44), both the physical temperature and the available gain of each of the elements composing the input and the output chains must be known.

As discussed earlier, over the input coaxial cable the physical temperature is not uniformly distributed. Assuming a linear distribution, it is treated as in thermal equilibrium at an average between RT and CT noted T_{a-IC}. Considering the dominating impact of the CA, this same practice is commonly adopted with this type of measurements as reported in [104]. As mentioned earlier, the physical temperature of the CA, T_{a-CA}, is measured using a cryogenic thermal sensor. The CA and the fixture can be approximated to be at the same thermal equilibrium. Then, T_{e-IN} is expressed using the Friis formula as:

$$T_{e-IN} = T_{a-IC}(L_{IC} - 1) + T_{a-CA}L_{IC}[(L_{CA} - 1) + (L_{FI} - 1)\,L_{CA}] \tag{45}$$

Here the subscript “FI” refers to the input of the fixture, including the bias circuit, the microstrip line and the gate bond wire.

Similarly, T_{e-OUT} is:

$$T_{e-OUT} = T_{a-CA}(L_{FO} - 1) + T_{a-IC}(L_{OC} - 1)L_{FO} \tag{46}$$

The subscript “OC” denotes the output cable, and “FO” refers to the output of the fixture, including the bias circuit, the microstrip line and the drain bond wire. Both the gate and drain interconnecting bonding-wires from the microstrip lines on the fixture to the transistor had to be de-embedded simultaneously with the other fixture elements, so they were not considered as part of the DUT. Since a set of 4 bond

wires was used in parallel to connect the source pad to the ground, provided by the coper-wall of the fixture, the total source inductance is negligible and was accounted as part of the DUT.

The estimation of the available gains, and correspondingly the losses and the noise temperature of the passive elements, depends on the S-parameters measured using a VNA. At CT, a correction of the VNA calibration must be performed, as discussed earlier. In order to tackle this challenge, the following procedure was used.

It is based on the reasoning that the equivalent cryogenic effects, with respect to the RT calibration, can be treated as a virtual adaptor that is added at CT with respect to the RT reference planes. Also, it assumed that no additional mismatches are caused by the cooling-down at the frequencies of interest (< 8 GHz). Thus, a standard Short-Open-Load-Thru (SOLT) calibration is first performed at the desired reference planes at RT. Then, a 1-port measurement of a known reflective standard, a short which impedance,Γ_L, is measured at RT and CT [110]. Thus, considering the S-matrix of the virtual 2-ports which accounts for the cryogenic effects, as:

$$S_V = \begin{bmatrix} S_{11-V} & S_{12-V} \\ S_{21-V} & S_{22-V} \end{bmatrix} \tag{47}$$

The passivity implies $\mathrm{S}_{12-\mathrm{V}} = \mathrm{S}_{21-\mathrm{V}}$. Its input reflection obtained from the 1-port measurement writes as:

$$\Gamma_{IN-V} = S_{11-V} + \frac{S_{12-V}^2\,\Gamma_L}{1 - S_{22-V}\Gamma_L} \tag{48}$$

The assumption of the mismatch errors' absence leads to $S_{11-V} = S_{22-V} = 0$. Then, the insertion loss from the cryogenic effects is:

$$S_{12-V} = \sqrt{\frac{\Gamma_{IN-V}}{\Gamma_L}} \tag{49}$$

In the ideal case $\Gamma_{\mathrm{L}} = 1$, and $\mathrm{S}_{12-\mathrm{V}}$ is directly obtained from the 1-port measurement. The same is applied at each of the 2-ports termination that requires the correction, during the same cooling cycle. This cryogenic calibration method was previously applied in [110]. In [104], the use of the "fixture removal" tool available only in the modern VNAs was suggested. This function relies on the same reasoning as that of the procedure described above.

However, an additional step is required for the extraction of the S-parameters of the coaxial cables. As they are embedded in the system and bent to fit the cryostat setup, they cannot be measured directly. Thus, the first step consists of performing and saving a SOLT calibration at the external end of the coaxial cable at RT. Then, at the opposite end of the cable located in the CT stage of the cryostat, the standards are measured and used to de-embed their S-parameters at RT. The cryogenic effects can be afterwards corrected using the aforementioned procedure.

Alternatively, it was for instance suggested in [105] to perform a single measurement of the lines connected back to back. Half of the total measured insertion loss is then assigned to each cable. Since a perfect symmetry of the setup is assumed, additional considerations concerning the measurements setup would be in this case required. Once the losses from the cables determined, the losses of the cold-attenuator could be also similarly extracted based on the same assumption. In the next section, the results from this latter method applied to a reference LNA will be compared to those from the procedure describe above.

Once the S-parameters of the input cable, the attenuator and output cables are determined, the rest of the measurement system can be de-embedded from the total S-parameters measurements using matrices transformations. Moreover, the S-parameters of the transistors are obtained from on-wafer measurements in a cryogenic probe station, before mounting the fixture. While the bias circuits can be measured separately, the S-matrix of and the fixture elements can be accurately modelled using an EM simulator knowing their respective dimensions and physical parameters. These latter were tuned within 20 % of their nominal values, selecting the best fit result against multiple measurements with the transistor at different bias points.

To illustrate the result of the noise de-embedding procedure, the measured noise temperature from a similar sample as studied in [A] is presented in Figure 23 and compared to the simulated curves. These data were obtained at CT ~ 10 K. An excellent agreement of the measured and simulated data is obtained, at the different tested bias points and over the entire frequency range.

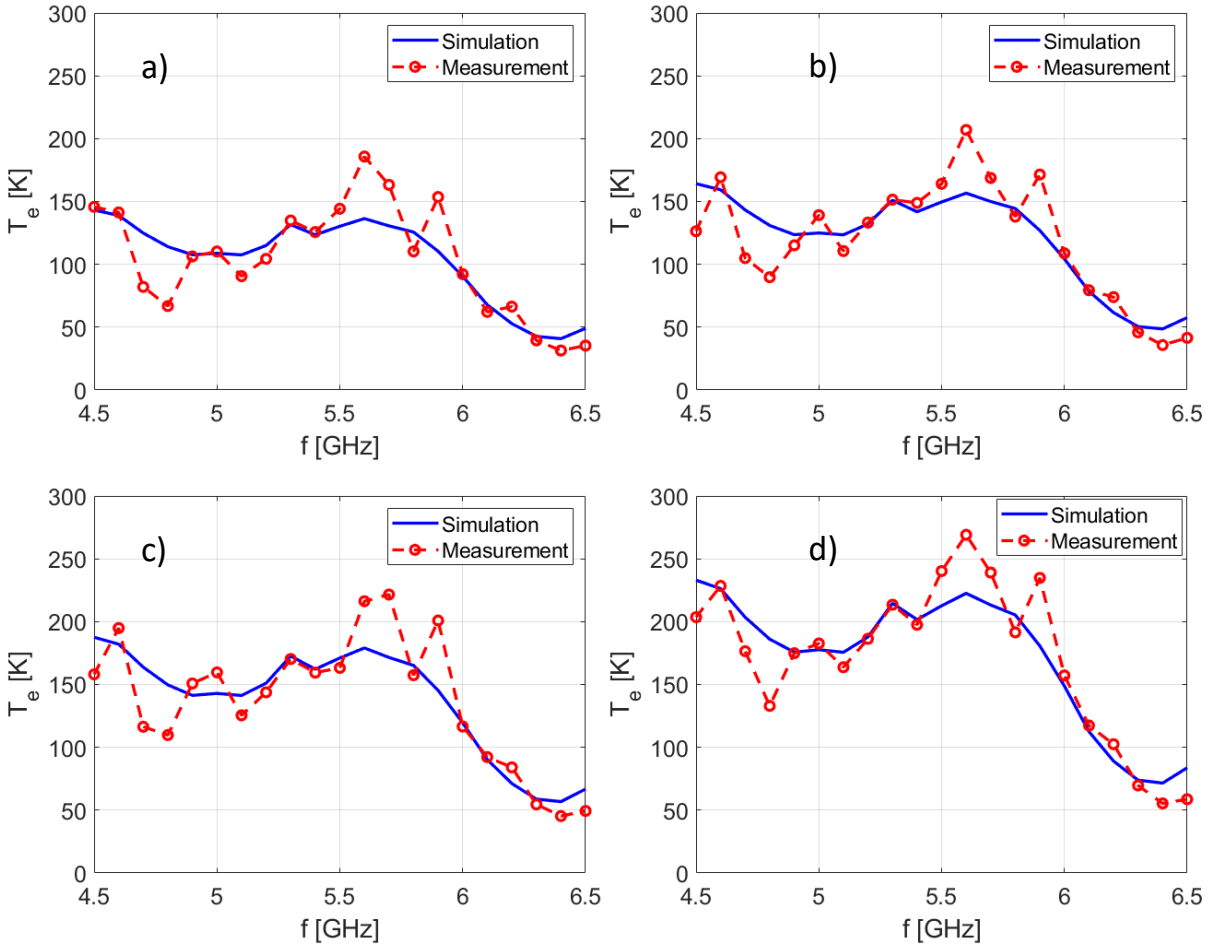

Figure 23: Comparison of the frequency-dependence of the modelled noise temperature (in blue) and the measured noise temperature (in red) of the DUT on-fixture, at V_{DS} [V] = 5 at different V_{GS} levels. a) V_{GS} [V] = -1.4, b) V_{GS} [V] = -1.3, c) V_{GS} [V] = -1.2, d) V_{GS} [V] = -1.1.

4.5. Measurements verification and uncertainty analysis

In order to gain insight into the validity of the cryogenic noise measurements, the de-embedding procedure introduced above and the confidence range in the estimation of the DUT noise temperature, a calibrated LNA of similar technology as reported in [111] was characterized as a reference. Hence in this section this LNA is referred to the as the Device Under Test (DUT). The reference LNA was measured in two different setups, noted setup # 1 and setup #2. The method relying on the gain measurements to estimate the losses of the different input and output chains was compared to the procedure based on the S-parameters measurements, both described earlier. The former method is referred to as method #1, while the de-embedding based on the measured S-matrices is referred to as method #2. Also, the measurements of the LNA gain using the noise Figure meter (NFM) were compared to those using the VNA in setup #1.

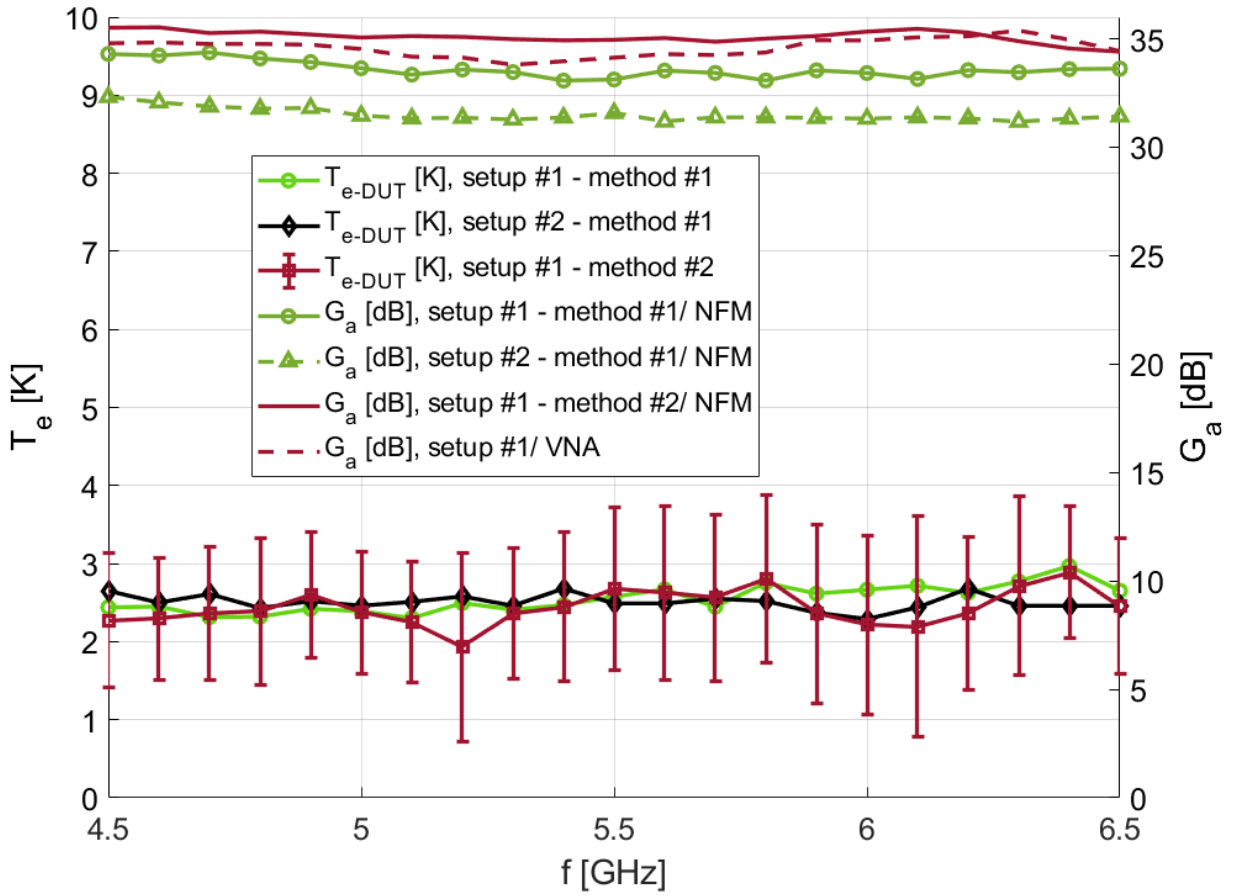

Figure 24: Comparison of the results of the calibrated LNA measured at ~ 10 K. The error bars are providing the RSS uncertainty of the noise temperature measured at each frequency point.

After its cooling to around 10 K, the noise temperature of the LNA, here denoted T_{e-DUT}, was de-embedded using the procedure described earlier. An overall good agreement is observed between the different data, demonstrating the efficiency of the calibration and de-embedding procedure. It simultaneously supports the repeatability of the results that can be obtained using the CA method, despite the use of different instrumentations calibrated at different places and times.

A quantitative estimation of the uncertainties around the noise temperature can be obtained through a sensitivity analysis of the different sources of errors. In the case of the measurements presented in Figure 24, a summary of the considered sources of errors is provided in table 2. The total uncertainty on the noise temperature of the DUT resulting from the sum of all the sources of errors, averaged over the entire considered frequency range of the noise characterization, is around ± 1.5 K. This uncertainty estimation is comparable with those obtained by other groups and published works. Note that the uncertainty estimation is usually presented in a root of the sum of squares (RSS) form, under the assumption that all the considered sources of error are uncorrelated, which corresponds in our case to ±0.8 K. For instance, a total (and RSS) uncertainties of ±1.3 K (±0.6 K), ±2.3 K (± 1.2 K), ±1.4 K (±0.7 K RSS) were reported in respectively [105], [74] and [78] .

Table 2: Summary of the uncertainty analysis of the results in Figure 24.

Source of error	Tolerance	Average resultant error in T_e [K]
Noise diode ENR	±0.15 dB	± 0.6
Noise diode temperature sensor	±1 K	± 0.02
Cryogenic temperature	± 12 mK	± 0.012
Input chain mismatch losses	±0.2 dB	± 0.6
Y-Factor	±0.02 dB	± 0.24
		± 1.45

The mismatch errors ascribed to the input chain, are usually ignored [74], [78] due to the difficulty surrounding their de-embedding and estimation. Also, an uncertainty on the physical temperature of the cryogenic attenuator that adds to that specified for its dedicated temperature sensor, was pointed out in [74]. This latter relates to the potential gradient of temperature between the outer conductor and the core resistive parts of the cold attenuator. It was considered ± 0.5 K in [74] using a similar cold attenuator-based setup. Adding this possible contribution to the initial analysis leads to a total uncertainty of ± 1.9 K (± 1 K RSS).

4.6. Summary

This chapter provided an overview of the challenges surrounding the microwave noise characterization at cryogenic temperatures. Different solutions to tackle these challenges were presented, especially through a specific test setup based on the Y-Factor and using the CA method. It was also presented a de-embedding procedure to extract the noise temperature of the DUT, specifically the GaN-HEMTs, embedded in a cryogenic environment. The validity of these measurements and de-embedding was verified using a known device, the estimated accuracy was compared to other works in the literature revealing the reliability of the presented procedure.

5. Noise Performance of GaN HEMT at cryogenic temperatures

In this chapter, the state-of-the-art noise performance of GaN HEMTs at cryogenic temperatures are presented. The results are based on the first extracted cryogenic noise model of GaN-HEMTs, presented in [A]. The experimental verification of the gate-width dependence of the same noise model is discussed in section 5.2. Finally, from the perspective of exploring one of the possibilities to optimize the noise performance, a study of Niobium (Nb)-based superconducting-gates is presented.

5.1. First cryogenic noise characterization and modeling of GaN-HEMTs

Using a standard process, the noise performance of the GaN technology at the cryogenic temperature of ~10 is demonstrated for the first time in the literature through [A] and discussed in this section. The Pospieszalski noise modeling approach, introduced in chapter 3, was used for this purpose. The model was completed with the cryogenic measurements of the noise temperature of the device using a single 50 noise source and the CA method, applying the procedure presented in chapter 4.

Considering the case of a sample with a gate-periphery of $L_g\ [\mu m] \times N_f \times W_g\ [\mu m] = 0.2 \times 2 \times 25$, Figure 25-a presents the minimum noise temperature at RT and CT from the extracted noise model.

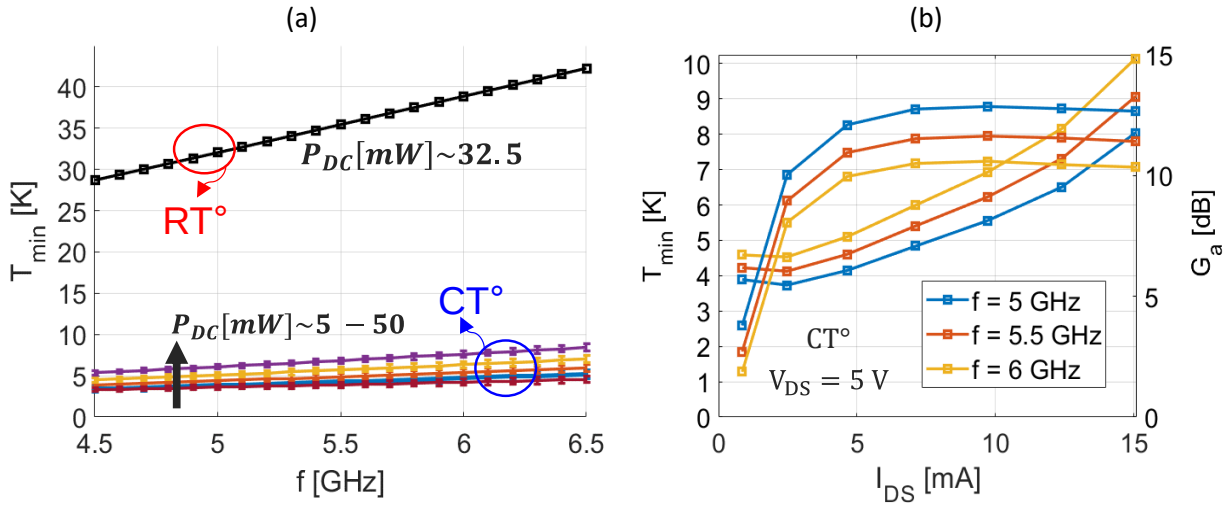

Figure 25 a) Frequency-dependence of T_{min} at RT and CT. b) Bias-dependence of the extracted T_{min} and the associated gain G_a at CT, at f [GHz] = 5 – 5.5 – 6 at V_{DS} = 5 V. Reproduced from [A].

Comparing the results at RT and CT, it is noted a substantial reduction of T_{min} by a factor of ~ 7.6 over the studied frequency band (Figure 25-a). The resulting noise model aligns with the conclusions from the DC and small-signal characterization presented above; the drop of the access resistances combined with the increase of the transconductance explain the recorded improvements as further detailed in [A]. The overall dependence with temperature of the noise contribution of GaN-HEMTs was found consistent with other works and the literature dealing with different HEMT technologies. In particular, the results confirm the substantial drop recorded using commercial GaN-LNAs upon their cooling to ~10 in [21]. The variations of T_{min} also compare to those obtained with GaAs and InP HEMTs in [66] [112].

From the extracted cryogenic noise model, the best T_{min} at CT was calculated ~4.1 ± 0.5 K, averaged over the measured frequency band. In addition to the fact that this is one of the very first cryogenic noise performance of GaN HEMTs reported in the literature, the results confirm a promising potential of this technology to compete for cryogenic low-noise applications. Indeed, referring to the current status of the existing technologies as presented in Chapter 3, the estimated best T_{min} of the GaN-HEMT at CT compares already directly to other technologies, especially those based on GaAs. Simultaneously, the cryogenic GaN-HEMT presents a relatively higher power dissipation. Indeed, the best cryogenic noise performance was achieved at a power consumption P_{DC} of about 12.5 mW (Figure 25-b). This value is about an order of magnitude larger than the state of the art in terms of the lowest power dissipation obtained with InP and SiGe technologies which is, as mentioned in chapter 3, around 0.1 mW. Also, the estimated noise performance of GaN-HEMTs compares by a factor of ~ 3 - 4 larger than the state-of-the-art of cryogenic HEMTs based on the InP material within the same frequency-band. It should be remined, however, that the results of GaN presented in this section constitutes the first iteration assessing the cryogenic noise potential of this technology. The other technologies, on the other hand, are taking advantage of an earlier development and optimizations of their structures within at least last 10 years.

In fact, the same extracted model provides certain insights on the possible improvements of the technology. From the perspective of identifying the technological parameters enabling the optimization of this performance as proposed in [A], the access resistances were found to contribute to the minimum noise temperature by at least 1 K increasing with both the frequency and bias conditions (cf. Figure 11 – [A]). This is complying with the analytical approximation of T_{min} provided in chapter 2.

As located before the gain stage of the transistor, represented by g_{m-int}, the resistances associated with the source and gate terminals are the most important contributors. The source resistance is linked to two parameters. The first is partly embedded in the 2DEG region, and is therefore dependent on the epitaxial properties and the electrons' confinement. The second parameter concerns the resistivity of the ohmic contact. This latter is around 0.3 Ωmm as estimated from TLM measurements at RT, which represents an order of magnitude higher than that usually obtained with the InP-based HEMTs [50] with a weak temperature dependence. Thus, this part of the transistor could present one of the bottlenecks to enable its future optimization. On the other hand, the gate resistance is mainly due to its metallization. Hence, in [B], it was studied the feasibility of using a superconducting-Nb materialization of the gate and its impact on the noise performance.

Also, the noise contribution from the gate leakage was calculated by considering a shot-noise current source in parallel with the gate-to-source impedance following the proposed approach in [67]. It was found to contribute by up to 4 % at the best bias point. It contributes, however, in a larger proportion at low frequencies as seen in Figure 26. This is consistent with the theoretical work in [113]. This finding could also be helpful for the design of cryogenic low noise amplifier, especially to comply with the requirements in terms of wide bandwidth covering relatively low-frequencies.

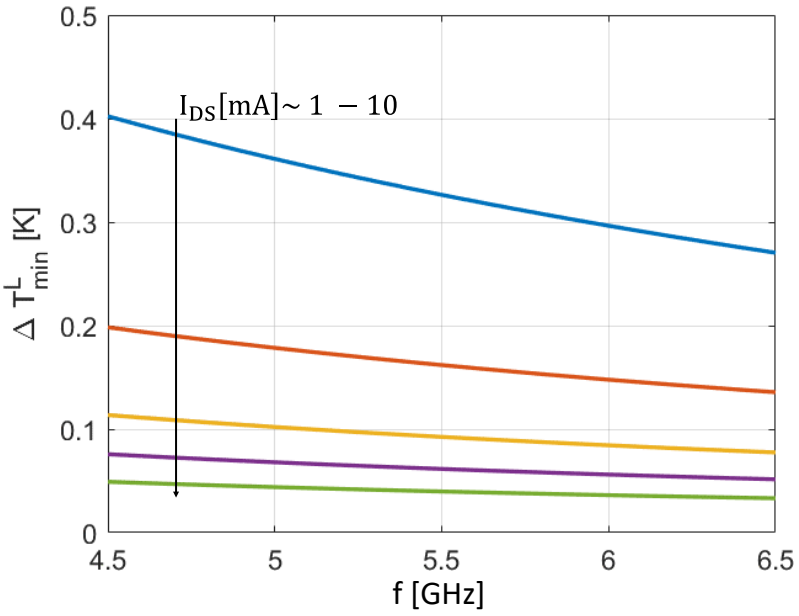

Figure 26: The frequency-dependence of the effects of the gate leakage on T_{min} at CT – Reproduced from Paper [A].

5.2. Gate-width dependence of the cryogenic noise model

From the perspective of the design of LNAs based on the studied technology, the choice of the size of the transistor is detrimental to comply with the different applications requirements [113]. In the formulation of the noise model presented above, the dependence on the gate-width is implicitly resulting from the that of the SSM parameters. Thus, the scalability of the noise model and device performance was experimentally investigated by measuring different devices with a total gate width of 150 µm, 100 µm in addition to the 50 µm case shown above, all present a 2 gate-fingers layout. The 4 NPs were then extracted for each device using the procedures presented earlier, together with their respective bias dependences. The results of the gate-width dependences for the 4 NPs are presented in Figure 27. As an exception among the 4 NPs, T_{min} is found almost unsensitive to the variation of the gate-width. Both the real and imaginary parts of the optimum impedance decrease when increasing the gate-width (Figure 27-b). The noise resistance R_n was found to decrease with width (Figure 27-c).

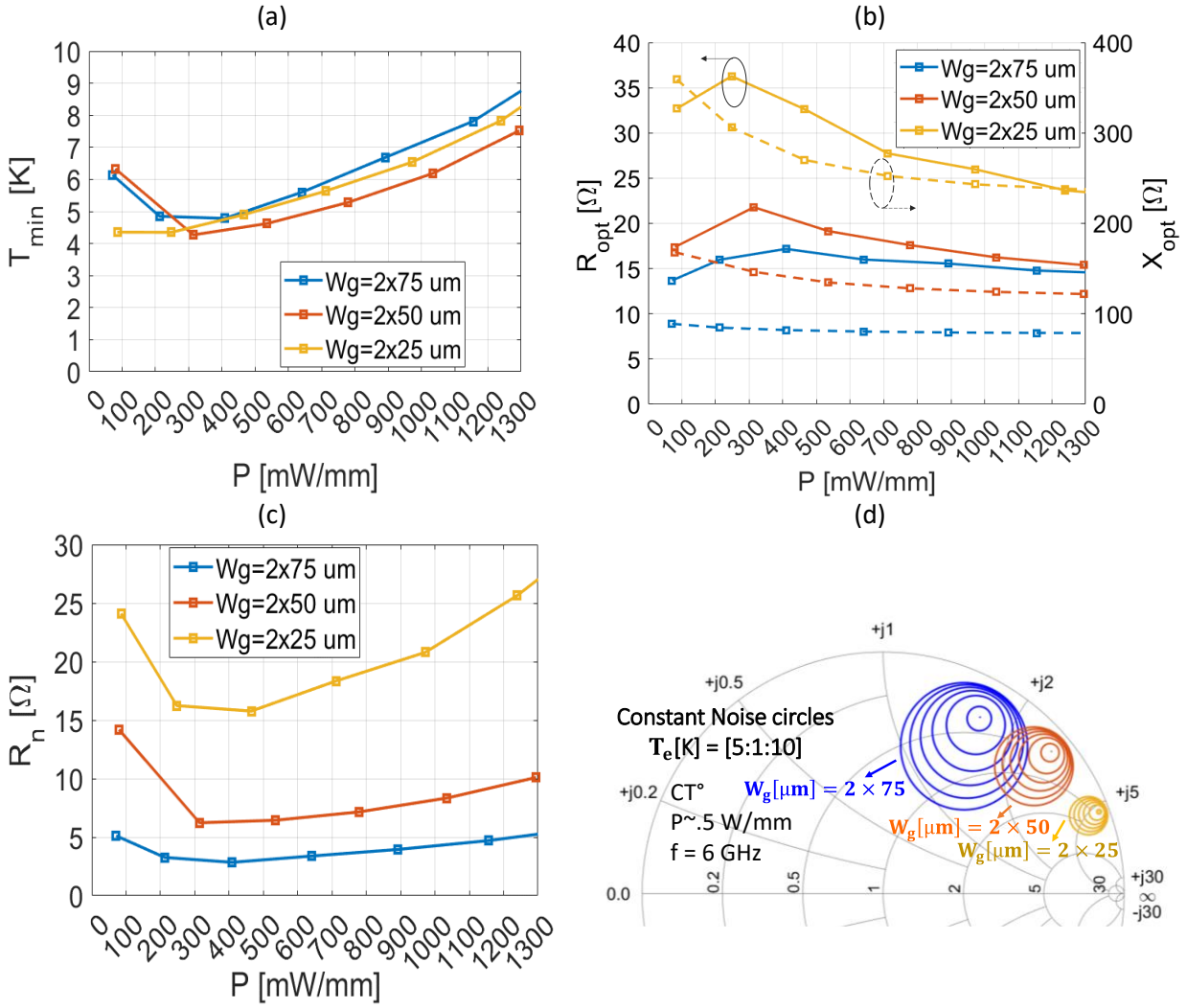

Figure 27: Variations as a function of power dissipated for different gate widths: 2x25 um (orange), 2x50 um (red), 2x75 um (blue) of a) T_{min} c) R_{opt} and X_{opt}c) R_n .d) constant circles of noise temperatures T_e [K] = 5:1:10, at f = 6 GHz and power dissipation of 0.5 W/mm. Reproduced from Paper [C].

These concluded variations of the 4NPs with the gate-width are in line with those reported in the literature for other HEMTs [114] [115]. Simultaneously, the results confirm the prior estimation of a best T_{min} in the range of 4 – 5 K. This holds, then, valid as long as the epitaxial and the lateral dimensions are kept identical.

In terms of power dissipation, in the range of 200 – 500 µW/µm all the studied devices exhibit a T_{min} ranging between 4 – 5 K. Confronting the bias dependences of the different devices, the best drain current was found to scale as expected by the same factor as that of the gate-width scaling.

The variations of R_n and Z_{opt} with the gate-width are indicating a decreased sensitivity of the design towards possible deviation from the optimum impedance when a transistor with a larger periphery is used. In other words, the design of a LNA devices based on the device with the largest gate-width of 2x75 µm would allow further gain-matching at the expense of a lower penalty on the noise performance. This

is best illustrated using the constant noise temperature circles plotted in the Smith Chart in Figure 27-d. The transistor with the largest gate-width of 2x75 µm is found to provide the widest constant noise circle, that is more options for the LNA designer to achieve the noise and gain-matching. However, such a choice of the transistor size restricts the power dissipation capabilities of the design.

5.3. Towards GaN-HEMTs with superconducting-gate

The importance of the role played by the gate resistance was suggested through the analysis of the noise model presented in Figure 7 and the approximation of T_{min} in equation (19). Moreover, in the previous section, the width-dependence of the input impedance, to which contributes the gate resistance, their impact on the optimum impedance, the noise resistance and consequently the noise and gain-matching of the transistor were experimentally revealed. Addressing these observations, the introduction of a superconducting gate electrode could be expected to provide two major contributions. The noise source associated with the gate tends to cancel, as in this case the sheet resistance of the superconducting-metallization tends to zero. For the same reason, the scaling of the gate resistance also cancels [B].

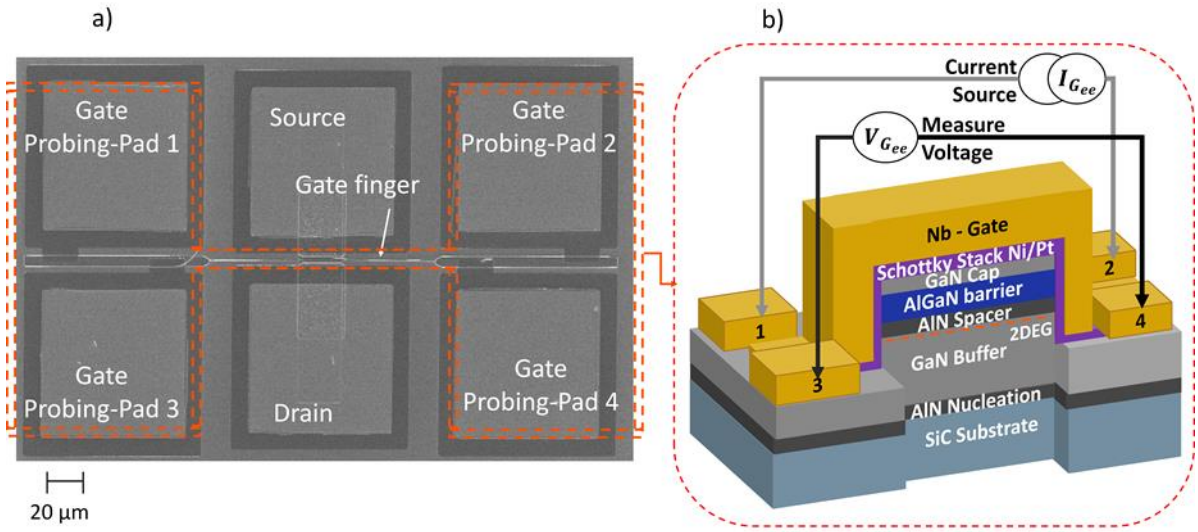

Figure 28: a) SEM picture of a device featuring 1-finger gate, incorporating four gate probing pads, as designed for the DC end-to-end gate resistance measurements b) Schematic cross-section view of the gate finger, with illustration of the setup used for the end-to-end measurement of the gate resistance: a current is forced through one pair of the gate probing pads, while the second pair is used to measure the voltage drop across the gate finger.

The possiblity and benefits of using a Nb-superconducting gate electrode in GaN HEMTs were investigated in [B]. Serving as references, devices with the identical structure and dimensions but with Au-gates were simultaneously measured and their results compared to those of their Nb-gated counterparts to assess the impact of the superconducting gate.

First, the temperature-dependence of the sheet resistance of the gate-metal was measured in a cryogenic system down to 4 K. The 4-probes type of measurements were used to this end, as shown in Figure 28. As practical for this type of tests, devices featuring one gate-finger with both Au and Nb gate metallization were tested first (Figure 28). Using the same configuration, samples with different gate lengths ranging

from 0.5 µm down to 0.15 µm were characterized. As shown in Figure 29, these measurements revealed a superconducting transition in the Nb-gates occurring at a critical temperature T_c ~ 9.2 ± 0.5 K. The extracted sheet resistance of the Au-gate at RT and CT were respectively ~ 3.5 nΩm/square and 0.5 nΩm /square. This substantial reduction of the sheet resistance with temperature of the Au-metallization also shows the source of the benfit on the noise performance from the cooling down of the device.

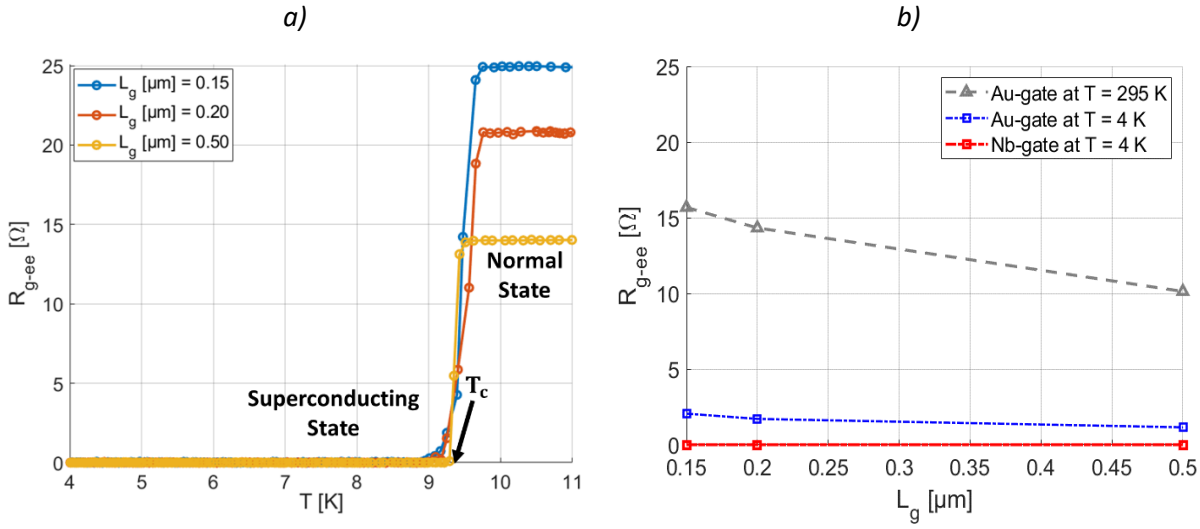

Figure 29: Variation of the end-to-end gate resistance of the Nb-gated device with the cryogenic temperature down to 4 K. b) Variation of the end-to-end gate resistance with Lg in the case of the Au-gated and Nb-gated devices

The gate superconductivity in transistors with two gate-fingers and presenting the layout configuration shown in Figure 4 was also verified. In this case, the devices were measured using a cryogenic probe station. The extraction of the gate resistance was in this case based on the measured S-parameters and the small signal model presented in chapter 3, following the procedure which was further detailed in [B]. As shown in Figure 30, in the devices featuring 2 gate-fingers the gate resistance was also minimized through the activation of the superconductivity of Nb below its critical temperature. This conclusion was verified to hold true independently of the gate-width. Thus, from the LNA design perspective, using the

superconducting Nb-gate release the consideration of the gate resistance and its impact when it comes to choose of a size of the transistor that fits best the application requirements.

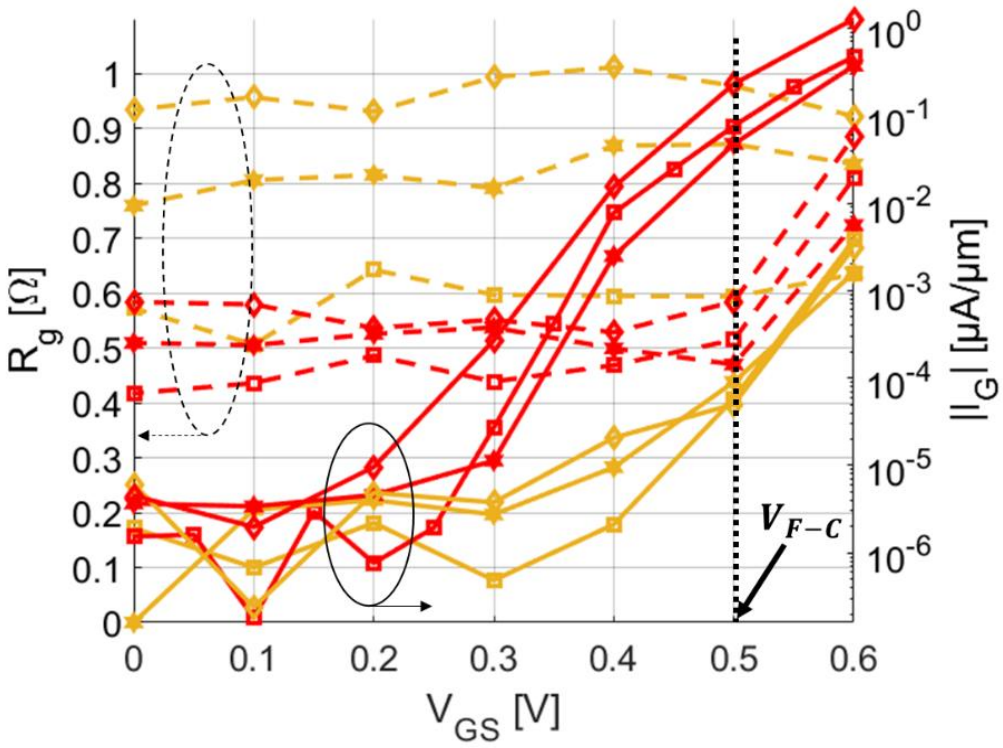

Figure 30: The gate-bias dependence of R_g (left axis) as calculated from the small-signal model and I_G (right axis), in Au-gated (in orange) and Nb-gated (in red) transistors. The markers square, hexagonal and diamond refer respectively to the unit gate widths of 25, 50 and 75 µm. At V_{GS} ~ V_{F-C}, I_G reaches a current density of ~ 0.1 µA/µm which coincides with a sudden significant rise of R_g.

Also, the study of the variation of R_g with the gate-bias revealed a correlation of the break of the superconductivity of the Nb-gate with the onset of the forward Schottky conduction of the gate, as at a certain $V_{GS} \geq V_{F-C}$ a sudden rise of R_g was observed. This feature was verified independently on the gate width, as shown in Figure 30. Note that in the latter Figure V_{GS} was swept to a maximum of 0.6 V to avoid the destruction of the Schottky gate. It is, however, clearly seen that for all the studied gate-widths, R_g rises by a factor of at least 1.6 within a step of only 0.1 V around $V_{GS} \sim V_{F-C}$. No significant change of R_g in the Au-gated transistor with the same dimensions was neither observed in that case. This behavior is explained by the existence of a superconducting critical current, exceeding of which destroys the superconductivity in Nb, which was equal to the Schottky current around V_{F-C} [116].

A second conclusion from the extraction based on the S-parameters is the fact that Indeed, from Figure 30 and as further discussed in [B], within a margin of error the average gate resistance was estimated 0.4 – 0.5 Ω in the Nb-gated transistors independently of the gate-width. On the other hand, and as expected, a linear proportionality of R_g with the gate-width in the Au-gated transistors was observed. As the absence of gate length scaling of the devices with Nb-gate further confirms its stable and repeatable

transition to a superconducting state at $V_{GS} < V_{F-C}$, the remaining part in the calculated R_g in this case should be attributed to the probing path of the gate electrode.

Concerning the impact on the noise performance, the GaN-HEMT with Nb-gate present a T_{min} about 5 K higher than its counterpart with Au-gate (Figure 31-a) which was around 8 K at 5 GHz. It was found that the superconductivity of the Nb-gate was broken at a drain bias several times below the optimum one, which may explain the resulting noise performance. This was verified using end-to-end measurements of the gate resistance, while applying a drain to source bias, in one gate-finger devices with the identical dimensions as the previously studied transistor. The superconducting-to-normal transition was revealed at a power dissipation level of about 5 µW/µm (Figure 31-b). Consequently, at the relevant drain current levels for the low-noise operation, the Nb-gated transistor present an equivalent R_g about 3 times higher than that of the Au-gated counterpart according to these measurements.

(a) (b)

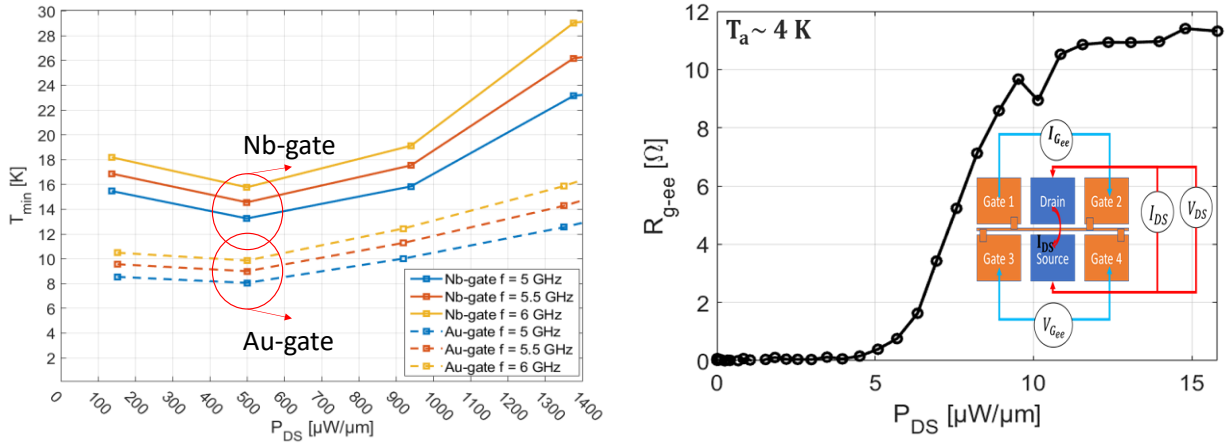

Figure 31: a) Comparison of calculated T_{min} vs. the dissipated power, $P_{DS} = V_{DS} \times I_{DS}$, at CT in GaN-HEMTs with Au and Nb-gates at f [GHz] = 5 – 5.5 - 6. b) Variation of the end-to-end gate resistance of the Nb-gate with the channel power dissipation, at temperature T_a ~ 4 K. The inset shows a schematic representation of the test structure with the 4-points configuration, used to measure the end-to-end gate resistance while varying the drain to source bias. Reproduced from [B]

The break of the superconductivity in this case can be ascribed to a rise of the physical temperature locally around the gate from ~ 4 K up to T_c ~ 9.2 K. This is a consequence of the self-heating resulting from the I_{DS} flow in the 2DEG channel and provided that the thermal impedance of the device allows such a gradient. Thus, the practical use of the GaN technology with superconducting Nb-gates for low-noise applications might be conditioned in the future by the enhancement of the heat-sinking capability of the structure.

Besides, it should be noted that the comparison of the results of the Au-gated transistors from this section with those presented in [A] reveals an important role of the gate capacitive coupling of the channel noise. Indeed, these transistors present a difference in the gate field-plate dimensions: F_{pgs} and F_{pgd} were respectively 50 % and 25 % shorter in [A]. This difference affects the gate capacitance, and consequently

the cut-off frequency of the devices. The latter has a significant impact on T_{min}, as previously described through equation 19.

6. Conclusions & Future Perspectives

This thesis was aiming to assess the potential of GaN-HEMTs for low-noise applications at cryogenic temperatures. Devices based on this technology with 0.2 µm gate length were designed, their cryogenic static, microwave and noise performance were characterized and analyzed. Through this study, a first model describing the microwave noise behavior at cryogenic temperatures was proposed. The model relies on accurate and well-established HEMT modeling and measurements approaches. Moreover, the results of the model were verified on different GaN-HEMTs samples and with different total peripheries. The extracted noise model allows an accurate implementation of the design of a future first cryogenic GaN-based LNA. Also, as both the frequency- and bias- dependences of the model were extracted, the cryogenic noise model provides the required information for the design of LNAs, which considers the different requirements set by the application in terms of temperature, frequency of operation and power consumption.

The estimated lowest noise temperature of the cryogenic GaN-HEMTs was revealed to be less than a factor of 4 as to compare directly to the state of the art in this field. Prospectively, aiming at the development of the GaN-technology for cryogenic low-noise applications, different possibilities to enhance the microwave and low noise performance of the GaN-HEMTs were proposed and investigated. Among these directions, it was demonstrated for the first time that GaN-HEMTs can integrate Nb-based superconducting gate electrodes. This was shown to minimize the resistance associated with the gate, independently of its geometry and periphery. Simultaneously, it was demonstrated that the power limitation arising from the self-heating of the device is still preventing to maintain the superconductivity of the gate even while the device is operated at low-noise bias conditions. Further enhancement of the heat sinking capabilities of the device may enable the full potential of this technology. Another possibility would be the investigation of the potential of similar superconducting materials, but with higher critical temperature. This would allow a larger critical level of power dissipation from the channel that leads otherwise to the break of superconductivity.

Furthermore, from the extracted model it was assessed a significant impact of the source and drain access resistances limiting the noise performance of the device. In fact, these resistances are controlled by the technological processes. Among the existing solutions that might address their limitations, it can be suggested, for instance, the doping of the region underneath the ohmic contacts [117]. Another solution would imply the scaling of the lateral dimensions, minimizing especially the gate-to-source distance [87].

Although relatively low, the gate leakage was found to provide a noise contribution, which is particularly significant at low frequencies. This limitation can be addressed through further electrical insulation of the single samples in the wafer using ion implantation, instead of mesa etching [118]. Another way to minimize the gate leakage would be to rely on a Metal-Insulator-Semiconductor-HEMTs (MISHEMTs) type of structures, instead of Schottky-gated HEMTs. This is involving the incorporation of a thin insulating layer between the gate and the top-layer of the epitaxial structure. This latter can provide a larger barrier of potential at the gate electrode, reducing the probability for the conduction of the gate current towards the intrinsic structure. This type of structures and their advantage in terms of low gate-leakage were demonstrated in the literature [119]. Besides, a potential combination of a GaN-MISHEMT structure with a superconducting gate might be possible considering of the results presented in [B]. In this case, the

impact of the additional insulating layer on the superconductivity of the gate and its bias dependence would deserve further studies.

Also, it was shown that an optimized design of the device may imply a gate geometry without a source and drain field plates. The capacitive effects associated with the latter were shown to sensitively limit the microwave characteristics at cryogenic temperatures. However, the removal of the field plates is associated with an increase of the gate resistance through a reduction of the gate cross-section (equation 6). This may, in turn, negatively impacts the noise performance through the increase of the thermal noise associated with the gate. The same applies to further reduction of the gate length to increase the cut-off frequency. Thus, it is suggested to combine a design with shorter gate length and no-field plates with that featuring several gate-fingers to reduce the gate resistance. On the other hand, since the use of superconducting gates leads to the suppression of the scaling of the gate resistance with the gate length as experimentally verified in [B], this may also motivate further efforts to enable their full potential at the low-noise bias conditions. In fact, addressing the self-heating limitations of the device would simultaneously enhance its competitivity in terms of power dissipation compared to the other technologies.

Finally, a general review of the latest advances in the field of the low-noise amplification technologies was provided. It was concluded that the GaN-HEMTs offer a unique combination of low-noise and high power-handling capabilities. This feature is expected being increasingly requested by modern low-noise applications, including those operating at cryogenic temperatures and RFI environments. The relatively larger power dissipation, compared to other technologies, is one of the main challenges facing the GaN-HEMTs for low-noise applications. Nevertheless, the technological development of the GaN-HEMTs is increasingly shortening the gap with other more established technologies which took advantage from their earlier development. These advances are due to an aggressive lateral scaling of the device, the optimization of the vertical epitaxy as well as that of the ohmic and Schottky contacts. The impact of these improvements at cryogenic temperatures are still to be demonstrated in the future.

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Cette thèse est dédiée à mon père et ma mère.

Paper A

Noise Characterization and Modeling of GaN-HEMTs at Cryogenic Temperatures

Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V.

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Paper B

GaN HEMT with superconducting Nb gates for low noise cryogenic applications

Mebarki, M.A., Ferrand-Drake Del Castillo, R., Pavolotsky, A., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V.

Physica Status Solidi A, 2022.

Paper C

A Cryogenic Scalable Small-Signal & Noise Model of GaN HEMTs

Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V.

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