A Cryogenic Scalable Small-Signal & Noise Model of GaN HEMTs

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***Abstract*— We present a detailed study of a scalable small signal and noise model at the cryogenic temperature of ~10 K of Gallium Nitride (GaN) - based High Electron Mobility Transistors (HEMTs). The results confirm a clear potential of the GaN technology for the cryogenic low noise applications as the model predicts a minimum noise temperature of ~ 4 K at the physical temperature of ~ 10 K. The improvement of the noise cryogenic performances is attributed to the decrease of the access resistances and the enhancement of the electron transport mechanisms. Moreover, the scalability of the model over the measured different gate peripheries is explored and provides new insights on the possibilities of further optimization of this technology for the cryogenic and low noise operation. Potentially, GaN HEMTs would provide enhanced dynamic range with the noise performance similar to InP devices.**

Keywords*— *AlGaN, cryogenic, GaN HEMT, LNA

I. Introduction

Cryogenic low noise amplifiers (LNA) constitute a crucial part of the systems dealing with extremely weak signals, as it is particularly the case in the radio astronomy receivers. This however often takes place in the presence of disturbing signals from communication and other microwave applications, e.g. radars. Most recently, the GaN-based HEMTs were demonstrated as a potential novel candidate for the development of cryogenic LNAs in [1]. Indeed, even though the matching networks in the reported GaN-LNAs were exclusively optimized for room temperature (RT) conditions, they exhibited an impressive improvement of their noise performance by almost a factor of 10, achieving ~8 K noise temperature, when cooled down to ~ 10 K. These results opened up new perspectives for the development of the GaN-technology for cryogenic applications. Indeed, in addition to the potential fulfillment of the gain and noise requirements, the targeted systems could benefit from the superior linearity and robustness which is inherent to the GaN-material over the competing technologies. Furthermore, given the recently reported enhancement of the heterodyne receivers incorporating GaN and attributed to the latter material properties [2], the integration of GaN-LNAs could be of interest from the technological perspective.

Thus, in order to enable the full potential of the emerging cryogenic GaN-HEMTs for low noise applications, it is a prerequisite to determine small signal model (SSM) and noise models at the temperatures and frequencies of interest. Also, it is important to relate the physical dimensions of the devices to their noise characteristics. Indeed, the availability of such a relation allows the designer to choose a size of the transistor which is best adapted to the overall system requirements. Moreover, it can provide insights for the optimization of the technology itself. Therefore, in addition to allowing the assessment of the reliability, the scalability of the models helps to reduce the number of iterations and the costs required for the optimization of both the cryogenic GaN-HEMTs and the LNAs based on this technology. To the best of our knowledge, there is still a lack in the literature of a cryogenic model of GaN HEMTs dealing with the scalability of the data.

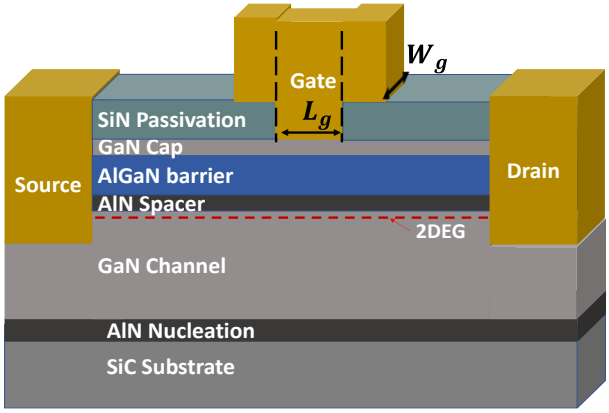

Fig. 1: Cross-section view of the epitaxial structure of the device.

This work proposes a scalable small signal and noise model of AlGaN/GaN HEMTs with a gate length of 0.2 µm at cryogenic temperatures (CT) of about 10 K. The validity of the model was investigated against the measurements for different total gate widths ranging from 50 µm to 150 µm. The HEMTs featured a 2 gate-fingers design. The typical cross-sectional view of the epitaxial structure of the devices is shown in Fig. 1. The static, microwave and noise characteristics of the same technology at cryogenic temperatures were recently studied in [3]. The details of the fabrication process are reported in [4].

II. II. Experimental Work

At both RT and CT, the devices were characterized on-wafer in a cryogenic probe station by using a parameter analyzer as well as a vector network analyzer. Fig 2 presents the typical measured I-V curves of the DUT at RT and CT, which feature a substantial decrease of the on-resistance of the HEMTs at CT.

For the high frequency noise tests, the devices were mounted in a fixture and measured in a cryogenic setup. The Y-factor technique and the cold-attenuator method [5], using a 20-dB attenuator, were implemented for the cryogenic noise characterization. We employed for this purpose a 50 Ω noise source and an Agilent MXA N9020A signal analyzer with its Noise Figure Measurement option. The noise measurements were performed within a frequency range of 4.5 to 6.5 GHz.

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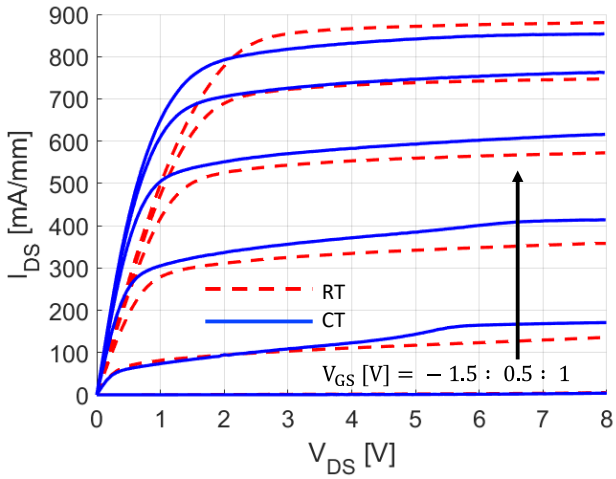

Fig. 1: Typical I_{DS}-V_{DS} curve of the DUT at RT and CT

The extraction of the noise parameters of the different HEMTs were performed by the de-embedding the contribution and noise temperature of the different elements in the cryogenic test system. Hence careful cryogenic calibration was performed prior to subtracting the noise contributions of the input and output chains of the system [6].

III. III. Results and Discussion

Relying on the measured S-parameters of the device, the extraction of the SSM followed the approach presented in [7]. Fig. 3 illustrates the equivalent small signal model, with the different noise sources associated with the lumped elements. The model revealed a consistent scalability of the SSM parameters with the transistor bias and its gate width, at both RT and CT, as can be seen in Fig. 4, 5 and 6 presenting respectively the variation of the access resistances, the intrinsic transconductance and gate to source capacitance. The figures reveal a significant increase of the intrinsic transconductance, g_{m-int}, together with the decrease of the access source and drain resistances, R_s and R_d respectively.

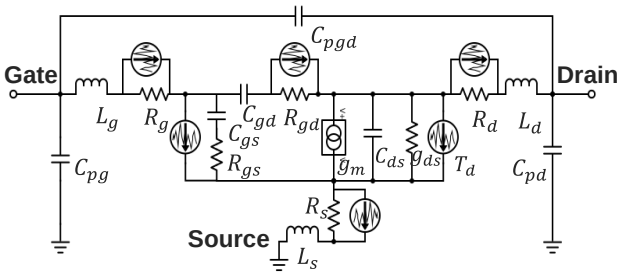

Fig. 2: Illustration of the equivalent small signal model, with the current noise sources associated with the different lumped elements

The inverse proportionality of R_s and R_d with the gate width reflects their dominating intrinsic nature. As recently reported in [8], using a similar technology, the gate resistance also reduces significantly at cryogenic temperatures. The gate resistance scales directly with the gate-width. The same applies to the gate-to-source capacitance, C_{gs}, impacting the input impedance of the device (Fig. 6).

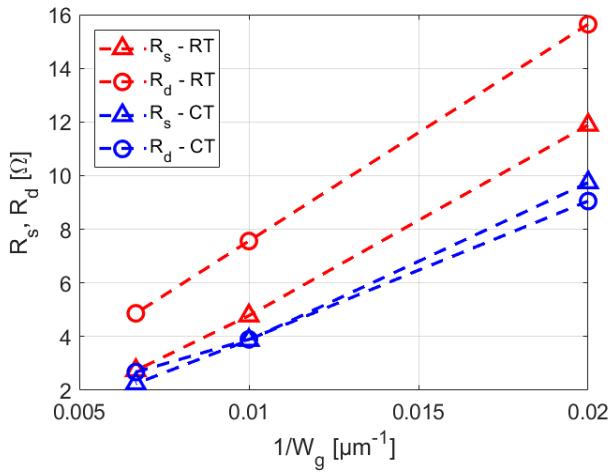

Fig. 3 Variation with the unit gate width of R_s (triangle markers) and (circle markers) R_d at RT (red) and CT (blue).

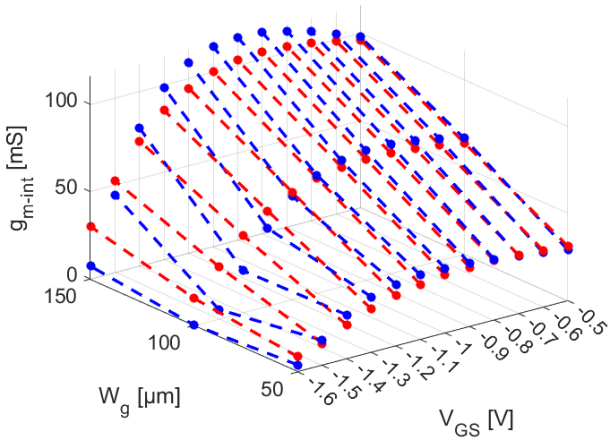

Fig. 4: Bias dependence of g_{m-int} and its variation with the gate width at RT (red) and CT (blue) at V_{DS} = 5 V..

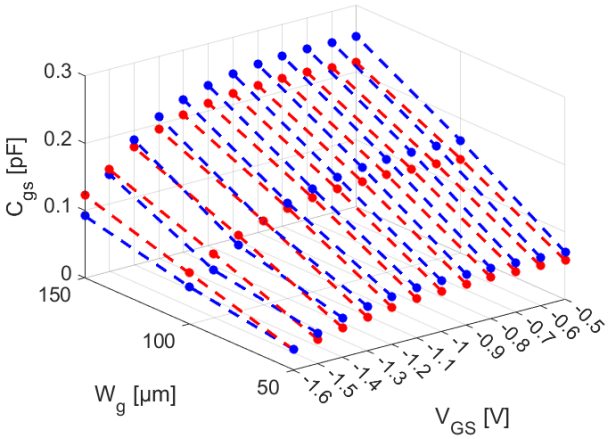

Fig. 5: Bias dependence of C_{gs} and its variation with the unit gate width at RT (red) and CT (blue) at V_{DS} = 5 V.

The combination of the decrease of the access resistances and the increase of the transconductance leads to a reduced impact of the thermal noise associated with the parasitic resistances of the device at cryogenic temperatures.

Once the cryogenic SSM and its scalability were determined, the Pospiezalski model [9] was implemented in order to extract the noise parameters of the devices. The model relies on the SSM parameters and the extraction from the noise measurements of the fitting parameter, T_d,

accounting for the temperature related to the drain to source resistance. This latter is considered being different from that of the lattice, due to the confinement of the electrons in the 2-dimensional electrons gas (2DEG), and is proportionally dependent on the power dissipation of the device.

As presented in Fig. 7, the optimum noise temperature, $T_{min-opt}$ [K] at CT was found in the range of 4 – 5 K independently of the gate-widths. The observed weak variation of the minimum noise temperature with the gate-width is consistent with the conclusions from other works in the literature dealing with the scalability of the noise data of other FET and HEMT technologies [10]. The optimum bias point (V_{DS}, I_{DS}), at which $T_{min-opt}$ is obtained, was found to scale by approximately the same factor as the gate width (Fig. 7). As a consequence of the variation of of the small signal model with the gate-width, the other noise parameters scale with the gate width. Indeed, as it was demonstrated in [10], the radius of the constant noise figure circles varies with the gate width. Therefore, the radius of the constant noise circle can be optimized given an optimal gate width value. A broad noise circle facilitates the search of a good compromise on the gain and noise performances of the practical LNA. Fig. 8 shows the effects of this property in our model. The same plot shows the variation of the optimum reflection factor $\Gamma_{opt}^{W_g}$, with W_g.

The constant circles of the noise temperature ranging from 5 K to 10 K of the three studied transistor gate widths are plotted around the power dissipation level of 0.5 W/mm at the frequency f = 6 GHz. The transistor with the largest gate-width is found, in this case, to provide the broadest constant noise circles. In fact, this variation reflects also the decrease of the noise resistance R_n [Ω], with the gate-width.
The decrease of R_n leads to a reduced sensitivity of the minimum noise temperature towards the deviations from the optimum impedance. However, a transistor with a larger gate width will drive more current (Fig. 8). This will in turn affect the overall power consumption of the application system.
This might be especially critical when LNAs of multiple stages are implemented. The choice of the transistor size needs then to satisfy both the system requirements and the practicality of the design.

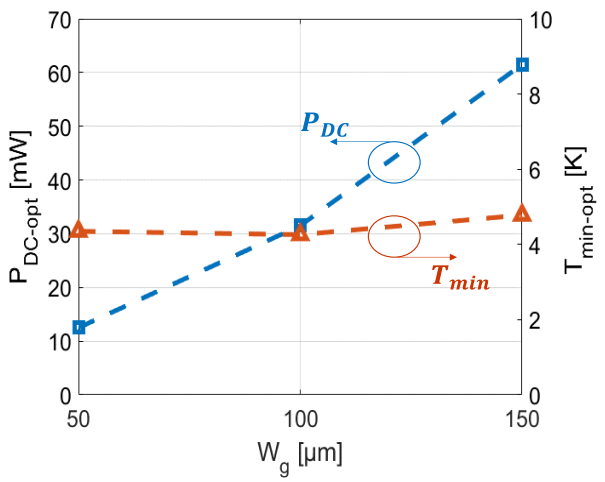

Fig. 7: Width-dependence of the predicted optimum noise bias (left vertical scale) and optimu noise temperature (right vertical scale) at CT.

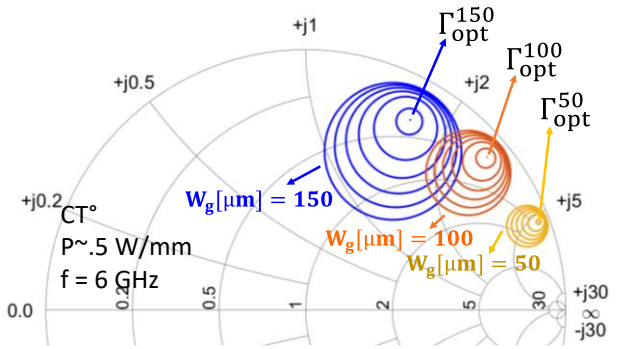

Fig. 8: Variation of the constant noise circles of T_e [K] = [5,6,7,8,9,10] for different gate widths: 2x25 um (orange), 2x50 um (red), 2x75 um (blue) at CT, at f = 6 GHz and power dissipation P ~ 0.5 W/mm.

IV. IV. Conclusion

This work experimentally verified for the first time the scalability with the gate periphery of a small signal and microwave noise model of GaN-HEMTs operating at the physical cryogenic temperature of ~10 K.

The results show a promising low-noise performance of GaN at cryogenic temperatures, as an optimum noise temperature 4.5 ± 0.5 K was obtained at CT from the different studied devices with the total gate-widths ranging from 50 up to 150 µm. This result is comparable to more established cryogenic low-noise technologies. Further optimization at the device level might lead to an enhanced competitivity of the GaN technology in this field. In addition, the extracted models provide the key elements for the future design of cryogenic GaN-based LNAs.

Acknowledgment

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