GaN High-Electron-Mobility Transistors with Superconducting Nb Gates for Low-Noise Cryogenic Applications

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GaN High-Electron-Mobility Transistors with Superconducting Nb Gates for Low-Noise Cryogenic Applications

Mohamed Aniss Mebarki, Ragnar Ferrand-Drake Del Castillo,* Alexey Pavolotsky,* Denis Meledin,* Erik Sundin,* Mattias Thorsell,* Niklas Rorsman,* Victor Belitsky,* and Vincent Desmaris**

The successful integration of superconducting niobium (Nb) gate electrodes into cryogenic gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) is reported. This is achieved through a specifically developed microfabrication process. The device's DC, microwave, and noise performances at cryogenic temperatures, down to 4 K, are studied and presented. The superconductivity of the gate is tested using DC end-to-end measurements. A clear superconducting state transition at a critical temperature, T_c, of ≈9.2 K is shown. This is further verified with GaN HEMTs with two gate fingers and a gate length of 0.2 μm, through the extraction and validation of a small-signal model at $T < T_c$. Additionally, the superconductivity of the gate is verified for several gate widths and lengths, showing a significant reduction of the gate resistance independently of its dimensions. Finally, a comparative study of the cryogenic microwave noise performances of the GaN HEMTs with gold (Au) and Nb gates is presented. The Au-gated device presents a competitive optimum noise temperature, $T_{min\text{-}opt}$, of ≈8 K at 5 GHz, demonstrating the potential of this technology for cryogenic low-noise applications. The Nb-gated device presents a 5 K higher $T_{min\text{-}opt}$, which is found to be related to the suppression of the superconductivity of the Nb gate at the optimum-noise bias.

1. Introduction

The applications dealing with the processing and detection of extremely weak signals, such as quantum-computing systems as well as the instrumentation in radio-astronomy and space-science fields, require ultimate low-noise performance. High-electron-mobility transistors (HEMTs) are widely used in these applications, operating at cryogenic temperatures in order to reduce the noise and comply with challenging requirements. The gallium nitride (GaN)-based technology emerges as a potential candidate for the low-noise cryogenic applications, given the significant improvements of the material properties at low temperatures.[1,2] Furthermore, the noise performance of the GaN-based low-noise amplifiers (LNAs) was experimentally demonstrated to improve when cooled down to 4 K[3]

One of the physical parameters limiting the noise performances of the GaN HEMTs, and more generally those of field-effect transistors (FETs), is related to the resistance of the gate electrode metallization. Indeed, this resistance introduces a thermal noise source,

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which negatively affects the overall microwave and noise performances of the device.[4] Moreover, the scalability of the gate resistance may impose additional compromises on the design criteria of the device. For instance, a larger gate length would result in a smaller gate resistance but critically limits the high-frequency capabilities of the device as the cutoff frequency is inversely proportional to the gate length. The reduction of the gate width has the same benefit but may compromise the trades-off related to the LNA design in terms of power, small-signal gain, and noise.[5,6] Also, the gate resistance can be reduced by optimizing its cross section. This is, however, usually achieved at the expense of additional parasitic effects, which also limit both the small-signal gain and the noise of the transistor.[7,8] Furthermore, as a consequence of the skin-depth effect in normal metals, it is known that the microwave conduction losses related to the metallization will increase with the frequency. This also leads to the deviation of the gate resistance from that of the dc operation at high-frequency limits.[9]

In this work, we propose to address the challenges on the cryogenic microwave low-noise operation of the GaN-HEMTs imposed by the gate electrode by the introduction of a superconducting material. For this purpose, niobium (Nb) material offers several advantages. In fact, Nb presents a zero DC resistance at temperatures below its critical temperature of about 9.2 K. The critical temperature of Nb is thus higher than the minimum physical temperature that can be reached using a helium-based cooling system, which is also usually required for the characterization and the practical operation of the cryogenic LNAs.

For Nb, to maintain its superconductivity in the high-frequency operation, only a thickness equivalent to around three times that of the London magnetic penetration depth, λ_L, is required. For sputtered Nb, typical λ_L is ≈85 nm.[10] Thus, that for the same metallization thickness as that of the conventional gate metallization usually made of Gold (Au), within the targeted microwave range, Nb is potentially able to cancel the conduction losses and the associated noise source with respect to both the frequency of operation and the dimensions of the gate. This represents an advantage from both the technological and the operational points of view.

Through this article, we first demonstrate the successful integration of the superconducting Nb gate to the GaN HEMTs. Then, the cryogenic DC, microwave, and noise performances of the fabricated devices are presented and analyzed.

2. The Device Structure and Fabrication

Figure 1a presents a cross-sectional view of the epitaxial structure of the studied HEMTs. To study the effect of the gate metallization on the different characteristics and performances of the devices, HEMTs with Nb gates and HEMTs with Au gates were fabricated on the same die following identical processing steps, except for gate metallization. The processing details common to both types of transistors are presented in this paragraph, while the gate processing will be further separately described below. The HEMT epitaxial structure is based on a 1.8 µm-thick GaN buffer layer grown on an AlN nucleation layer residing on top of SiC substrate. The buffer insulation was obtained by Fe doping. The barrier consists of nominally 11 nm-thick AlGaN layer, with 29% Al fraction. An AlN spacer, of 1.5 nm, separates the barrier from the channel to enhance the confinement of the 2D gas electrons (2DEG). On top of the barrier is a GaN cap with 2 nm nominal thickness, followed by SiN passivation layer of 60 nm.

The devices were isolated by mesa etching to a depth of 150 nm. The ohmic contacts were obtained by the recessed Ta ohmic contact.[11] The nominal gate-to-source distance, L_{GS}, was 0.75 µm and that of the gate-to-drain, L_{GD}, 1.5 µm.

The transmission line measurements (TLM) indicated a contact resistance of 0.32–0.36 Ω mm and a sheet resistance of 247–250 Ω sq^{-1}. The 2DEG sheet carrier concentration and the electron mobility, extracted at room temperature (RT) by Hall measurements after fabrication, were 1.09×10^{13} cm^{-2} and 2090 cm^2 Vs^{-1}, respectively.

The gates were defined by electron beam (e-beam) lithography. The Schottky contact was obtained using Ni/Pt stack of 20/30 nm, in both the Au-gated and Nb-gated devices. The Au-gate metallization was deposited by e-beam evaporation with thickness of 300 nm.

In the case of the Nb gates, the deposition was performed by means of DC magnetron sputtering with the same thickness of 300 nm. The Nb deposition process was previously detailed in

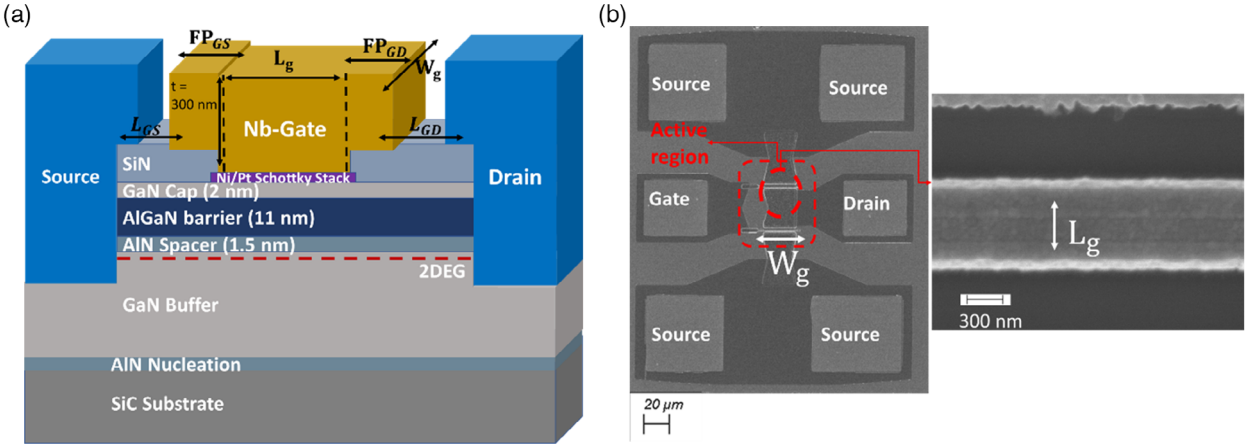

Figure 1. a) Cross-section view of the epitaxial structure of the devices. b) SEM image of a fabricated device; in the inset, the gate finger is magnified.

the study by Pavolotsky et al.[12] A palladium (Pd) layer of 50 nm was deposited on top to prevent the oxidation of Nb. Field-plate extensions of the gate toward the source and drain, FP_{GS} and FP_{GD}, respectively, were set to 0.2 µm. A scanning electron microscope (SEM) image of a fabricated sample with 2×25 µm gate periphery is shown in Figure 1b, where higher magnification of the gate finger region is also reported.

3. Electrical Characterization

The electrical characterization was performed on-wafer at room temperature, RT, and the cryogenic temperature, CT, in a cryogenic probe station. An Agilent B1500A semiconductor parameter analyzer was used for the DC characterization. In **Figure 2**, the typical DC transfer characteristics of 2×25 µm devices, with Au gate and Nb gate with identical dimensions, and the gate length of $L_g = 0.2$ µm are presented. We note that both transistors present similar characteristics, indicating the noncompromising impact of the Nb gate on the DC operation.

Also, as expected, a substantial improvement of the DC performances is observed at CT as compared with RT. From the I_{DS}–V_{DS} curve, the on-resistance of respectively the Nb-gated and Au-gated devices improved from 1.63 and 1.6 Ω mm to 0.89 and 0.88 Ω mm, which represents a decrease of ≈45%. The maximum drain-to-source current, I_{DS}, at a gate-to-source voltage, V_{GS}, of 0 V, was increased by ≈11%, from 861.3 and 868.1 mA mm^{-1} at RT to 955.6 and 954.9 mA mm^{-1} at CT. The maximum extrinsic transconductance, g_m, also increased from 449 and 431 at RT to 538 and 518 mS mm^{-1} at CT, representing an improvement of ≈20%.

4. The Characterization of Gate Superconductivity

As can be inferred from the layout of the device shown in Figure 1, the gate has a distributed nature over the active device. From the electrical point of view, the gate resistance is embedded in a series connection with the probing pads and the active device. Therefore, the contribution of gate metallization can be difficult to be accurately estimated by only relying on an equivalent lumped model. Thus, in order to characterize the resistivity—or the superconductivity in the case of Nb—of the gate metal, the end-to-end resistance measurements were carried out allowing its direct extraction.

4.1. Direct Extraction by DC End-To-End Measurements

The DC end-to-end characterization was performed with a four-point configuration. A layout including two pairs of probing pads connected to the gate electrode was designed. **Figure 3**a shows the SEM image of a fabricated sample with this configuration. The test setup illustrated in Figure 3b was used. Considering the gate finger as a rectangular conductor, at a physical temperature, T, the gate end-to-end DC-resistance, R_{g-ee}, is then related to its dimensions by

$$R_{g-ee}(T) = \frac{\Delta I_{Gee}}{\Delta V_{Gee}} = \rho_g(T)\frac{W}{tL} \quad (1)$$

where I_{Gee} is the forced current through one pair of the gate pads, V_{Gee} the measured voltage drop through the second pair, W is the gate-finger width, L its length, t its thickness, and ρ_g is the gate metal resistivity.

Samples with different gate lengths ranging from 0.15 to 0.5 µm were tested at temperatures down to ≈4 K and measured using the configuration described above (Figure 3b) at V_{DS} [V] = I_{DS} [A] = 0.

The variation of R_{g-ee} with the physical temperature was then measured, with an estimated accuracy of the temperature reading of ≈0.5 K. The results are shown in **Figure 4**a. At a critical temperature, $T_c = 9.2$ K, a clear superconducting transition is distinguished below where the measured gate resistance tends to zero. All the tested samples with the different gate lengths presented the same feature, confirming the repeatability of the results and the process. For comparison, R_{g-ee} of Au-gated devices with identical dimensions and layout were measured. Figure 4b shows the dependence of the measured gate end-to-end resistance with respect to L_g, with fixed gate width and field plate extensions. It is observed that, in contrast to the effect of the

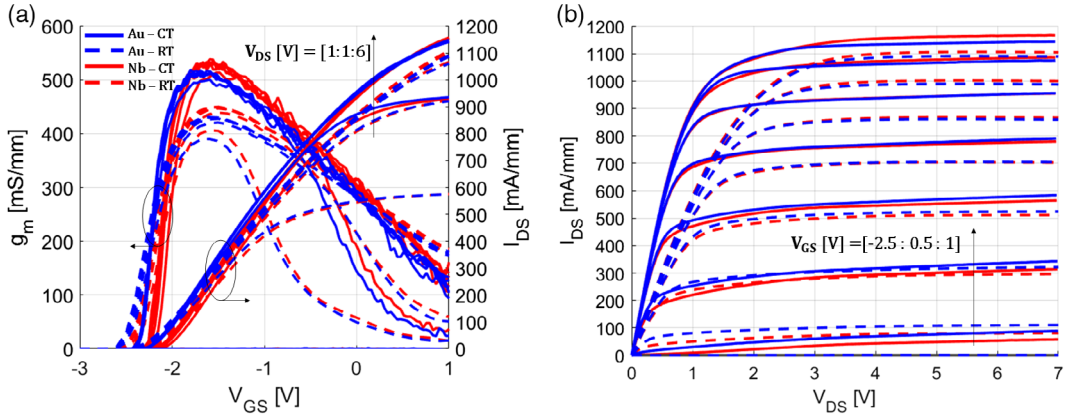

Figure 2. The DC transfer characteristics of devices with Au gate (blue) and Nb gate (red), at RT (dashed lines) and CT (continuous lines). a) Variations of the extrinsic transconductance, g_m, and the drain-to-source current, I_{DS}, with V_{GS}. b) I_{DS} (V_{DS}) curve.

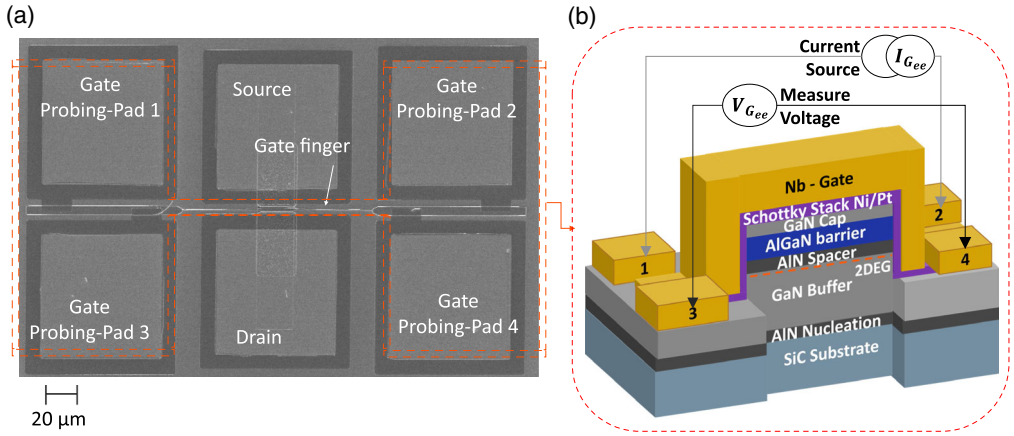

Figure 3. a) SEM picture of a device featuring 1-finger gate, incorporating 4-gate probing pads, as designed for the DC end-to-end gate resistance measurements. b) Schematic cross-section view of the gate finger, with illustration of the setup used for the end-to-end measurement of the gate resistance: a current is forced through one pair of the gate probing pads, while the second pair is used to measure the voltage drop across the gate finger.

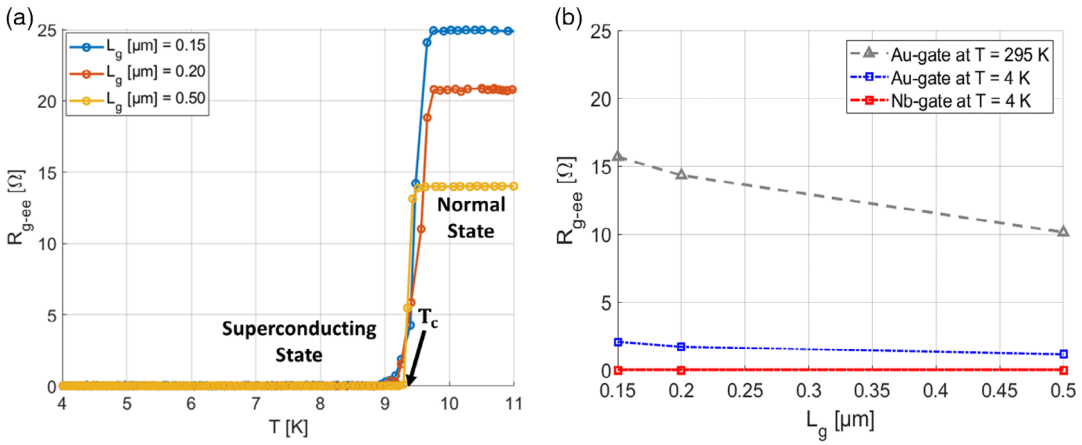

Figure 4. a) Variation of the end-to-end gate resistance of the Nb-gated device with the cryogenic temperature down to 4 K. b) Variation of the end-to-end gate resistance with L_g in the case of the Au-gated and Nb-gated devices.

superconductivity of the Nb gate, the Au gate resistance increases inversely with the gate length as expected. In addition, we note the significant reduction of the Au-gate resistivity at CT compared with RT which highlights one of the sources of the general improvements of the normal transistor's performances at low temperatures.

4.2. Small-Signal Model-Based Extraction

Following the approach in the study by Rorsman et al.[13], the equivalent model shown in **Figure 5** was used to describe the transistor at $V_{DS} = 0$ V. Prior to the extraction of the gate resistance, R_g, first, the parasitic capacitances C_{pg}, C_{pd}, and C_{pgd}, representing the pad capacitances and the coupling effect of the gate, drain, and the gate to drain, respectively, were de-embedded from the cold-FET S-parameters.[14] Then, the retrieval of R_g is best performed using the Z-representation. The gate impedance, involving the Schottky resistance, R_{sch},

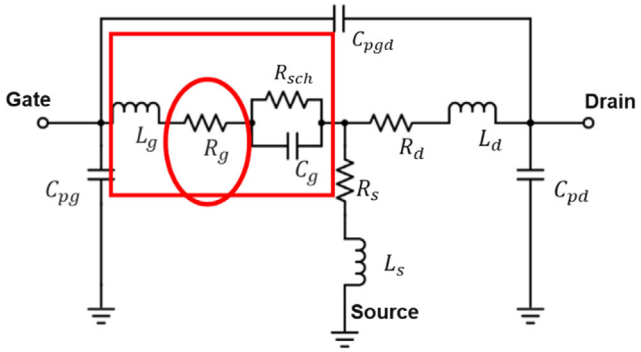

Figure 5. Equivalent model of the DUTs at $V_{DS} = 0$ V. The representations of the gate impedance and the gate resistance are highlighted.

the gate capacitance, C_g, and the gate inductance, L_g, can be described using the equation

$$Z_g(V_{GS}) = Z_{11} - Z_{12} = R_g + \frac{R_{sch}(V_{GS})}{1 + (\omega R_{sch}(V_{GS})C_g(V_{GS}))^2} + i\omega\left(L_g - \frac{C_g(V_{GS})R_{sch}^2(V_{GS})}{1 + (\omega R_{sch}(V_{GS})C_g(V_{GS}))^2}\right) \quad (2)$$

where $\omega = 2\pi F$, F is the frequency. By fitting against the Z-transform of the measured S-parameters, an iterative procedure allows to determine L_g, C_g, and R_{sch}. Subtracting these elements from the Equation (2), R_g is then equivalent to the real part of Z_g at the high-frequency limit.

In **Figure 6**, 2×25 µm devices with 0.2 µm gate length are considered, and the extracted Z_g model is compared with the measured Z_g, at the cryogenic temperature $T < T_c$. It is seen that the model succeeds to describe the measurements, in the case of both the Au-gated and Nb-gated devices, at both the considered gate bias levels. We note that at $V_{GS} = 0$ V, the Nb-gated device presents a lower gate resistance than that with the Au gate. It is, however, larger at $V_{GS} = 0.7$ V.

In order to analyze the small-signal model-based extraction of the gate resistance, the following should be considered. First, the gate resistance defines, in this case, all the resistive elements in series connection from the gate contact pad toward the active region of the device. The gate–metal resistance, about which no information was provided in the model, is one part of it and is expected to dominate it for fully nondepleted channel conditions. More importantly, with the radio-frequencies (RF) input provided from one end of the gate, the gate metal resistance should be in this case divided by a factor of 1/3 compared with that obtained from the DC end-to-measurements. This is to consider its distributed nature as detailed in the study by Razavi et al.[4]. The small-signal model-based extraction of R_g, at $V_{GS} = 0$ V, is then consistent with the DC end-to-end measurements, a lower Nb-gate resistance than that made of Au being an indication of the Nb superconductivity. This is further supported by the fact that the Nb-gate resistance would otherwise present a larger difference compared with the Au gate, as observed from the end-to-end measurement (Figure 4).

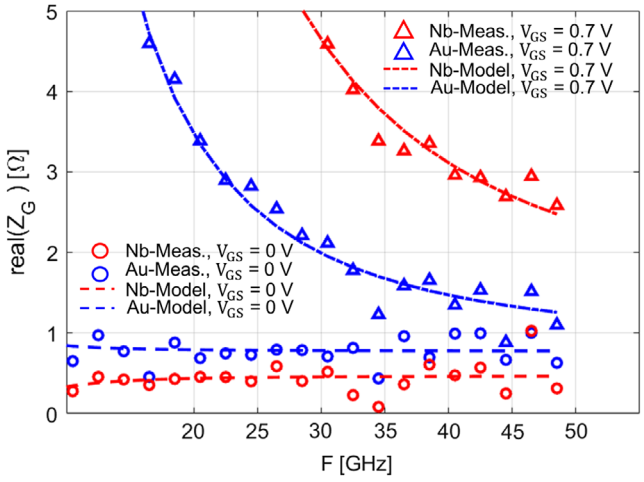

Figure 6. The frequency dependence of the measured and modeled real part of the gate impedance, at $T < T_c$, at $V_{GS} = 0$ V and $V_{GS} = 0.7$ V.

In order to study the bias dependence of the extracted R_g, we note that in the model illustrated in Figure 5 the bias dependence is initially assumed to originate from C_g and R_{sch}. Nevertheless, since no prior information on the bias dependence of the gate metal resistivity is provided to the model, no restrictions are imposed on the bias dependence of R_g. The model neglects the effect of the channel capacitance considering the full channel condition. When this condition is not fulfilled the channel resistance can be much higher than that related to the gate electrode, compromising the accuracy of the extraction of the gate resistance. Indication about reaching the full channel condition can be provided by the variation of the real part of Z_g with respect to V_{GS} which then tends to saturate after the pinch-off. Therefore, it is convenient to define a voltage window with relatively high V_{GS}. Besides, in the reverse mode of the Schottky gate, R_{sch} is large and the term associated with it in the real part of Z_g tends to vanish at sufficiently high frequency. However, R_{sch}, representing the Schottky contact resistance, becomes significantly bias dependent after the forward state is enabled by a positive gate voltage, noted V_F. This also explains the frequency dependence at $V_{GS} = 0.7\,V > V_F$ of the real part of Z_g, shown in Figure 6, in which its saturation with the frequency is shifted compared with that at $V_{GS} = 0$ V as a consequence of lower R_{sch}.

Comparing the V_{GS} dependence of the Au-gate resistance with that of Nb, presented in **Figure 7**, we observe that R_g of the Au gate remains almost constant with V_{GS}. The Nb-gate resistance has the same trend but only up to $V_{GS} = 0.5$ V. At higher V_{GS}, we note a progressive and significant increase of the Nb-gate resistance, which then correlates with the onset of the forward Schottky current. In Nb, the superconductivity can be destroyed by the current reaching a critical current density, which has a power law dependence with the physical temperature.[15] The significant increase of the Nb-gate resistance is in this case an indication of reaching the critical current level, since the Schottky current at $V_{GS} > V_F$ is relatively large, ranging from 0.003 to

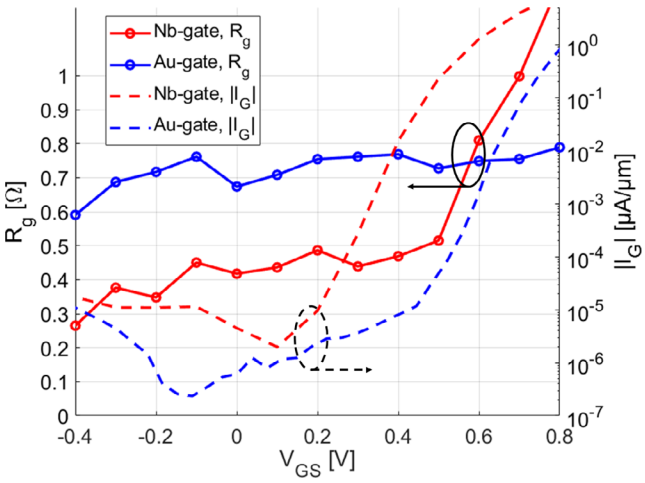

Figure 7. The gate-bias dependence of the measured and modeled gate resistance, at $V_{DS} = 0$ V and $T < T_c$, of the Au-gated and Nb-gated device. The gate current leakage variation is plotted to highlight the increase of R_g of the Nb gate, correlating with the onset of the forward Schottky conduction.

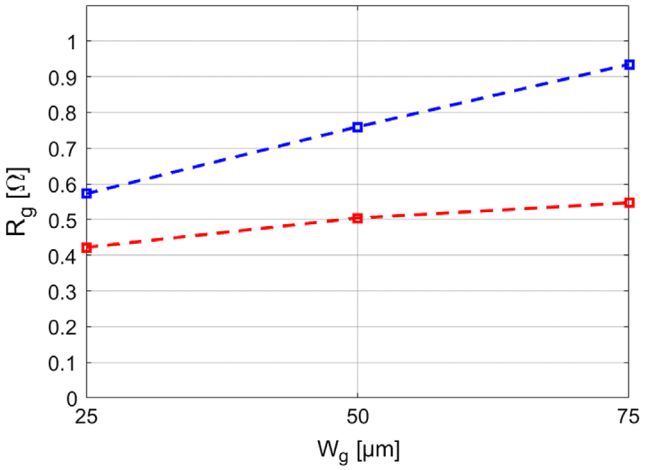

Figure 8. Variation with the unit gate width, W_g, at $T < T_c$ of the gate resistance R_g, as extracted from the small-signal model at $V_{DS} = 0$ V and $V_{GS} = 0$ V, of the devices with Nb gate (in red) and Au gate (in blue).

0.1 MA cm^{-2}. In addition, the conduction of the forward Schottky current through the intrinsic device can lead to the heating of the Nb-gate. The suppression of the superconductivity of Nb leads then to a larger increase of the Nb-gate resistance as V_{GS} increases above 0.5 V, compared with that of the Au gate.

Moreover, we extracted the gate resistances of samples with different unit gate widths, W_g, ranging from 25 to 75 μm, with the same gate length and number of gate fingers. **Figure 8** presents the gate resistances of the Au-gate and Nb-gate devices around $V_{GS} = 0$ V. The results confirm the conclusion about the effect of Nb on the gate resistance, which is found to remain constantly lower than that of the Au gate. The latter scales with the width as expected. The remaining part of the Nb gate resistance can therefore be attributed to the resistance of the contact pads.

5. The Impact on the Noise Performance

The impact of the superconducting Nb gate on the cryogenic noise performances of the GaN HEMTs was studied considering the case of the 2 × 25 μm device with a 0.2 μm gate length. For comparison, the Au-gated device with identical dimensions was also measured. The cryogenic microwave noise characterization was performed using the test setup shown in **Figure 9**.

A single 50 Ω noise measurement is used with the cold-attenuator method, as it provides good accuracy and minimizes the uncertainties in the gradient of the temperature through the passive input chain before the transistor.[16] The Agilent MXA N9020A power spectrum analyzer, with its noise measurement option, was employed. The calibration of the cryogenic setup was performed through the de-embedding of the noise contributions of the input and output chains, extracted using their respective S-parameters and the knowledge of the physical temperature at each stage.[17] Using a calibrated LNA,[18] the maximum uncertainty of the noise temperature measurements was estimated to be less than 1.5 K.

To model the minimum noise temperature which the transistor can achieve, we used the approach in the study by Pospiezalski[19], referred to as Pospiezalski's model. It relies on the equivalent circuit of the transistor as illustrated in **Figure 10**.

The effective drain noise temperature, T_d, is obtained from the noise measurements. The extracted T_d versus the power dissipation at $V_{DS} = 4$ V of both devices under test (DUTs), with Nb-gate and Au-gate, is shown in **Figure 11**. As T_d accounts for the self-heating effect of the channel, it naturally increases linearly with I_{DS}. Almost equivalent values for the same power dissipation are found for both the Au-gated and Nb-gated devices.

The variation of the minimum noise temperature with the power dissipation at $V_{DS} = 4$ V was then extracted, as presented in **Figure 12** at the frequencies ranging from 5 to 6 GHz. The

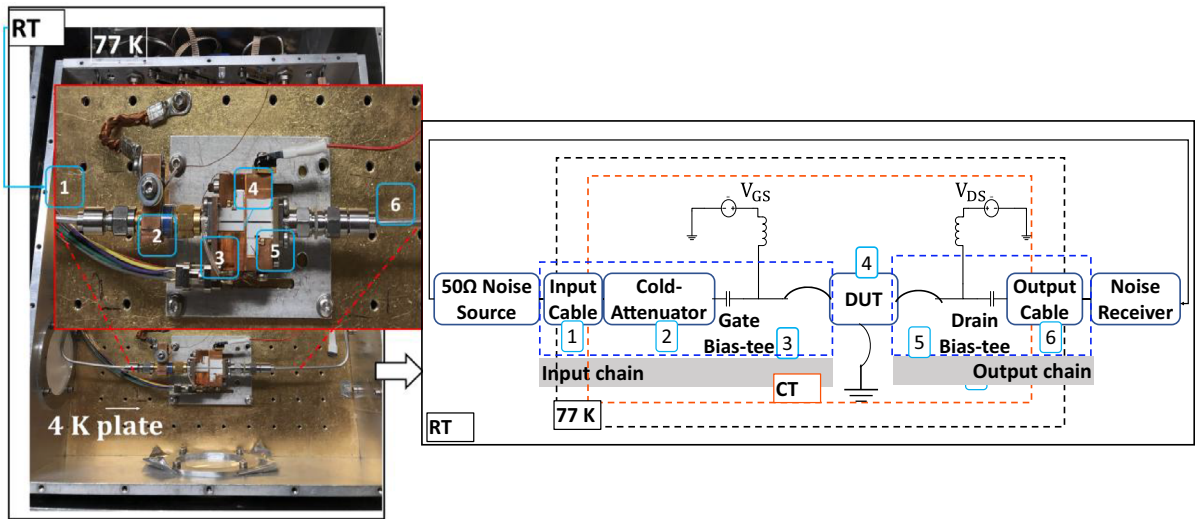

Figure 9. On the right, photo of the cryogenic test setup used for the microwave noise measurements and, on the left, its block diagram. The numbers associated with each element are presented correspondingly in the photo and the block diagram. The reference planes for the de-embedding of the noise contribution of the DUT are defined with respect to the input and output passive chains.

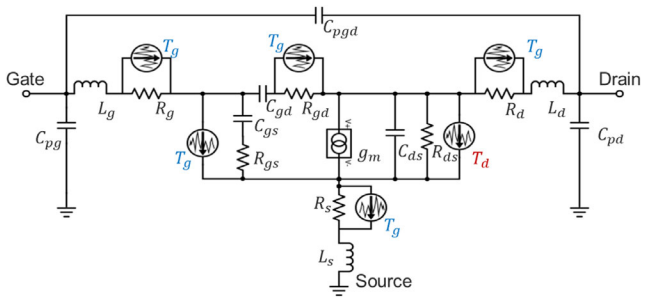

Figure 10. Equivalent small-signal model of the device at $V_{DS} > 0$ used for the cryogenic noise modeling at an ambient temperature tending to T_g.

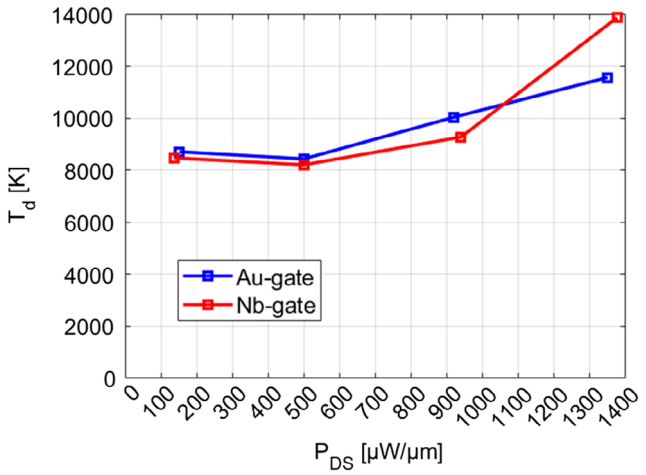

Figure 11. Variation of the fitting parameter T_d with the power dissipation in the Au-gated device (in blue) and the Nb-gated device (red).

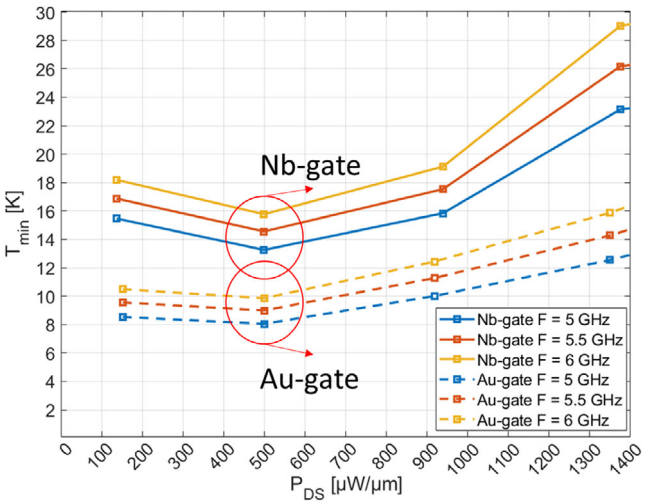

Figure 12. The extracted minimum noise temperature variation with the power dissipation from the channel, given by $P_{DS} = I_{DS}V_{DS}$, of the $2 \times 25 \times 0.2\,\mu m$ with Au-gate and Nb-gate devices at the cryogenic temperature below the critical temperature of Niobium.

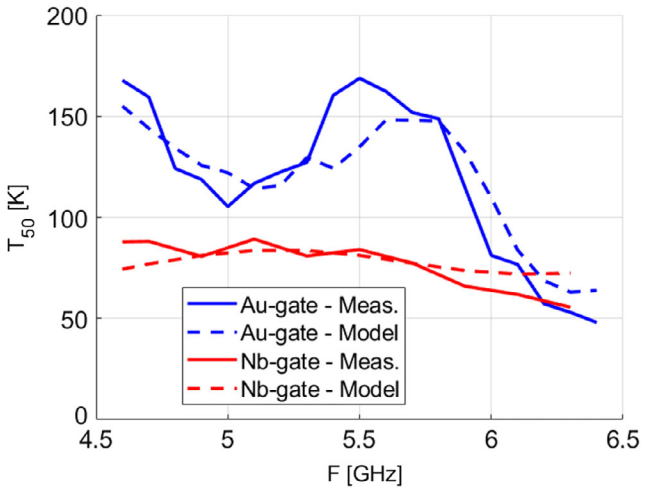

Figure 13. A comparison of the modeled (dashed lines) and the measured (solid lines) frequency dependence of the noise temperature of the DUTs at $P_{DS} = 500\,\mu m\,\mu W^{-1}$ and $V_{DS} = 4\,V$, after the de-embedding of the passive input and output chains.

minimum noise temperature is obtained with a power dissipation of $\approx 500\,\mu W\,\mu m^{-1}$. **Figure 13** shows the frequency dependence at this bias point of the measured and the modeled noise temperature of the DUTs, after the de-embedding of the passive input and output chains, denoted T_{50} [K]. A good agreement of the model with the measurements is observed. **Table 1** summarizes the small-signal model and the noise model parameters, used for the extraction of the optimum noise performances.

The Nb-gated device presents a minimum noise temperature of around 13 K at 5 GHz. This is found to have a higher minimum noise contribution compared with the Au-gated device by ≈5 K, which is estimated to be around 8 K. The minimum noise temperature of the GaN HEMTs with the Nb gate in the superconducting state was expected to improve compared to that with the Au gate, due to the suppression of the thermal noise associated with gate metallization. However, the superconductivity of the Nb gate has to be verified at the same biasing conditions as those of the low-noise operation.

Indeed, in the general formulation of the small-signal model, the resistances associated with the device's electrodes are assumed to be bias independent. This allows simplifying the extraction procedure without compromising its validity, as long as the resistivity of the electrodes follows a relatively slow variation with the physical temperature. However, as presented in Section 4, in the case of the Nb gate, the resistance shows an abrupt increase around its critical temperature. A rise of the physical temperature locally around the gate from ≈4 K up to $T_c = 9.2$ K is, in fact, likely to occur as a consequence of the self-heating resulting from the I_{DS} flow in the 2DEG channel provided that the thermal impedance of the device allows such a gradient. In order to verify this hypothesis, we carried out the end-to-end measurements while applying a drain-to-source bias to monitor the variation of the gate metal resistance with the power dissipation from the channel. The results of the device with the same dimensions as that studied in the previous section

Table 1. The parameters of the cryogenic noise model at the optimum-noise bias of the DUTs.

	R_g [Ω]	R_d [Ω]	R_s [Ω]	L_g [pH]	L_s [pH]	L_d [pH]	R_{gs} [Ω]	R_{ds} [Ω]	R_{gd} [Ω]	C_{gs} [fF]	C_{ds} [fF]	C_{gd} [fF]	g_m [fF]	T_d [K]
Au-gate	0.67	7.85	7.97	43	1	35.7	2.9	1957.3	22.6	123.4	2.08	19.6	30.7	8431.3
Nb-gate	0.42	7.68	7.84	43.3	1	39.8	7	2582.7	37.5	165	1.39	16.4	30.6	8203.3

are presented in **Figure 14**. It was found that the superconductivity of the Nb gate is broken with a channel power dissipation level of only $\approx 5\,\mu W\,\mu m^{-1}$. Implying that at the optimum-noise bias, the Nb gate has a larger resistance than that of the Au gate. The result may explain the difference in the noise performance of the device with Nb gate compared with that with the Au gate. This also demonstrates and quantifies the impact of the gate resistance on the noise performances.

6. Conclusion

We demonstrated the integration of the superconducting Nb gate with the GaN HEMTs. An ultimate reduction of gate resistance was achieved. The superconductivity of the Nb gate was experimentally verified using the end-to-end measurements in DC operation. The gate resistance in the microwave regime was extracted using a small-signal model which was validated against the measured S-parameters. The small-signal model-based extraction confirmed the advantage of the Nb gate over Au, resulting from superconductivity. The gate superconductivity was verified for several gate widths and lengths, showing that the Nb gate allows suppressing of the scaling effect of the gate resistance with the gate dimensions which are inherent to the normal metal-based gates. This implies a release in the design criteria of the systems based on the GaN HEMTs with Nb gate, as the choice of the dimensions of the device can then be adapted to the other relevant parameters for the application without affecting the gate resistance. The cryogenic DC, microwave, and noise characteristics of the GaN HEMTs with superconducting Nb gate were extracted and studied. The overall improvement of the devices' performances after cooling confirms the potential of the GaN technology for low-noise cryogenic performance. The comparison of the noise performances with the Au-gated device indicated that at the optimum-noise bias, the Nb-gated device has a larger noise contribution associated with the gate. The effect is due to the increase of the local temperature around the gate, leading to the suppression of its superconductivity and the corresponding increase of its resistance. The normal-state transition of the Nb gate before the optimum-noise bias was verified experimentally, attributing the effect to the self-heating resulting from the channel power dissipation. The results suggest that further optimization of the device is required in order to enable the full potential of the GaN HEMTs with the Nb gate by maintaining its superconductivity at low-noise operation conditions.

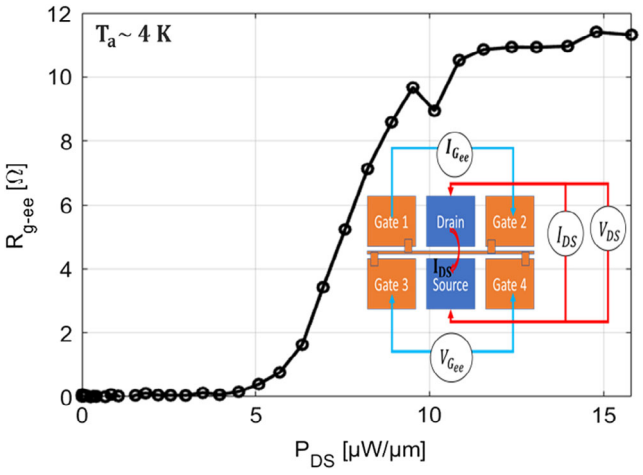

Figure 14. Variation of the end-to-end gate resistance of the Nb gate with the channel power dissipation, at an ambient temperature T_a of ≈4 K. The inset shows a schematic representation of the test structure with the four-point configuration, used to measure the end-to-end gate resistance while varying the drain-to-source bias.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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cryogenic high-electron-mobility transistors, GaN, Nb

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