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RF PA Predistortion using Non-Linear RF-DACs

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***Abstract*—Traditionally, analog and/or digital predistortion is used to linearize power amplifiers (PAs), at the cost additional hardware. We here present a novel linearizion method using segmented non-linear RF-DACs to linearize PAs at no additional hardware cost. Through the DAC bias, we are able to control the expanding non-linearity, bringing a large flexibility. Through simulations, we have demonstrated the robustness and flexibility with this approach, achieving excellent overall linearity over a large range of DAC and PA bias conditions.**

***Index Terms*—Linearization, Non-linear scaling, Power amplifier (PA), Predistortion, RF-DAC.**

I. Introduction

Wireless networks increasingly use millimeter wave (mmW) frequencies, where broad and continuous spectrum is available. The 5G mmW-bands for example are often around 3 GHz wide [1]. Also, spectrum-efficient modulation schemes require highly linear transmitters. With massive multiple-input-multiple-output (mMIMO), a large number of antennas and transmitters are densely combined, particularly at mmW, resulting in strict energy and thermal budgets [2].

To fulfil the linearity requirements, either the power amplifiers (PAs) need to operate at significant power back-off, or a predistorter is required to compensate for the non-linear PA characteristic. Traditionally, analog predistortion (APD) or digital predistortion (DPD) are used to generate the expanding function needed to linearize the PA [3]. In APDs, diodes are most commonly used to either compensate signal-dependent bias-variations [4], or in combination with couplers to form reflective RF linearization [5], [6]. APDs based on transistors operating in cold-mode have also been shown [7]. APDs often present a significant loss in addition to their large footprint [5]. With DPDs, the linearization is performed in the digital domain, before the modulator, thus allowing for linearization of the entire transmitter. Although digital processing is highly flexible, computations need to be performed at the full modulator sample rate, *i.e.*, several times larger than the signal bandwidth [3], potentially reaching beyond 10 GS/s [8]. Parallel implementations are possible, but the computational cost is at best the same [2]. Hybrid linearization approaches have also been presented as a way to reduce the DPD complexity by performing coarse linearization in the analog domain [9]–[11]. Although simpler APD and DPD circuits can be used, this approach requires both additional analog hardware and digital computations at the full sample rate.

RF-DAC-based modulators are a competitive alternative for realizing wideband modulation and up-conversion in a single component. Segmented non-linear RF-DACs have been demonstrated to linearize the compression effects in RF-DACs both in the low gigahertz range [12] and for a complete Cartesian IQ-modulator at mmW frequencies [8].

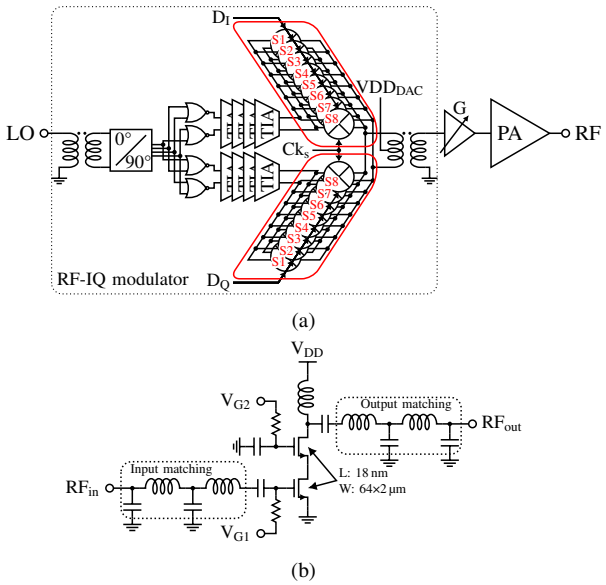


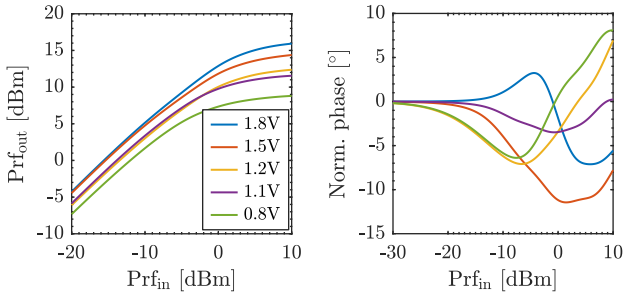
Fig. 1. (a) A schematic showing the transmitter concept used as base for the evaluation. (b) A schematic of the stacked PA used to evaluate the linearization.

In this work, we present a novel linearization approach that utilizes the non-linear scaling concept to linearize not only the RF-DACs themselves, but also a PA driven by the DACs. With a tunable DAC characteristic, excellent overall linearization can be achieved over a large range of DAC and PA bias conditions. Based on simulations, we also show that neither additional hardware, nor additional computations are needed for this linearization to work. The approach is therefore highly attractive in wideband mMIMO applications.

II. System illustration

An illustration of the targeted transmitter topology is shown in Fig. 1a. Non-overlapping quadrature LO signals are generated and fed to the two segmented non-linear RF-DACs, followed by a gain stage and finally the PA. The gain stage G is introduced to model PAs with similar non-linear characteristics but different input power requirements. In an actual implementation, this gain stage may be omitted.

A PA prototype, designed for 18–30 GHz in 22 nm FDSOI CMOS, is employed to verify the proposed linearization concept. A schematic of the PA is shown in Fig. 1b. The PA



(a) (b)

Fig. 2. (a) PA output power, and (b) PA normalized output phase, plotted versus PA input power at various PA supply voltages, for the example PA shown in Fig. 1b.

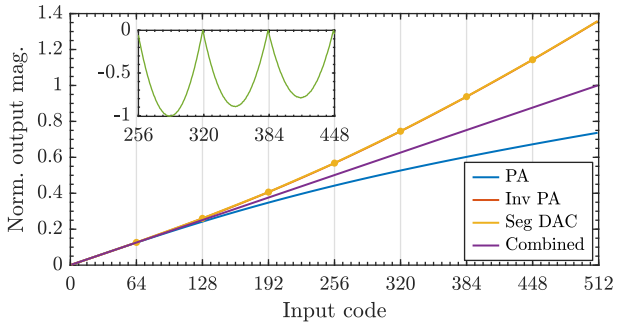


Fig. 3. The PA characteristic, its inverse, the segmented DAC scaling, and the output resulting from combining the segmented DAC with the PA, plotted versus DAC input code. The inset shows the error between the segmented scaling and the inverse of the PA characteristic in LSB.

uses a stacked configuration to achieve higher output power. The NMOS transistors have 64 fingers, with a gate length and width of 18 nm and 2 µm, respectively. The PA is biased in class-AB mode, with a gate bias of 300 mV and a nominal V_{DD} of 1.8 V. The AM/AM and AM/PM characteristics are shown relative to the input power in Fig. 2 for various supply voltages. The nominal bias voltage (V_{G2}) for the top transistor is 1.45 V, but is reduced to 1 V for supply voltages <1.2 V.

III. Linearization

To linearize a non-linear circuit, such as a PA, the driving circuit must provide an inverse of the non-linearity. In contrast to the APD and DPD approaches, a segmented expanding non-linear DAC is used here. As a starting point, the segment scaling is chosen to generate an approximated inverse of the PA's AM/AM response. In Fig. 3, the PA characteristic is plotted versus DAC input code. The inverse PA characteristic is then used to compute the segmented scaling, here with 8 segments. As the DAC also will experience some compression, iterative improvements will be required to find a scaling that inverts the combined DAC and PA compression.

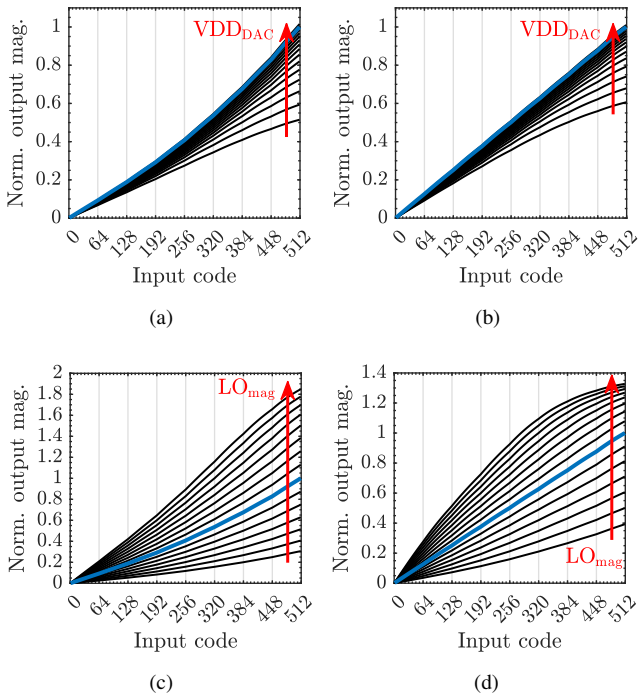
Compression in the DAC itself depends on the DAC bias settings, *i.e.*, the supply voltage and LO magnitude. Through changing these settings, we can control the DAC compression, thus counteract the expanding non-linear scaling. Fig. 4 shows the output magnitude normalized to the design point (the blue curve) versus input code for both the DAC and the combined DAC and PA. The effect of an increased DAC supply voltage is shown in Figs. 4a and 4b and the effect of an increased LO magnitude is shown in Figs. 4c and 4d. While the DAC in almost all cases provides an expanding non-linear output, the combined output shows both expanding and compressing behaviour, demonstrating the tuning capabilities. The DAC AM/PM characteristic changes little with bias settings so cannot be tuned much in this way.

A DPD may require a higher DAC resolution in addition to the high computational effort. This is since digitally expanding a quantized signal before compressing it in the analog domain results in a higher code density for the upper range, at the cost of a reduced code density in the lower range. In contrast, the segmented expanding non-linear DAC combined with a non-linear PA provides a uniform code density throughout the entire range.

For the evaluation, we have used an RF-DAC with 8 segments and a size ratio of 2.685 between the largest and smallest segments. Relative to a uniform DAC, with the same minimum unit cell, this scaling increases the total DAC transistor width by 62 %. This is however the only change in hardware cost brought by this linearization method.

IV. Evaluation

The proposed linearization concept was evaluated through individual circuit simulations of the key components. The



(a) (b) (c) (d)

Fig. 4. Normalized output magnitude (a) for DAC versus supply voltage, (b) for DAC combined with PA versus supply voltage, (c) for DAC versus LO magnitude, and (d) for DAC combined with PA versus LO magnitude. The curves are normalized relative to the design point, the blue curve.

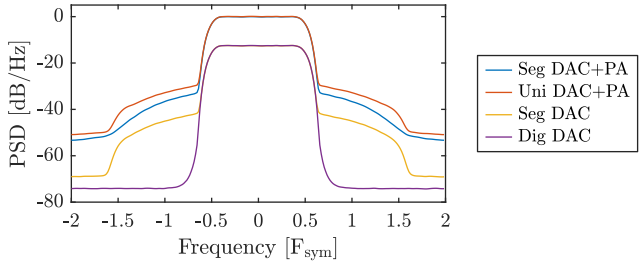


Fig. 5. PA output spectra when driven by a segmented and by a uniform DAC at the same average output power, and spectra for digital DAC input and segmented DAC output. Performance metrics for the uniform and segmented DAC are presented in Table I.

PA was simulated at its center frequency. The results were used in high-level simulations of the combined circuit. With non-overlapping LO signals, I/Q cross-modulation distortion can be kept very small [8], making it possible to simulate the RF-DACs individually. The quadrature LO signals were generated by ideal voltage sources, representing the non-overlapping pulses up to the third harmonic. All simulations used 8-segment 10 bit signed RF-DACs. For modulated signals, two such DACs were combined to form a Cartesian IQ-modulator. We used 256QAM single carrier signals, up-sampled 4 times using an RRC-filter with factor 0.2. As simulations are based on the dominating quasi-static behaviour, the signal bandwidth has no effect.

A. Linearization at nominal bias condition

The nominal bias settings used to derive the DAC scaling were chosen to be an LO magnitude of 250 $mV_{pk\text{-}pk}$ and a DAC supply voltage of 0.9 V. Fig. 5 shows output signal spectra when driving the PA (V_{DD} =1.8 V), at equal output powers with segmented and with uniform DACs. Spectra for the digital input and the output of the segmented DAC are also shown. The segmented-DAC output shows bandwidth expansion due to the non-linearity; yet, out-of-band emissions after the PA are clearly reduced when using the segmented DAC.

Table I presents the improved EVM and ACPR achieved when using the segmented scaling. With the uniform DAC, the reduced PA compression is a result of higher code density for the upper range, resulting in a reduced peak-to-average power ratio. The segmented DAC provides a uniform code-to-magnitude spacing across the range.

B. Linearization across DAC bias settings

Based on Fig. 4, it is clear that when changing the supply voltage or the LO magnitude, we can tune the non-linear characteristics of the segmented DAC. The static RMS linearity and maximum phase change for the combined DAC and PA are shown in Figs. 6a and 6b for various combinations of LO magnitude and supply voltage. The nominal design point is marked with a white dot. The red overlaid contours show the PA compression, calculated as the small-signal gain minus the gain achieved using the highest DAC code. As the DAC output power depends on the bias conditions, we can achieve good linearization across different compression levels, allowing us to control the PA output power. The performance was also evaluated using modulated signals to analyse the influence of magnitude and phase non-linearities. EVM and ACPR is shown in Figs. 6c and 6d. With the two DACs used for modulated signals, a slightly higher output power is achieved compared to the static case, resulting in a slightly shifted optimum. The modulated-signal optimum is more shallow than in the static case, so the linearization technique does not rely on fine-grained DAC bias control. Because of the narrower optimum observed in the static case, the following subsections will focus on the static linearity.

TABLE I
MODULATED-SIGNAL PERFORMANCE AT EQUAL PA OUTPUT POWER.

	Uni DAC	Seg DAC
EVM [%]	3.71	2.69
ACPR [dBc]	−34.4	−38.1
Peak PA compression [dB]	2.5	3

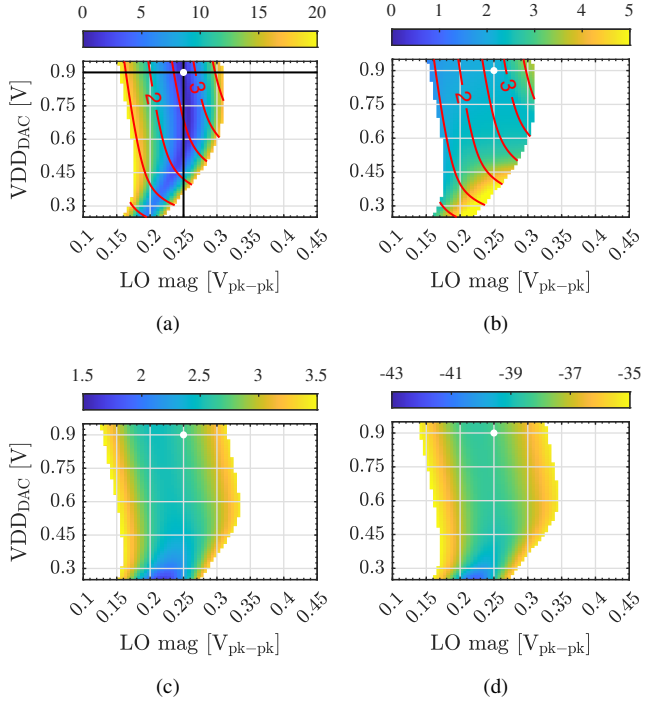


Fig. 6. Static performance ((a) RMS linearity [LSB], and (b) maximum phase variation [°]) and modulated performance ((c) EVM [%], and (d) ACPR [dBc]) versus supply voltage and LO magnitude. Red contours indicate PA compression in dB. White dot highlights the nominal design point. The black lines in (a) connects to the AM/AM characteristics presented in Fig. 4.

C. Linearization across DAC output power

So far, we have presented results for when the DAC output power has been designed for the PA input requirements, and for adjusting the DAC supply voltage. To further demonstrate the flexibility with this linearization approach, we now adjust the gain parameter (G) by ±5 dB, changing the PA's input power requirement. The static performance is shown in Fig. 7.

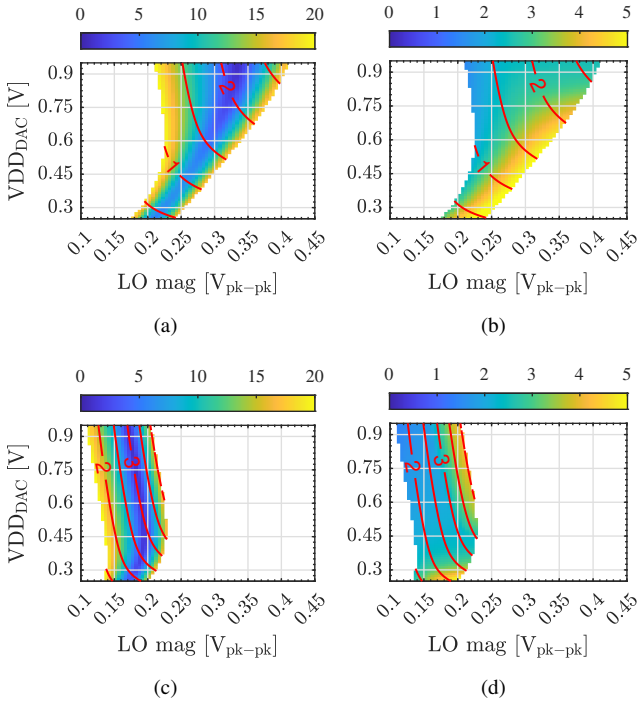


Fig. 7. Comparison of static performance at different gain settings. (a) RMS linearity [LSB] and (b) maximum phase variation [°] for a gain of −5 dB. (c) RMS linearity [LSB] and (d) maximum phase variation [°] for a gain of 5 dB. Contours in red show PA compression in dB.

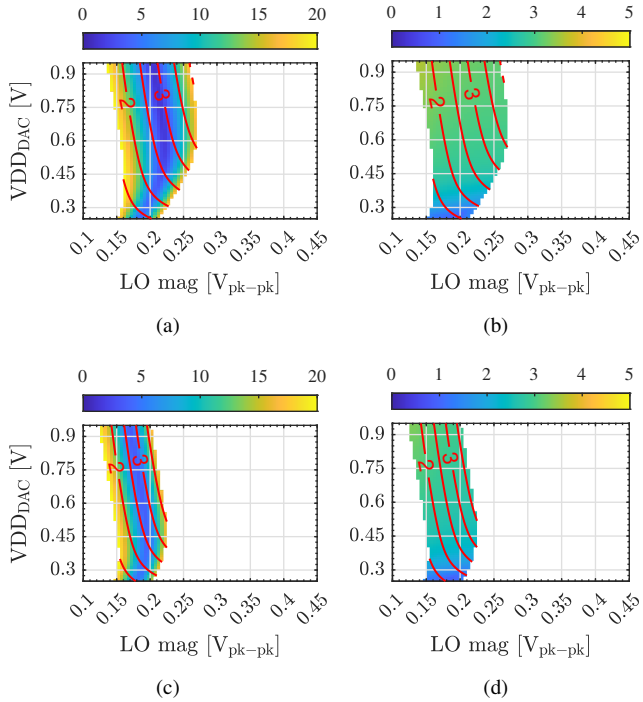


Fig. 8. Comparison of static performance at different PA supply voltage settings. (a) RMS linearity [LSB] and (b) maximum phase variation [°] for a 1.2 V PA supply voltage. (c) RMS linearity [LSB] and (d) maximum phase variation [°] for a PA supply voltage of 0.8 V. Contours in red show PA compression in dB.

With a reduced gain, a larger DAC output power is required; thus, the optimum is shifted toward larger LO magnitudes, as seen in Figs. 7a and 7b. Correspondingly, with an increased gain, a lower DAC output power is required, shifting the optimum towards using lower LO magnitudes, as shown in Figs. 7c and 7d. Since the nominal DAC compression contribution depends on the LO magnitude, the amount of PA compression that can be compensated for also varies.

D. Linearization at different PA bias conditions

Changes in PA output power have so far resulted only from changing the DAC operating point. For efficient PA operation also at reduced peak output power, it is desirable to reduce PA supply voltage, which however changes the PA's characteristics as seen in Fig. 2. Fig. 8 show the static performance for PA supply voltages of 1.2 V and 0.8 V. Since a reduced PA supply voltage results in sightly increased compression for a given input level, it is expected that optimum linearization is achieved at reduced LO magnitudes. We can here also observe that the changed non-linear PA characteristic does not have a significant impact on the achieved linearization.

Reducing the PA supply voltage to 0.8 V results in a 5.3 dB output power reduction when a constant input power is provided. When also accounting for the changes in DAC output power resulting from adapting the linearization, a 7.1 dB peak power back-off can be achieved while keeping the DAC supply voltage at 0.9 V. As the DAC supply voltage also can be reduced, an even larger back-off range can be achieved.

Throughout our evaluation, we have observed a similar relationship between the static and modulated performance as shown in Fig. 6 also for the other cases; but figures are omitted for space reasons.

V. Conclusion

In this paper, we present a novel linearization concept that is capable of linearizing PAs at no additional hardware cost, neither in the analog domain nor in the digital domain. Through simulations, we have demonstrated excellent linearization over a large range of bias conditions, both for the RF-DACs and for the PA, thus, showing the robustness and flexibility of this approach. Although modulated performance has been evaluated using a Cartesian IQ-modulator, the principles can also be applied on a system using a polar IQ-modulator. In addition, the concept also relaxes the requirement for the modulator resolution as no additional resolution is needed for the DPD.

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