Investigation of Isolation Approaches and the Stoichiometry of SiN<inf>x</inf> Passivation Layers in “Buffer-Free” AlGaN/GaN

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Investigation of Isolation Approaches and the Stoichiometry of SiN_x Passivation Layers in "Buffer-Free" AlGaN/GaN Metal–Insulator–Semiconductor High-Electron-Mobility Transistors

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Critical process modules for the fabrication of metal–insulator–semiconductor high-electron-mobility transistors (MISHEMTs) based on a novel 'buffer-free' AlGaN/GaN heterostructure grown with metal–organic chemical vapor deposition (MOCVD) are presented. The methods of isolation and passivation for this type of heterostructure are investigated. Utilizing nitrogen implantation, it is possible to achieve off-state destructive breakdown voltages (BVs) of 2496 V for gate–drain distances up to 25 µm, whereas mesa isolation techniques limit the BV below 1284 V. The stoichiometry of the SiN_x passivation layer displays a small impact on the static and dynamic on-resistance. However, MISHEMTs with Si-rich passivation show off-state gate currents in the range of 1–100 µA mm^{-1} at voltages above 1000 V, which is reduced below 10 nA mm^{-1} using a stoichiometric SiN_x passivation layer. Destructive BVs of 1532 and 1742 V can be achieved using gate-integrated and source-connected field plates for MIHEMTs with stoichiometric and Si–rich passivation layers, respectively. By decreasing the field plate lengths, it is possible to achieve BVs of 2200 V. This demonstrates the implementation of MISHEMTs with high-voltage operation and low leakage currents on a novel "buffer-free" heterostructure by optimizing the SiN_x stoichiometry.

1. Introduction

The GaN-based high-electron-mobility transistor (HEMT) is considered a potential candidate for future power electronic switching devices due to its high breakdown field and good electron transport properties.[1] GaN-based heterostructures are typically grown on Si due to the low manufacturing cost of Si wafers. This necessitates the growth of strain relaxation layers and a thick (Al)GaN buffer layer to reduce the number of extended defects as a result of the large lattice mismatch between GaN and Si.[2,3] Unintentionally doped (UID) GaN is typically rendered lightly n-doped due to the incorporation of oxygen atoms or nitrogen vacancies during metal–organic chemical vapor deposition (MOCVD) growth.[4,5] This can lead to high vertical off-state currents in GaN-on-Si HEMTs, which limit the breakdown voltage (BV). Carbon is typically introduced into the thick buffer layer to reduce these off-state leakage currents. The carbon atoms in the nitrogen site (C_N) act as a deep acceptor level in GaN,[6] which can compensate the unintentional donors and therefore increase the resistivity. However, introducing high carbon concentrations in the buffer layer has also been associated with dynamic on-resistance ($R_{on,dyn}$) dispersion.[7,8]

Previously, we have presented a heterostructure that can avoid carbon-related trapping effects in the GaN layers and, therefore, potentially reduce $R_{on,dyn}$.[9] In this heterostructure, no highly doped buffer layer is used. Instead, a 265 nm UID GaN layer is grown between a thin AlGaN barrier layer and an AlN nucleation layer. Furthermore, the AlGaN/GaN/AlN heterostructure is grown on a semi-insulating SiC substrate, providing good vertical isolation. Although the cost of semi-insulating SiC substrates is high relative to Si substrates, the advantages of using the buffer-free heterostructure on SiC include improved lattice mismatch between GaN and the substrate, reduced epitaxial growth time, higher thermal conductivity and a lower thermal resistance between the active region and the substrate (due to a thinner GaN layer). Moreover, technological improvements in SiC substrate growth have rapidly increased due to increasing demands for SiC-based power electronic diodes and transistors, which have led to a reduced cost for SiC substrates. Therefore, GaN-on-SiC HEMTs could become an alternative to GaN-on-Si HEMTs in future power electronic switching devices. Power electronic GaN–on–SiC HEMTs can also be cointegrated with

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microwave electronics. In such applications, semi-insulating SiC substrates may be more advantageous due to their superior thermal and insulating properties. However, to realize high-voltage operation with low $R_{on,dyn}$ on this new material, both the passivation layer and the isolation of the active areas have to be optimized. In this article, we investigate different isolation approaches and the effect of different stoichiometries in the SiN_x passivation layer.

Besides buffer-related trapping effects, surface states have been shown to cause current collapse and $R_{on,dyn}$ dispersion in GaN HEMTs,[10] resulting in increased on-state losses. Surface-related trapping effects can be mitigated through proper surface treatments and the deposition of a passivation layer.[10] SiN_x, deposited with either plasma-enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD), is commonly used as a passivation layer. The SiN_x passivation layer provides a positive charge to the (Al)GaN surface that neutralizes the negative polarization surface charge.[11] In addition, LPCVD SiN_x provides a high interface quality and reduced oxygen content at the SiN_x/(Al)GaN interface, making it the preferred choice for GaN–based HEMTs.[12] Stoichiometric SiN_x (Si_3N_4), as opposed to Si-rich SiN_x, improves the isolation and suppresses off-state gate leakage currents.[13] However, it has been suggested that GaN HEMTs with carbon-doped buffer layers are susceptible to greater $R_{on,dyn}$ dispersion when depositing stoichiometric SiN_x passivation layers.[13,14] This is caused by a change in the conductivity in the GaN epi due to the diffusion of hydrogen ions through the GaN epi during the deposition of the SiN_x passivation layer.[15] Therefore, highly insulating passivation layers could potentially be used without compromising $R_{on,dyn}$ in the "buffer-free" heterostructure without carbon doping. Here, AlGaN/GaN metal–insulator–semiconductor HEMTs (MISHEMTs) with Si-rich and stoichiometric SiN_x passivation layers were fabricated on the "buffer-free" heterostructure, and their on-state and off-state characteristics were compared. The devices were characterized in terms of DC, pulsed *I–V*, and off-state BV.

In addition, a proper isolation technique must be implemented to further increase the off-state BV and prevent high lateral off-state leakage. High resistivity has been achieved for GaN with implantation of N,[16,17] He,[16] Ar,[18] or Kr[18] or by dry etching with Cl-based plasma to form a mesa. Although mesa isolation techniques are more straightforward, implantation isolation has proven to be the best choice to increase off-state BVs in GaN HEMTs with buffer layers. However, a study comparing implantation and mesa isolation in this new heterostructure has not yet been conducted. The potential benefit of having a thin GaN layer grown directly on the nucleation layer is the ability to easily dry etch (when using mesa isolation) or implant down to the semi-insulating SiC substrate.

To test the high-voltage properties of this heterostructure, we investigate the impact of N implantation isolation and mesa isolation on the off-state BV and leakage currents in MISHEMTs fabricated on the "buffer-free" heterostructure.

2. Epitaxial Design and Device Fabrication

The epitaxial heterostructure grown on a high-purity semi-insulating SiC substrate in this study consists of four layers (from the bottom to the top): a 43 nm AlN nucleation layer, a 265 nm UID GaN layer, an 18.5 nm $Al_{0.22}Ga_{0.78}N$, and a 2.5 nm GaN cap (**Figure 1**a). The heterostructure, termed QuanFINE, was grown by SweGaN AB using MOCVD. The dislocation density in the UID GaN layer is in the low $10^8\,cm^{-2}$, and the carbon concentration is $\sim 3 \times 10^{16}\,cm^{-3}$. Further details on the epitaxial growth and crystal quality have been presented by Lu et al. and Chen et al.[19,20]

The device fabrication started with the deposition of a SiN_x passivation layer using LPCVD with dichlorosilane (H_2SiCl_2) and ammonia (NH_3) as Si and N precursors, respectively. Two different passivation layers were deposited: a 101 nm layer using a H_2SiCl_2/NH_3 flow ratio of 98/360 (Sample A) and a 176 nm layer using a H_2SiCl_2/NH_3 flow ratio of 224/23 (Sample B). The chamber pressure was set to 250 mTorr for both Sample A and B, while the deposition temperature for Sample A and B was 770 and 820 °C, respectively. A J.A. Woollam RC2 ellipsometer was used to estimate the thicknesses and refractive indices of the two layers. Refractive indices of 2.02 (2.00) and 2.40 (2.34) were extracted at a wavelength of 633 nm (830 nm) for Sample A and B, respectively. The Si content in the SiN_x layers was estimated using the relationship given by Dehan et al.,[21] where the N/Si ratio can be calculated using the refractive indices of the layers at 830 nm. The high refractive index in the SiN_x of Sample B indicates N/Si ratio of ~1.02, while a refractive index of 2.00 (Sample A) results in N/Si ratio of 1.36. In this work, the SiN_x on Sample A is referred to as "stoichiometric SiN_x", or "Si_3N_4," as the N/Si ratio is close to 4/3, while the SiN_x on Sample B is referred to as "Si-rich SiN_x."

A 40–43 nm LPCVD stoichiometric SiN_x gate dielectric was deposited using the same deposition parameters as Sample A, after forming a gate recess etch into the passivation layer. The gate recess forms the gate length (L_g), which was 2 and 4 μm for Sample A and Sample B, respectively. The ohmic contacts consisted of a 15/280/20 nm Ta/Al/Ta stack,[22,23] which resulted in average contact resistances of 0.44 Ω mm for Sample A and 0.75 Ω mm for Sample B. A 600 nm PECVD SiO_x second dielectric was deposited following the ohmic contact formation. The gate–source distance (L_{gs}), gate–drain distance (L_{gd}), and device width (W_g) were 2, 5–40, and 100–200 μm, respectively. The gate-integrated field plate lengths (L_{gfp}) were 0.75 μm toward the source and 4 μm toward the drain. The source-integrated field plate length (L_{sfp}) was 0 or 5 μm (as measured from the edge of the gate field plate). A top-view microscope image of a typical fabricated MISHEMT is shown in Figure 1b. In addition to the to MISHEMTs, a dielectric leakage test structure[24] was fabricated on Samples A and B. A schematic and microscope image of the test structure can be seen in Figure 1c,d, respectively.

Two techniques were used to isolate the material surrounding the active areas: nitrogen implantation and mesa isolation etched to the SiC substrate. For the sample with nitrogen implantation isolation, three implantation energies were used: 30, 100, and 180 keV with implantation doses of 5×10^{12}, 10^{13}, and $1.8 \times 10^{13}\,cm^{-2}$, respectively.

The stopping and range of ions in matter (SRIM) program was used to simulate the three nitrogen implantation profiles (**Figure 2**a) and the resulting vacancy concentration profiles (Figure 2b). The mesa isolation was formed with a dry etch using Cl_2/Ar gas chemistry with a 100 W reactive-ion etch power and a 50 W inductively coupled plasma power in an Oxford Plasmalab

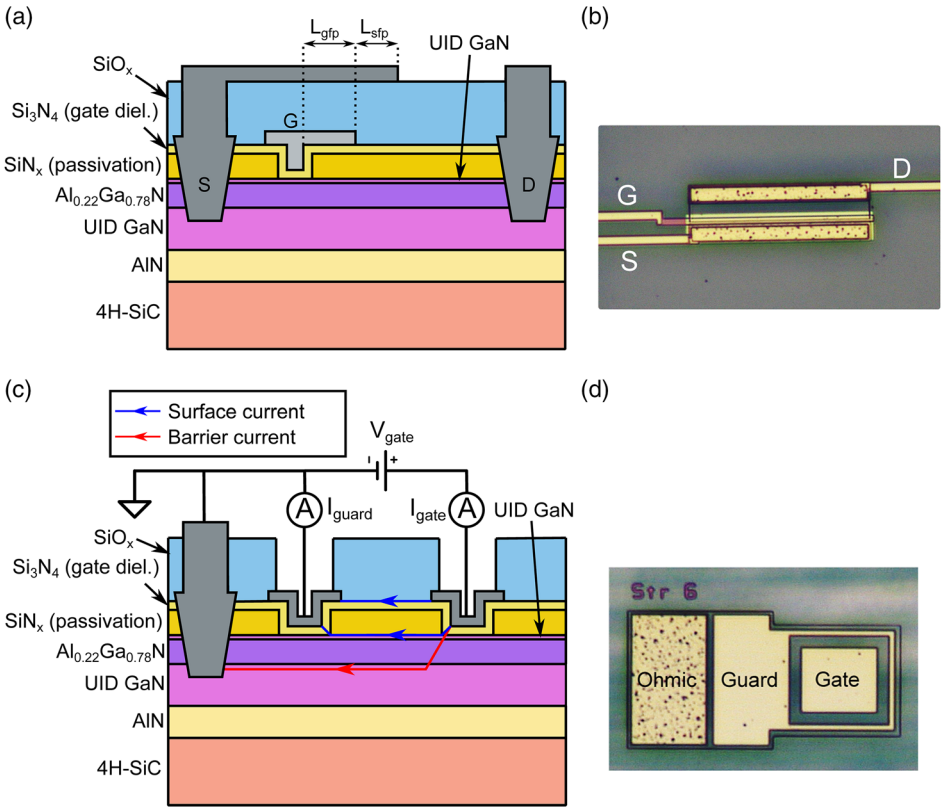

Figure 1. a) Schematic and b) microscope image of a MISHEMT fabricated on a "buffer–free" heterostructure. c) Schematic and d) microscope image of a dielectric leakage test structure.

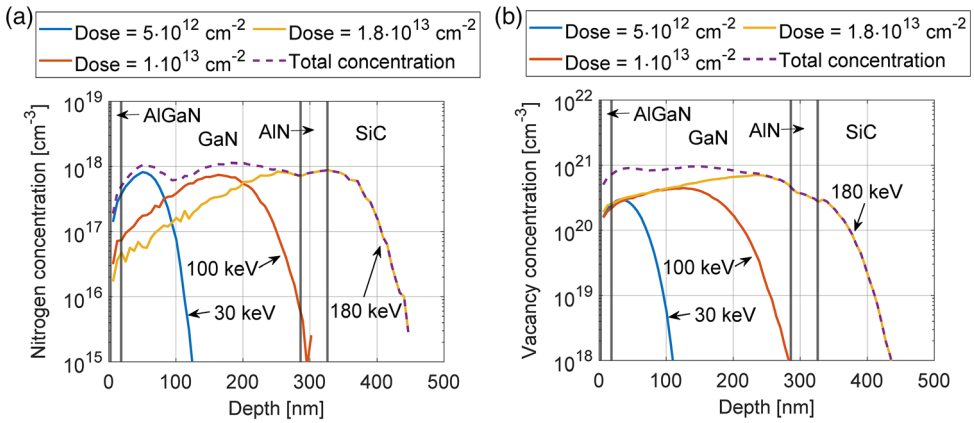

Figure 2. Simulated a) nitrogen and b) total vacancy concentration in a "buffer-free" heterostructure after nitrogen implantation.

100 system. The resulting mesa step height was measured to 400 nm using a step profilometer. In both of these samples, a Si-rich SiN_x passivation layer was used.

3. Results

3.1. Impact of Isolation Techniques

Off-state BVs were measured on MISHEMTs with nitrogen implantation and mesa isolation around the active device areas using a Keysight B1505A Parameter Analyzer. The effect of nitrogen implantation on the off-state breakdown voltage is evident in **Figure 3**a, where destructive breakdown voltages of 1480–2496 V could be achieved for MISHEMTs on Sample B with $L_{gd} = 12$–25 µm, $L_{gfp} = 0.75$ µm, and $L_{sfp} = 0$ µm. This can be contrasted with mesa isolation, where the breakdown voltage was limited to 1284 V up to $L_{gd} = 25$ µm.

The breakdown electric fields, as calculated by BV/L_{gd}, are 98–123 and 51–85 V µm^{-1} for implantation and mesa isolation, respectively. The MISHEMTs with nitrogen implantation

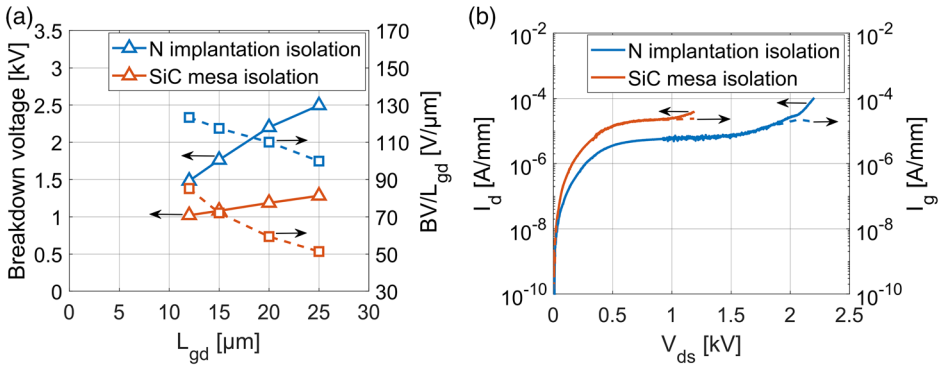

Figure 3. a) Destructive breakdown voltages of short field plate MISHEMTs with a Si-rich SiN_x passivation layer with gate–drain distances of 12–25 μm. b) Off-state breakdown characteristics of a short field plate MISHEMT with Si-rich SiN_x passivation layer and $L_{gd} = 20$ μm.

Table 1. Breakdown voltage comparison with GaN-based HEMTs found in the literature with the 1 mA mm^{-1} breakdown current criterion.

References	Substrate	BV [V]	L_{gd} [μm]	BV/L_{gd} [V μm^{-1}]
This work	SiC	1480	12	123
This work	SiC	1762	15	117
[17]	Si	1800	10	180
[25]	Si	1590	15	106
[26]	Si	1900	15	127
[27]	SiC	3000	30	100
[28]	Si	1230	15	82

isolation display breakdown fields which are comparable with GaN-based HEMTs with Si and SiC substrates in the literature, where values in the range of 82–180 V μm^{-1} have been demonstrated (**Table 1**).[17,25–28] Although GaN-on-Si HEMTs with carbon-doped buffers layers show vertical breakdown fields above 200 V μm^{-1},[3] the buffer layer can limit the off-state breakdown voltage. Therefore, increasingly thicker buffer layers are required to target higher breakdown voltages. However, in the "buffer-free" heterostructure, the vertical breakdown in the SiC substrate is not primarily limiting the breakdown voltage.[9] The reduced breakdown for the mesa–isolated MISHEMTs is likely caused by surface states induced by the dry etch used to form the mesa or by a high electric field peak in the SiC trench.

Regardless of the isolation technique, there is a predominant drain–gate leakage current in the range of 1–100 μA mm^{-1} above 1000 V (Figure 3b), despite having a highly insulating stoichiometric SiN_x gate dielectric.

The HEMTs with implantation isolation display leakage currents lower by a factor of 4 at 1000 V compared with HEMTs with SiC mesa isolation. The high leakage current and reduced breakdown voltage caused by Cl_2/Ar plasma etching can be reduced using postetch treatments using tetramethylammonium hydroxide (TMAH).[29] However, the extent to which this can reduce the large breakdown voltage difference between "buffer-free" HEMTs with nitrogen implantation and mesa isolation techniques (Figure 3a) was not studied in this work.

Even though a small difference in off-state leakage can be observed between the two isolation techniques, both show high currents in the μA mm^{-1} range. This indicates that the high leakage is primarily caused by the Si-rich passivation, gate dielectric, or both (see Section 3.1). Therefore, the stoichiometry of the SiN_x dielectric(s) has to be tuned to improve the electrical isolation to suppress current levels below 1 μA mm^{-1} in the off state.

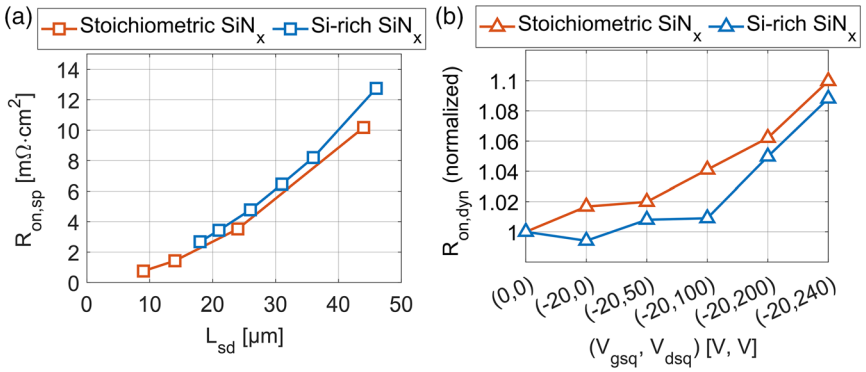

Figure 4. a) Specific on-state resistances for MISHEMTs with Si-rich and stoichiometric SiN_x passivation with varying source–drain distances. b) $R_{on,dyn}$ measured at $V_{gs} = 0$ V, and $V_{ds} = 1$ V after biasing V_{dsq} up to 240 V with an on/off-state time of 1/99 μs.

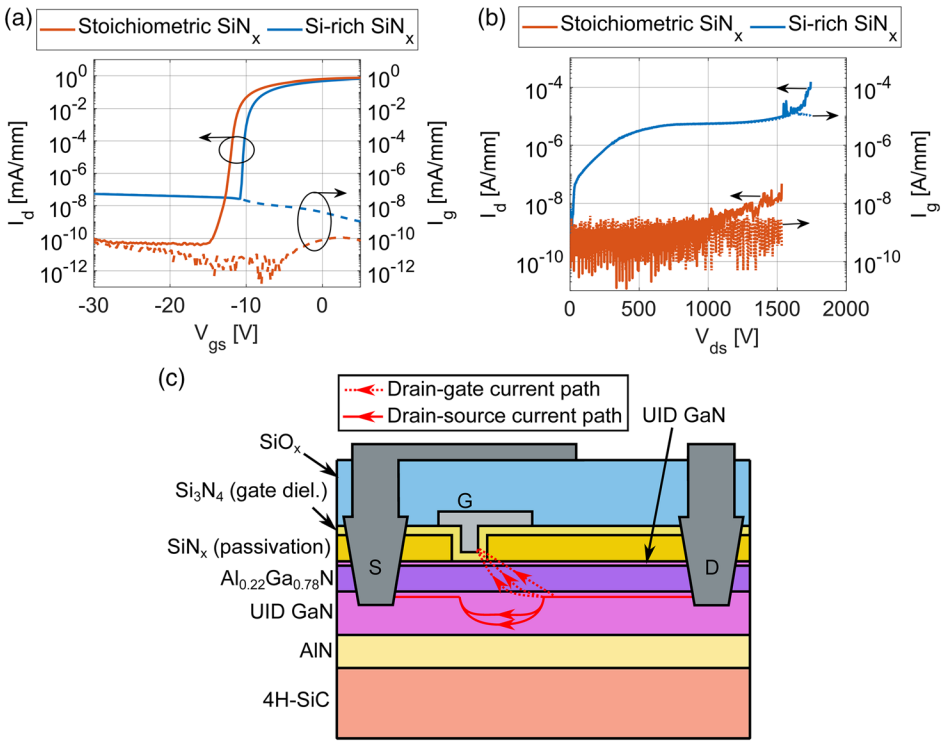

Figure 5. a) Transfer characteristics for MISHEMTs with long field plates and with $V_{ds} = 40$ V. b) Off-state breakdown characteristics of MISHEMTs with long field plates with $V_{gs} = -30$ V. c) A schematic showing potential off-state leakage current paths in the MISHEMTs with Si-rich and stoichiometric SiN_x passivation layers.

3.2. Impact of SiN_x Stoichiometry

The specific on-resistances ($R_{on,sp}$) were obtained from the output characteristics at $V_{gs} = 0$ V, $V_{ds} = 1$ V of MISHEMTs with source–drain distances ($L_{sd} = L_{gs} + L_g + L_{gd}$) varying between 9 and 46 µm (**Figure 4**a), using a Keysight B1500 parameter analyzer. Low $R_{on,sp}$ of 0.75 and 10.2 mΩ cm^2 for $L_{gd} = 5$–40 µm was obtained, which shows that the electron transport properties are not adversely affected by having a thin UID GaN layer grown directly on the AlN nucleation layer. The SiN_x stoichiometry did not seem to have any significant impact on the static on-state resistance. The difference in contact resistance between the two samples can explain the small discrepancy in the resistance.

The $R_{on,dyn}$ was measured on MISHEMTs with an $L_{gd} = 20$ µm (Figure 4b) using an AMCAD 3200 system. The devices were pulsed from an off-state bias point with a gate voltage (V_{gsq}) of –20 V and with a drain voltage (V_{dsq}) that varied from 0 to 240 V (measurement system limit) to an on-state at $V_{gs} = 0$ V and $V_{ds} = 1$ V. The on-state time was set to 1 µs, while the off-state time was set to 99 µs. All $R_{on,dyn}(V_{gsq}, V_{dsq})$ values extracted from the pulsed I–V measurements were normalized against $R_{on,dyn}(0\,V, 0\,V)$. $R_{on,dyn}$ was increased from 12.79 (12.88 Ω mm) to 14.07 Ω mm (14.01 Ω mm) on MISHEMTs with stoichiometric (Si-rich) SiN_x passivation layers, representing an increase of 10% (9%). In GaN HEMTs with carbon-doped buffer layers, stoichiometric SiN_x passivation layer can lead to normalized $R_{on,dyn}$ of 4–6, while the Si-rich passivation layers show a much smaller dispersion.[13,14] In contrast, the stoichiometry of the SiN_x passivation layers did not seem to have the same impact on $R_{on,dyn}$ up to a V_{dsq} of 240 V in the "buffer-free" MISHEMTs. This indicates that the trapping effects are not significantly affected by the stoichiometry in the passivation layer. However, despite not being affected by the type of passivation, it is still possible that the increase in $R_{on,dyn}$ is caused by traps in the UID GaN layer, AlN nucleation layer, or at one of the III-nitride interfaces.

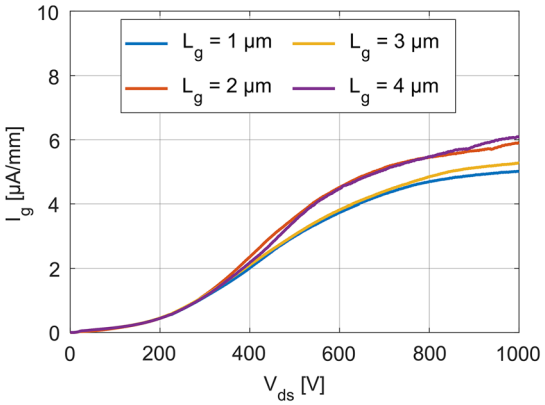

Figure 6. Off-state gate current for MISHEMTs with Si-rich SiN_x passivation layer with varying gate lengths.

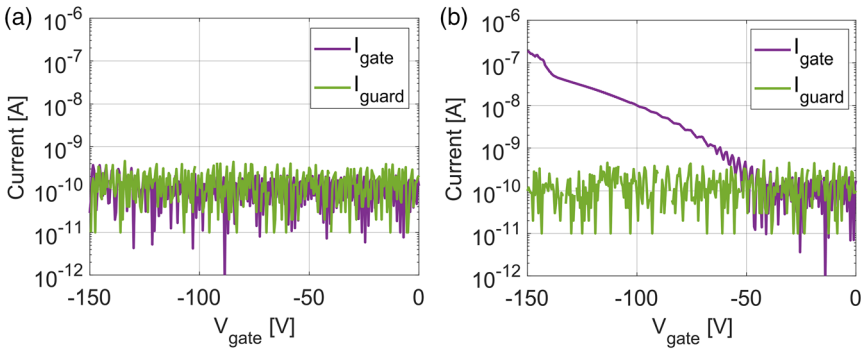

Figure 7. Dielectric leakage test with a) stoichiometric and b) Si-rich SiN_x.

MISHEMTs on Sample A and B showed a marked difference in terms of off-state leakage currents (**Figure 5**a,b). These MISHEMTs were fabricated with $L_{gfp} = 4\,\mu m$ and $L_{sfp} = 5\,\mu m$. Using a stoichiometric SiN_x passivation layer and gate dielectric, the gate current was reduced from 4×10^{-8} to $4.7 \times 10^{-11}\,A\,mm^{-1}$ at $V_{gs} = -20\,V$ (Figure 5a). At voltages above 1000 V, the gate current remains below $10\,nA\,mm^{-1}$, while the drain current increases to a maximum of $47\,nA\,mm^{-1}$ (Figure 5b). This indicates a small drain–source leakage current (punch-through) in the UID GaN layer underneath the depleted gate region (Figure 5c), which shows that the GaN, AlN, and the semi-insulating SiC provide sufficient electron confinement. In the HEMTs with Si-rich SiN_x passivation layer, the high drain currents are likely caused by currents through the passivation layer and gate dielectric (Figure 5c).

Gate leakage currents up to 1000 V were also measured for HEMTs with Si-rich SiN_x passivation and gate lengths between 1 and 4 μm to make the comparison between MISHEMTs of Sample A and B fairer (**Figure 6**). No significant difference in gate leakage between the three gate lengths can be seen. Therefore, the high gate current seen in Figure 5 is not caused by a large gate area. A gate length of 2 μm or less could be used to minimize the on-state resistance without compromising off-state leakage currents.

The dielectric leakage test structure shows that the gate current (I_{gate}) and guard current (I_{guard}) in Sample A are below 1 nA for gate voltages (V_{gate}) between 0 and −150 V (**Figure 7**a), which indicate that both the barrier current and surface-related currents are small. However, in Sample B, the barrier current through the SiN_x films and AlGaN layer increased by almost three orders of magnitude for Sample B when the gate voltage (V_{gate}) decreased from −40 to –150 V (Figure 7b). This suggests that the large off-state drain–gate currents were caused by leakage through the gate dielectric, passivation layer, and AlGaN barrier down to the 2D electron gas rather than by surface-related leakage currents at (or surrounding) the SiN_x/GaN interface. The destructive breakdown voltages of the two measured MISHEMTs with $L_{gfp} = 4\,\mu m$ and $L_{sfp} = 5\,\mu m$ was 1532 and 1742 V for the Si-rich and stoichiometric-passivated MISHEMT, respectively (Figure 4b). However, MISHEMTs with shorter field plates display higher breakdown voltages (Figure 3a), showing that the field plate design is not optimized for the highest breakdown voltage in Figure 5. By decreasing the length of the field plates, it was possible to increase the breakdown voltage from 1742 to 2200 V (Figure 3b and 4b). However, the drain–gate current remains high ($>1\,\mu A\,mm^{-1}$) regardless of the field plate length. By combining short gate and source field plates with a stoichiometric SiN_x passivation and gate dielectric, the breakdown voltage could be increased further while maintaining a low gate leakage current.

4. Conclusion

MISHEMTs with two isolation techniques and two SiN_x passivation layers were fabricated on a "buffer-free" AlGaN/GaN-on-SiC heterostructure to study their impact on the DC, pulsed *I–V*, and high-voltage off-state characteristics. Drain-gate leakage currents were suppressed by more than two orders of magnitude at high voltages using stoichiometric instead of a Si-rich SiN_x passivation layer without compromising the dynamic on-state resistance in the measured interval. The high drain–gate currents observed in the MISHEMTs with a Si-rich passivation layer were likely not caused by surface-related currents but instead by leakage from the gate metal down to the 2DEG through the SiN_x layers. When using a stoichiometric SiN_x passivation layer, the primary leakage mechanism at high voltages was a drain–source leakage current in the III-nitride heterostructure rather than a drain–gate leakage. MISHEMTs with nitrogen implantation isolation allowed for the highest off-state breakdown voltages compared with mesa isolation down to the SiC substrate. By combining the stoichiometric SiN_x passivation layer with short field plates, an enhanced breakdown voltage with drain leakage currents in the $1–100\,nA\,mm^{-1}$ can be achieved, which shows the potential of this material for high-voltage power electronic HEMTs.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

AlGaN/GaN, buffer free, high voltages, mesa isolations, metal–insulator–semiconductor high-electron-mobility transistors, nitrogen implantation, SiN_x passivations

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