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Noise Characterization and Modeling of GaN-HEMTs at Cryogenic Temperatures

Mohamed Aniss Mebarki, Ragnar Ferrand-Drake Del Castillo, Denis Meledin, Erik Sundin, Mattias Thorsell, Niklas Rorsman, Victor Belitsky, Vincent Desmaris

***Abstract*—We report on the noise characterization and modeling of AlGaN/GaN HEMTs at a cryogenic temperature of ~10 K within the frequency range of 4.5 to 6.5 GHz. This work is the first model in the literature describing the high frequency noise behaviour of GaN-based HEMTs at cryogenic temperatures using a two-parameter-noise concept. The suggested model, which is based on measured noise figures and scattering parameters, provides the frequency and the bias-dependence of the cryogenic noise properties of AlGaN/GaN HEMTs. The noise contributions from the intrinsic device, the parasitic network and the gate leakage are separately extracted. The contribution of the access network is found of the order of 1 K and increases with the frequency, while the gate leakage has an impact of the order of 0.1 K and increases at low frequency. The model provides a basis for the future design and implementation of GaN-based cryogenic low noise amplifiers.**

***Keywords* — HEMTs, GaN, Low Noise Amplifiers, Modeling**

I. Introduction

The GaN-based high electron mobility transistors (HEMTs) present a unique combination of high linearity and robustness with competitive low-noise characteristics, owing to the material's electrical and thermal properties. The performances of the GaN-based low noise amplifiers (LNA) may compete with their counterpart based on GaAs or InP at room temperature (RT) and down to 60 K physical temperature [1] [2] [3]. It is well known that the best noise performances of semiconductor technologies are usually recorded at substantially lower temperatures, at which the carrier transport properties are enhanced. This property is extensively exploited in applications of signal detection with high sensitivity. In particular, the choice of the transistors can be a key determinant of the overall noise performance of the radio-astronomy receivers [4]. In addition to their potential natural integration with heterodyne mixers [5] [6], the superior linearity and dynamic range of GaN HEMTs over conventional technologies make them very attractive for radio-astronomy cryogenic instrumentation and inherently excellent robustness against Radio Frequency Interference (RFI).

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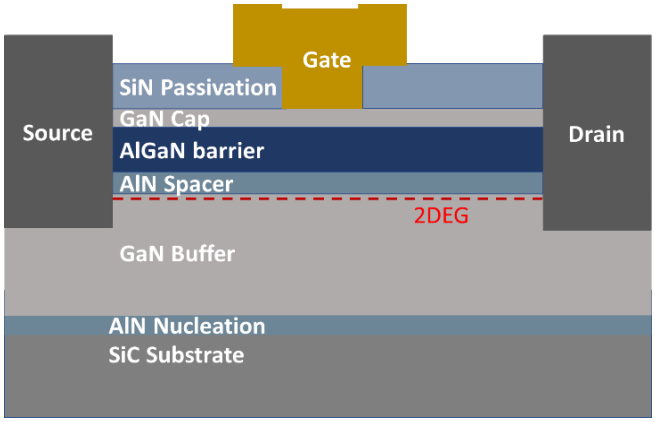

Fig. 1: Cross-section schematic view of the epitaxial structure of the studied HEMT

Previous studies have investigated the cryogenic DC, RF and transient characteristics of GaN-based HEMTs and concluded an overall improvement in performances [7] [8] [9] [10]. This is attributed to a significant increase of the electron mobility of in the two-dimensional electron gas (2DEG) at low temperatures [11] [12]. In addition, the noise figure of commercial GaN LNAs, designed for RT operation and large power handling, was recently reported to substantially improve when operating at ~10 K [13]. These observations support the use of the GaN-based technology as a novel candidate for microwave cryogenic low-noise applications. However, the microwave noise performance and modeling of GaN-based HEMTs when operating at cryogenic temperatures, necessary for optimal performance of GaN-Based LNAs, remains unexplored to date.

This work presents a detailed study of the bias and frequency dependent noise modeling of AlGaN/GaN HEMTs at the cryogenic temperature of ~10 K, based on noise measurements in the range of frequencies from 4.5 GHz to 6.5 GHz, enabling an accurate estimation of the minimum noise temperature presented by a GaN-HEMTs.

II. Device Description

Fig. 1 shows a schematic cross section of the epitaxial structure of studied transistor. It consists of AlGaN/GaN HEMT with a gate length of 0.2 µm. The heterostructure was composed

of unintentionally doped (u.i.d) 2 nm GaN cap layer, 11 nm $Al_{0.29}Ga_{0.71}N$ barrier, 1.5 nm AlN spacer layer. The 2DEG resides in the 1.8 µm thick GaN buffer layer. The buffer, grown on AlN nucleation, is Fe-doped. The details of the fabrication process are similar to the ones described in [14]. The source to drain distance was 2 µm and the source to gate distance was 0.75 µm. The gate width of the device is 2 x 25 µm. The choice of the transistor gate periphery is mainly motivated by the minimization of the transistor's power dissipation for better accuracy at cryogenic temperature, where the cooling power is limited.

III. Electrical Characterization

A. DC Characterization

The DC characterization was performed on-wafer using Agilent B1500A semiconductor parameter analyzer at RT and at the cryogenic temperature (~10 K), denoted CT, in a cryogenic probe station. Fig. 2 shows the typical I-V curve of the device at RT and CT. The DC characteristics of the device at RT are consistent with those reported previously using similar technologies [14] [15]. The on-resistance, R_{on}, decreased from 1.86 Ω.mm at RT to 1.19 Ω.mm at CT.

Only a minor shift was observed in the pinch-off voltage, which was around -1.6 V. Also, no significant increase in the maximum current density was observed at CT, even when forward biasing the gate. This behavior differs from the one reported in [8] [16], but could be ascribed to trapping effects becoming more dominant at CT and either located in the AlGaN barrier or surface-related; in line with the results of the cryogenic GaN-HEMTs in [17] and [18]. This is in addition to the potential effects of the buffer traps due to its Fe-doping [19] [20], combined with the slow-down of the emission time of traps at cryogenic temperatures [18] [21]. A kink clearly observable in the I_{DS} – V_{DS} curve, and which is more pronounced at CT compared to RT at the same bias, further supports this possibility.

Furthermore, a significant decrease of the gate leakage at CT compared to RT is observed, as shown in Fig. 3 at V_{DS} = 0 V.

Nevertheless, the scope of this study concerns the cryogenic low-noise operation of the device, which corresponds to the gate bias region not affected by the onset of the Schottky conduction and taking advantage of the reduction of the access resistances, the related enhancement of the channel conduction and the reduced contribution of the gate leakage. All these features are beneficial for the improvement of the overall noise performance of the device at CT.

B. RF Characterization and Small-Signal Model

Second, the on-wafer S-parameters of the device were measured up to 40 GHz, using a Vector Network Analyzer (VNA), model ZVA67 from Rhode & Schwartz.

Following the approach in [22], the intrinsic small signal parameters were directly extracted. Fig. 4 illustrates the equivalent small signal model used to describe the device at both RT and CT.

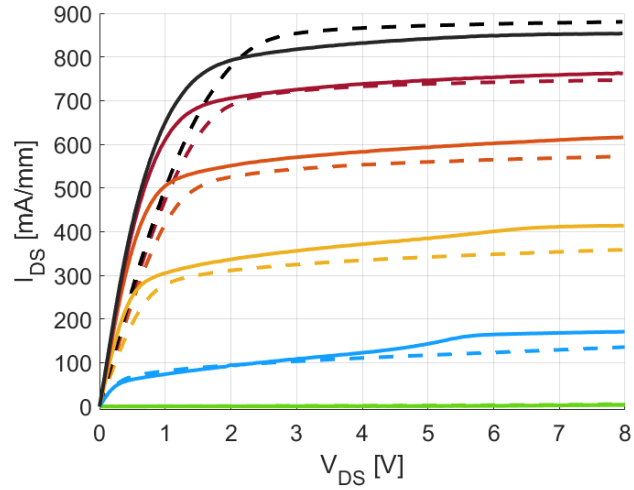

Fig. 2: Typical drain to source current-voltage (I_{DS}-V_{DS}) curve at RT (dashed lines) and CT (solid line), at V_{GS}=-1.5 V to 1 V with steps of 0.5 V from respectively down to top.

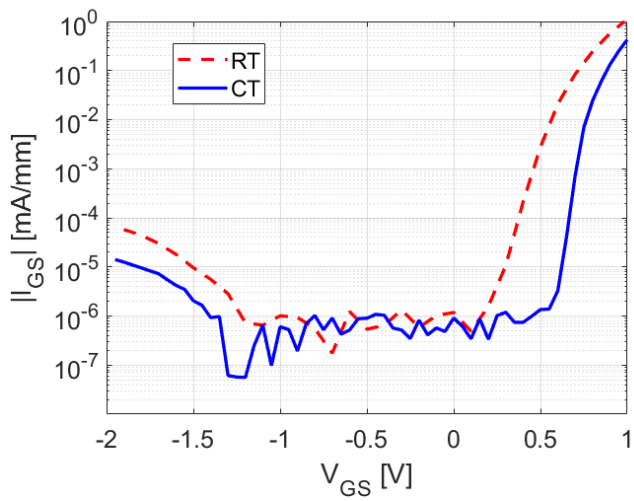

Fig. 3: Typical gate to source current-voltage (I_{GS}-V_{GS}) curve at RT (red dashed lines) and CT (blue solid line) at V_{DS} = 0 V.

The validity of the model was verified using the following error function:

$$\epsilon = \frac{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}} - S_{ij_{modeled}}|}{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}}|} \quad (1)$$

Where $S_{ij_{measured}}$ and $S_{ij_{modeled}}$ are respectively the measured and modelled S-parameters, i and j denoting the port number, over the frequency range from f_{min} = 0.2 GHz to f_{max} = 40 GHz. Fig. 5 shows the variation of the error function as a dependence on the bias at CT. Over the entire considered bias range relevant for the low-noise operation, V_{DS} from 4 to 10 V and V_{GS} from -1.6 to -0.5 V, an average error in the range of 2 to 3 % was recorded.

In the following discussion, a drain bias of V_{DS} = 5 V was chosen, as it provides a good balance between high RF gain, low power dissipation, and limited self-heating, which is convenient for the noise characterization.

Being one of the main parameters impacting the noise performance, the intrinsic transconductance, denoted $g_{m\text{-}int}$, was

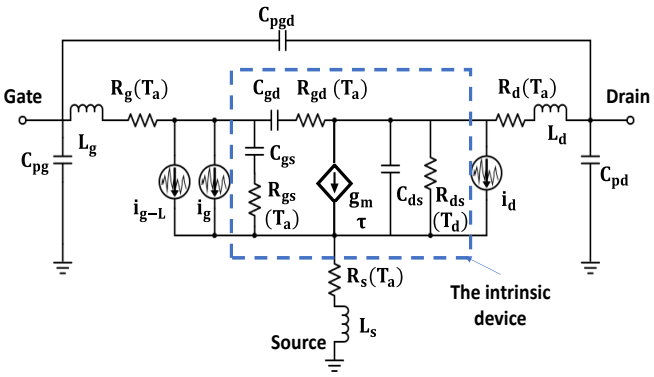

Fig. 4: Illustration of the equivalent small signal model, with the noise current sources considered in the noise model: i_g, i_d, $i_{g\text{-}L}$, referring to those associated with the gate, drain and gate leakage.

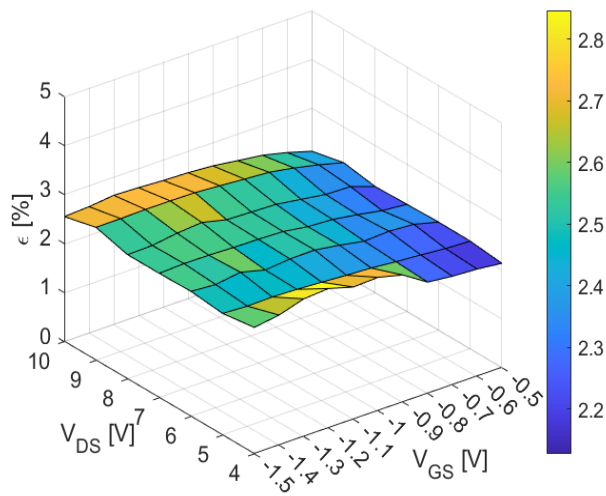

Fig. 5. Error function on the small signal model as function of the gate and drain bias at CT

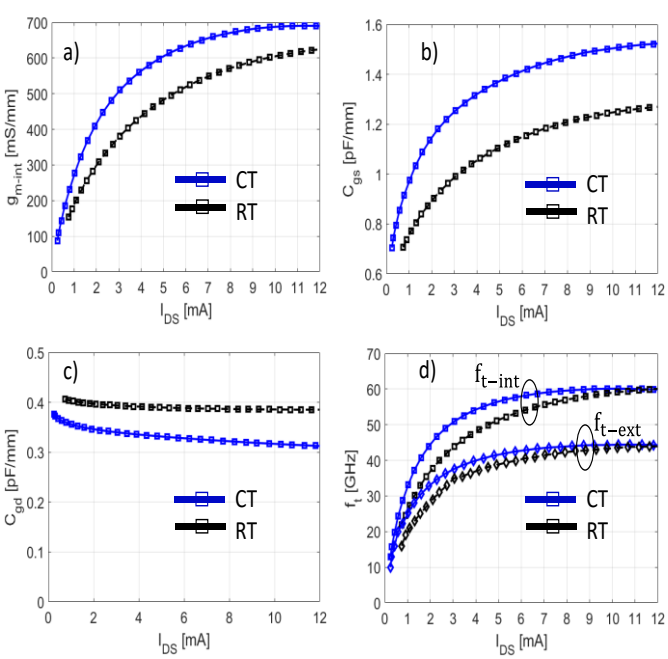

Fig. 6: The current dependence at V_{DS}=5 V of the intrinsic small signal parameters at RT (black) and CT (blue). a) $g_{m\text{-}int}$ b) C_{gs} c) C_{gd} d) f_t,

observed to significantly increase at CT. As seen in Fig. 6a, we also note a steeper slope of $g_{m\text{-}int}$ around the pinch-off bias region, reflecting an enhancement of the transport mechanisms in the channel and a better control of the gate over it. The gate to source capacitance, C_{gs}, increases at CT as shown in Fig. 6b. The C_{gs}-I_{DS} variation is found particularly temperature-sensitive as we observe a stepper increase and an earlier saturation at CT. The C_{gs} behaviour could be related to the variation with the temperature of the material properties and the distribution of the carriers, as was previously observed in other III-V devices [23] [24]. The gate to drain capacitance, C_{gd}, was found less bias and temperature-dependent as seen in Fig. 6c, which indicates about its relatively small effect on the variation of the noise properties of the transistor. The resulting intrinsic cut-off frequency of the device, $f_{t\text{-}int}$, improved by few gigahertz at CT, as shown in Fig. 6d together with the extrinsic $f_{t\text{-}ext}$ as extracted from the measured current-gain, which is mainly related to the increase of the transconductance.

IV. Noise Measurements, De-Embedding and Modeling

The cryogenic noise performance of the GaN HEMT was characterized in the range of frequencies from 4.5 GHz to 6.5 GHz. We used the cold-attenuator (CA) method to obtain the cryogenic noise measurements, relying on a 50 Ω noise source and a cooled 20 dB attenuator in front of the transistor mounted on a test fixture [25]. Compared to other methods, the CA offers several advantages from both the accuracy and the practical points of view [26]. First, the method is less prone to calibration errors since a single noise source is required and placed outside the cryostat. Time-wise, the noise measurements can be obtained over only one cooling cycle. Second, it allows minimizing the uncertainty resulting from the gradient of temperature over the input chain and the Excess Noise Ratio (ENR). This is achieved through the fact that in this configuration the contribution of the cold attenuator dominates over the other elements of the measurements system connecting the noise source to the device under test (DUT).

A. De-Embedding of the Equivalent Noise Temperature

Fig. 7 shows the setup used for the cryogenic noise measurements. The noise measurements were performed using the Agilent MXA N9020A power spectrum analyzer with its noise measurement option. A commercial 50 Ω noise source of 6 dB ENR form Keysight (N4002A) was employed. Given the impact of the cold attenuator contribution in the de-embedding of the measured data, a temperature sensor was directly clamped to it in order to accurately estimate its physical temperature as can be seen in Fig. 7. The noise receiver block, placed outside the cryostat, includes the spectrum analyzer and an isolated low-noise preamplifier to ensure a large signal-to-noise ratio of the measurements. Its noise contribution was estimated and de-embedded prior to the measurements.

The de-embedding of the noise contribution of the input and output chains of the test setup was obtained through the measurements of their respective S-parameters at the temperature of interest. For this purpose, a cryogenic calibration was performed using the approach employed in [27].

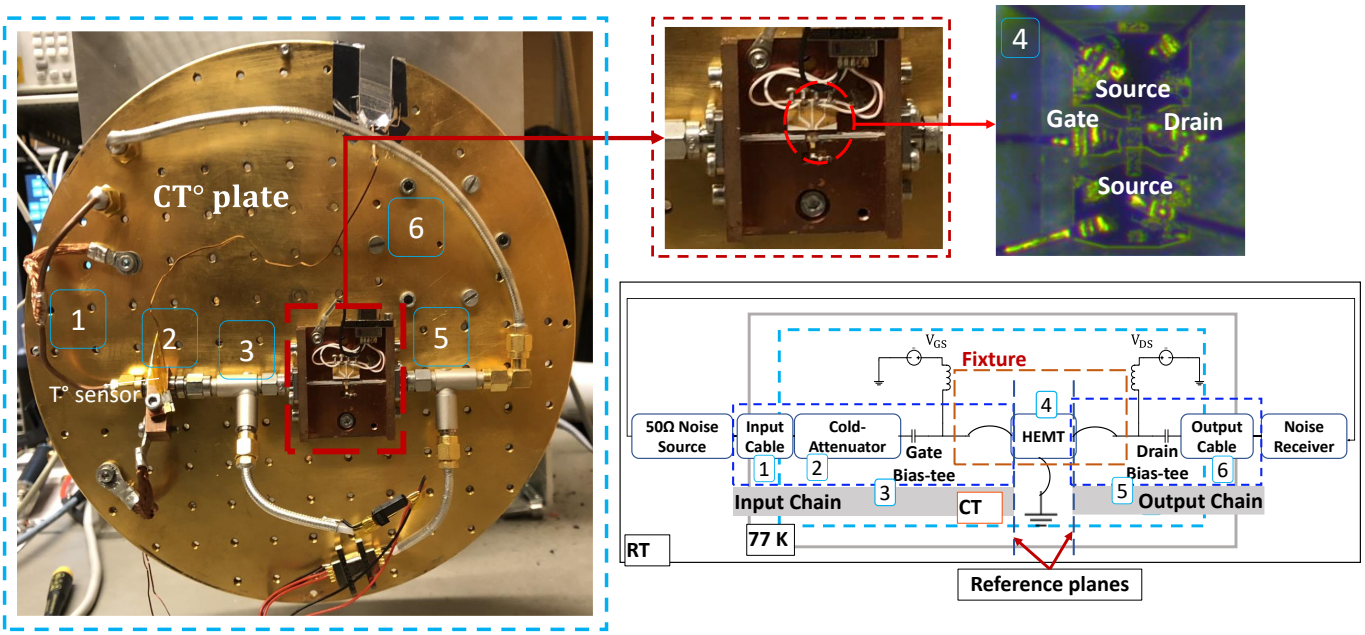

Fig. 7: Image of the cryogenic noise measurements setup (left) with the corresponding block schematic (right). The image was mirrored to facilitate the readability of the schematic from left to right. In the top right is shown a microscopic top-view image of the transistor with the interconnecting bond wires, as mounted on fixture for the noise measurements. The reference planes used for the extraction of the noise model of the DUT are indicated in the schematic. As 4 bond wires are used in parallel to connect the source pad to the ground, there total inductance is negligible and were accounted as part of the DUT.

The equivalent noise temperature of the DUT, $T_{e\text{-}DUT}$, was then extracted using the Friss formula:

$$T_{e-DUT} = G_{IN}[T_{e-sys} - \left(T_{e-IN} + \frac{T_{e-OUT}}{G_{IN}G_{DUT}}\right)] \qquad (2)$$

$T_{e\text{-}IN}$ and $T_{e\text{-}OUT}$, G_{IN} and G_{DUT} are the equivalent temperature of the input and output chains, and the available gain of the input chain and the DUT, respectively.

Four noise parameters are employed to describe the noise properties of the transistor. These are the noise resistance, R_n, the real and imaginary parts of the optimum impedance, R_{opt} and X_{opt}, and the minimum noise temperature, T_{min}. The noise temperature of the transistor as a function of the generator impedance, $Z_s = R_s + jX_s$, and the four noise parameters is given by [28]:

$$T_n = T_{min} + NT_0 \frac{|Z_S - Z_{opt}|^2}{R_s R_{opt}} \qquad (3)$$

where $Z_{opt} = R_{opt} + jX_{opt}$ is the optimum impedance, and $N = R_n G_{opt}$ with G_{opt} is the real part of the optimum admittance. $T_0 = 290$ K is the standard noise temperature.

The uncertainty on the noise measurements associated with the instruments and the mismatches was considered and computed using the approach in [31]. Table I provides a summary of the errors attributed to the instrumentation, considering the specifications provided by the respective manufacturers. In the case of the sensor of the physical temperature of the cold attenuator, a DT-470 model from Lakeshore, an accuracy of ±0.012 K is specified [32]. In addition, ±0.5 K due to the potential gradient of temperature between the outer conductor and the core resistive parts of the attenuator was considered, in line with the estimation obtained in [33]. The total resulting average uncertainty on the modeled minimum noise temperature (T_{min}) was ± 0.5 K. An average uncertainty of ± 2 Ω and ± 2.4 Ω were estimated for R_n and R_{opt} respectively. The error is marginal for the optimum reactance, X_{opt}, since it is mainly dependent on the input impedance of the transistor extracted from the small signal model.

TABLE I
INSTRUMENTATION UNCERTAINTIES IN THE MEASUREMENT OF THE NOISE TEMPERATURE OF THE DUT

Y-factor uncertainty on the noise figure [29]	±0.02 dB
ENR [30]	±0.15 dB
Uncertainty on the estimation of the gain [29]	± 0.1 dB
Physical temperature of the cold attenuator	±0.51 K

Furthermore, the accuracy of the noise measurements and the de-embedding at CT was also assessed using a calibrated cryogenic LNA [34]. An average total uncertainty on the noise temperature of the order of ± 1.5 K was verified.

B. Noise Model Extraction

In order to extract the 4 noise parameters defining (3) from the de-embedded measured data using (2), the Pospiezalski's model is used [28]. This method has previously been cryogenically implemented, combined with the 50 Ω noise measurements, for reliable modelling of other technologies [24] [33] [35].

At each bias point, considering that within the frequency band of interest only the thermal noise is relevant and hence accounted for, the extraction of the noise properties of the DUT is conditioned by the knowledge of both the small signal model and the noise temperature associated with each of its equivalent resistive elements. In fact, we consider a noise current source at the gate node, denoted $\overline{i_g}$, and a noise current source at the drain node, denoted $\overline{i_d}$, in shunt with the noiseless device, as illustrated in Fig. 4. It is also assumed that a correlation exists between both of these noise sources. The gate current leakage also introduces a noise contribution that is discussed below.

This representation defines the admittance form of the noise correlation matrix of the intrinsic device, denoted $C_{y^{int}}$, which is related to its Y-matrix, Y_{int}:

$$Y_{int} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ -Y_{gd} - \frac{\mathrm{Im}(Y_{gs})}{Y_{gs}^*} Y_{gm} & Y_{ds} + Y_{gd} \end{bmatrix} \quad (4)$$

where Y_{gs}, Y_{gd} and Y_{ds} represent the gate-source, gate-drain and drain-source admittances respectively, and $Y_{gm} = g_m e^{j(\frac{\pi}{2} - 2\pi F \tau)}$. Moreover, all the equivalent resistances in the transistor are assumed to be at a temperature T_g which tends to the environment temperature T_a except the channel resistance which temperature is denoted T_d. It is assumed to be several magnitudes higher depending on the DC power dissipation. Then, $\overline{i_g}$ and $\overline{i_d}$ can be expressed as function of T_g and T_d as [28] [36]:

$$C_{Y^{int}} = \begin{bmatrix} \langle i_g^2 \rangle & \langle i_g i_d^* \rangle \\ \langle i_g^* i_d \rangle & \langle i_d^2 \rangle \end{bmatrix} \quad (5)$$
$$= \begin{bmatrix} T_g(R_i|Y_{gs}|^2 + R_{gd}|Y_{gd}|^2) & T_g\left(R_i|Y_{gm}|^* + R_{gd}|Y_{gd}|^2\right) + T_d g_{ds} \\ T_g(R_i|Y_{gm}| + R_{gd}|Y_{gd}|^2) + T_d g_{ds} & T_d g_{ds} + T_g R_i |Y_{gm}|^2 + T_g R_{gd}|Y_{gd}|^2 \end{bmatrix}$$

with g_{ds}=1/R_{ds}. T_g and T_d are the only unknowns in (5), and are treated as fitting parameters. Since the four noise paraments of the device are derived from its noise correlation matrix, they can also be expressed as function of T_d and T_g. One can conveniently express the relationship between the noise correlation matrix, the fitting parameters, T_d and T_g, and the four noise parameters using the chain (ABCD) form of (5) after applying the appropriate matrix transform as:

$$C_A = T_s C_Y T_s^\dagger = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \begin{bmatrix} R_n & \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}^*} \\ \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}} & R_n|Y_{opt}|^2 \end{bmatrix} \quad (6)$$

where T_s is the transform matrix. In the case of the intrinsic device, it is defined as $T_s = \begin{bmatrix} 0 & A_{12} \\ A_{22} & 1 \end{bmatrix}$, such as the ABCD transform of (4) is given by $A_{int} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}$. † denotes the Hermitian operator.

Therefore (3) is a function of T_d and T_g. As (2) and (3) are equivalent, T_d and T_g can be determined through the least square fitting of the model to the de-embedded measured noise. The result of this procedure allows to fully describe the noise behavior of the device, based on its equivalent small signal model, at any given physical temperature and bias conditions.

V. Results and Discussion

Fig. 8 shows the results of the cryogenic noise measurements and modelling of the device at V_{DS} = 5 V in the low- noise bias region (I_{DS} ranging from 2.5 to 10 mA).

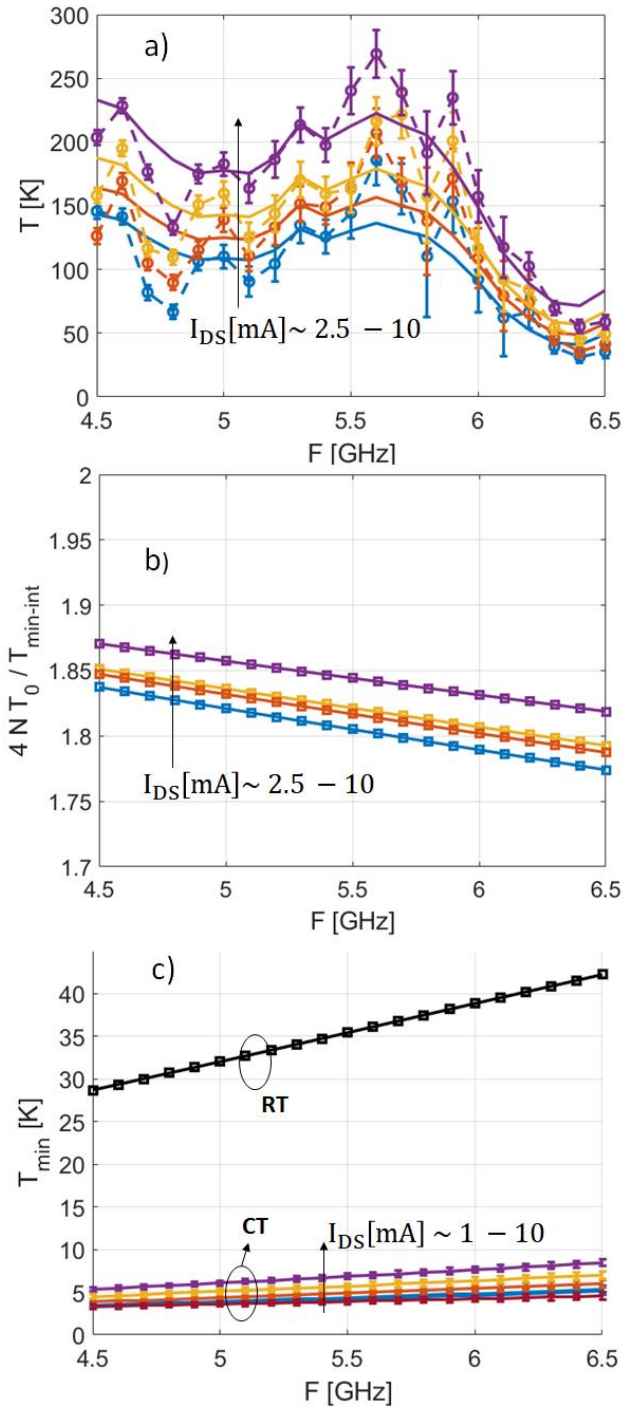

Fig. 8: a) The frequency-dependence at CT of the measurements (dashed-dotted lines) and the modeled noise temperature (solid lines) of the DUT. b) Frequency-dependence of $\frac{4NT_0}{T_{min-int}}$ c) Extracted T_{min} at the same conditions and the best-noise bias points at CT and RT.

The reference planes indicated in Fig. 7 are considered for the de-embedding of the noise temperature of the device. Thus, it is considered that the parasitics of the HEMT, including the access resistances, are part of the DUT. The interconnecting gate and drain bond-wires were de-embedded in prior together with the input and output chains of the noise measurements system.

TABLE II
INTRINSIC AND EXTRINSIC SMALL-SIGNAL PARAMETERS, NOISE PARAMETERS AT F = 6 GHZ AND AVERAGE MINIMUM NOISE TEMPERATURE AT V_{DS} = 5 V AT CT AND RT

Temperature			CT		RT
Small Signal Model	Bias	V_{DS} [V]	5	5	5
		I_{DS} [mA]	2.4	4.6	6.5
	Intrinsic	C_{gs} [fF]	49.5	62.2	54.7
		C_{gd} [fF]	18.6	17.6	19
		C_{ds} [fF]	0.5	2.5	0.5
		$g_{m\text{-}int}$ [mS]	14	24.4	22
		R_i [Ω]	5.5	4.6	5
		R_{gd} [Ω]	16.5	16.9	24
		g_{ds} [mS]	0.35	0.65	0.79
	Extrinsic	C_{pg} [fF]	17.2	17.2	17.5
		C_{pd} [fF]	22	22	18
		C_{pgd} [fF]	3.85	3.85	3.85
		L_g [pH]	44.4	44.4	38.3
		L_s [pH]	1	1	1
		L_d [pH]	43.2	43.2	39.8
		R_g [Ω]	0.6	0.6	1.2
		R_s [Ω]	8.1	8.1	11.33
		R_d [Ω]	7.2	7.2	15.6
Noise Model		T_d [K]	2580	4050	7432
		R_{opt} [Ω]	37.2	35.9	106.5
		R_n [Ω]	16.1	15.2	55.4
		T_{min} [K]	4.1	4.7	35.5

The results indicate a good agreement between the measured and the cryogenic model-based noise temperature of the device over the entire range of bias and frequency points of interest (Fig. 8a). Moreover, the physical validity of the extracted noise model can be verified through the condition on the parameter N introduced in [37] and [28], and defined using the following inequality:

$$1 \leq \frac{4NT_0}{T_{min}} \leq 2 \qquad (7)$$

Considering the intrinsic transistor, which noise contribution is denoted $T_{min\text{-}int}$, this condition is found to be satisfied over both the entire studied frequency and bias ranges as shown in Fig. 8b. The frequency dependence of the resulting estimated minimum noise temperature is presented in Fig. 8c. For comparison, the minimum noise temperature at RT at the best bias point of I_{DS} ~ 6.5 mA is also shown. Our noise model supports now the prior analysis of the DC and RF characterization of the GaN HEMT: a substantial reduction of the noise temperature is obtained when cooling down the device as the average T_{min} is found to drop by a factor of ~ 7.6.

Table II provides the full set of parameters used for the extraction of the noise model at RT and CT, at the typical low-noise bias points.

A. The bias dependence

Also, for completeness, the bias dependence of the other parameters of the cryogenic noise model at several frequencies across the measured band are presented in Fig. 9. A close inspection of the model indicates that at the lowest measured drain current, T_{min} reaches its lowest value only for the frequencies above 5.5 GHz. Further increasing the drain current results in a relatively better noise performance at lower frequencies. This can be attributed to an increased contribution of the gate leakage as will be discussed in the next sub-section. In fact, the minimum noise temperature is expected to substantially increase at all frequencies below a certain level of I_{DS} due to the suppression of the gain. However, accurate noise characterization at lower I_{DS} is difficult to achieve, mainly due to the low associated gain.

The further increase of T_{min} with I_{DS} could be attributed to the decrease of the transconductance and the self-heating of the transistor. In fact, T_{min} is initially proportional to f_t, which is linearly dependent on the carrier velocity in the channel. However, the effective channel temperature also affects significantly the bias dependence of T_{min}. As shown in Fig. 10, T_d presents a significantly rapid increase with respect to I_{DS}. T_d reflects the self-heating effect in the channel, which then leads to a degradation of T_{min} before the maximum cut-off frequency is reached. Besides, comparatively with RT, T_d is found to drop by a factor of ~ 1.7 – 1.8. This estimation is in line with those found with other HEMT technologies in the literature [24] [38]. According to our model, the GaN-HEMT presents an average best noise performance over the studied frequency range (4.5 – 6.5 GHz) of ~ 4.1 ± 0.5 K at a power consumption P_{DC} of about 12.5 mW. This estimated performance is comparable with the state-of-art results in the same frequency band based on other materials such as SiGe [39] and GaAs [40]. It should be noted that no prior optimization of the transistor, in terms of materials or dimensions, to minimize its noise temperature was performed. Further adjustments of the layout and the epitaxial designs are then likely to make the AlGaN/GaN HEMT technologies approaching the results of the InP HEMTs [41]

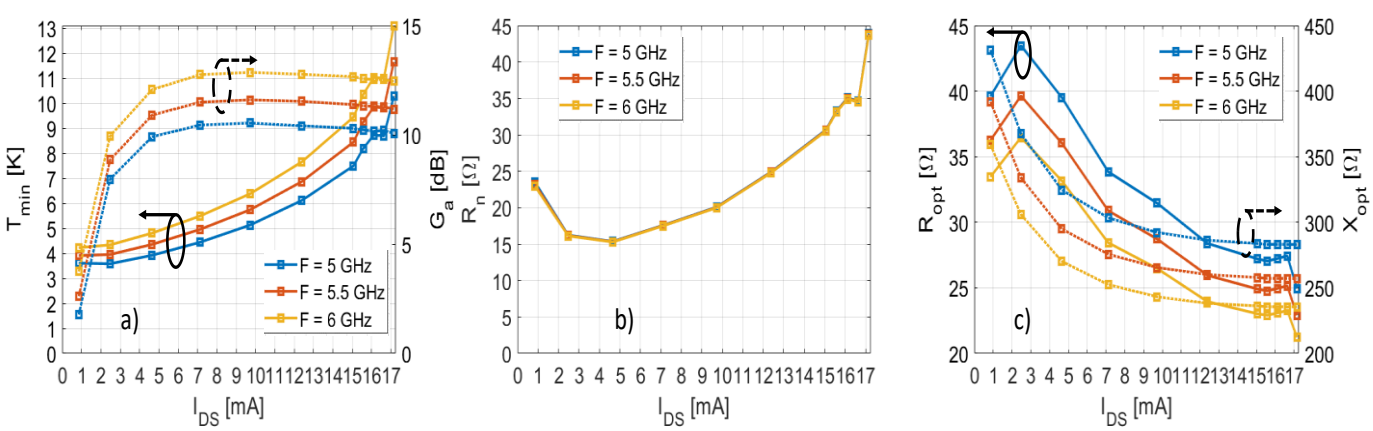

Fig. 9: Bias-dependence of the noise model parameters at CT, V_{DS} [V] = 5 and F [GHz] = 5, 5.5, 6 a) T_{min} b) R_n c) R_{opt} and X_{opt}

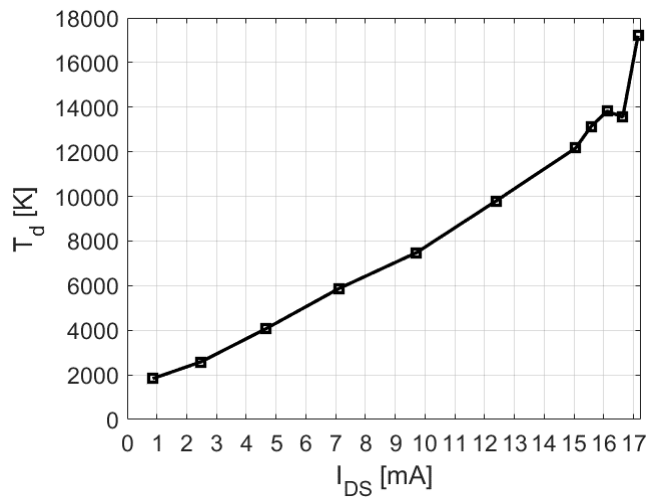

Fig. 10: The bias-dependence of T_d at CT at V_{DS} = 5 V

[42], which is usually the technology of choice for the targeted applications [43].

B. The contributions of the parasitic and the gate leakage

In order to provide further insights on the possibilities of such an optimization, the noise contribution of the extrinsic device network was examined. The approach introduced in [36] and [44] was implemented for this purpose. Accordingly, denoting C_{Z-int} and C_{Z-tot} the noise correlation matrix in its impedance form of respectively the intrinsic device and the total DUT, the noise contribution of the extrinsic network, $C_{Z\text{-}ext}$ is obtained as [36] [45]:

$$C_{Z-tot} = C_{Z-ext} + C_{Z-int} \quad (8)$$

Fig. 11 shows the bias dependence of the potential improvement of the minimum noise temperature, denoted ΔT_{min}^{int}, considering the suppression of the contribution of the parasitic network at different frequencies, ranging from 5 to 6 GHz. The contribution of this latter is found to be of the order of 1 K. In addition, we observe an increase in the same order with the frequency. The results mainly reflect the potential of reducing the access resistances, which can be possible by different ways as optimizing the device lateral layout or optimizing the process and materials involved in the formation of the contacts and electrodes.

Another parameter which could significantly contribute to the equivalent noise temperature of the transistor is the gate leakage. On the basis of the study reported in [46], the gate current leakage introduces shot noise between the gate and the channel. It is equivalent to a noise current source in parallel between the gate and source nodes (Fig. 4), and can then be expressed as [46]:

$$|i_{g-L}| = \sqrt{2qI_g} \quad (9)$$

where I_g is the DC measured gate current leakage and $q = 1.6 \times 10^{-19}$ is the Coulomb charge. Denoting ΔT_{min}^{L} the potential improvement on T_{min} from the suppression of the gate leakage, the frequency dependence of the contribution of this latter is shown in Fig. 12 for different levels of I_{DS}. In average,

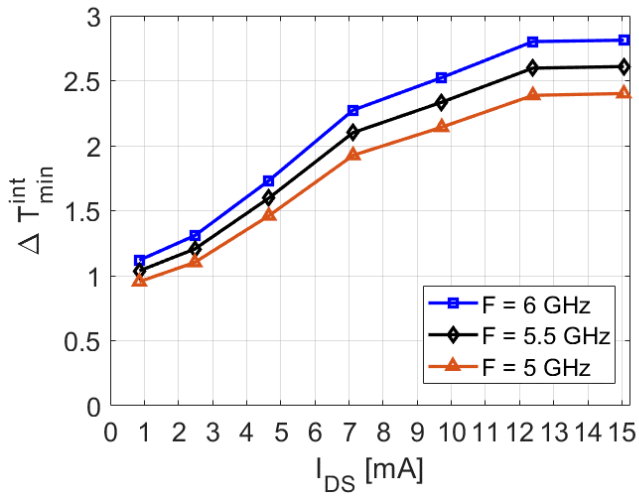

Fig. 11: The bias-dependence of effects on T_{min} at CT and F= 5:0.5:6 GHz from the parasitic network

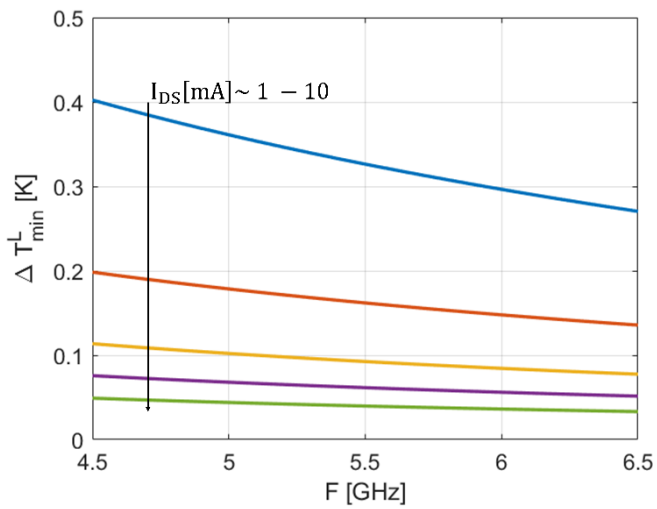

Fig. 12: The frequency-dependence of the effects of the gate leakage on T_{min} at CT.

at the best bias point the gate leakage contribution represent around 4% of the modelled T_{min}.

The effect of the gate leakage on the minimum noise temperature of the device is found to be more pronounced at low frequency. Its optimization would then be beneficial to enable better noise performances at both the low power dissipation and low frequency conditions.

CONCLUSION

We presented the microwave noise characterization and model of the AlGaN/GaN HEMT with 0.2 µm gate length at ~10 K, for prospective implementation of GaN HEMTs in cryogenic LNAs. The suggested bias and frequency dependent noise model is following a well-established two-parameter-noise concept. The small signal model, on which it relies, was studied and validated over the frequency and bias ranges of interest. A good agreement of the modelled noise parameters with the experimental measurements was obtained. Moreover, potential improvements in the device noise performance can be investigated and quantified from the derived model, e.g., the optimization of the access resistances. Although relatively low, the gate leakage also contributes to the noise especially at low

frequency. Further studies aiming optimization of the entire AlGaN/GaN HEMT structure and material for optimum operation at cryogenic temperatures should bring further improvements in the performance.

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