Multifunctional Spin Logic Operations in Graphene Spin Circuits

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Spin-based computing, combining logic and nonvolatile magnetic memory, is promising for emerging information technologies. However, the realization of a universal spin logic operation, representing a reconfigurable building block with all-electrical spin-current communication, has so far remained challenging. Here, we experimentally demonstrate reprogrammable all-electrical multifunctional spin logic operations in a nanoelectronic device architecture, utilizing graphene buses for spin communication and mixing and nanomagnets for writing and reading information at room temperature. This device realizes a multistate spin-majority logic operation, which is reconfigured to achieve (N)AND, (N)OR, and XNOR Boolean operations, depending on the magnetization of inputs. The results are in good agreement with the predictions from a spin-circuit model, providing an experimental demonstration of a spin-based logic unit that takes advantage of the vector nature of spin, as opposed to conventional scalar charge-based devices. These spin logic operations in large-area graphene are fully compatible with industrial fabrication processes and represent a promising platform for scalable all-electric spin-based logic-in-memory computing architecture.

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I. INTRODUCTION

Utilizing electron spin as a state variable for logic-in-memory architecture has significant potential, allowing the design of circuits beyond the von Neumann architecture and realizing low-power, compact, and fast information technologies [1,2]. It offers the possibility to combine nonvolatile memory with spin logic to achieve highly efficient integrated components for information technology and artificial intelligence [3]. Multiple proposals to realize spin logic devices have been put forward, including spin transistors [4], magnetologic gates [5], all-spin switches [6], magnetoelectric spin-orbit devices [7], and concepts based on magnetic domain-wall motion [8] and spin-wave interference [9,10]. Although such technologies may not be able to outperform complementary metal oxide semiconductor (CMOS) circuits for general logic applications, they may nevertheless prove beneficial for certain application-specific computing operations [11].

The magnetologic and all-spin-logic concepts are attractive due to their all-electrical control, reconfigurability, and possible integration with existing technologies [12,13]. Beyond such logic operations, utilizing weighted summation of spin currents based on the vector nature of spins can be useful for advanced neuromorphic computing [14,15]. The realization of these concepts is severely restricted by the short spin-coherence length in metallic spin interconnects. However, with the advent of long-distance spin communication in large-area multiterminal graphene spin circuits [16–18], the realization of spin-based computational schemes should be feasible. Up to now, only a few basic building blocks for spin logic are experimentally realized, such as a spin "exclusive or" (XOR) operation using spin current in graphene and silicon channels [19,20]. Although these developments are necessary, they are insufficient to realize universal, reconfigurable, and multifunctional spin logic devices. In contrast, a

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spin-majority logic gate, where the majority of input states determine the output logic state, is identified as a logic primitive for spintronic circuits [21]. Such a spin-majority logic device, paired with an inversion functionality, forms a universal Boolean set representing a reconfigurable building block for future information technologies [22]. However, an experimental realization of a comprehensive and reconfigurable multifunctional spin logic device based on pure spin current is so far lacking.

Here, we demonstrate all-electrical multifunctional spin logic operations based on pure spin currents at room temperature. We take advantage of efficient spin communication between nanomagnetic input and output terminals in a large-area chemical-vapor-deposited- (CVD) graphene integrated spin circuit. The basic mechanism relies on the mixing of spin currents within the graphene channel, i.e., the intrinsic capability to add and cancel out spin densities in a linear regime with electrical control of individual spin inputs using tunable bias currents. This reconfigurable and multifunctional spin logic device realizes spin-majority logic (SMAJ); AND, OR, and XNOR logic operations; and their inversion (NOT), according to the information encoded in the magnetization direction of the magnetic electrodes. These results are confirmed by circuit simulations in SPICE where the device structure is modeled using spin-transport-based circuit models [23,24] to gain detailed insights into the experimental observations.

We believe this is an essential experimental demonstration of a key component of all-spin-logic (ASL) operating at room temperature, namely, a multiterminal spin-circuit platform that realizes the addition and cancellation of pure spin currents for multifunctional logic operations. Similar binarylike weighted summation is discussed for charge-based architectures, where weighted charge currents are

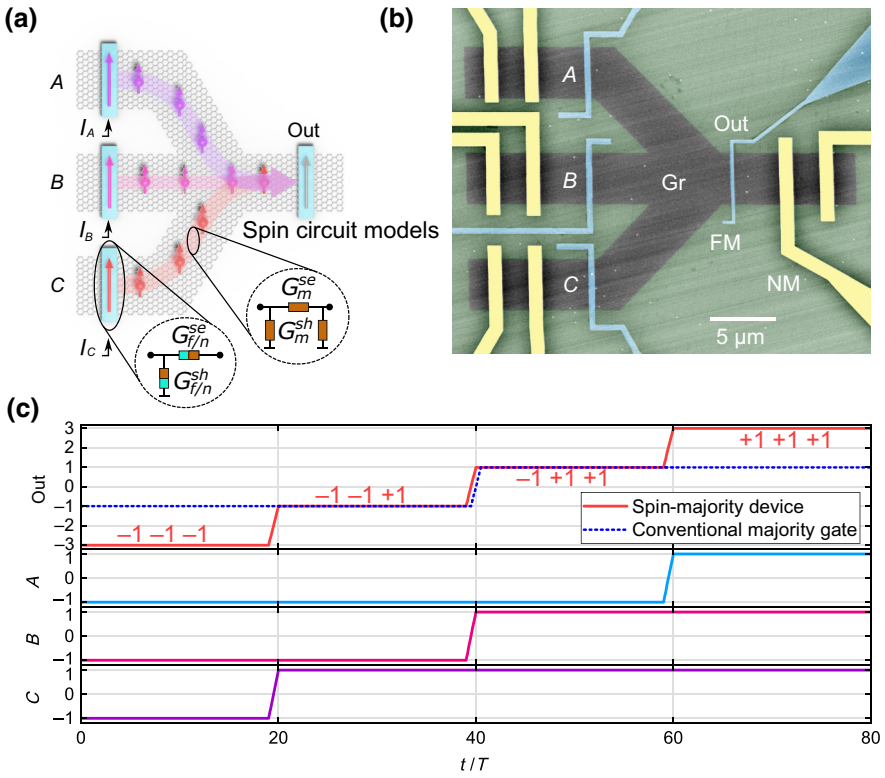

FIG. 1. Spin-majority logic device in a graphene-based spin-integrated circuit. (a) Schematic of a spin-majority logic device with a three-input fan-in circuit, where ferromagnetic contacts are used for writing and reading spin information, and the graphene channel is used for information communication via pure spin currents. (b) Colored SEM image of the spin-majority logic device. Device consists of a three-input (A, B, C) and one-output (O) multiterminal fan-in CVD Gr circuit with ferromagnetic electrodes (Co/TiO_2, blue color). Type of injected spin polarization, spin up (1) or spin down (0), can be controlled by changing the magnetization of electrodes or by applying electrical bias currents of opposite polarities ($+I$ or $-I$) to achieve spin injection or extraction. Resultant spin state is probed as an output voltage signal after spin transport and mixing in the graphene buses. Nonmagnetic electrodes (Au/Ti, yellow) are used as reference contacts. (c) Simulation comparing the output signal of a conventional charge-based majority gate and a spin-majority logic device for different combinations of input states. Majority gate logic output is true (or 1) when half or more arguments are true; otherwise it is false (or 0). To simulate the device, spin-circuit models employ conductance matrices, G, to capture spin transmission through FM/Gr interfaces and spin diffusion and relaxation in graphene. Spin-based realization shows multiple signal levels, which provide additional information on the number of inputs that constitute the majority.

added or subtracted in the context of in-memory computing, which is an active area of current research [25]. Our spin-based summing unit adds another dimension to this function due to the vector nature of spin, as opposed to the scalar nature of charge. The magnetic inputs of the device can be designed with an arbitrary alignment of their polarization axes on the two-dimensional (2D) plane, allowing for nonbinary weights [15,16]. Our spin-summation unit in CVD graphene is scalable using advanced lithography and fully compatible with industrial fabrication processes.

II. RESULTS AND DISCUSSION

The basic building blocks for the realization of multifunctional spin logic devices are the channel materials, which allow excellent spin communication in complex circuit architectures, and ferromagnetic elements, which represent nonvolatile memory and act as the source and drain for spin-polarized carriers. Graphene is an ideal material to be utilized as a spin interconnect in the proposed spin logic concepts because its low intrinsic spin-orbit coupling allows long spin-coherence lengths [26]. In particular, recent advances with the demonstration of robust room-temperature spin-interconnect functionality of large-area chemical-vapor-deposited (CVD) graphene with more than 30-μm spin-communication distance, and the realization of complex spin-circuit architectures make it a prime candidate to build scalable spintronic technologies [16,27–30]. We take advantage of such excellent spin-transport properties in CVD graphene on a 4-inch Si/SiO_2 wafer for the fabrication of spin logic devices. Figures 1(a) and 1(b) show a schematic illustration and scanning electron microscope (SEM) image of the nanofabricated CVD graphene-based multifunctional spintronic device contacted with ferromagnetic (FM) TiO_2/Co and nonmagnetic (NM) Ti/Au electrodes (see fabrication details in Sec. IV and Supplemental Material Notes 2 and 3 [31]).

We analyze the spin-majority logic device operations using four-component (one charge and z-, x-, and y-polarized spins) physics-based spin-circuit models for the nonmagnetic graphene (Gr) channel and the FM inputs, as shown in Fig. 1(a). The model captures both spin diffusion and relaxation in the graphene channel and electron transmission and spin mixing at the FM/Gr interface (see details in Supplemental Material Note 1 [31]). Simulations on a three-input spin-majority device show four-state output with two positive and two negative states, see Fig. 1(c). Each input magnet electrically injects a spin current, i_S, that propagates along the channel and reaches the output magnet, which acts as a spin-selective voltage probe that converts the spin current in the channel into a charge voltage. When all the inputs produce spin-down or spin-up currents ("0" or "1" states), they add up in the channel to $-3i_S$ or $+3i_S$, respectively, and the output voltage is $\propto\pm 3i_S$. When one of the magnets has an opposite logic state compared to the others, a spin-current cancellation leads to an output voltage of $\propto\pm i_S$. Thus, the voltage level indicates whether all three or only two of the inputs have the same logic, and the output sign reveals if the majority state is 0 or 1.

A. Spin communication in a graphene circuit

First, we measure spin communication in the graphene circuit connected with magnetic memory elements [Fig. 2(a)]. Figure 2(b) shows the gate dependence of graphene channel resistance (Dirac curve), demonstrating that all branches exhibit uniform p-type doping, typical for wet-transferred CVD graphene on SiO_2 [32]. The spin-transport measurements are performed in the nonlocal geometry [Fig. 2(a)], where a bias current, I, applied between an input FM and graphene creates spin accumulation under the contact, which then diffuses through the graphene interconnect and is detected by the output magnet in the form of a voltage signal, V. To perform spin-valve measurements, we sweep an in-plane magnetic field, B_y, along the easy axis of the magnets, which switches the magnetization direction of FMs between the parallel (P) and antiparallel (AP) configurations and results in sharp changes in the detected spin voltage, as shown in Fig. 2(c). A small spin-independent linear background is subtracted from the data. It most likely originates due to current-spreading or thermal effects and can be suppressed by optimizing the device design or by using an auxiliary voltage source [19,33–36]. In addition, this background may become negligible if the spin-signal magnitude can be increased, e.g., by increasing the tunnel spin polarization of FM electrodes using hexagonal boron nitride (hBN) as a tunnel barrier [37]. Next, Hanle spin-precession measurements are performed by applying an out-of-plane magnetic field, B_z, which induces spin precession and dephasing in graphene [Fig. 2(d)]. The curves are fitted with a standard Hanle equation [38] to estimate spin parameters in all channels with a spin lifetime of $\tau \sim 250$ ps, spin-diffusion coefficient of $D \sim 0.036$ $m^2\,s^{-1}$, and spin-diffusion length of $\lambda \sim 3$ μm. This demonstrates good spin-communication properties in the multiterminal graphene spin circuit.

Different channel lengths, small variations in spin-transport parameters, and disparity in tunnel spin polarization of each input FM electrode may result in unequal magnitudes of spin voltage in different graphene branches. We observe a larger signal amplitude in the middle branch compared to the other two branches [Figs. 2(c) and 2(d)], which is attributed to a slightly smaller distance between injector B and the output. In the future, this can be avoided at the device design stage by ensuring that the spin-transfer distance is the same for all branches with similar spin-injection efficiency of the FM contacts. To balance the spin-signal magnitude produced by all inputs at the output, we calibrate the bias-current values by measuring the

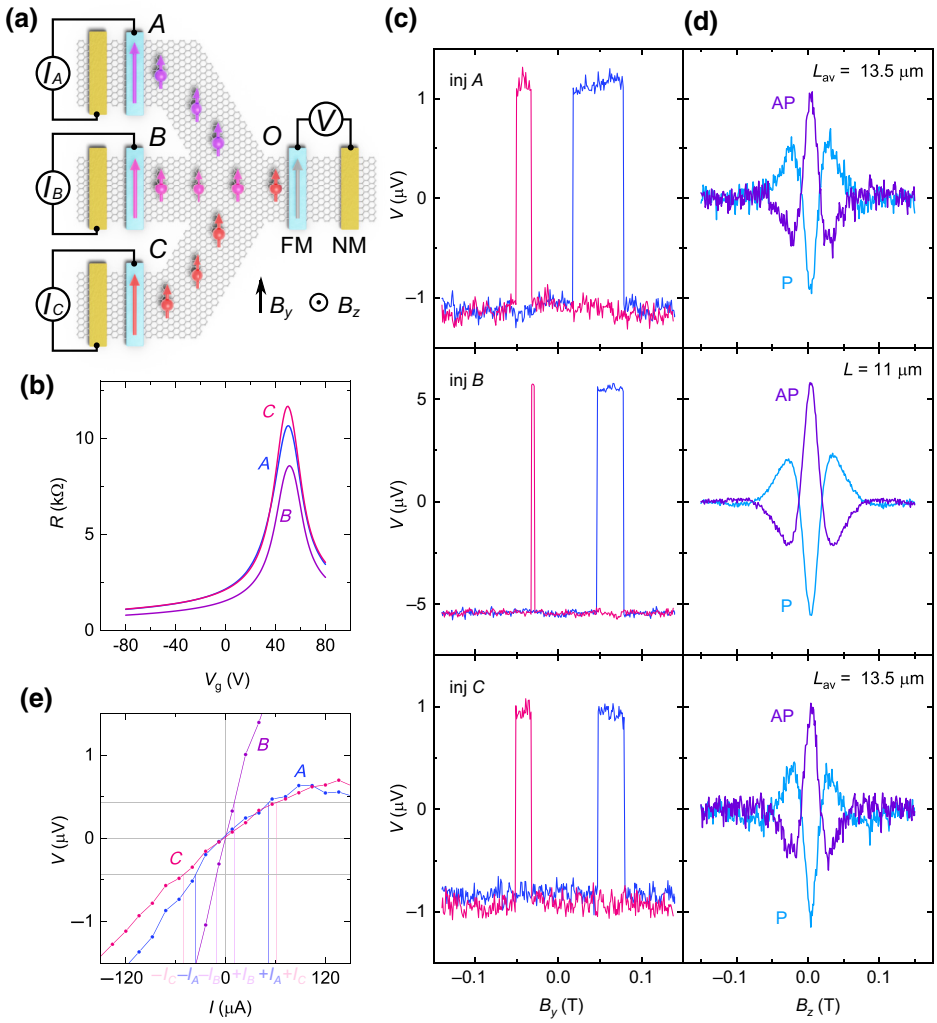

FIG. 2. Spin communication in the graphene circuit. (a) Schematic with a measurement geometry for characterizing spin transport in graphene branches *A*, *B*, and *C*. (b) Gate dependence of the graphene channel resistance in each branch. (c),(d) Spin-valve and Hanle spin-precession measurements for each channel with inputs from *A*, *B*, and *C* with magnetic field sweeps in B_y and B_z directions, respectively. Measurements are performed for parallel (P) and antiparallel (AP) magnetic orientations of input and output ferromagnetic contacts. Measurements are performed with a bias current of $I = -200$ μA. (e) Bias dependence of the spin-valve signal magnitude (V) for each injector. Gray horizontal lines represent the selected output voltage level (limited by the nonlinearity observed for injectors *A* and *C*), and corresponding vertical lines determine the values for positive and negative bias currents used in majority logic measurements. All the measurements are performed at room temperature.

spin-signal magnitude as a function of bias current for each channel, as shown in Fig. 2(e). We observe nonlinearity in the bias dependence, which is a common feature seen in nonlocal spin valves with ferromagnetic tunnel contacts. Its origins can be related to thermal effects, magnetic proximity, spin drift, or energy-dependent spin-resolved density of states at the Gr/FM interface [39–42]. These effects can be minimized through optimization of the tunnel barrier fabrication, e.g., via the incorporation of few-layer hBN to improve spin accumulation and reduce adverse proximity effects between the FM layer and graphene [37]. In the present device, this nonlinearity results in different values of bias current required to achieve the same absolute value of spin voltage at negative and positive polarities. By choosing a desired output voltage level [marked by the gray horizontal lines in Fig. 2(e)], we determine the positive and negative values of the bias currents, I_A, I_B, and I_C, to be used for the following bias-controlled spin logic measurements. The output spin-voltage magnitude is sufficient for the present spin logic operations; however, it can be further enhanced by downscaling the graphene spin-circuit dimensions and improving the spin polarization of the ferromagnetic contacts by using hBN [43], unconventional oxide [44] tunnel barriers, or van der Waals magnets [45,46] (see Supplemental Material Note 4 for quantitative estimations and further discussion [31]).

B. Spin mixing in a two-input spin circuit

Mixing of spin currents is one of the basic spin logic operations, allowing fan-in and fan-out spin signals and multiple information processing operations to be performed. As spin currents decay over the spin-diffusion length, it is crucial to investigate how they combine and divide in a multiterminal graphene spin circuit. We realize the spin-addition and -subtraction operations using the simultaneous injection of spin currents from two different ferromagnetic input terminals [Fig. 3(a)]. Figure 3(b) shows the spin-valve signals obtained separately in two different branches (ΔV_A and ΔV_B) of the device, and a resulting output spin-valve signal with both inputs working at the same time ($\Delta V_A + \Delta V_B$). The magnitude of the output spin valve in this case represents the sum of the spin signals from both inputs, demonstrating a linear spin-addition regime.

Alternative to using a global external magnetic field to control the injected spin-polarization orientation by switching the magnetization of ferromagnetic input electrodes, the polarity of injected spins can be selected by applying positive or negative bias currents to the individual inputs. In this method, the magnetization of all contacts remains fixed throughout the measurement, whereas the sign of the bias current determines whether the inputs work in the spin-injection or spin-extraction regimes. This approach is beneficial, since the application of the magnetic field is not a viable option for integrated spin circuits, and it does not allow all possible logic states of the device that has more than two magnetic inputs to be prepared. Complete control over the magnetization of each individual injector in the future may be achieved by incorporating spin-transfer-torque (STT) or spin-orbit-torque (SOT) modules that can switch FM magnetization electrically, in a similar fashion to STT or SOT magnetic random-access memory cells. When using the bias current to control the state of each injector, we define the input state of 1 as the application of the positive bias current leading to spin-up injection and the state of 0 as the application of the negative bias current leading to the spin-down injection (practically achieved by spin-up extraction). These operations result in spin mixing and an output spin-dependent voltage, as shown in Figs. 3(c) and 3(d), from SPICE simulation and experimental results, respectively, for different input states defined by bias currents as a function of time [Fig. 3(e)]. The output of this two-input spin logic device shows three stable states corresponding to the regimes where both input magnets inject spin-up currents (11), spin-down currents (00), or opposite spin currents (01 and 10). For the same logic states at both inputs, the same type of spin current is injected in the channel, which adds up to provide a high-voltage state at the output. On the other hand, when the inputs inject opposite spin currents, they get cancelled out,

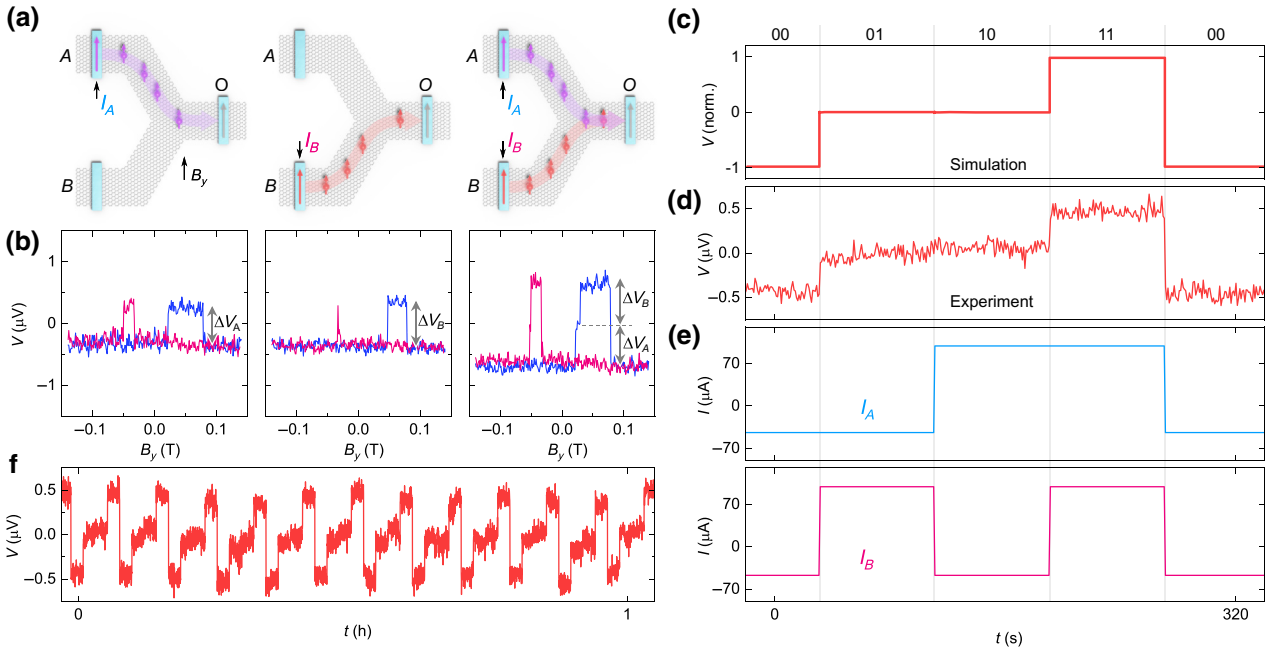

FIG. 3. Spin mixing in a two-input fan-in device. (a),(b) Spin-valve signals obtained using individual inputs A and B, and spin-addition or spin-cancellation operations performed by simultaneously injecting spins from both branches of the device. (c),(d) Output spin voltage at the detector as a function of time; panels show spin-circuit-based simulation and experiment, respectively. (e) Sequence of the applied bias currents to the two input contacts A and B. (f) Device performance over several cycles. All the measurements are performed at room temperature.

resulting in a zero output voltage. This resembles the conventional negated exclusive OR (XNOR) logic operation, with output 0 and 1 logic states being zero and nonzero voltages, respectively; however, the spin XNOR operation in Fig. 3 has not two but three output states, and therefore, distinguishes between 11 and 00 states, according to the output voltage sign. Also, the output voltage sign can be inverted by reversing the magnetization states of all injectors or the detector before the experiment (see Fig. S2 in the Supplemental Material [31]). The stability of the spin-addition device operation is demonstrated in Fig. 3(f), where the output voltage over multiple operation cycles is shown. Such fan-in and fan-out [16] geometries show that spin current can be precisely controlled by the spin-injection bias and spin resistances of each graphene branch in a circuit. These experiments demonstrate the possibility to define electrically the spin-input states of a spintronic logic device, which is a vital ingredient for developing spin-based logic circuits.

C. Spin-majority logic operation

Finally, after establishing the essential ingredients, such as spin-communication and spin-addition functionalities, we investigate the all-electrical spin-majority logic operation using three inputs of the device simultaneously [Fig. 4(a)]. According to the truth table of the majority gate [Fig. 4(b)], its output should be 1 if at least two of the three inputs are in the 1 state; otherwise, the output is 0. Thus, a majority logic gate represents digital functions on the basis of majority decisions and can be reprogrammed by fixing one of the three input variables to 0 or 1, such that it can function as an AND or OR gate for the remaining two inputs. The negative and positive bias currents are used to represent the 0 and 1 states of the inputs, creating spin currents of opposite polarization in the graphene circuit (spin down and spin up, respectively). Magnetization of the input and output FMs are aligned in the same direction, and the bias-current magnitude is chosen from the bias-dependence calibration [Fig. 2(e)]. Figure 4(c) shows spin-circuit-model-based SPICE simulation results of the three-input spin-majority device, which provide insights into the underlying mechanisms of the experimental results presented in Fig. 4(d). Both simulations and experiments use a sequence of currents for the three inputs, as shown in Fig. 4(e), which goes through all possible logic combinations. The output signal switches between four stable voltage levels; two levels correspond

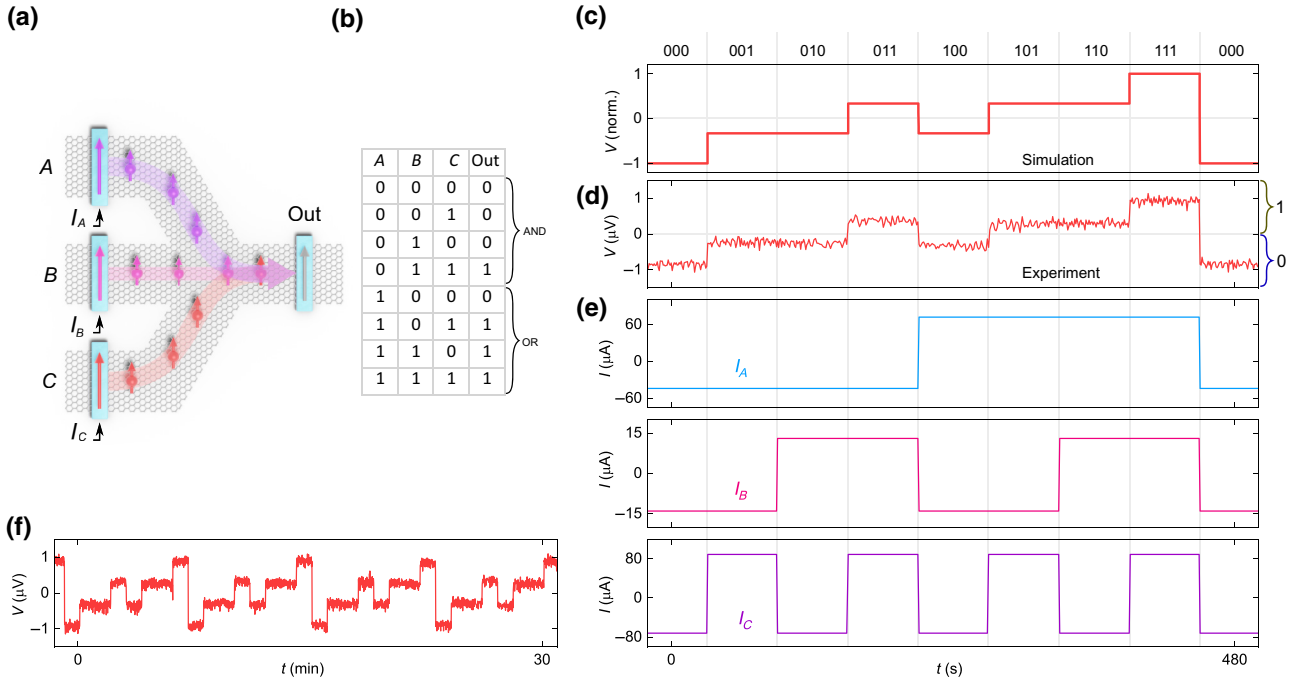

FIG. 4. Spin-majority logic operation with the three-input fan-in device. (a) Schematic of the spin-majority logic device, where all three spin inputs (A, B, C) are used simultaneously, and the majority of the injected spin polarizations define the nonlocal output (O) spin voltage. (b) Truth table for a majority gate. Output is true when at least two of the inputs are true. By fixing any of the inputs as 0 or 1, the output for the remaining two inputs represents an AND or OR operation, demonstrating the reconfigurability of the gate. (c),(d) Spin-circuit-model-based simulation and experimental realization, respectively, of the spin-majority logic device achieved by applying a sequence of the pulse bias currents to all inputs [I_A, I_B, I_C, panel (e)] as a function of time to probe all possible logic states. $+I$ results in spin injection and $-I$ leads to spin extraction. (f) Device performance over several cycles. All the measurements are performed at room temperature.

to the stronger majority cases (111 and 000) and the other two levels correspond to weaker majority cases (011, 101, 110 and 001, 010, 100). When charge-based background contributions are eliminated, we can add a comparator and label the output as logic 1 when the resulting nonlocal spin-voltage signal is positive; otherwise, it is 0. From this convention, it is clear to see that the resulting signal indeed complies with the majority gate truth table and that the gate can be reprogrammed to realize AND or OR operations by fixing any of the inputs as 1 or 0, respectively, when the input magnets are parallel to the output magnet. The majority logic device operation can also be controlled by the magnetic field; however, this approach does not allow all possible combinations of the input states to be probed, as the magnetization switching order is determined by the individual coercive fields of the FMs (see Fig. S3 within the Supplemental Material [31]). However, this approach can be used to achieve the inversion of the output signal (see Fig. S4 within the Supplemental Material [31]) when the input magnets are antiparallel to the output magnet, thus allowing NAND and NOR functions to be realized. The three-input spin-summation operation is stable over several cycles, as shown in Fig. 4(f), demonstrating that such graphene integrated circuits are robust and promising building blocks for spin logic applications.

III. SUMMARY AND OUTLOOK

We demonstrate a prototype all-electrical multifunctional spin logic device operating with pure spin currents in an integrated graphene spin circuit at room temperature. This is made possible by fabricating multiterminal spin circuits using large-area CVD graphene channels and demonstrating fan-in spin-addition and -subtraction operations with pure spin currents. The all-electrical operations are achieved by using tunable bias currents to control individual spin inputs of XNOR and SMAJ functions, which can also be reconfigured to perform (N)AND and (N)OR operations. To understand the underlying mechanisms of the experimentally realized spin logic devices, we use spin-circuit-model-based multiphysics simulations in SPICE. The simulations agree well with the experimental results and provide insights into spin-current addition and cancellation, leading to multistate output. Binary-like weighted summation is discussed in charge-based architectures where weighted charge currents are added or subtracted in the context of in-memory computing [25]. Our spin-based summing unit expands this function with additional dimensions due to the vector nature of spin instead of the scalar nature of charge. With this, the magnetic inputs of the device can be designed with an arbitrary alignment of their polarization axes on the 2D plane, allowing for nonbinary weights [15,16]. These results can open the door for next-generation spin-based information technology with promising applications in logic-in-memory architectures and non-von Neumann computing paradigms [47–49].

IV. METHODS

A. Fabrication of devices

Large-area CVD graphene (from Grolltex Inc.) is grown on Cu foil and transferred onto a 4-inch wafer with 285-nm SiO_2 on n^{++}Si substrate, with prefabricated alignment markers. The graphene circuits are patterned by electron beam lithography (EBL) and oxygen plasma etching. Both the nonmagnetic Ti(10 nm)/Au(80 nm) and ferromagnetic (TiO_2/Co) tunnel contacts are defined using two EBL processes, followed by electron beam evaporation of metals and lift-off processes. The ferromagnetic contacts are produced by electron beam evaporation of about 3-Å Ti in two steps, each followed by *in situ* oxidation in a pure oxygen atmosphere to form a TiO_2 tunnel barrier layer of about 6 Å. In the same chamber, we deposit 40 nm of Co, after which the devices are finalized by lift-off in acetone at 65 °C. See Supplemental Material Note 2 for a discussion of the fabrication and measurement features of large-area graphene-based multiterminal spin logic devices [31,50–52].

B. Spin- and charge-transport measurements

The final devices are wire-bonded and measurements are performed inside a cryostat under vacuum conditions at room temperature with a magnetic field and a sample rotation stage. In the spin-majority logic device measurements, individual Keithley 6221 current sources are connected to each of the three input FM (TiO_2/Co) electrodes to apply bias currents, and the nonlocal output voltage is detected by a Keithley 2182A nanovoltmeter; the gate voltage is applied using a Keithley 2400 source meter. The three-terminal resistance of FM contacts is in the range of 1–2 and 0.3–1 kΩ for NM Ti/Au contacts, whereas graphene exhibited a sheet resistance of 565 Ω. An application of the gate voltage between the n^{++}Si substrate and graphene across the 285-nm oxide layer of SiO_2 is used to quantify the carrier concentration in graphene. The spin logic measurements are performed at zero gate voltage, which corresponds to hole doping with the carrier density of $n = -3.8 \times 10^{12}$ cm^{-2} and field-effect mobility of $\mu = 2900$ cm^2/Vs. See Supplemental Material Note 3 for details of electron- and spin-transport parameters of large-area graphene devices [31].

C. Simulation

The SPICE model for the spin-majority gate is constructed by dividing the structure into several sections and representing the sections with corresponding physics-based spin-circuit models for nonmagnetic graphene and magnetic TiO_2/Co contacts. The spin-circuit models

consist of four components: one charge and z-, x-, and y-polarized spins. The boundary conditions for charge and spin terminals are assigned according to the experimental configurations. The charge terminals are connected to current sources for the input magnets, while the spin terminals are grounded to consider spin absorption within the magnets. The charge terminal of the output magnet is open circuit, and the spin terminals are ground. The boundary conditions for spin terminals in the graphene channel are all open circuit. For the input branches in the graphene channel, the boundary terminals for charge are ground so that the charge current injected through the input magnets can complete their paths. For the output branch of the graphene channel, the boundary terminal for the charge current is open. We apply pulse-current sources to the input magnets and observe the open-circuit charge voltage at the charge terminal of the output magnet in the transient simulations done in HSPICE.

Data that support the findings of this study are available from the corresponding authors on reasonable request.

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D.K. fabricated and measured the graphene spin logic devices and circuits. A.M.H, B.K., and B.Z. helped with device fabrication and optimization. D.K. and S.P.D conceived the idea and designed the experiments, analyzed and interpreted experimental data, and compiled the figures. S.S and S.D performed the spin-circuit simulations. D.K., S.S., S.D., and S.P.D wrote the manuscript with input from all co-authors. S.P.D. supervised the research project.

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