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An 800 W Four-Level Supply Modulator for Efficient Envelope Tracking of RF Transmitters

Connor Nogales, Zoya Popović, Gregor Lasser

***Abstract*—Modern RF communication and electronic warfare applications require systems capable of amplifying signals with high bandwidths and high peak to average power ratios (PAPR). One technique used to meet these demands is supply modulation also known as envelope tracking where the drain voltage of the power amplifier (PA) is dynamically changed according to the signal envelope. The limiting factor with supply modulation is typically the efficiency and switching speed of the power converter. The power converter must also be capable of producing high power levels when supplying an array of PA units or a single high power transmitter. This paper demonstrates the design and characterization of a four-level discrete supply modulator with a peak output power of 800 W operating at a maximum switching frequency of 10 MHz. The modulator switches between four discrete voltages from 10 to 20 V. GaN on silicon HEMT power transistors are selected for the switching devices after conducting a survey of commercially available silicon MOSFET, silicon-carbide MOSFET, and GaN on silicon power transistors. Trace interconnect models are developed to achieve accurate predictions of the time domain waveforms, including ringing at the switching edges. These interconnects are first analyzed using full-wave electromagnetic simulations, and then modeled with RLC networks suitable for time domain simulations. For a test signal with equal duty cycle between the four levels, an efficiency greater than 94.0% is demonstrated for average output powers exceeding 91.6 W. When tracking the envelope of an 8 MHz 64-QAM signal, an average efficiency of 93.5% is achieved providing a peak power of 800 W.**

***Index Terms*—Envelope tracking, GaN, Multi-Level Converter, Power Amplifier, Supply Modulation.**

I. Introduction

Modern communication and electronic warfare systems require power amplifiers (PAs) to amplify modulated signals with a high peak to average power ratio (PAPR). Complicated modulation formats are often used for efficient spectrum utilization. However, this introduces a varying envelope signal with a high PAPR. This changing signal envelope is at odds with achieving high overall power efficiency of a classical PA since the amplifier spends significant time operating at power levels lower than the peak, referred to as "backoff". To improve efficiency in backoff, various techniques are used. For example, load modulation in PAs such as Doherty [1], [2], [3] and outphasing amplifiers [4], [5] provide backoff efficiency enhancement by adding a second power amplifier at the carrier frequency. Another downside to these techniques is that they utilize lossy and band-limiting combining structures. The load modulated balanced amplifier (LMBA) can achieve large bandwidths with good backoff efficiency [6], [7]. However, the LMBA requires a third RF power amplifier which adds significant complexity. An alternative to load modulation is supply modulation where the supply voltage of the PA is dynamically changed based upon the instantaneous power of the signal [8], [9], [10], [11]. A distinct advantage of supply modulation is that the technique can be applied to a PA at any RF carrier frequency and is therefore carrier agnostic, provided the supply modulator (SM) and PA have comparable output power levels. Furthermore, the design of the individual RF PA is greatly simplified as compared to a load-modulated PA. In addition, supply modulation can be implemented in conjunction with any of the load modulation techniques previously mentioned in order to further enhance

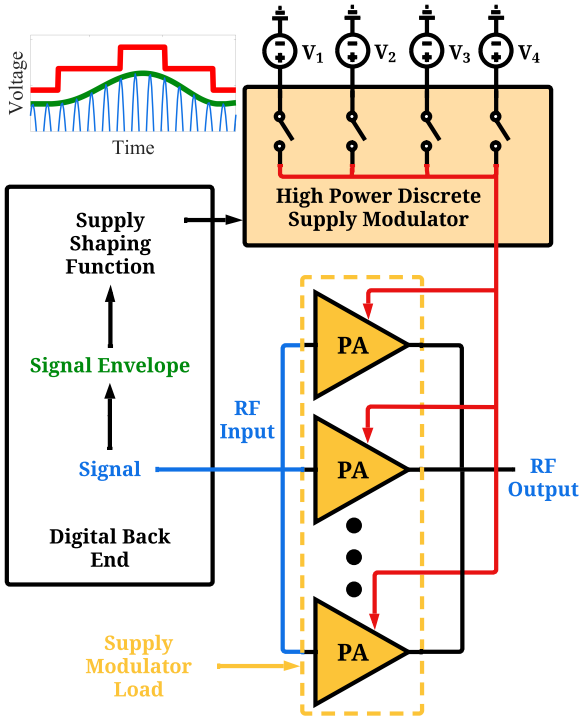

Fig. 1: Block diagram of a high power supply modulator simultaneously feeding several power amplifiers in parallel. The signal envelope (shown in green) is digitally processed through a shaping function which determines the switch timing and output waveform of the supply modulator.

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the backoff efficiency, as demonstrated in [12], [13], [14]. The primary bandwidth limitation of supply modulation comes from the envelope signal bandwidth which exceeds the RF signal bandwidth at least by a factor of three [15]. An effective supply modulator must have a large enough bandwidth and slew-rate to track the signal envelope accurately.

One of the major challenges with supply modulation is designing a high bandwidth (fast switching) and highly power efficient supply modulator. Continuous supply modulators (CSM), utilizing buck converter topologies have been demonstrated with switching frequencies up to $865\,\mathrm{MHz}$ [16], [16]–[22]. These supply modulators must switch at frequencies a few times greater than the signal envelope bandwidth [15] and the efficiency of all switch-based power supplies drops linearly with frequency. Therefore, it becomes challenging to track high bandwidth signals efficiently using a continuous supply modulator. An alternative to CSM are discrete supply modulation (DSM) architectures such as multi-level converters (MLC) [23]–[32] which switch between several discrete voltage levels. The primary advantage of DSM is that it reduces the number of switching instances as compared to CSM while still providing substantial improvements in PA efficiency. This boosts the efficiency of the supply modulator and enables accurate tracking of higher signal bandwidths, at the expense of some distortion which can be corrected through digital pre-distortion [26]. Increasing the number of voltage levels can improve the PA efficiency, however the supply modulator efficiency might suffer due to a higher number of switching instances. A comparison of using different numbers of voltage levels is given in [33], [34], and in this work we choose 4 levels.

Most DSM PAs demonstrated to date are limited to tens of watts of power provided by the dynamic supply. For applications such as radar and arrays of multiple PAs [35], [36], higher-power DSMs are required and some higher-power examples are reviewed in Table I. Supply modulation of multiple PAs, e.g. in an active transmit antenna array, is advantageous since it improves system efficiency, while reducing the thermal load on the RF PA element, which is often the limiting factor in array performance [37]. Furthermore, when an array is supplied from a single power converter there is minimal complexity added to the system. Monolithic microwave integrated circuit (MMIC) supply modulators [21], [16], [17], [23], [26] can achieve relatively high switching frequencies and efficiencies, however the peak output powers significantly greater than $20\,\mathrm{W}$ have not been demonstrated. Higher output powers can be achieved with hybrid topologies [25], [28], [20] however, this typically comes at the cost of switching speed. Therefore, if high power is a priority over switching speed, the hybrid topology is favorable. The goal of this paper is to demonstrate the design and experimental results for a high-power four-level SM with an output power approaching a $1\,\mathrm{kW}$, which can supply modulate a single high-power PA, several PAs (50–100 W each) in a power combiner, or a large number of medium-power (10 W) PAs in a phased array.

The high power multi-level converter (HPMLC) presented in this work is demonstrated to track an $8\,\mathrm{MHz}$ 64-QAM signal with a maximum switching frequency of $10\,\mathrm{MHz}$ and a peak output power of $800\,\mathrm{W}$. To the best of the authors knowledge, this significantly exceeds the power and switching speed of the highest published peak output power DSM of $500\,\mathrm{W}$ while tracking a $400\,\mathrm{kHz}$ envelope signal presented in [28]. The paper is organized as follows: first, the transistor choice for the DSM is presented through a survey of trade-offs in high power transistors. Next, the design and implementation of the HPMLC is shown, including model generation for the trace interconnects. The results of HPMLC characterization in terms of its efficiency and ringing performance using a four-level equal duty cycle waveform are then presented. Finally, tracking signal results are shown on the example of the envelope of a 64-QAM signal with an $8\,\mathrm{MHz}$ bandwidth, when the DSM is loaded with both a purely resistive and an RC load emulating a high-power RFPA, as shown in detail in [38], or an array of multiple PAs, for peak powers ranging from $25\,\mathrm{W}$ to $800\,\mathrm{W}$.

II. High Power Transistor Survey and Comparison

The most critical component of a HPMLC design is the choice of the switching transistor. It is desirable to use a transistor with a low on-state resistance (R_{on}), minimal input and output capacitance (C_{in}, C_{out}), and small rise/fall times ($<10\,\mathrm{ns}$). Furthermore, in high power, low voltage applications, a high maximum drain current ($I_{\mathrm{d-max}}$) is necessary. Unfortunately these parameters are often at odds with each other. For instance, a low R_{on} with high $I_{\mathrm{d-max}}$ can be obtained by stacking many devices in parallel, however this increases the capacitance and lowers the switching speed of the device.

A survey and comparison of commercially available high power transistors is performed to assist in switching device choice. This study examines silicon (Si) MOSFET, silicon carbide (SiC) MOSFET, and gallium nitride (GaN) HEMT technologies while specifically targeting devices with low C_{out} and R_{on}. The R_{on} is plotted against $I_{\mathrm{d-max}}$ for each surveyed device in Fig. 2a where the area of each dot is proportional to the device C_{out}. In addition, the C_{out} is plotted against $I_{\mathrm{d-max}}$ in Fig. 2b where the area of each dot is proportional to the device R_{on}. The surveyed devices all have breakdown voltages greater than $25\,\mathrm{V}$ which is consistent with the required drain supply voltage of GaN HEMT power amplifier devices. All the values of the survey were obtained directly from the manufacturer's device data sheet.

More detailed specifications of the devices used in this comparison are given in Table II in the Appendix.

From Fig. 2 it is apparent that SiC MOSFET devices consistently have the smallest C_{out}, however they suffer from a relatively large R_{on}. The small C_{out} of SiC devices is partially a result of the capacitance of these devices being specified at very high voltages ($>600\,\mathrm{V}$). The Si MOSFET devices are competitive with GaN both in terms of C_{out} and R_{on}, however the intrinsic body diode built into the MOSFET structure would result in reverse conduction if used in a multi-level converter. A common approach to preventing reverse conduction due to the body diode is to place an external

TABLE I: Key specifications of state of the art continuous and discrete supply modulators with peak output powers up to 500 W in GaN and MOSFET technologies

Type	Technology	Package	Peak Pout (W)	Efficiency (%)	Test Signal/Peak Switching Frequency	Ref.
Buck Converter	GaN	MMIC	16	72.5	NA/400 MHz	[16]
Buck Converter	GaN	MMIC	10	> 90	3 MHz envelope/40 MHz	[17]
Buck Converter	GaN	Hybrid	50	> 90	NA/1 MHz	[18]
Buck Converter	GaN	Hybrid	68	92.3	20 MHz envelope/25 MHz	[19]
Multi-Level Buck Converter (3 level)	GaN	Hybrid	115	> 90	20 MHz envelope/25 MHz	[20]
Buck Converter	GaN	MMIC	> 7.5	> 80	NA/865 MHz	[21]
MLC (4 level)†	GaN	MMIC	3.5*	88.2	20 MHz LTE/40 MHz***	[23]
MLC (4 level) with Linear Regulator	GaN	Hybrid	40	75	5 MHz envelope/1 MHz	[24]
8 Level Power DAC	GaN	Hybrid	159	84.5	10 MHz LTE/NA	[25]
8 Level Power DAC†	GaN	MMIC	20	85-95	20 MHz LTE/NA	[26]
MLC (3 level) with Linear Regulator	MOSFET	Hybrid	50	75.5	1 MHz sine wave/100 kHz	[27]
Multi-Level Buck Converter (2 level)	GaN	Hybrid	500	93	400 kHz envelope signal/1 MHz	[28]
MLC (6 level) with Linear Regulator	MOSFET	Hybrid	50	79.7	300 kHz sine wave/NA	[29]
MLC (2 level)†	GaN	Hybrid	62	82-92	40 MHz OFDM/100 MHz	[30]
MLC (3 level)†	GaN	Hybrid	20.6**	NA	120 MHz signal/400 MHz***	[31]
MLC (4 level)†	**GaN**	**Hybrid**	**800**	> 94	**8 MHz 64-QAM signal/10 MHz**	**This Work**

*average Pout, **average Pout derived from data in paper, ***derived from minimum pulse width, †Individual dc source voltages were generated externally using bench power supplies

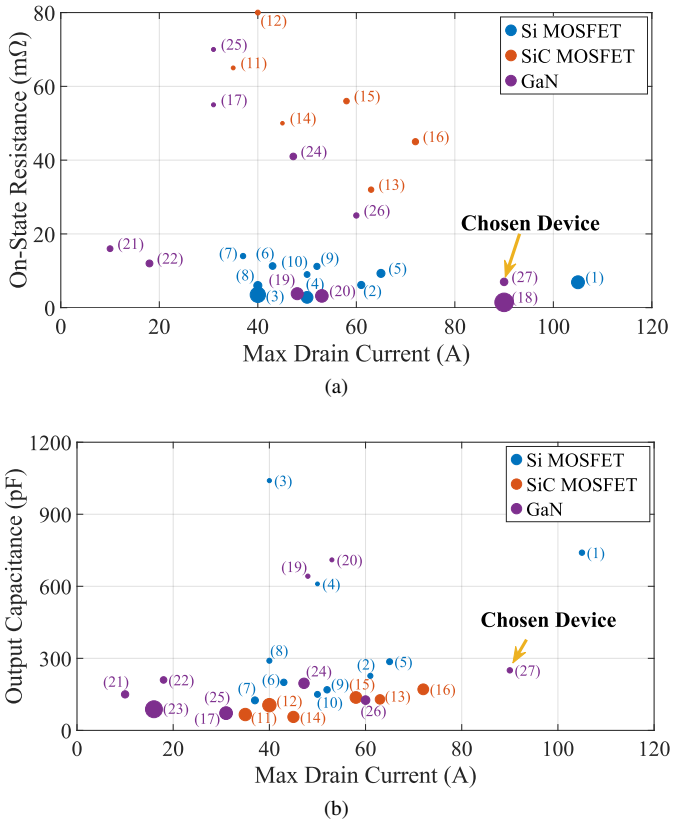


Fig. 2: (a) On-state resistance vs maximum drain current and (b) output capacitance vs maximum drain current for commercially available transistors in MOSFET, SiC MOSFET, and GaN technologies. The size of each point in (a) is proportional to the device C_{out} and in (b) R_{on}. Numbers refer to TABLE II in the appendix.

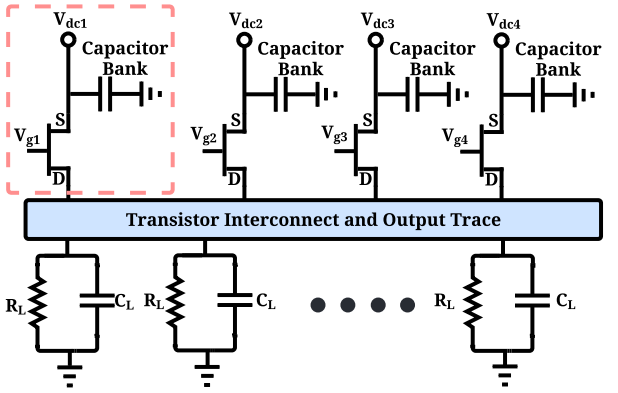
diode in series with all but the highest voltage level switch [31]. However, for high current applications this is not a feasible solution since the losses in a diode scale with current not voltage and substantially degrade the efficiency, making MOSFET structures an undesirable choice.

An alternative to Si MOSFET devices are e-mode GaN HEMTs which do not have an intrinsic body diode. Reverse conduction can however still occur in GaN devices when the gate-drain voltage exceeds the device threshold voltage and the drain-source voltage is negative. Therefore, in order to ensure that reverse conduction does not occur in a device that is intended to be biased off, it is necessary to make the nominal off-state gate voltage less than the lowest voltage level plus the threshold voltage. This enforces a limit on the voltage range of the HPMLC due to the minimum gate-source or gate-drain voltage that the device can tolerate as described in [39].

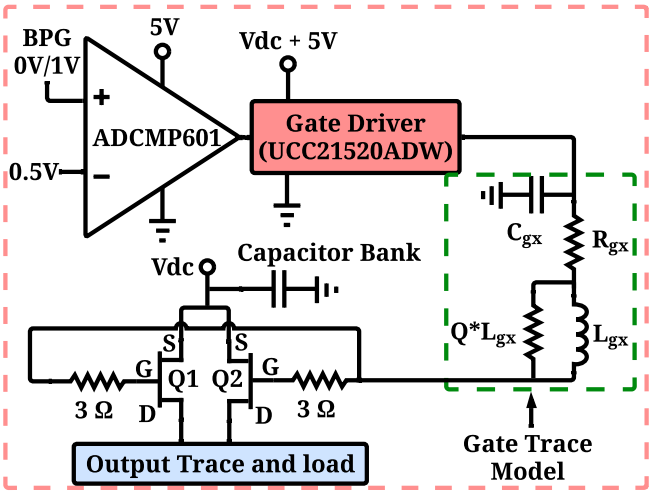
Ultimately, the chosen device is a GaN HEMT manufactured by GaN Systems (GS61008T) [40]. This device has a $I_{\text{d-max}} = 90\,\text{A}$, $C_{\text{in}} = 600\,\text{pF}$, $C_{\text{out}} = 250\,\text{pF}$, and $R_{\text{on}} = 7\,\text{m}\Omega$. Furthermore, the $V_{\text{gs,min}}$ of this device is $-10\,\text{V}$. This device meets the maximum drain current and voltage requirement while maintaining a low input and output capacitance relative to other surveyed GaN HEMTs. However, the primary motivation for choosing this device is the large minimum gate-source voltage that the device can tolerate which is $-10\,\text{V}$ and much larger than other GaN HEMTs and allows for a dynamic voltage range of the HPMLC of 10 V.

III. Supply Modulator Design and Simulation

The HPMLC switches between four dc voltage levels which are generated from external power supplies. A high-level schematic of the HPMLC is shown in Fig. 3a; the output is



(a)



(b)

Fig. 3: (a) Overview schematic of the high power multi-level converter. Each parallel RC circuit represents an individual PA being supply modulated. (b) Schematic of single switching cell highlighted in top left of Fig.3a. The gate trace is modeled as an RLC circuit with the values extracted from an EM simulation of the trace.

connected to one of four voltage levels by transistor switches. The load consists of N number of parallel RC circuits each of which represents an individual PA unit. The capacitor bank in Fig. 3a consists of four different capacitor packages and sizes with the aim of ensuring a stable dc input voltage to each of the GaN devices while the device is switching. A detailed explanation of the capacitor bank can be found in [39]. Fig. 3b shows an individual switching cell which is repeated for each of the four voltage levels. Each cell consists of two GaN transistors in parallel. A comparator (ADCMP601) is used to convert the 1 V switch control signal into the 5 V logic level required by the gate driver. The switch control signal is generated externally using a bit pattern generator (BPG) capable of generating synchronized pulses in multiple channels.

The criteria for choosing the gate driver is a required fast rise/fall time ($<$10 ns) and an output voltage large enough to fully turn on each of the switches (25 V). The chosen gate driver is manufactured by Texas Instruments (UCC21520ADW); it features a rise and fall time of 6 ns and 7 ns respectively with a peak output voltage of 30 V. Furthermore, the input is capacitively isolated from the output which allows the *on* and *off* output voltages of the gate driver to be set independently of the digital control signal. Thus, for each driver the *on* voltage is set to 5 V above each switch voltage level and the *off* voltage is set to 10 V in order to ensure that the gate-source voltage does not drop below the minimum of -10 V while avoiding reverse conduction.

The realized HPMLC shown in Fig. 4 is manufactured on a four-layer FR4 board and is populated with commercially available components. In order to maximize current handling and minimize parasitic capacitance and inductance, vias connect the top two layers of the output trace to form the signal path, and the bottom two layers are connected to form the ground path. The GaN switches are located under the bronze colored heat sink with a sheet of thermal interface material from Laird Technologies (A14692-30) that ensures good thermal contact between the top of the switches and the heat sink.

A. Reverse Device Operation

In a standard multi-level converter design, the source of each transistor is connected to the output. This topology creates a feedback in each device from the output to the gate through the gate-source capacitance. This can create undesired reverse conduction during voltage level transitions when turned-off devices experience a voltage spike on their gate from feedback through the gate-source capacitance. This effect where two devices are simultaneously biased on is known as shoot-through. From the LTspice model provided by the manufacturer, it is observed that the gate-drain capacitance is an order of magnitude smaller than the gate-source capacitance. Therefore, in order to investigate the effect that the size of the feed-back capacitor has on the switching

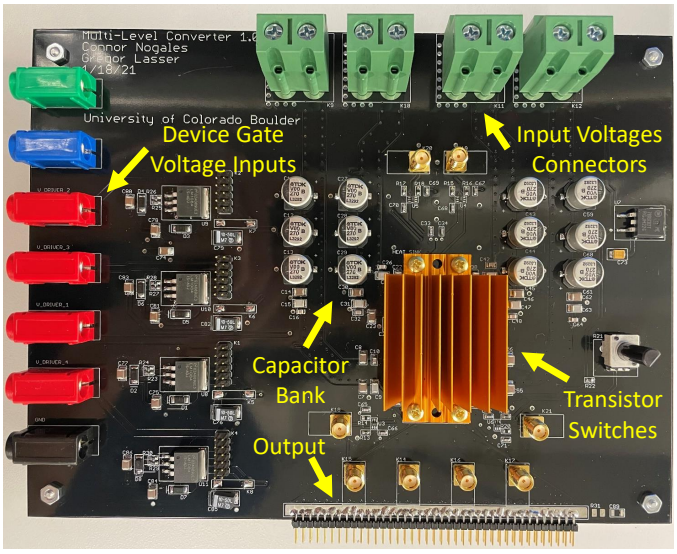


Fig. 4: Photograph of the high power multi-level converter.

waveform, the HPMLC is simulated in regular configuration with the source connected to the output, and in a reverse configuration with the drain connected to the output.

The simulated output voltage, ideal output voltage, and gate voltage of the highest voltage level (20 V) are shown in Fig. 5 with the gate and output traces modeled using the technique described in Section III-B below. In this simulation the HPMLC is switched from the second to highest voltage level (16.6 V) to the lowest level (10 V) and loaded with a medium power load of 1.25 Ω in parallel with 160 pF.

By examining Fig. 5 it is clear that when the devices are operated in standard configuration with the source connected to the output, shoot-through occurs when the device is switched to the lowest voltage level. This will distort the output waveform and degrade the efficiency of the converter. In contrast, the flipped configuration results in less feedback from the output to the gate and no shoot-through. Therefore, the HPMLC was designed with the devices implemented in reverse configuration with the drains connected to the output and sources connected to the input dc voltage as seen in Fig. 3a.

B. Trace Modeling

The ringing that occurs upon each voltage level transition limits the switching speed of the converter and mixes with the RF signal of the PA. This creates side-bands in the spectrum, and degrades the linearity of the PA [41]. The ringing in the HPMLC is created due to interactions between the transistor capacitance and the output trace parasitics. Attempts were made to model the output trace as an RLC network in [39], however, the output and gate trace RLC modeling was too simple and did not accurately predict the output voltage waveform. The expanded RLC output and gate trace models used in this work accurately predict time domain simulations.

The output trace was EM simulated in AWR's Axium 2.5D method of moments (MOM) solver from dc to 2 GHz. A port was placed at the location of each transistor and the output,

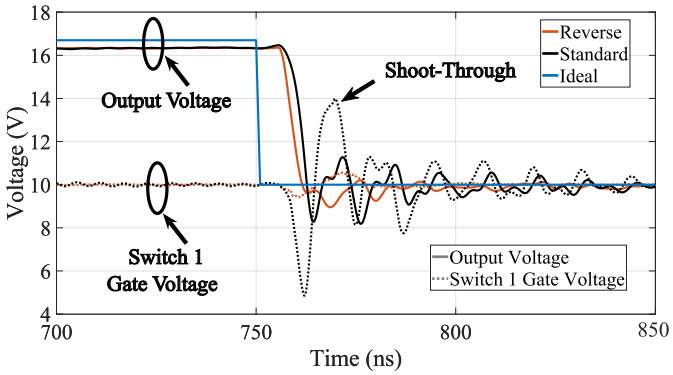


Fig. 5: Simulated time domain waveforms of the output and switch 1 gate voltages for standard and reverse transistor orientations when transitioning from the switch 2 to switch 4 with an RC load of (1.25 Ω || 160 pF). Each respective switch voltage is $V_{\mathrm{dc1}} = 20V$, $V_{\mathrm{dc2}} = 16.7V$, $V_{\mathrm{dc3}} = 13.3V$, $V_{\mathrm{dc4}} = 10V$ with the gate turn-on voltage of each switch set to be 5 V above the switch dc voltage.

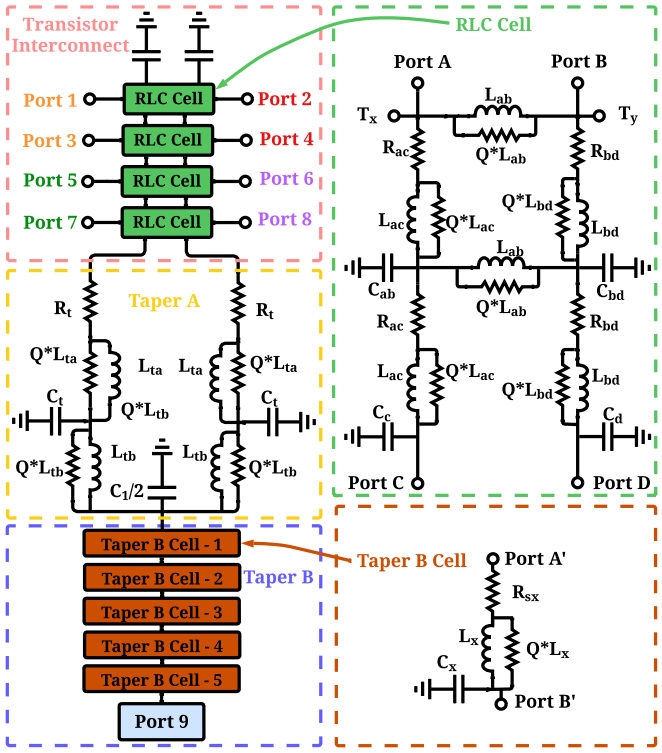
resulting in nine total ports. The aim of this model was to capture the mutual resistance, inductance, and capacitance between each individual transistor and the output. Since the simulated frequency domain S-parameter data cannot be used in time domain simulations and automatic extraction of equivalent models did not yield accurate results, the equivalent RLC circuit shown in Fig. 6a, with its physical port and section locations shown in Fig. 6b was fit to the simulation results.

The equivalent RLC circuit is split into three parts. Starting from the top of Fig. 6b the transistor interconnect is highlighted in pink, followed by taper A which is a bottle neck shaped trace highlighted in yellow, and finally at the bottom is taper B which is a trapezoid shaped trace highlighted in purple. Each of these sections is modeled with series resistances, shunt capacitances, and series inductors in parallel with resistors as shown in Fig. 6a. The value of the parallel resistor is the product of the corresponding inductance and a separate Q-factor variable. The Q factor is assumed to be the same across the network in order to reduce the number of variables. The finite Q of the inductors help the RLC network to match the frequency behavior of the simulated trace, including resonances that occur. The extraction of the RLC values was obtained through two simultaneous goal functions between the EM model and RLC model from dc to 600 MHz. The first was fitting the S-parameters between the two models in a 50 Ω environment. The second was ensuring that the dc resistance between ports 1 and 9 matched the simulated dc resistances when ports 2 - 8 are left open.

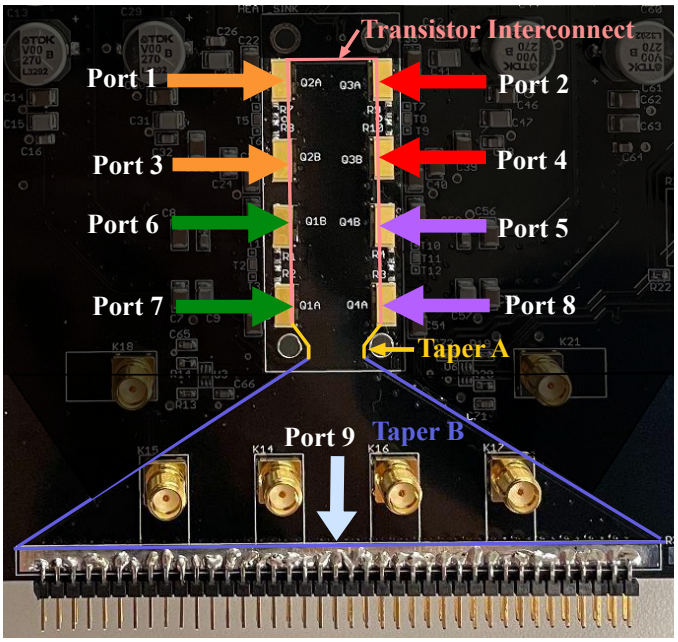
Since the dc resistance of the trace is critical to accurately predict the dc losses of the HPMLC, it was weighted 15 times higher than the S-parameter goal function. By taking advantage of the vertical symmetry of the output trace, using the same Q value for each parallel RL component, and assuming each of four RLC cells in Fig. 6a are identical, the total number of variables was reduced from 120 to 25. In taper B a progressive increase in capacitance values and decrease in inductance values was enforced as the taper moved to larger widths. The interconnects between the gate drivers and the external gate resistors of the switching devices are modeled in a similar fashion using a single RLC network as shown in Fig. 3b. These traces are individually EM simulated for each driver to switch interconnect, and the RLC model is fit to this data using the same cost function as for the output trace.

The simulated output voltage of the HPMLC is compared to a measurement in Fig. 7 showing the effect of the trace modeling. The converter switches between four equally spaced voltage levels ranging from 10 to 20 V with equal duty cycle and a switching frequency of 4 MHz. The load is a parallel resistor-capacitor combination with values of 1.25 Ω and 160 pF. In simulation, the gate drivers are implemented as ideal voltage sources with a rise/fall time consistent with the driver data-sheet. The dead time in simulations is 2 ns, consistent with the measurements. For the temperature dependent transistor models, the thermal resistance to ambient is modeled as 3.5 °C/W. The bypass capacitor bank is modeled to include the series inductance and resistance parasitics taken from the data-sheets of each capacitor.

The gate and output traces have a significant effect on the



(a)



(b)

Fig. 6: (a) Schematic of RLC output trace model and (b) associated physical location of the ports in the output trace. The trace is split into three parts: the transistor interconnect highlighted in pink, taper A highlighted in yellow, and taper B highlighted in purple

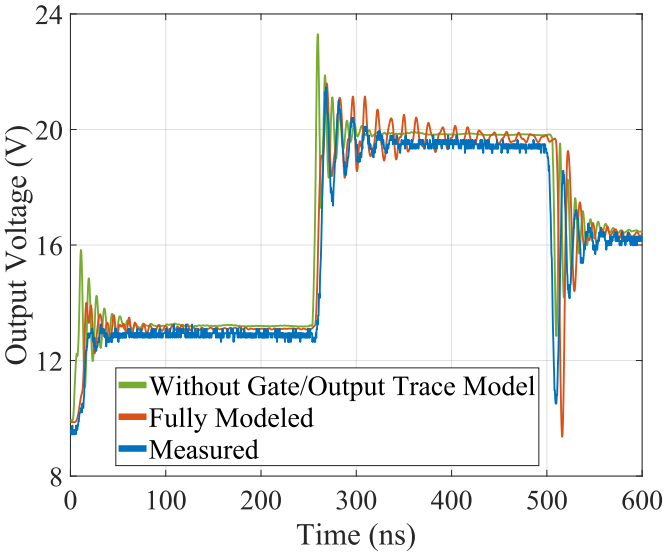


Fig. 7: Simulated HPMLC output voltage comparing measurement and simulation using different modeling detail on the interconnects using an RC load of (1.25 Ω || 160 pF).

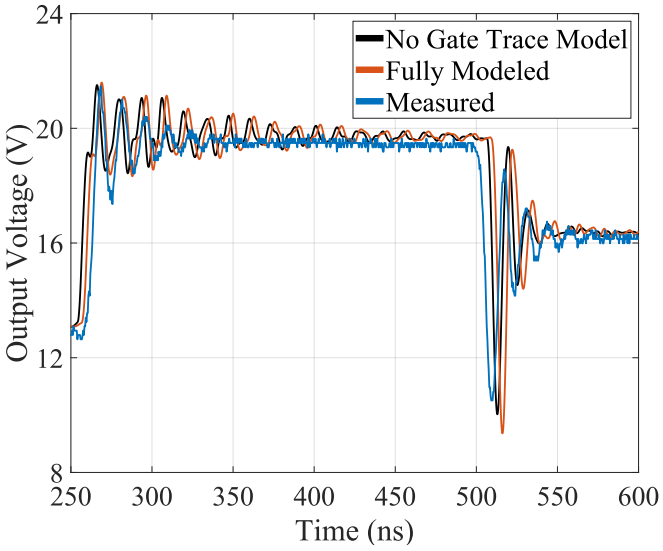


Fig. 8: Simulated HPMLC output voltage comparing measurement and simulation highlighting the effect of the gate trace using an RC load of (1.25 Ω || 160 pF).

ringing of the waveform. Fig. 7 shows that if the traces are not included in the model, the ringing overshoot, frequency, and duration is not accurately predicted. In this paper, the gate and output trace RLC modeling complexity is greatly expanded over the output trace modeling in [39] and results in an significant accuracy improvement of the predicted waveform. If the gate trace modelling is not included, the result is shown in Fig. 8 and compared with the full model and measured data. It can be seen that the main contribution of the gate trace is a phase shift which results in a better prediction of the waveform in the rise region up to 20 V.

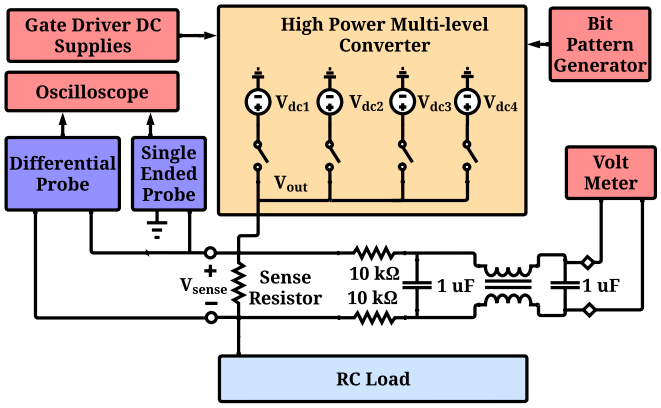


Fig. 9: Test setup block diagram. The current is measured using a differential probe across the sense resistors. The filtered dc component of the voltage drop is used to calibrate the offset of the differential probe.

IV. Measurements

A. Test Setup

The measurement setup is shown in Fig. 9. The bit pattern generator is programmed in MATLAB to output 1 V rectangular pulses from several channels simultaneously with rise/fall times of approximately 70 ps. The BPG is used to independently control each gate driver on the HPMLC and apply dead times. The dc voltage supplies for the gate drivers and four voltage levels are supplied externally. The output voltage waveform is captured using an oscilloscope with a sampling rate of 2.5 Gs/s. The current waveform is measured using a differential voltage probe placed across the sense resistor shown in Fig. 9. The current waveform is filtered with a common-mode choke and 1 µF capacitors, and the resulting dc component of the current is measured using a voltmeter. The current waveform measured by the differential probe is then offset such that its average value is equal to the dc current measured by the voltmeter. The sense resistor value is calibrated with the HPMLC supplying 10 V dc and taking the current reading from the dc power supply in conjunction with the voltage across the sense resistor. Finally, the output voltage waveform is measured using a separate high impedance probe referenced to ground.

The performance of the HPMLC is evaluated using two sets of signals. One signal switches between the four voltage levels periodically with equal duty cycle. The other is the envelope of a 64-QAM signal transmitting at a baud rate of 5 mega-symbols per second corresponding to a bandwidth of approximately 8 MHz with a root raised cosine filter utilizing a roll-off factor of 0.25. The signal length is 1000 symbols and repeats continuously. In order to change the power level of the converter, the load resistance is reduced from 20 Ω to 0.4 Ω in 9 steps.

The load resistance is designed to emulate different numbers of PAs being simultaneously supply modulated, as illustrated in Fig.1. The single PA unit considered is a 10 W GaN PA similar to the one detailed in [42], operating at a drain voltage of 20 V with 50% drain efficiency, corresponding to a resistance of $R = 20\,\Omega$. For each of the measurements, the purely resistive case is compared to the case of an RC load for an individual PA drain capacitance of $C = 10\,\text{pF}$. For N amplifiers, the load is scaled according to:

$$R_\text{L} = \frac{R}{N} \quad \text{and} \quad C_\text{L} = N \cdot C \tag{1}$$

B. Measured Performance Results

The efficiency of the HPMLC producing a four level equal duty cycle signal is shown in Fig. 10 for different output powers at switching frequencies from 1 MHz to 10 MHz. The results are shown with the parallel RC load described in Eq. 1 with N ranging from 1 to 50, as well as the purely restive load of with $C_\text{L} = 0\,\text{pF}$. The efficiency calculations include the power consumption of the entire HPMLC, excluding the BPG. The power consumption of the gate drivers is largely independent of the load and depends heavily on the switching frequency. Therefore, at lower output powers the efficiency drops significantly since the ratio of the gate-driver power consumption to the total output power dominates. Furthermore, since the nominal *off* voltage of the gate drivers is connected to the 10 V rail, when a switch is turned off, the charge stored in the input capacitance of the device is transferred to the 10 V rail. This energy is therefore recycled and the efficiency gets a slight boost as described in [39]. The efficiency in Fig. 10 peaks at approximately 175 W and drops slightly at the higher power levels, due to the ohmic losses in the switches which are additionally increased by higher R_on due to raised device temperatures. Overall the efficiency remains above 94% across all switching frequencies for power levels exceeding 75 W.

The HPMLC is also evaluated at different power levels while tracking a 64-QAM signal described in section IV-A. The ideal target drain signal is chosen for flat gain at 9 GHz based upon CW measurements of a 10 W, 6 to 12 GHz MMIC PA [42] with the RF input power chosen for maximum efficiency. First an ideal continuous drain signal is generated, then this signal is discretized to the HPMLC voltage levels. In order to appropriately discretize the continuous drain signal, a minimum pulse width must be enforced so that the supply

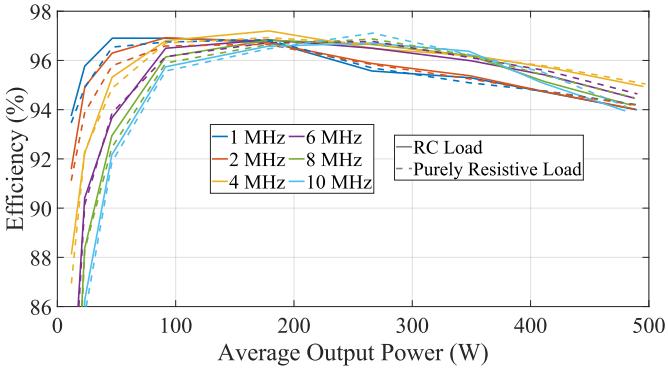


Fig. 10: Supply modulator efficiency with an equal duty cycle four-level waveform at switching frequencies and average output powers ranging from 1 to 10 MHz and 11.7 W to 497.1 W under purely resistive and RC loads.

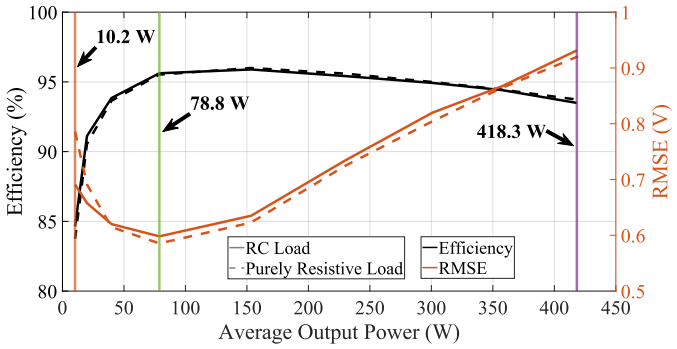


Fig. 11: Supply modulator efficiency and RMSE while tracking an 8 MHz 64-QAM signal between average output powers of 10.2 W and 418.3 W for a purely resistive and RC load.

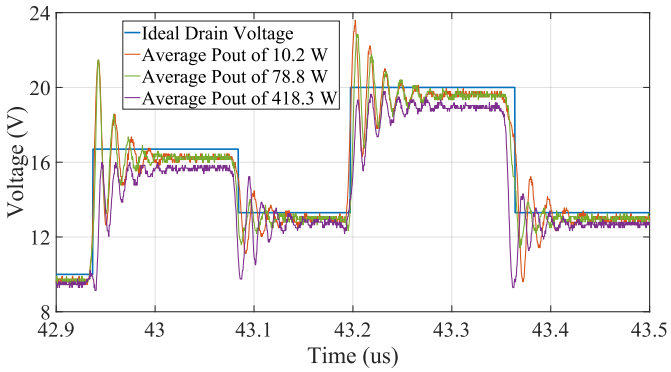


Fig. 12: Measured output voltage with three different parallel RC loads of (20 Ω || 10 pF - orange), (5 Ω || 40 pF - green), and (0.4 Ω || 480 pF - purple). These waveforms are compared to the ideal drain signal when tracking a 8 MHz 64-QAM signal.

modulator does not attempt to switch faster than it is capable of doing. For this HPMLC the minimum pulse width/maximum switching frequency is limited by the ringing duration upon each switching instance. Therefore, the maximum switching frequency of the HPMLC is set to 10 MHz corresponding to a minimum pulse width of 100 ns. The resulting discretized drain envelope signal has a minimum pulse width of 100 ns and a maximum pulse width of 228.8 ns.

The efficiency and root mean square error (RMSE) of the HPMLC generating the 64-QAM envelope signal is plotted for different average output powers in Fig. 11. We here use the RMSE to show the deviation of the output trace from an ideal DSM with ohmic losses to quantify the effects of ringing. Therefore, the ideal drain comparison signal for each load is adjusted to match the measured steady-state voltage of each voltage level. For low output powers (e.g. 10.2 W) the RMSE for the RC load is quite high due to large ringing at all voltage transitions. The purely resistive load shows an even worse RMSE of 0.79 V. At a load of 78.8 W it reaches a minimum of 0.59 V and then rises again for higher output powers, with little difference between the purely resistive and RC load.

The output voltage waveform of the HPMLC tracking the 64-QAM signal with average output powers of 10.2 W, 78.8 W, and 418.3 W is shown in Fig. 12 under the previously described RC load conditions. The measured waveforms are compared to the ideal drain signal which has not been adjusted for voltage drop. When switching to higher voltage levels, the ringing between loads of 10.2 W and 78.8 W is nearly identical, however when switching down to the lowest voltage level, the ringing overshoot and duration is significantly lower at 78.8 W. For higher output powers we observe an increased lag to reach the the steady state output voltages, thus resulting in a higher RMSE as shown in Fig. 11.

Conclusion

A four-level discrete supply modulator with a peak measured output power of 800 W at 20 V with an efficiency over 90% is presented. The tracker is intended for improving the average efficiency of high-power RF amplifiers with high peak-to-average ratio signals. The transistors used as switches in the circuit are GaN on Si substrate, chosen after a careful analysis of available devices in terms of parameters such as input/output capacitance and on-state resistance, as well as absence of a body diode.

A possible limitation of the HPMLC circuit architecture is ringing in the output waveform, since it directly affects the output signal of the RF amplifier. The paper describes an approach for accurately predicting the ringing so that it can be minimized. It is shown that detailed broadband electromagnetic modeling of the input and output metal traces in combination with a geometry oriented RLC model is required to predict the time-domain waveforms.

The HPMLC is tested with a purely resistive load, as well as several parallel RC loads, emulating multiple RF PAs in a combiner. Using an equal duty cycle four-level test signal with switching frequencies ranging between 1 and 10 MHz efficiencies exceeding 94% are achieved for average output powers exceeding 91.6 W and up to peak power levels of 800 W. Testing with the envelope of a 64-QAM, 8 MHz-signal similar efficiencies are obtained, achieving an RMSE below 0.93 V across all measured average output power levels ranging from 10.2 W to 418.3 W. To the best of the authors' knowledge, this represents the highest power and efficiency envelope modulator that demonstrated tracking of a 8-MHz high peak-to-average ratio signal.

Future work includes investigating methods for increasing bandwidth, e.g. by increasing switching speed. The detailed electromagnetic simulations are critical for understanding the ringing phenomena. Ringing reduction techniques are of continued interest to allow for higher switching-speeds without introducing RF distortion. Finally, it is of practical interest to demonstrate this high-power supply modulator for improving the efficiency of multiple high-power RF amplifiers.

V. Appendix

The key specifications of the devices surveyed in Fig. 2 are shown in Table II. The GaN devices manufactured by Efficient Power Conversion (EPC) have very low R_{on} values and capacitances competitive with other GaN devices. However,

the $V_{\mathrm{gs-min}}$ for EPC devices is $-4\,\mathrm{V}$ which limits the output voltage range of the modulator in the circuit configuration used in this work. Out of all the surveyed GaN devices with a $V_{\mathrm{gs-min}}$ of at least $-10\,\mathrm{V}$, the GaN System device (GS61008T) provides the best R_{on} with reasonable C_{in} and C_{out} values and hence was chosen in this work.

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TABLE II: Key parameters of the Si MOSFET, GaN, and SiC MOSFET transistors with $I_{\mathrm{d-max}}$ ranging from 10 to $105\,\mathrm{A}$ and a minimum V_{br} of $25\,\mathrm{V}$. The associated R_{on} and C_{out} is plotted vs $I_{\mathrm{d-max}}$ in Fig. 2

Technology (# in Fig. 2)	$I_{\mathrm{d-max}}$ **(A)**	R_{on} **(mΩ)**	C_{out} **(pF)**	C_{in} **(pF)**	**Volt. of $C_{\mathrm{out/in}}$ Spec. (V)**	V_{br} **(V)**	$V_{\mathrm{gs-min}}$ **(V)**	T_{rise} **(ns)**	T_{fall} **(ns)**	**Part #**
Si MOSFET (1)	105	6.9	1900	180	20	150	-20	46	6	IPB083N15N5LF
Si MOSFET (2)	61	6.2	227	1006	12	30	-20	NA	NA	PSMN9R0-30YL,115
Si MOSFET (3)	40	3.5	1040	3595	15	30	-16	17	10	SiS476DN
Si MOSFET (4)	50	2.8	610	4750	20	40	-20	9	9	SiR414DP
Si MOSFET (5)	65	9.3	286	422	15	30	-20	8.2	3.2	CSD17527Q5A
Si MOSFET (6)	43	11.3	200	400	12	25	-8	5.4	4.2	MCP87130
Si MOSFET (7)	37	14	125	545	25	30	-10	12.3	9.8	BUK9M17-30E
Si MOSFET (8)	40	6	291	670	12	25	-20	2.2	1.8	BSZ060NE2LS
Si MOSFET (9)	52	11.2	169	1067	25	40	-10	13	9	BUK9Y12-40E
Si MOSFET (10)	50	9	150	680	25	30	-20	8.2	12.5	TSM090N03E
SiC MOSFET (11)	35	65	66	760	600	1700	-8	8	4	C3M0065090J
SiC MOSFET (12)	40	80	105	2250	1000	1200	-10	9	18	C2M0080170P
SiC MOSFET (13)	63	32	129	3357	1000	1200	-8	18	9	C3M0032120K
SiC MOSFET (14)	45	50	56	3825	800	1200	-30	12	15	GA20JT12-263
SiC MOSFET (15)	58	56	137	1762	800	1200	-5	20	10	NVH4L040N120SC1
SiC MOSFET (16)	72	45	171	3672	1000	1700	-5	20	18	C2M0045170D
GaN (17)	31	55	72	380	400	600	-10	8	15	IGO60R070D1
GaN (18)	90	1.45	1530	2150	15	30	-4	NA	NA	EPC2023
GaN (19)	48	3.8	642	1453	50	100	-4	NA	NA	EPC2053
GaN (20)	53	3.2	710	980	20	40	-4	NA	NA	EPC2015
GaN (21)	10	16	150	220	20	40	-4	NA	NA	EPC2014C
GaN (22)	18	12	210	360	50	100	-4	NA	NA	EPC2016C
GaN (23)	16	150	46	720	480	650	-18	4.5	4	TPH3206PSB
GaN (24)	47.2	41	196	1500	400	650	-20	14	12	TP65H035WSQA
GaN (25)	31	70	72	380	400	600	-10	8	15	IGOT60R070D1
GaN (26)	60	25	126	518	400	650	-10	12.4	22	GS66516T
GaN (27)	**90**	**7**	**250**	**600**	**50**	**100**	-10	**NA**	**NA**	**GS61008T**

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