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A parameter extraction methodology for graphene field-effect transistors

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Abstract **— Graphene field-effect transistors have now been around for more than a decade and their transfer characteristics extensively used for device characterization. Model parameters like low-field charge-carrier mobility and device contact/series resistance have often been the main interest. However, not until recently have the methods for device characterization themselves been the focus of research publications. In this paper, I report on a structured methodology for extracting and validating the extracted GFET model parameter values based on the physics of field-effect transistors in general and of graphene field-effect transistors in particular. During the extraction process the GFET resistance is divided into two parts, a constant part, and a gate-voltage-dependent part where the constant part often has been believed to represent the series/contact resistance. However, part of it depends on the channel length and contains first-order information about mobility degradation. Finally, I show that the main influence of the quantum capacitance can be captured by an equivalent oxide thickness replacing the insulator thickness.**

Index Terms **—** ***graphene field-effect transistors, model parameter extraction, charge-carrier mobility, series/contact resistance, mobility degradation.***

I. Introduction

Admittedly, it might appear somewhat late to present new advice on how to extract graphene field-effect transistor (GFET) model parameters from current-voltage measurements more than a decade after the device models were published. Nevertheless, consistent parameter extraction procedures are important, particularly when far-reaching conclusions tend to be drawn from extracted parameter values concerning charge-carrier mobility on the one hand, and series and contact resistances on the other hand. The timeliness of the topic was recently accentuated by a review paper urging for consistency in reporting and benchmarking emerging FET technologies [1]. Moreover, the recent application of the Y-method for characterizing GFETs shows that still today great efforts are spent on finding reliable and consistent methodologies for extracting GFET model parameters [2].

In this paper, I will present a simple method for extraction of GFET model parameters from the drain current vs. gate voltage transfer characteristic using only a few well selected measurement points. The method has its roots in the 3-point method often used for wafer-scale characterization of MOSFETs [3] [4]. The proposed method can be seamlessly combined with the method presented by De La Moneda *et al.* already in the early 1980´s [5]. Their method uses the dependence of the drain-to-source resistance R_{DS} on the gate voltage to separate a constant series resistance from a voltage-dependent channel resistance. As far as I understand their method never won wide acceptance for characterizing MOSFETs mainly because it requires beforehand knowledge of the threshold voltage, the definition of which is not all that clear. However, for GFETs the method is ideal because of the well-defined minimum conductivity point.

Before discussing the parameter extraction process in more detail, I will use the next section to review the model used to describe the GFET transfer characteristic. Thereafter, the proposed extraction procedure is demonstrated and validated using measurement data from state-of-the-art top- and bottom-gated GFETs based both on exfoliated graphene and on chemical vapor deposited (CVD) graphene.

II. GFET Modeling

Models are used to predict the performance of graphene field-effect transistors. Based on physical parameters like gate length L, gate width W, oxide thickness t_{ox} and permittivity ε_{ox}, charge carrier mobility μ, series resistance due to the access areas and the source/drain contact resistances R_C, and finally the Dirac voltage V_{Dirac}, the GFET drain current can be predicted as a function of the density of charge carriers n_{tot} and the applied drain-source voltage, V_{DS},

$$I_D = \frac{W}{L} q n_{tot} \mu \left(V_{DS} - R_C I_D \right), \tag{1}$$

where q is the electron charge. The charge-carrier density n_{tot} (electrons or holes) in the graphene channel region can be modeled by [6][7],

$$n_{tot} = \sqrt{n_0^2 + n^2}\,, \tag{2}$$

where n_0 is the density of residual charge carriers at the minimum conductivity Dirac point, and n is the density of charge carriers induced by the transversal field caused by the gate-source voltage V_{GS}.

For the mobility and its dependence on the density of charge carriers, an effect known as mobility degradation, a first-order model was introduced and validated in [9] based on the work of Dorgan *et al.* [8],

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$$\mu = \frac{\mu_0}{1 + n_{tot} / n_{ref}}, \tag{3}$$

where μ_0 is the low-field mobility at low charge-carrier densities, and where n_{ref} is a fitting parameter on the order of 10^{12} cm^{-2} representing the charge-carrier density for which the low-field mobility is reduced to half.

Under the assumption of a constant gate capacitance C_{ox}', the total charge-carrier density becomes[1]

$$n_{tot} = \frac{C_{ox}'}{q}\sqrt{V_0^2 + V_{GCO}^2}, \tag{4}$$

where $V_0 = qn_0/C_{ox}'$ is a fitting parameter related to the residual charge density qn_0 [12], and where $V_{GCO} = (V_{GS} - V_{Dirac} - V_{DS}/2)$ is the gate-to-channel overdrive voltage. This definition of the overdrive voltage yields the average charge-carrier density in the channel instead of the density at the source and has the advantage of making the charge-carrier density model (4) independent of the series resistance. It also takes care of the V_{DS}-dependence of the minimum conduction point and makes V_{Dirac} a voltage-independent model parameter. As shown in [9], the mobility degradation model in (3) can now be written on a form like the one used for MOSFETs for decades [13] [14],

$$\mu = \frac{\mu_0}{1 + \theta\sqrt{V_0^2 + V_{GCO}^2}}, \tag{5}$$

where $\theta = C_{ox}'/(qn_{ref})$ is known as the mobility degradation coefficient. By substituting (4) and (5) into the drain-current model (1), the GFET resistance, $R_{DS} = V_{DS}/I_D$, can be written as the sum of a series/contact resistance R_C and a voltage-dependent channel resistance proportional to the gate length,

$$R_{DS} = \frac{V_{DS}}{I_D} = R_C + \underbrace{\frac{1}{k}\left(\theta + \frac{1}{\sqrt{V_0^2 + V_{GCO}^2}}\right)}_{\text{channel resistance} \sim L}, \tag{6}$$

where $k = (W/L)\mu_0 C_{ox}'$ is the well-known FET transconductance parameter. The model equation indicates that the gate-voltage dependence of the charge-carrier mobility in the channel adds a contribution θ/k to the channel resistance [2]. It might be interesting to note that circuit designers at Texas Instruments already in the mid-1960´s found that a series resistance θ/k should be added to the MOSFET channel resistance to model the dependence on the transversal field of the charge-carrier mobility [15].

III. Model Parameter Extraction

There are two aspects of modelling. First, models like the one described in the previous section, are predictive. This means that the device behavior can be predicted given that the model parameters are known. This is different from simulations, the results of which are not predictable beforehand. Secondly, once models are validated, they can be used to find or extract the model parameters from experimental data.

From the parameter extraction point-of-view, the GFET resistance model in (6) is a model with four parameters, k, R_{eff}, V_{Dirac}, and V_0,

$$R_{DS} = \frac{V_{DS}}{I_D} = R_{eff} + \frac{1/k}{\sqrt{V_0^2 + V_{GCO}^2}}. \tag{7}$$

Here, $R_{eff} = R_C + \theta/k$ is an effective resistance containing not only the contact/series resistance R_C but also a part θ/k of the channel resistance caused by the mobility degradation. Before the introduction of the mobility degradation model in [9], the effective resistance was often believed to represent the series/contact resistances. But, even if mobility degradation was not discussed in the original model used by Meric *et al*. [6] and Kim *et al*. [7], such information is in fact embedded in the effective "series" resistance. Therefore, it is not correct to label the model a "constant-mobility model" as is often done in the literature. The two contributions to the effective resistance R_{eff} can be separated by means of its dependence on the channel length L for a set of GFETs of different channel lengths. However, this topic is beyond the scope of this paper.

Among the four model parameters, k and R_{eff} are physics-based model parameters describing the GFET behavior as a field-effect transistor, while V_{Dirac} and V_0 are related to the GFET behavior at the maximum resistance point. V_0 is related to the residual charge density, but its role is more of a fitting parameter in the semi-empirical model used to add the two contributions to the total charge-carrier density. Let us proceed to see how these model parameters can be extracted.

Model parameters can be extracted from experimental data in many ways as reviewed for MOSFETs in [16]. However, given the accuracy by which measurements can be performed using advanced equipment, an experienced device engineer needs very few data points for this process. For determining four GFET model parameters, i.e., k, R_{eff}, V_{Dirac}, and V_0, all that is needed is the Dirac voltage and a minimum of three experimental ($R_{DS,}$ V_{GCO}) data points.

The Dirac voltage is easily obtained from the minimum conductance point which is different from the difficulty of agreeing on what is the exact threshold voltage of a MOSFET. Having determined the Dirac voltage, we need a minimum of three more experimental resistance values for determining k, R_{eff}, and V_0. Fig. 1a shows an example of how an experienced device engineer would choose those three ($R_{DS,}$ V_{GCO}) points bearing in mind the physics of FETs in general and the physics of GFETs in particular. The first point is the maximum resistance point at the Dirac voltage ($R_{Dirac,}$ 0). Then two more resistance values are needed, and these should be measured at gate voltages where the influence of the residual charges are negligible i.e., well away from the Dirac voltage. These two data points are marked 2, and 3 in Fig. 1a. Finally, for checking the asymmetry of the resistance curve, i.e., the asymmetry of the transfer characteristic, we need two more resistance values from the electron side (V_{GCO}>0). These are marked 4 and 5.

[1] The constant capacitance model assumes a constant quantum capacitance in series with the oxide capacitance. The resulting capacitance can be described as an equivalent oxide capacitance C_{ox}' with an equivalent oxide thickness (EOT) somewhat larger than the nominal oxide thickness. These assumptions are discussed and justified in the appendix

A. Parameter extraction from three R_{DS} values

The model parameter extraction process is now quite simple and straightforward. By entering the (R_{DS}, V_{GCO}) data pairs for points 2 and 3 into equation (7) assuming V_0=0, a system of two linear equations is obtained. The solution of this system will return values for k and R_{eff}. Once these two model parameters are known, V_0=[k(R_{Dirac}-R_{eff})]$^{-1}$ can be found from the maximum resistance R_{Dirac}. Repeating the extraction process for the electron side using data from points 4 and 5, a preliminary set of parameter values is obtained.

A graphical illustration of the extraction process using the voltage-dependence of R_{DS} to separate k from R_{eff} is shown in Fig. 1b. Here the four resistance values 2 and 3 for the hole side, and 4 and 5 for the electron side (marked as crosses) are plotted vs. (V_0^2+V_{GCO}^2)$^{-1/2}$ assuming V_0=0. From the slopes and y-intercepts of the straight lines through these data points, values for model parameters k and R_{eff} are obtained for the hole and electron sides, respectively. With a value for V_0 now available, the values for (V_0^2+V_{GCO}^2) can be updated yielding improved values for the model parameters. After the extraction process has converged, all remaining experimental R_{DS} values can be added to the graph. As can be seen, the experimental R_{DS} values that were not used for determining the trendlines line up almost perfectly along the two straight lines for holes and electrons thereby giving a first indication of the accuracy of both the constant capacitance model and the parameter extraction process.

B. Trendline extraction from more than three R_{DS} values

For minimizing the risk of having chosen outlier data points, or data points affected by measurement noise, as could be the case when relying on as few as three data points for the parameter extraction, any number of experimental resistance values from the overdrive voltage ranges between points 2 and 3, and between points 4 and 5, can be used for letting least-squares trendlines determine parameters k and R_{eff} for holes and electrons, respectively. This method is well-known for extracting MOSFET model parameters and has been in use since the early 1980´s when it was first published by De La Moneda *et al*. [5]. The two methods can be used seamlessly in that the least-square fitting process reduces any set of more than two data points to two "best points".

C. Validation of extracted parameter values

For resting assure that we have found the correct parameter values it is of utmost importance to validate the extracted model parameter values. Let me show two validation methods. First, by subtracting the value extracted for R_{eff} from the experimental R_{DS} data, data for an ideal GFET without any series resistance and without any mobility degradation should be obtained. The conductance G_{DS}=(R_{DS}–R_{eff})$^{-1}$ of such an ideal device should exhibit a linear dependence on the gate overdrive voltage [17], and the slope of this relationship should confirm the extracted k-value. Fig. 1c shows this to be the case. Second, the value extracted for R_{eff}, the effective resistance, could be confirmed by plotting $R_{DS}Y$ vs. Y=I_D/$\sqrt{g_m}$, as proposed by Pacheco-Sanchez *et al*. [2], where g_m=$\partial I_D/\partial V_{GCO}$ is the transconductance.

This method allows for extracting R_{eff} under the assumptions of V_0<<V_{GCO} but comes at the cost of a numerical differentiation. As shown in Fig. 1d, the trendline slopes of the $R_{DS}Y$ vs. Y plot confirm the effective resistance values found in Fig. 1b. In both Figs. 1c and 1d the endpoints of the voltage

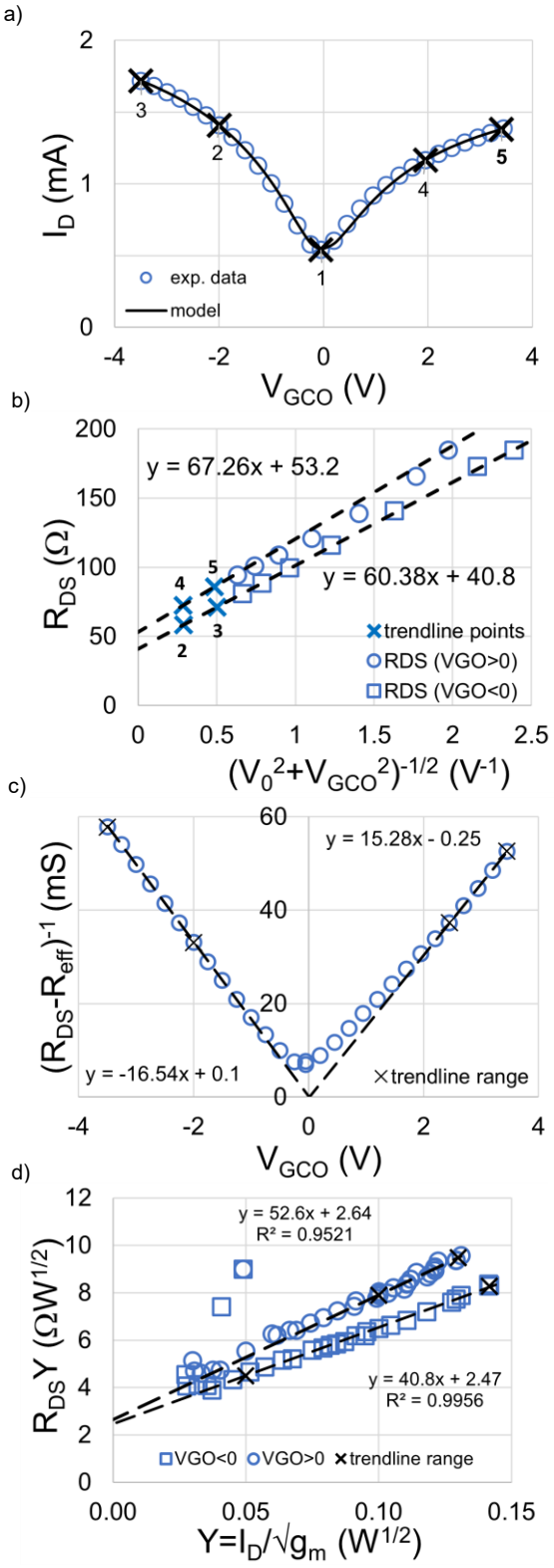

Fig. 1. (a) Experimental GFET transfer curve (circles) from the work of Habibpour *et al*. [18], model (solid line), and the five data points used for model parameter extraction (crosses). (b) R_{DS} vs. (V_0^2+V_{GCO}^2)$^{-1/2}$ graph yielding 1/k (slope) and R_{eff} (y-intercept) for holes (squares) and electrons (circles). (c) Validation plot of GFET conductance vs. gate overdrive voltage assuming R_{eff}=0. (d) $R_{DS}Y$ vs. Y validation plot confirming effective resistance values extracted in Fig. 1b.

ranges used for determining the trendlines are marked with crosses. The results of the parameter extraction and validation are summarized in Table 1.

Table 1. Summary of parameter extraction and validation

Parameters	3-point extraction	validation
k (holes) (mA/V^2)	16.5	16.6
k (electrons) (mA/V^2)	14.9	15.3
R_{eff} (holes) (Ω)	40.8 (0.8 Ωmm)	40.8
R_{eff} (electrons) (Ω)	53.2 (1.1 Ωmm)	52.6

D. GFET used to illustrate parameter extraction

The experimental data used in this section to illustrate the proposed parameter extraction procedure were obtained from a 2×10-µm wide, 1 µm long, top-gated GFET fabricated on exfoliated graphene on a high resistivity silicon substrate covered by a 300-nm silicon dioxide film [18]. The top-gate dielectric was formed by natural oxidation of a 2-nm-thick aluminum layer followed by 25-nm Al_2O_3 deposited by e-gun evaporation. The pads consist of Ti/Pd/Au metal layer stacks defined by e-beam lithography. The source-to-drain pad separation was 1.2 µm.

IV. State-of-the-art device examples

The proposed parameter extraction process based on the constant-capacitance model described in the previous section has been extensively tested on different types of GFETs, not only GFETs on exfoliated graphene. In a previous conference presentation, results were shown from its application to top-gated CVD GFETs on different substrates including Si/SiO_2 substrates with and without Al_2O_3 interfacial layers [19]. Some of these results are shown again in Fig. 2. Even if the device channel length is 0.5 µm, this device represents state-of-the-art when it comes to transit frequency and maximum frequency of oscillation (43 GHz and 46 GHz respectively). Because of poor scaling properties, the quest for higher frequencies has focused on low contact/series resistances and on substrate materials with high optical phonon energies rather than on scaling the channel length.

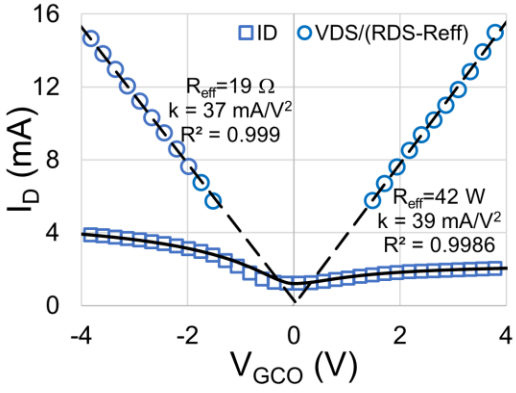

Fig. 2. Graph showing the experimental (squares) and model (line) transfer characteristic of a top-gated CVD GFET on a SiO_2/Si substrate with an Al_2O_3 interfacial layer, and the ideal FET behavior of the same GFET with its effective resistance subtracted. Experimental data from [20].

In the following, focus is on applying the extraction methodology to a set of short-channel, back-gated GFETs with a dielectric so thin that one would expect the quantum capacitance to challenge the constant-capacitance model. These devices with state-of-the-art channel lengths were fabricated at IEMN in Lilles using CVD graphene on high-resistivity SiO_2/Si substrates. Full details on the layout, fabrication and characterization of these devices can be found in [21]. In joint efforts with IEMN, UAB in Barcelona has characterized these devices from the aspects of the influence of traps [22], the effects of mobility degradation [2], and the effects of velocity saturation on low-frequency noise [23].

Finally, I will apply the proposed extraction methodology based on a constant-capacitance model to a top-gated GFET on exfoliated graphene from the pioneering paper by Kim *et al*. [7] where the device was evaluated using a voltage-dependent quantum-capacitance model.

A. Back-gated short-channel CVD GFETs

The first device under test in this subsection is a 2×12-µm dual-channel back-gated 300-nm GFET fabricated on a high-resistivity SiO_2/Si substrate. Prior to transferring the CVD graphene, aluminum back-gate fingers were defined on the SiO_2 surface. Natural oxidation of the aluminum formed a 4-nm Al_2O_3 dielectric between the bottom gate and the graphene film [21].

In the context of this paper, these GFET devices are of interest for their short channel lengths and their thin dielectrics (~4 nm) suggesting that the influence of the quantum capacitance would be non-negligible. Experimental transfer characteristics obtained by using opposing pulse-sweep measurements at three different drain-to-source voltages (0.1, 0.2, and 0.3 V) published in [22] are shown in Fig. 3a. The analysis of these data showed that the drain conductance $G_{DS}=I_D/V_{DS}$ is almost independent of the drain voltage V_{DS} except for the V_{DS}/2-shift of the minimum conduction point. Therefore, resistance data from all three drain voltages were used to separate the effective resistance from the transconductance parameter.

For characterizing this device, resistance data obtained at overdrive voltages ranging from -2.35 to -0.65 V were used as shown in Fig. 3b. The trendline parameters shown are those obtained after the parameter values converged and a value was found for V_0 (0.25 V). This figure also shows how the resistance data not used for the extraction line up along the trendline thereby indicating a good model fit to experimental data. The relative error between the trendline and experimental data also shown in the figure is less than 3%. As expected, the error is smallest in the voltage range used for extracting the trendlines and somewhat larger towards the Dirac point.

Fig. 3c shows the important validation step in which the ideal conductance $G_{DS}/W=(R_{DS}-R_{eff})^{-1}W^{-1}$, has been plotted vs. the gate overdrive voltage. Away from the Dirac point, this graph should show a straight line with the same slope k as already extracted from the $R_{DS}W$ vs. $(V_0^2+V_{GCO}^2)^{-1/2}$ graph in Fig. 3b. This is also the case and in agreement with the first principles examination of transfer curves in [17].

Finally, Fig. 3d shows the model using the extracted model parameters fitted to the experimental conductance data for three

different drain voltages (0.1, 0.2, and 0.3 V). Good agreement is obtained with a relative error less than 5%.

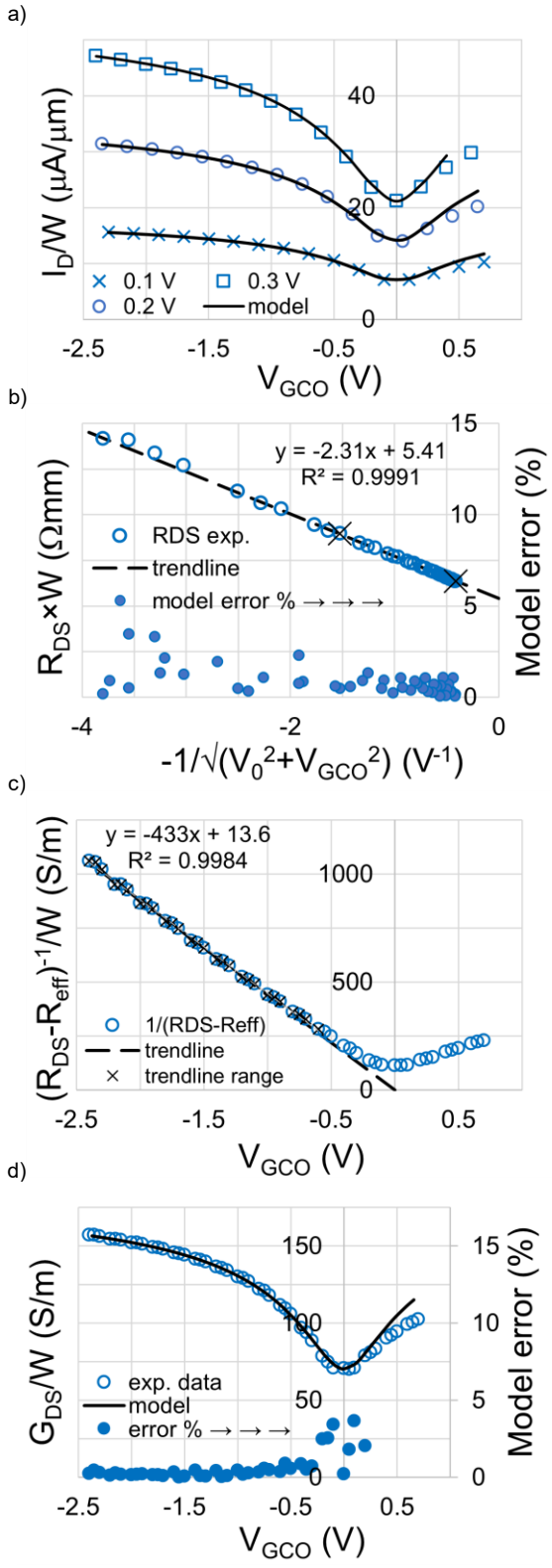

Fig. 3. (a) Experimental GFET transfer curves for three different drain-to-source voltages. Data from [21]. (b) R_{DS} vs. $-1/\sqrt{(V_0^2+V_{GCO}^2)}$ graph yielding $1/k$ (slope) and R_{eff} (y-intercept) for holes. Also shown is the relative error. (c) Validation plot of GFET conductance vs gate overdrive voltage assuming R_{eff}=0. (d) Model fit to experimental data using extracted model parameters, and model error.

More measurements from the same type of GFETs have been published by Mavredakis *et al.* [23] in their study of the velocity saturation effect on low-frequency noise in short-channel GFETs. In their paper, they published experimental transfer characteristics obtained for up to five different drain-to-source voltages (30, 60, 100, 200 and 300 mV) for GFETs of three different gate lengths (100, 200, and 300 nm).

Also, for these devices the drain conductance $G_{DS}=I_D/V_{DS}$ was found to be (almost) independent of the drain-to-source voltage. Fig. 4a shows a plot vs. $(V_0^2 + V_{GCO}^2)^{-1/2}$ of the experimental R_{DS} values obtained for GFETs of three different gate lengths and up to four applied V_{DS} voltages with excellent linear behavior. Not forgetting the important validation step, this is shown in Fig. 4b with $(R_{DS}-R_{eff})^{-1}$ plotted vs. V_{GCO}. Again, a linear FET behavior is confirmed with the same k-values that could be derived from Fig. 4b. Please, note that the slopes in Fig. 4b equals $1/k$. The extraction process confirms the R_{eff} values found in [23], and an R_{eff} vs. gate length L_g plot (not shown) confirms the mobility degradation coefficient found in [2]. However, this last parameter value should be taken with a grain of salt as the mobility was not found to be constant across the three gate lengths. Finally, Fig. 4c shows the model fit to experimental G_{DS} data obtained at four drain voltages (60, 100, 200 and 300 mV) for GFETs of the three different gate lengths.

Based on the observed linearity of both the R_{DS} vs. $(V_0^2 + V_{GCO}^2)^{-1/2}$ plots in Fig. 4a and the ideal $G_{DS}=(R_{DS}-R_{eff})^{-1}$ vs. V_{GCO} plots in Fig. 4b one might conclude that the constant-capacitance model appears to give excellent fit to experimental data with errors less than 5% also for GFET devices with very thin dielectrics.

B. Pioneering top-gated GFETs on exfoliated graphene

The finding in the previous subsection of the constant-gate-capacitance model yielding excellent fit to experimental data also for GFETs with dielectrics so thin that the influence of the quantum capacitance could not reasonably be neglected leads me to reevaluate the pioneering work of Kim et al. [7].

Published already in 2009, their research has come to serve as a solid basis for the research on top-gated GFETs for more than a decade. They fabricated and evaluated in detail high-quality, top-gated 2.4 μm GFETs on exfoliated graphene. By fitting a model that considered a voltage-dependent quantum capacitance they obtained the results shown in Fig. 5a. Their work indicated a single mobility μ=8600 cm^2/Vs, an effective resistance of 1585 Ω, and a residual density of 2.3×10^{11} cm^{-2}.

However, even if the model fit to experimental data appears good to the eye, the value they found for the effective resistance does not pass the $(R_{DS}-R_{eff})^{-1}$ vs. V_{GCO} validation check in not returning the linear V_{GCO}-dependence expected of an FET with R_{eff}=0 [17]. It is also easy to see that the experimental data are not symmetrical around the Dirac point. This is emphasized by the R_{DS} vs. $(V_0^2 + V_{GCO}^2)^{-1/2}$ plots in Fig. 5b indicating different values for the hole and electron mobilities. However, the effective resistance seems to be the same for both negative and positive overdrive voltages. The value found in Fig. 5b for the effective resistance R_{eff}=1553 Ω also passes the $(R_{DS}-R_{eff})^{-1}$ vs. V_{GCO} validation step shown in Fig. 5c. Finally, the $R_{DS}Y$ vs. Y plot shown in Fig. 5d returns almost the same resistance value,

1545±10 Ω thereby validating the extracted model parameters of the constant-capacitance model.

The constant-capacitance model, with parameters extracted from the R_{DS} vs. $-(V_0^2+V_{GCO}^2)^{-1/2}$ plots in Fig. 5b, is shown fitted to experimental data in Fig. 6a. The relative errors, i.e., the relative differences between the two models and the experimental resistance data are shown in Fig. 6b. Much smaller errors are obtained for the constant gate-capacitance model used in this work than for the original model used in [7], particularly in the linear "field-effect regions" away from the Dirac point. Only close to the Dirac point for $0<V_{GCO}<0.2$ V does the constant-capacitance model result in errors equal to those found in [7].

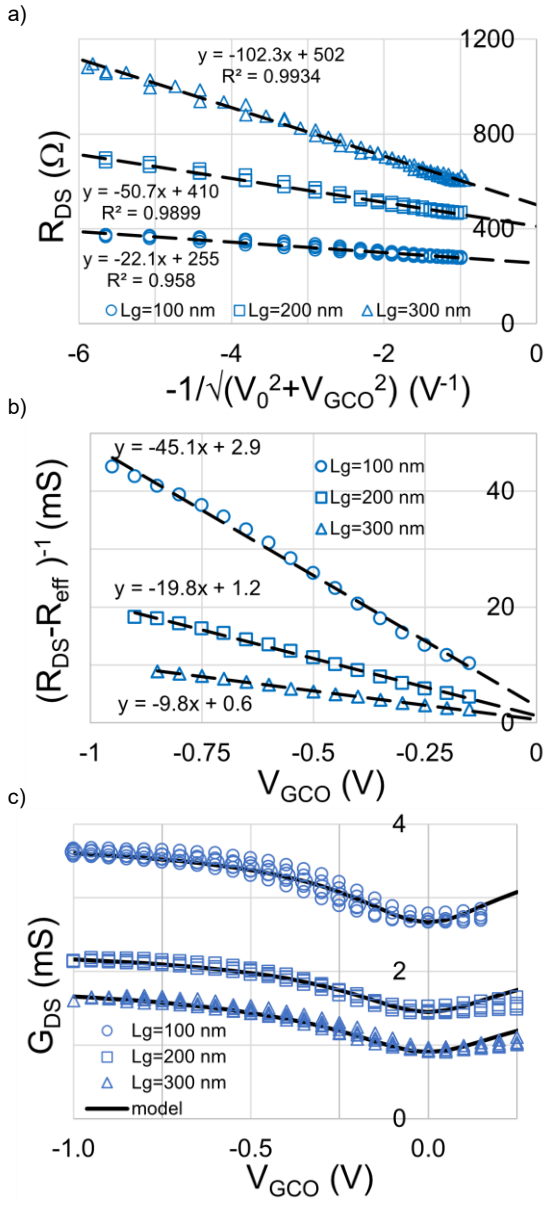

Fig. 4. (a) R_{DS} vs. $-(V_0^2+V_{GCO}^2)^{-1/2}$ graph yielding $1/k$ (slope) and R_{eff} (y-intercept) for holes in GFETs of three different channel lengths. (b) Validation plot of the GFET conductance vs gate overdrive voltage assuming R_{eff}=0. (c) Model using extracted model parameters fitted to experimental data from [22].

We can also note that the excessive resistance value extracted in [7] was compensated by a transconductance parameter

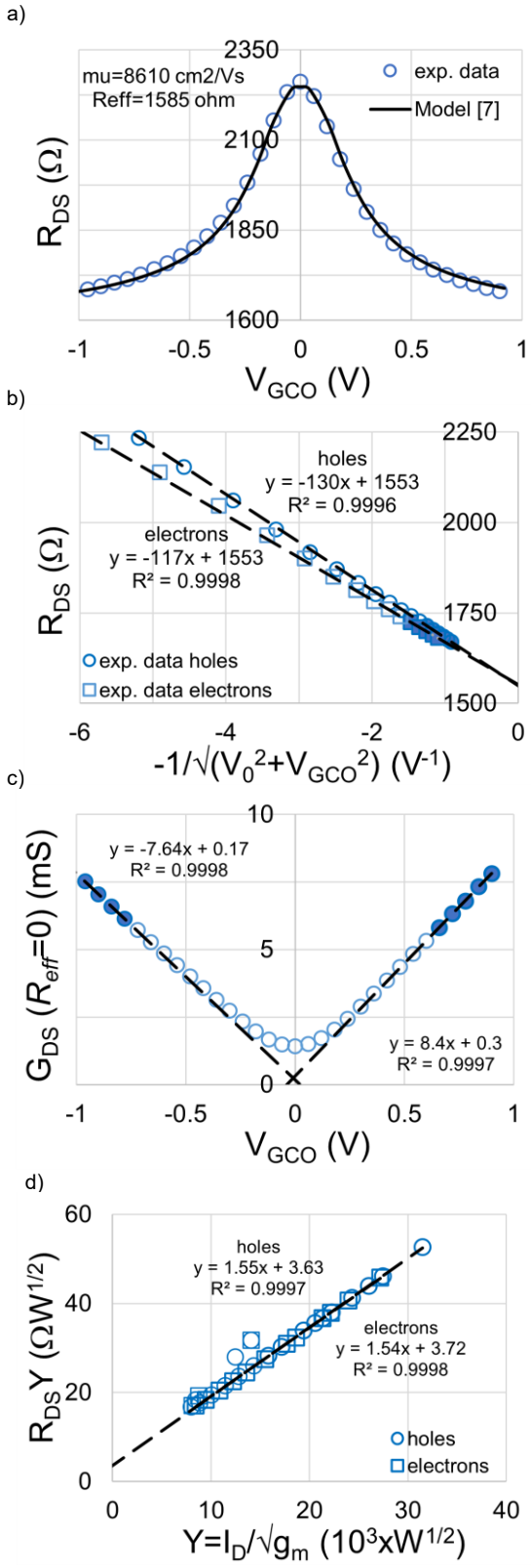

Fig. 5. (a) Model fit to experimental data from [7]. (b) R_{DS} vs. $-(V_0^2+V_{GCO}^2)^{-1/2}$ graph yielding $1/k$ (slope) and R_{eff} (y-intercept) for holes and electrons. (c) Validation plot of the GFET conductance vs. gate overdrive voltage assuming R_{eff}=0. (d) $R_{DS}Y$ vs. Y validation plot confirming extracted effective resistance values.

k=12.8 mA/V^2 much larger than those extracted for holes (7.64 mA/V^2) and electrons (8.4 mA/V^2) using the constant-capacitance model. Therefore, the mobility is probably not quite as high as indicated in their paper (8860 cm^2/Vs), but still among the highest published for GFETs on exfoliated graphene.

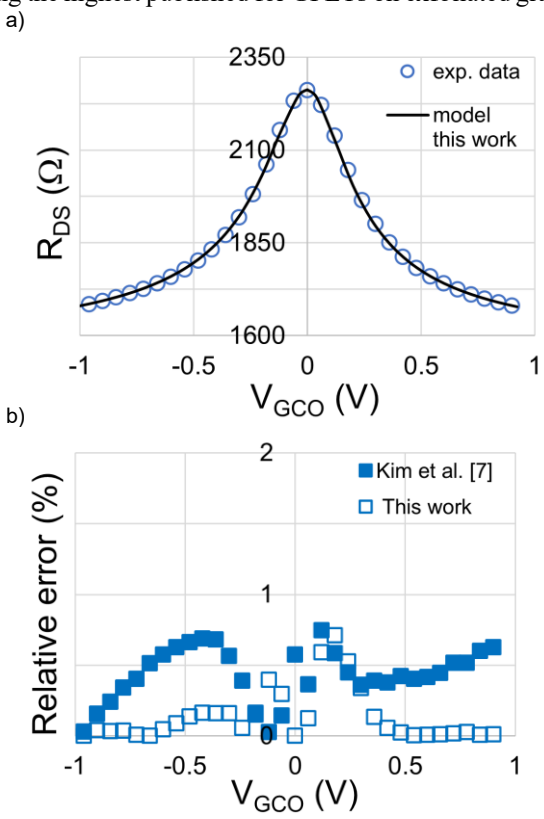

Fig. 6. (a) Constant-capacitance model fitted to experimental data from [7] using model parameters from this work. (b) Relative difference between models and experimental data.

V. Conclusion

In this paper, I have proposed a method for extracting the low-field GFET model parameters from R_{DS} vs. $(V_0^2+V_{GCO}^2)^{-1/2}$ plots by adapting to GFETs a method once proposed for MOSFETs [5]. Contrary to when applied to MOSFETs, this method is shown to be both robust and accurate when applied to GFETs, the main difference being the well-defined Dirac point of a GFET compared to the less well-defined threshold voltage of a MOSFET. Given that a minimum of three data points is needed to extract the three model parameters modeling the GFET at low drain voltages, I have shown how to select these data points considering the physics of FETs in general, and the physics of GFETs in particular. Having determined the Dirac voltage, three resistance values were selected, one value being the maximum resistance at the Dirac point and two values being obtained for gate overdrive voltages well away from the Dirac point where the influence of residual carriers could be considered negligible. The slope and the y-intercept of a straight line through the latter two points in an R_{DS} vs. $(V_0^2 + V_{GCO}^2)^{-1/2}$ graph return the values needed for R_{eff} and k. Extraction robustness can be increased by selecting more than two R_{DS} values from the same voltage range and using least-squares trendlines for separating the effective resistance from the voltage-dependent part of the channel resistance. This minimizes the risk of having chosen outlier data or data affected by measurement noise. The importance of validating the values extracted for k and R_{eff} using $(R_{DS}\text{-}R_{eff})^{-1}$ vs. V_{GCO} plots has been strongly emphasized.

Finally, it can be concluded that the linearity of the R_{DS} vs. $(V_0^2+V_{GCO}^2)^{-1/2}$ graph and of the $(R_{\rm DS}\text{-}R_{eff})^{-1}$ vs. V_{GCO} graph indicate two important findings: i) the gate capacitance is independent of the gate voltage except close to the Dirac point suggesting that the main influence of the quantum capacitance can be captured by an equivalent oxide thickness larger than the nominal thickness, ii) no second-order mobility degradation effects other than those embedded in the effective resistance were found in the GFETs investigated.

VI. Appendix

The constant-capacitance model used in this work has several advantages over more complex models including the simplicity by which model parameters can be extracted without relying on optimization tools and on prerequisite knowledge of parameters like oxide capacitance and Fermi velocity. As shown in this work, the accuracy of the constant gate-capacitance model is comparable or even better than the accuracy obtained with non-constant gate-capacitance models. The use of a constant-capacitance model is also supported by observations made by Bonmann et al. [24].

The quantum capacitance has been extensively studied theoretically. In [7] the following model was used for the oxide capacitance C_{ox} in series with a voltage-dependent quantum capacitance C_Q=$\sqrt{n}/\gamma$,

$$\frac{C_{ox}}{q}V_{GCO} = n + 2\gamma C_{ox}\sqrt{n} \text{ with } \gamma = \frac{\hbar v_F\sqrt{\pi}}{2q^2}, \quad \text{(A1)}$$

where $\hbar$ is Planck´s constant, and v_F is the Fermi velocity. For charge-carrier densities n>>n_0, the relationship between V_{GCO} and n can be shown to be almost linear with a slope given by

$$\frac{C_{ox}}{q}\frac{dV_{GCO}}{dn} = 1 + \frac{\gamma C_{ox}}{\sqrt{n}} \quad . \quad \text{(A2)}$$

The relationship between n and V_{GCO} can then be written

$$n = C_{ox}'V_{GCO}/q, \text{ with } C_{ox}' = C_{ox}/(1+\frac{\gamma C_{ox}}{\sqrt{n}}), \quad \text{(A3)}$$

a model describing the gate capacitance as an oxide capacitance with an equivalent oxide thickness $t_{ox}(1+\gamma C_{ox}\sqrt{n})$. Fig. A1 shows the normalized EOT/t_{ox} plotted vs. the absolute value of the overdrive voltage, using (A1) to find n, for the two oxide capacitance values 1350 nF/cm^2 and 306 nF/cm^2 used by Mavredakis *et al.* [23] and Kim *et al.* [7], respectively. In the voltage range V_{GCO}>0.5 V used to extract model parameters k and R_{eff}, the EOT is shown to be almost constant thereby justifying the approximation of a constant gate-capacitance model. For the case of C_{ox}=306 nF/cm^2 (t_{ox}=22 nm) we find a 7% increase in equivalent oxide thickness, while for C_{ox}=1350 nF/cm^2 (t_{ox}=4 nm) there is a 15% increase in equivalent oxide thickness. The linearity of the voltage-induced charge vs. V_{GCO} is shown in Fig. A2 indicating equivalent oxide capacitances of 285 and 1166 nF/cm^2, capacitance values that are 7% and 15% lower than the nominal values.

Finally, it might be interesting to note that the linearization made here is similar to the linearization made for MOSFETs in weak to moderate inversion for finding the ideality factor modeling the subthreshold swing [25].

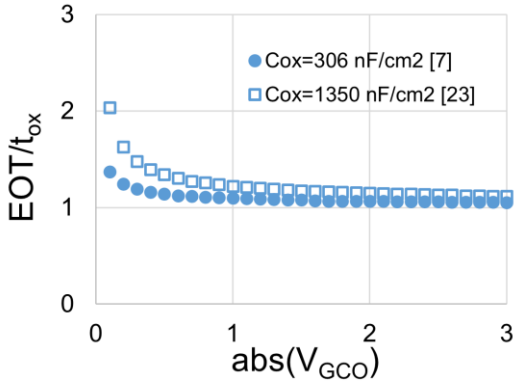

Fig. A1. Normalized equivalent oxide thickness vs. gate overdrive voltage.

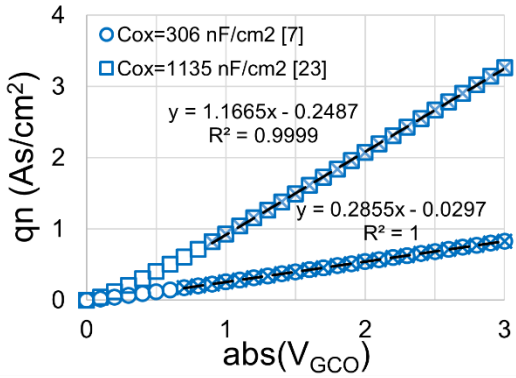

Fig. A2. Voltage-induced charge vs. gate overdrive voltage.

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