
CHALMERS
UNIVERSITY OF TECHNOLOGY

# Evaluation and Suppression Method of Turn-off Current Spike for SiC/Si Hybrid Switch

IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

*Digital Object Identifier 10.1109/ACCESS.2023.Doi Number*

# Evaluation and Suppression Method of Turn-off Current Spike for SiC/Si Hybrid Switch

**HAIHONG QIN[1], (Member, IEEE), SIXUAN XIE[1], ZHENHUA BA[1], XIANG LIU[1], WENMING CHEN[1], DAFENG FU[1], AND QIAN XUN[2]**

[1]Department of Electrical Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China
[2]Department of Electrical Engineering, Chalmers University of Technology, Gothenburg, SE 41279, Sweden

Corresponding author: Haihong Qin (e-mail: qinhaihong@nuaa.edu.cn).

This work was supported in part by the National Natural Science Foundation of China under Grant 51677089, and in part by the State Key Laboratory of Wide-Bandgap Semiconductor Power Electronic Devices, China, under Grant 2019KF001.

**ABSTRACT** SiC MOSFET/Si IGBT (SiC/Si) hybrid switch usually selects the gate control pattern that SiC MOSFET turns on earlier and turns off later than Si IGBT, with the aim of making the hybrid switch show excellent switching characteristics of SiC MOSFET and reduce switching loss. However, when SiC MOSFET turns off, the fast slew rate of drain source voltage causes the current spike in Si IGBT due to the effects of parasitic capacitance charging and carrier recombination, which will produce additional turn-off loss, thus affecting the overall efficiency and temperature rise of the converter. Based on the double pulse test circuit of SiC/Si hybrid switch, the mathematical model of the turn-off transient process is established. The effects of the remnant carrier recombination degree of Si IGBT, the turn-off speed of SiC MOSFET and the working conditions on the turn-off current spike of hybrid switch are evaluated. Although adjusting these parameters can reduce the turn-off current spike somewhat, additional losses will be introduced. Therefore, a new method to suppress the turn-off current spike is proposed to balance the power loss and current stress.

**INDEX TERMS** SiC MOSFET/Si IGBT, hybrid switch, current spike, suppression method

## I. INTRODUCTION

As a new type of wide bandgap semiconductor device, Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) has lower on-resistance, faster switching speed and better thermostability compared with Si insulated-gate-bipolar transistor (IGBT). Therefore, SiC MOSFET is widely used in wireless power transmission, photovoltaic power generation and other fields [1-4]. However, due to the limitations of wafer growth and chip technology, the current rating of SiC MOSFET is still lower than that of Si IGBT [5]. In addition, with the increase of SiC wafer area, the wafer yield decreases, resulting in higher manufacturing costs [6].

Therefore, in order to take advantage of the conduction characteristics of Si IGBT under high current and the switching characteristics of SiC MOSFET, researchers have proposed a hybrid switch [7]. For the driving circuit and control signal of SiC/Si hybrid switch, the gate control signals of SiC MOSFET and Si IGBT are controlled separately. In [8], it is proposed to use simple devices such as resistance and capacitance in the driving circuit to adjust the switching delay time between SiC MOSFET and Si IGBT. Once the resistance and capacitance values are determined, the switching delay time will also be fixed. In [9], researchers pointed out that due to the time-varying characteristics of junction temperature of SiC/Si hybrid switch, dynamically changing its switching delay time can reduce the loss, and a gate control method based on the swarm intelligent algorithm has been proposed. In addition, when Si IGBT turns off before SiC MOSFET with appropriate turn off delay time, Si IGBT can realize zero-voltage turn off so as to minimize the turn off loss of hybrid switch [10], [11]. By optimizing the gate control pattern, the hybrid switch can achieve the switching characteristics close to SiC MOSFET while improving the device current level [12-14], and greatly reduce the cost compared with the all-SiC scheme [15-17]. At present, researchers have carried out research on the characteristics, loss modeling, and control modes of SiC/Si hybrid switch. Reference [18] points out that the imbalance of parasitic inductance in the hybrid switch will affect the dynamic current sharing, thus affecting the conduction loss. And the current ratio of hybrid switch will affect the

characteristics and power loss of the device [19]. In [20], the active driving circuit is designed to adjust the hybrid switch current ratio to achieve the thermal balance of internal device, but the coupling relationship between loss and temperature is not considered. In [21], [22], the loss model of SiC/Si hybrid switch considering the electrothermal coupling relationship is established, and the junction temperature balance of internal devices of hybrid switch is realized by optimizing the switching control strategy. However, in the above studies on the loss model of the SiC/Si hybrid switch, the turn-off current spike is not considered.

For the turn-off current spike of SiC/Si hybrid switch, [23] proposed that the EMI would increase when the hybrid switch works in the pattern that SiC MOSFET switches before Si IGBT, and the turn-off delay time has a significant impact on EMI. In [24], by analyzing the switching process of SiC/Si hybrid switch, the existence of turn-off current spike is pointed out. In [25], the magnitude of turn-off current spike under different turn-off delay time was evaluated, but other circuit parameters were not researched, and the evaluation of turn-off current spike was still not comprehensive. When establishing the loss model of SiC/Si hybrid switch in [26], [27], the loss introduced by the turn-off current spike is considered. However, the power loss caused by the turn-off current spike is approximately calculated by the double pulse experimental results, which is not accurate enough. Since the turn-off current spike increases both the device current stress and the power loss of the SiC/Si hybrid switch, and also affect the setting of the dead time in the phase-leg configuration, it is necessary to evaluate the turn-off current spike to improve the efficiency and reliability of the converter. In [28], when SiC MOSFET switches before Si IGBT, EMI is effectively suppressed by reducing the switching frequency in the peak current region. In addition, under the gate control pattern that SiC MOSFET turns off later than Si IGBT, the turn-off current peak is well suppressed with the increase of turn-off delay time, but the influence of other circuit parameters is not considered [29].

In order to comprehensively evaluate the turn-off current spike of SiC/Si hybrid switch and reduce its impact as possible, a turn-off current spike suppression method considering reliability and optimal comprehensive loss is proposed. The method aims to reduce the current spike without affecting the comprehensive loss of hybrid switch. The turn-off loss model of SiC/Si hybrid switch is developed in Section II. In Section III, the main factors affecting the turn-off current spike are analyzed. Then the current stress and power loss are evaluated. In Section IV, a method to suppress the turn-off current spike is proposed, and the method is verified by experimental results. In Section V, some conclusions are given.

## II. TURN-OFF PROCESS MODEL OF HYBRID SWITCH

The schematic diagram of a SiC/Si hybrid switch is shown in Fig. 1. The hybrid switch is composed of low current rating SiC MOSFET and high current rating Si IGBT in parallel. It makes full use of the respective characteristics of the two devices and reduces the conduction loss of the hybrid switch.

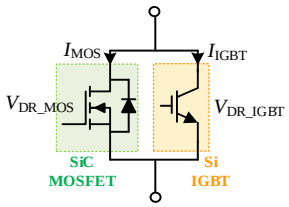



**FIGURE 1. Schematic diagram of a SiC/Si hybrid switch.**

In order to reduce the switching loss of the hybrid switch, the gate control pattern as shown in Fig. 2 is generally used. $V_{DR\_MOS}$, $V_{DR\_IGBT}$ are the driving voltage of SiC MOSFET and Si IGBT. $T_{on\_delay}$, $T_{off\_delay}$ are the turn-on delay time and turn-off delay time between SiC MOSFET and Si IGBT, respectively. In this gate control pattern, since the turn-on speed of Si IGBT is slower than that of SiC MOSFET, Si IGBT can realize zero-voltage turn-on when the turn-on delay time is zero. Also, since the Si IGBT turns off before the SiC MOSFET, the Si IGBT can achieve zero-voltage turn-off.

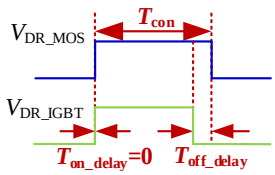



**FIGURE 2. Gate control pattern of the SiC/Si hybrid switch.**

In order to emulate operational conditions of a SiC/Si hybrid switch in the phase-leg configuration, a clamped inductive double-pulse test is used to model the turn-off behavior of the hybrid switch, as shown in Fig. 3.

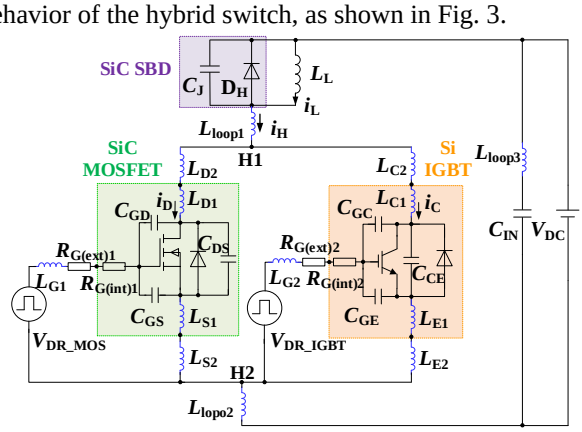



**FIGURE 3. Clamped inductive double-pulse test circuit.**

In Fig. 3, $V_{DC}$ is the bus voltage, $I_L$ is the load current. $D_H$ is the ideal SiC SBD, $C_J$ is the junction capacitance of SBD. $C_{GS}$, $C_{GD}$, and $C_{DS}$ are the parasitic capacitance of SiC MOSFET. $C_{GE}$, $C_{GC}$, and $C_{CE}$ are the parasitic capacitance of Si IGBT. $L_{G1}$, $L_{G2}$ are the gate loop parasitic inductance. $R_{G(int)1}$, $R_{G(int)2}$ are the internal resistance, $R_{G(ext)1}$, $R_{G(ext)2}$ are

the external driving resistance. $L_{D1}$, $L_{S1}$, $L_{C1}$, $L_{E1}$, $L_{loop1}$, $L_{loop2}$, $L_{loop3}$, $L_{D2}$, $L_{C2}$, $L_{S2}$, $L_{E2}$ are the parasitic inductance.

Figure 4 shows the turn-off waveform of SiC/Si hybrid switch considering parasitic parameters. The following will focus on the influence of turning of Si IGBT on the switching characteristics of SiC/Si hybrid switch.

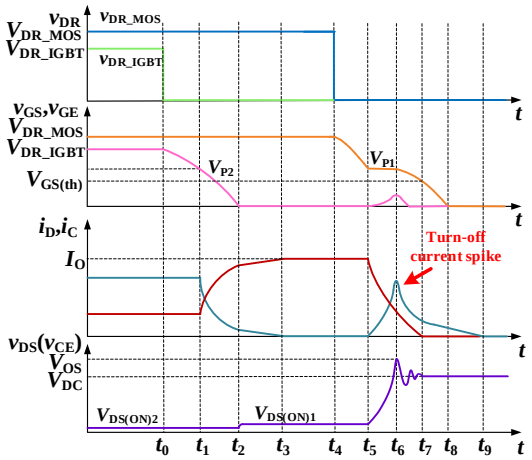



**FIGURE 4. Turn-off waveform of SiC/Si hybrid switch. From top to bottom: gate signal $v_{DR\_MOS}$ and $v_{DR\_IGBT}$, gate voltage $v_{GS\_MOS}$ and $v_{GS\_IGBT}$, drain current $i_D$ and collector current $i_C$, and drain-source voltage $v_{DS}$.**

At $t_5$, the voltage $v_{GS}$ decreases to $V_{P1}$, the voltage $v_{DS}$ rises slowly and the current $i_D$ starts to decrease, with the load current discharging the junction capacitance $C_J$ and output capacitance $C_{OSS2}$ (= $C_{CE}$ + $C_{GC}$). At the same time, the remnant carriers in the Si IGBT need to withstand the high d$v$/d$t$ during turn-off process, so there will be a very high rate of carrier extraction, thus causing the current spike. The magnitude of its carrier compound extraction current is related to the lifetime of the remnant carriers. In addition, the displacement current charged by the $C_{OSS2}$ will also be superimposed on the current spike. Therefore, the expression of turn-off current spike of SiC/Si hybrid switch is:

$$I_{C\_off\_peak}=\begin{cases}\left(I_L-i_{COSS2}\right)\cdot e^{-\tau\cdot T_{off\_delay}}+i_{COSS2}, T_{off\_delay}>t_{off\_IGBT}\\ I_L \qquad\qquad\qquad\quad , T_{off\_delay}\le t_{off\_IGBT}\end{cases} \tag{1}$$

Where

$$i_{COSS2}=C_{OSS2}\frac{\mathrm{d}v_{DS}}{\mathrm{d}t} \tag{2}$$

In (1), $t_{off\_IGBT}$ is the turn-off time of Si IGBT, $\tau$ is the time constant of Si IGBT turn-off current spike, and the magnitude is related to the carrier lifetime in the Si IGBT, which can be obtained by fitting the double pulse experiment. At the same time, the displacement current of $C_{GC}$ charging of Si IGBT will cause the positive spike of $v_{GE}$.

$$v_{GE}(t)=R_{G2}C_{GC}\cdot\frac{V_{P1}}{R_{G1}C_{GD}} \tag{3}$$

The turn-off loss $E_{off}$ of SiC/Si hybrid switch consists of three main components, which are SiC MOSFET's hard turn-off loss $E_{off\_MOS}$, SiC MOSFET's additional conduction loss $\Delta E_{con\_MOS\_off}$ during the turn-off delay time, and the loss caused by turn-off current spike $E_{off\_IGBT}$. The expressions of each component loss are as follows.

$$E_{off}=E_{off\_MOS}+\Delta E_{con\_MOS\_off}+E_{off\_IGBT} \tag{4}$$

$$E_{off\_MOS}=\int_{T_{off\_delay}}^{T_{off\_delay}+t_{off\_MOS}}v_{DS}\cdot i_D\mathrm{d}t \tag{5}$$

$$\Delta E_{con\_MOS\_off}=\int_{0}^{T_{off\_delay}}v_{DS}\cdot i_D\mathrm{d}t \tag{6}$$

$$E_{off\_IGBT}=\left(E_{hard\_off\_IGBT}-E_{oss\_off}\right)\cdot e^{-\tau\cdot t_{off\_delay}}+E_{res\_off} \tag{7}$$

where: $t_{off\_MOS}$ is the turn-off time of SiC MOSFET. $E_{off\_hard\_IGBT}$ is the hard turn-off loss of Si IGBT, $E_{oss\_off}$ is the loss of parasitic capacitance charging when Si IGBT is subjected to bus voltage.

It can be seen from (1) that the turn-off current spike is related to the degree of remnant carrier compounding and $i_{COSS2}$. Among them, the degree of remnant carrier compounding is related to the type of Si IGBT, driving parameters of Si IGBT, working conditions, and turn-off delay time $T_{off\_delay}$. $i_{COSS2}$ is affected by d$v$/d$t$, so the driving parameters of SiC MOSFET also affect the current spike.

## III. EVALUATION OF TURN-OFF CURRENT SPIKE

In this section, the simulation software LTspice is used to investigate the influencing factors of the turn-off current spike and their influence laws. The power devices used are SCT3060AL (650 V/27 A, SiC MOSFET) from Rohm and IKW40N60H3 (600 V/40 A, Si IGBT) from Infineon, and the simulation parameters are set as shown in Table I.

TABLE I
SIMULATION PARAMETERS FOR SIC/SI HYBRID SWITCH

| Symbol | Parameter | Value |
|---|---|---|
| $V_{DC}$ | bus voltage | 350 V |
| $I_L$ | load current | 25 A |
| $C_J$ | equivalent junction capacitance of SiC SBD | 80 pF |
| $T_{on\_delay}$ | turn-on delay time | 0 μs |
| $T_{off\_delay}$ | turn-off delay time | 0.5 μs |
| $V_{DR\_MOS}$ | driving voltage of SiC MOSFET | 18 V / −2 V |
| $R_{G1}$ | driving resistance of SiC MOSFET | 12 Ω |
| $L_{G1}$ | gate parasitic inductance of SiC MOSFET | 40 nH |
| $V_{DR\_IGBT}$ | driving voltage of Si IGBT | 15 V / −5 V |
| $R_{G2}$ | driving resistance of Si IGBT | 10 Ω |
| $L_{G2}$ | gate parasitic inductance of Si IGBT | 40 nH |

### A. DEGREE OF REMNANT CARRIER COMPOUNDING

#### 1) TYPE OF SI IGBT

At present, the Trench and Fieldstop technology eliminates the parasitic JFET region in IGBT, so that IGBT can not only obtain low saturation voltage drop, but also ensure sufficient breakdown voltage. Infineon launched IGBT 3 with Trench and Fieldstop technology in 2000, and then launched TRENCHSTOP™ 5 series by adjusting the spacing of trench, which can basically eliminate the current tailing of IGBT. Obviously, the different trench spacing will affect the degree

of remnant carrier. In order to explore its influence degree, Si IGBTs with different Infineon's technologies will be compared and tested as shown in Table 2.

TABLE II
MAIN PARAMETERS OF DIFFERENT IGBTS

| Si IGBT | Rating | $C_{GC}$ | Switching frequency |
|---|---|---|---|
| IKW50N60H3 (IGBT 3) | 600 V/50 A | 96pF | 20 k~100 kHz |
| IKW40N60H3 (IGBT 3) | 600 V/40 A | 64pF | 20 k~100 kHz |
| IKW30N65ES5 (IGBT 5) | 650 V/39.5 A | 7pF | 10 k~30 kHz |
| IKW30N65ET7 (IGBT 7) | 650 V/39.1 A | 62pF | 5 k~40 kHz |

The turn-off characteristics of SiC/Si hybrid switch with different IGBTs is shown in Fig. 5. It can be seen that the gate voltage spike and turn-off current spike in IGBT 3 are more obvious due to the wider trench spacing. It can be seen from (3) that due to different gate-collector capacitance $C_{GC}$, the gate voltage spike caused by the same d$v_{DS}$/d$t$ are different. At the same time, due to the existence of common source parasitic inductance in the package, the measured voltage spike is also related to the current spike change rate d$i$/d$t$. SiC MOSFET's hard turn-off loss $E_{off\_MOS}$ decreases as the drain-source voltage $v_{DS}$ spike decreases. Additional conduction loss $\Delta E_{con\_MOS\_off}$ due to constant $T_{off\_delay}$ is basically unchanged, IGBT's turn-off loss $E_{off\_IGBT}$ decreases with the decrease of current spike. Considering the current stress and total turn-off loss $E_{off}$, when the switching frequency is less than 40 kHz, it is recommended to select IGBT 7 for SiC/Si hybrid switch, and when the frequency is 40 kHz ~100 kHz, it is recommended to select IGBT 3 with smaller current rating for SiC/Si hybrid switch.

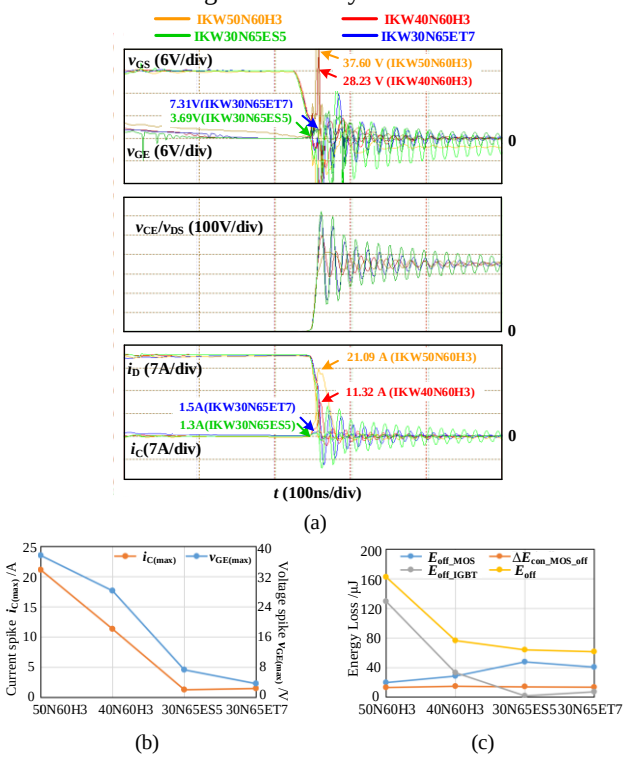



**FIGURE 5. The effect of different Si IGBTs on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

### 2) TURN-OFF DELAY TIME

The turn-off characteristics of SiC/Si hybrid switch with different turn-off delay time $T_{off\_delay}$ is shown in Fig. 6. When $T_{off\_delay}$ =0.1 μs, due to the slower turn-off speed of Si IGBT, when the SiC MOSEFT completely turns off, the load current is all transferred to the IGBT, which makes the Si IGBT produce hard switching loss. As $T_{off\_delay}$ increases, the turn-off current spike decreases from 31.63 A to 11.16 A, and at the same time, the voltage spike of $v_{DS}$ increases and stabilizes at about 480 V.

As can be seen from Fig. 6, under the condition that d$v$/d$t$ is basically constant, when $T_{off\_delay} \leq 0.2$ μs, the Si IGBT turns off later than SiC MOSFET, and the interaction between the common source parasitic inductance in the Si IGBT package and large d$i$/d$t$ causes the peak of $v_{GE}$. When $T_{off\_delay} > 0.2$ μs, the SiC MOSFET turns off later and the peak of $v_{GE}$ tends to be constant. When $T_{off_delay} < 0.9$μs, the current spike and its resulting loss $E_{off\_IGBT}$ decreases as $T_{off\_delay}$ increases. When $T_{off\_delay} > 0.9$ μs, the degree of Si IGBT carrier compound will be independent of time and the current spike and $E_{off\_IGBT}$ no longer decreases, but the increase of $T_{off\_delay}$ will increase the additional conduction loss of SiC MOSFET. According to the total turn-off loss curve, it can be seen that there is an optimal point for minimum loss, comprehensive consideration of turn-off current spike and $E_{off}$, $T_{off\_delay}$ is recommended to be 0.4 μs.

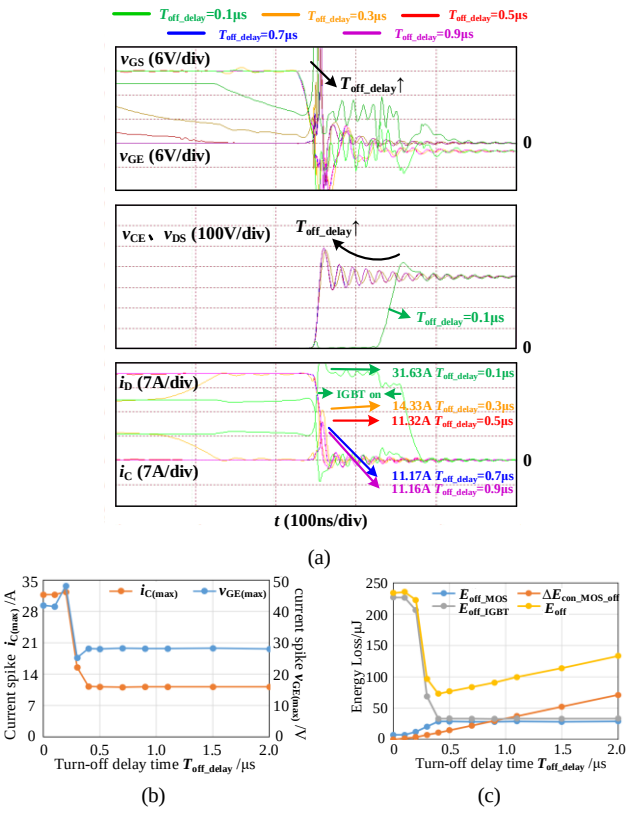



**FIGURE 6. The effect of turn-off delay time on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

### 3) TURN-OFF DRIVING VOLTAGE OF SI IGBT

When the turn-off driving voltage of Si IGBT is set to 0 V, −2 V, −4 V, −6 V, and −8 V, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 7. As the absolute value of the turn-off driving voltage increases, the width of the internal $N^-$ based space charge region increases after Si IGBT turns off, which reduces the carrier storage region, so the number of remnant carriers decreases, and the turn off current peak decreases from 11.32 A to 3.58 A.

When the absolute value of Si IGBT's turn-off driving voltage is less than 4 V, the peak value of gate voltage decreases with the decrease of the d$i$/d$t$ of turn-off current spike under the condition that d$v$/d$t$ is basically unchanged. When the absolute value of turn-off voltage is greater than 4V, the turn-off current spike does not change with the turn-off voltage, and the voltage spike also tends to be constant. With the increase of Si IGBT's turn-off driving voltage, SiC MOSFET's hard turn-off loss $E_{\text{off\_MOS}}$ increases. At the same time, the transfer time of current from Si IGBT to SiC MOSFET is reduced, and the SiC MOSFET's additional conduction loss $\Delta E_{\text{con\_MOS\_off}}$ increases. Finally, as the turn-off current spike decreases, $E_{\text{off\_IGBT}}$ decreases. Considering current spike and turn-off loss, the absolute value of turn-off driving voltage for Si IGBT should be greater than 4 V.

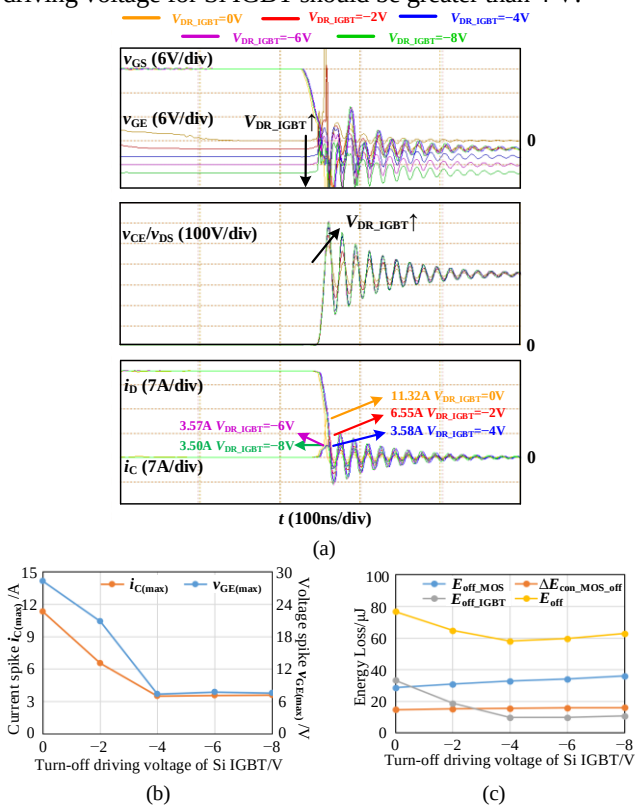



**FIGURE 7. The effect of Si IGBT's turn-off driving voltage on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

### 4) TURN-OFF DRIVING RESISTANCE OF SI IGBT

When the turn-off driving resistance of Si IGBT is set to 5 Ω, 10 Ω, 15 Ω, 20 Ω, and 25 Ω respectively, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 8. As the Si IGBT's turn-off driving resistance increases, the width of the internal $N^-$ based space charge region decreases after Si IGBT turns off, which increases the carrier storage area. Therefore, the number of remnant carriers increases, and the turn-off current peak increases from 9.6 A to 14.21 A. The additional rise of turn-off driving resistance for Si IGBT will make Si IGBT turn off later than SiC MOSFET, resulting in hard turn-off loss of Si IGBT.

Under the condition that d$v$/d$t$ is basically unchanged, the increase of turn-off driving resistance and current spike will result in higher peak value of $v_{GE}$. With the increase of turn-off driving resistance, the peak value of $v_{DS}$ decreases, and the SiC MOSFET's hard turn-off loss $E_{\text{off\_MOS}}$ decreases. At the same time, the transfer time of current from Si IGBT to SiC MOSFET increases, and SiC MOSFET's additional conduction loss $\Delta E_{\text{con\_MOS\_off}}$ decreases. Finally, the increase of the turn-off current spike results in higher $E_{\text{off\_IGBT}}$. When the turn-off driving resistance is greater than 15 Ω, Si IGBT's turn-off time $t_{\text{off\_IGBT}}$ is larger than $T_{\text{off\_delay}}$, so Si IGBT's turn-off loss $E_{\text{off\_IGBT}}$ will also include some hard turn-off loss. Considering the turn-off current spike and turn-off loss, the Si IGBT's turn-off driving resistance should be smaller.

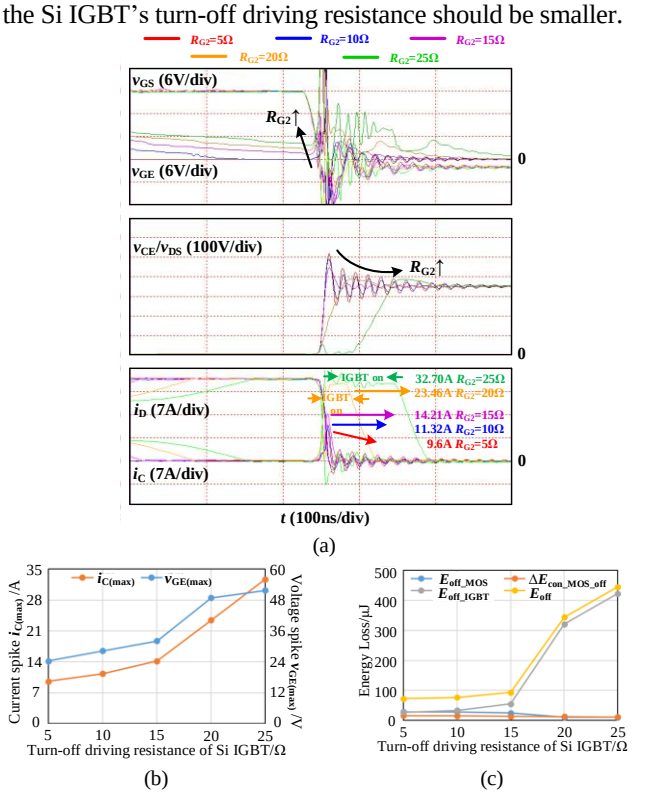



**FIGURE 8. The effect of Si IGBT's turn-off driving resistance on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

### 5) LOAD CURRENT

When the load current is set to 5 A, 10 A, 15 A, 20 A, and 25 A respectively, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 9. With the increase of load current, the current flows though Si IGBT and the number of carriers increases. Therefore, the turn-off current spike increases from 2.44 A to 11.32 A. At the same time, the peak value of $v_{DS}$ increased from 400 V to 490 V. SiC MOSFE's hard turn-off loss $E_{off\_MOS}$ and additional conduction loss $\Delta E_{con\_MOS\_off}$ increases with the increase of $I_L$. Si IGBT's turn-off loss $E_{off\_IGBT}$ increases with the increase of current spike, so the total turn-off loss $E_{off}$ increases.

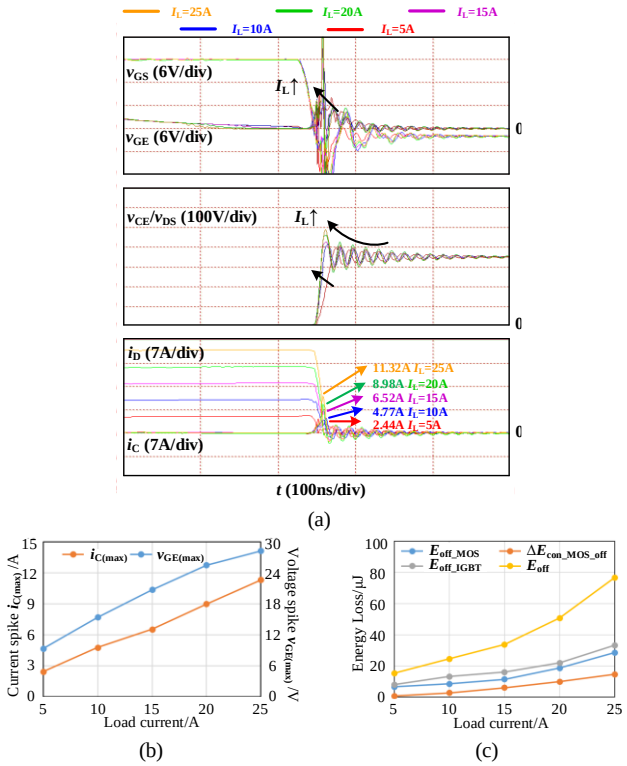



**FIGURE 9. The effect of load current on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

#### 6) BUS VOLTAGE

When the bus voltage is set to 150 V, 200 V, 250 V, 300 V, and 350 V, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 10. With the increase of bus voltage, Si IGBT needs to quickly remove the remnant carriers in its drift region, so the turn-off current spike increases from 3.2 A to 11.32 A. The increase of bus voltage makes the SiC MOSFE's hard turn-off loss $E_{off\_MOS}$ increase, and the increase of current spike results in higher Si IGBT's turn-off loss $E_{off\_IGBT}$. Finally, the total turn-off loss $E_{off}$ increases. Therefore, this paper analyzes the current spike suppression method under the working condition of maximum load current and bus voltage.

### *B. SWITCHING SPEED OF HYBRID SWITCH*

#### 1) TURN-OFF DRIVING VOLTAGE OF SIC MOSFET

When the turn-off driving voltage of SiC MOSFET is set to 0 V, −2 V, −4 V, −6 V, and −8 V, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 11. As the absolute value of the turn-off driving voltage increases, the increase of the voltage slew rate d$v_{DS}$/d$t$ and remnant carrier extraction rate of the Si IGBT make the turn-off current spike increase from 10.45 A to 12.28 A. It can be seen that increasing SiC MOSFET's turn-off driving voltage can reduce the SiC MOSFET's hard turn-off loss $E_{off\_MOS}$, but does not affect the SiC MOSFET's additional conduction loss $\Delta E_{con\_MOS\_off}$. Since the change of current spike is not obvious, $E_{off\_IGBT}$ is basically unchanged, thus the total turn-off loss $E_{off}$ increases.

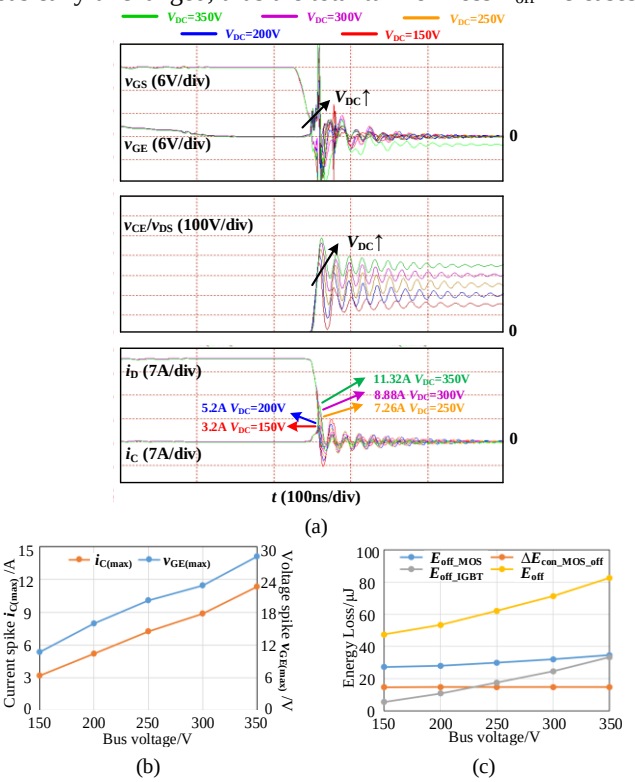



**FIGURE 10. The effect of bus voltage on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

#### 2) TURN-OFF DRIVING RESISTANCE OF SIC MOSFET

When the turn-off driving resistance of SiC MOSFET is set to 12 Ω, 17 Ω, 22 Ω, 27 Ω, and 32 Ω respectively, the turn-off characteristics of SiC/Si hybrid switch are shown in Fig. 12. As the turn-off driving resistance increases, the peak value of $v_{DS}$ decreases from 500 V to 440 V due to the decrease of the turn-off current slew rate d$i$/d$t$. At the same time, the d$v_{DS}$/d$t$ is significantly reduced, and the extraction rate of Si IGBT's remnant carriers is reduced, which reduces the current spike from 11.32 A to 0.92 A. At the same time, the SiC MOSFET's hard turn-off loss $E_{off\_MOS}$ increases significantly, while Si IGBT's turn-off loss $E_{off\_IGBT}$ decreases and the additional conduction loss $\Delta E_{con\_MOS\_off}$ is basically unchanged. In general, since the turn-off driving resistance of SiC MOSFET has the greatest influence on $E_{off\_MOS}$, the total turn-off loss $E_{off}$ increases.

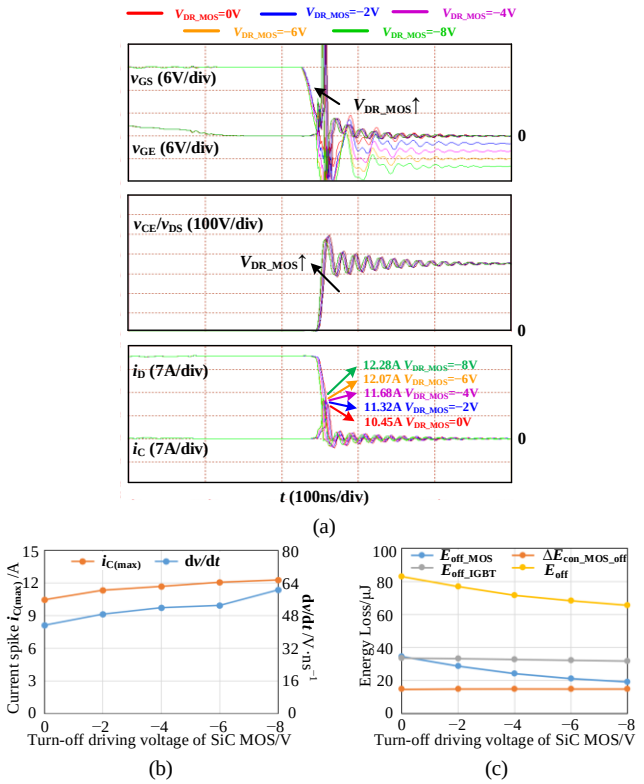



**FIGURE 11.** **The effect of SiC MOSFET's turn-off driving voltage on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

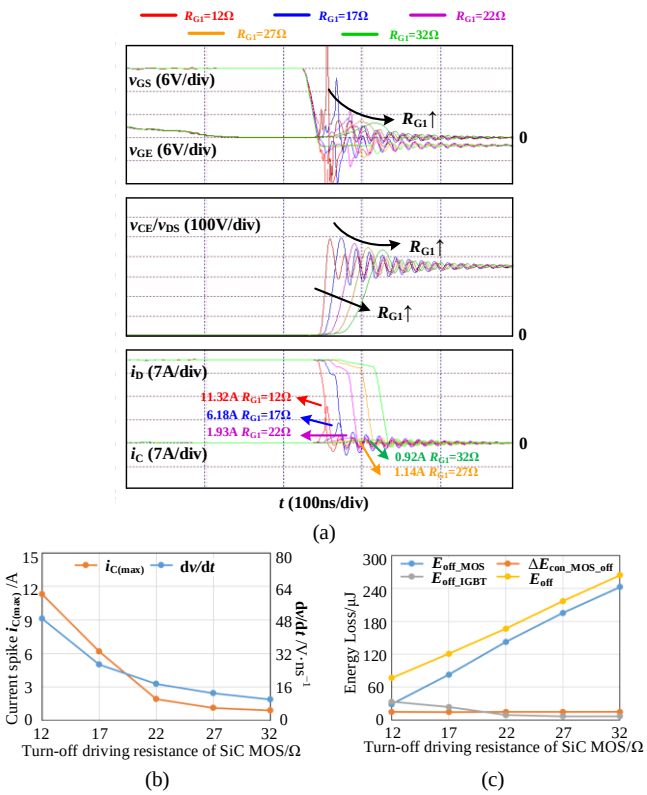



**FIGURE 12.** **The effect of SiC MOSFET's turn-off driving resistance on turn-off characteristics. (a) Turn-off waveform. (b) Turn-off voltage & current spike. (c) Turn-off loss.**

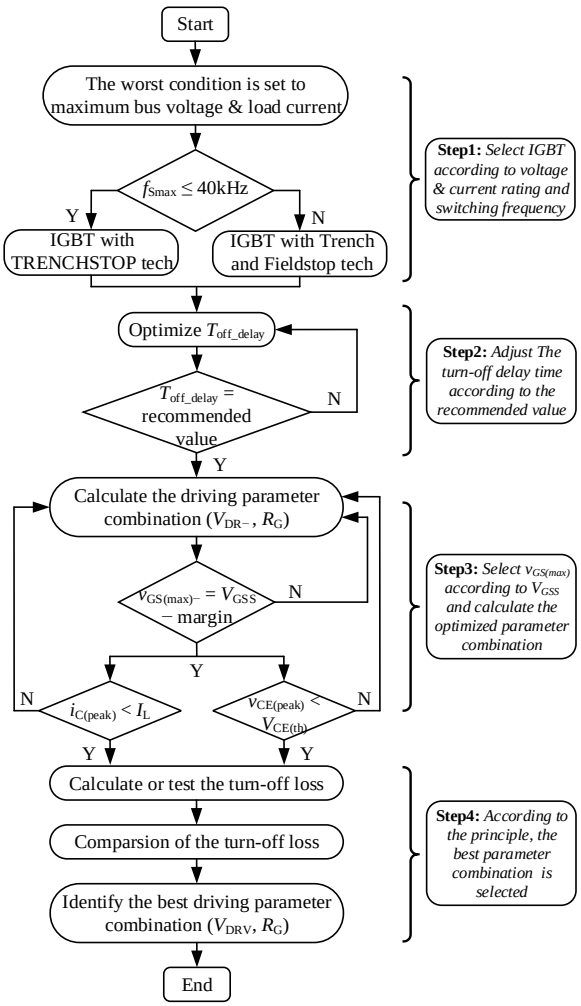



**FIGURE 13.** **Methodology for suppressing turn-off current spike of SiC/Si hybrid switch.**

## IV. SUPPRESSION METHOD OF TURN-OFF CURRENT SPIKE

Based on the above evaluation of the factors affecting the turn-off current spike, we propose a method to suppress the current spike, as shown in Fig. 13. This method is divided into 4 steps to illustrate the process of suppressing turn-off current spike. The main steps are described as follows.

Step I: Since the maximum value of turn-off current spike occurs at the largest voltage and current rating, it is necessary to optimize the parameters under this working condition. The appropriate Si IGBT type can be selected according to the switching frequency of the SiC/Si hybrid switch.

Step II: The turn-off delay time $T_{off\_delay}$ affects not only the value of current spike, but also the SiC MOSFET's additional conduction loss. Therefore, $T_{off\_delay}$ should be adjusted according to the recommended value.

Step III: In order to ensure the gate reliability, there is a margin between the maximum allowable negative gate-source voltage $v_{GS(max)-}$ and the gate-source withstand voltage $V_{GSS}$. Then the driving parameters combination ($V_{DR}$, $R_G$) is calculated according to the $v_{GS(max)-}$.

Step IV: Since the turn-off loss $E_{off}$ is different under different driving parameters, the driving parameters should be determined according to the principle of optimal loss.

In order to verify the effects of the suppression method on the turn-off current spike and comprehensive loss, a double-pulse test platform as shown in Fig. 14 is built to test the turn-off characteristics of SiC/Si hybrid switch. The power devices used in the test are SCT3060AL (650 V/27 A, SiC MOSFET), IKW40N60H3 (600 V/40 A, Si IGBT) and SCS240AE (650 V/40 A, SiC SBD).

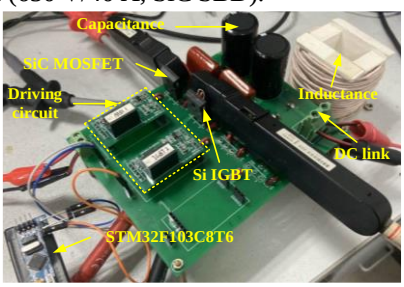



**FIGURE 14. Double pulse test platform for SiC/Si hybrid switch.**

### A. SELECTION OF Si IGBT TYPE

When different types of Si IGBT are selected, the turn-off characteristics of SiC/Si hybrid switch are shown in Fig. 15. IKW50N60H3 and IKW40N60H3 are two Si IGBTs with different current ratings, IKW40N60H3, IKW30N65ES5, and IKW30N65ET7 are three Si IGBTs with the same current rating but different trench technologies. It can be seen that IGBT 3 has the larger turn-off current spike than IGBT with TRENCHSTOP™ technology. The higher the current rating, the smaller the saturation voltage $V_{CE(sat)}$, the more carriers involved in conduction and the higher the turn-off current spike. According to the principle of optimal loss, when the switching frequency is less than 40kHz, the IGBT of TRENCHSTOP™ technology should be selected, and when the switching frequency is 40 kHz ~ 100 kHz, it is recommended to select IGBT 3 with smaller current rating.

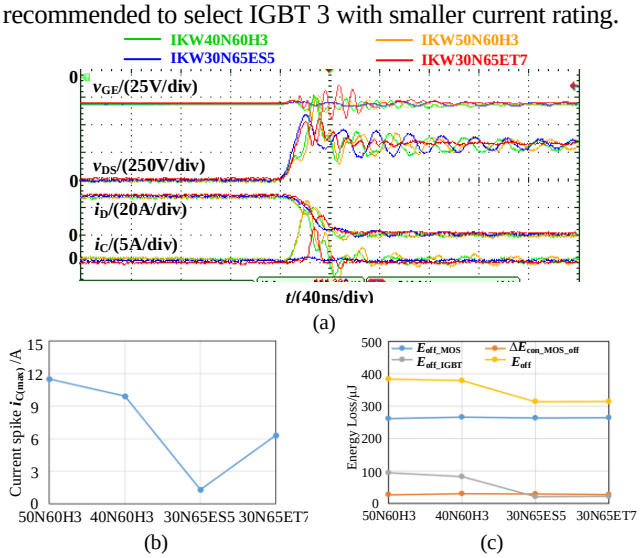



**FIGURE 15. Experimental results under different Si IGBTs. (a) Turn-off waveform. (b) Turn-off current spike. (c) Turn-off loss.**

### B. OPTIMIZATION OF TURN-OFF DELAY TIME

Increasing the turn-off delay time $T_{off\_delay}$ of SiC/Si hybrid switch will make the additional conduction loss $\Delta E_{con\_MOS\_off}$ increase linearly, and make Si IGBT's turn-off loss $E_{off\_IGBT}$ decrease, so there is an optimal turn-off loss $E_{off}$, and the optimal turn-off delay time is selected according to the principle of optimal turn-off loss.

When the $T_{off\_delay}$ is set to 0.1 μs to 3.0 μs, the turn-off characteristics of SiC/Si hybrid switch is shown in Fig. 16. It can be seen that when the $T_{off\_delay}$ is 0.1 μs, the IGBT turns off later and generates hard turn-off loss of 450 μJ, due to the Si IGBT's turn-off time is more than 0.1 μs. With the increase of $T_{off\_delay}$, the turn-off current peak decreases from 13.3 A to 3.9 A, which reduces the loss $E_{off\_IGBT}$ by 73.23 %.

Therefore, it is recommended to set $T_{off\_delay}$ to 0.5 μs when considering the turn-off loss under the working conditions of 350 V/25 A, which is close to the simulation results.

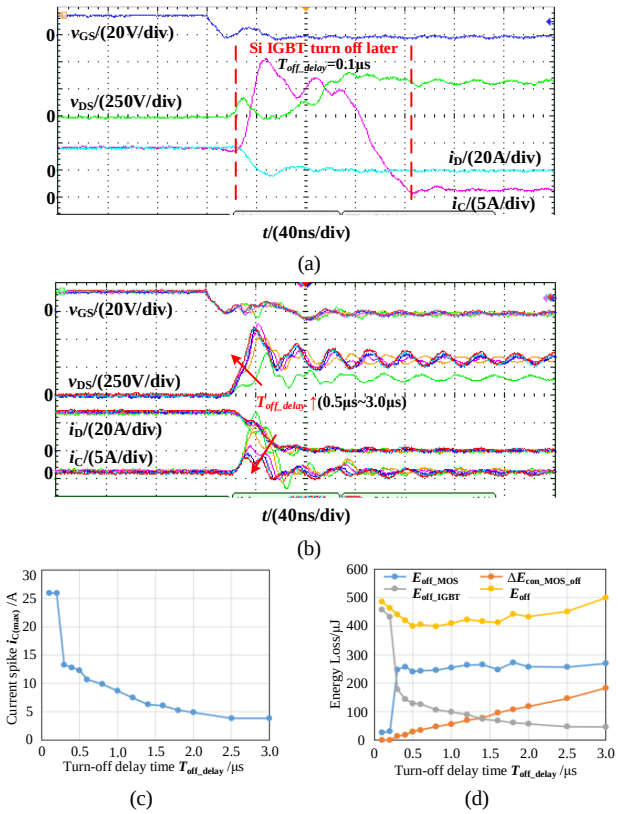



**FIGURE 16. Experimental results under different turn-off delay time. (a) Turn-off waveform, Si IGBT turn off later. (b) Turn-off waveform, SiC MOSFET turn off later. (c) Turn-off current spike. (d) Turn-off loss.**

### C. OPTIMIZATION OF DRIVING PARAMETERS

There is parasitic inductance in the driving circuit, which will cause gate oscillation. It is necessary to set the reasonable driving resistance and driving voltage to ensure the gate safety. Therefore, the turn-off current spike, turn-off loss and reliability should be comprehensively considered to optimize the driving parameters of SiC/Si hybrid switch. Firstly, the maximum negative voltage $V_{GS\,(max)-}$ and $V_{GE(max)-}$ is limited to be constant, then adjust the driving parameters, and the

optimization parameters are selected according to the principle of optimal turn-off loss. Obviously, as the driving resistance increases, the driving voltage can also be increased to improve the switching speed without affecting the safety.

### 1) TURN-OFF DRIVING PARAMETERS OF SI IGBT

For the Si IGBT's driving parameters, the increase of turn-off driving resistance $R_{G2}$ will make the turn-off time $t_{off\_IGBT}$ increase. In order to prevent Si IGBT from producing hard turn-off loss due to slow turn-off speed, $t_{off\_IGBT}$ needs to be smaller than $T_{off\_delay}$, so there is a maximum value for $R_{G2}$.

$$R_{G2} \le \frac{T_{off\_delay}}{2.3C_{ISS2} + C_{RSS2}\dfrac{V_{DS}}{V_{P2} - V_{DR\_IGBT-}}} \tag{8}$$

Within this range, when $R_{G2}$ increases, the turn-off loss $E_{off}$ will also increase, so $R_{G2}$ should be as small as possible. However, if the driving circuit becomes under-damped, the driving voltage can only be reduced correspondingly to ensure $V_{GE(max)-}$, which may increase the turn-off loss.

Increasing the absolute value of turn-off driving voltage $V_{DR\_IGBT-}$ can suppresses the turn-off current spike obviously, but when the absolute value of $V_{DR\_IGBT-}$ increases to 4 V, its improvement on the turn-off loss will not be obvious. At the same time, it is necessary to increase the driving resistance to ensure $V_{GE(max)-}$, which may also increase the turn-off loss.

In order to select the optimal combination of driving parameters, $V_{GE(max)-}$ is set to −15 V, and when $L_{G2}$ is 48 nH, the driving circuit's damping ratio is set to 0.55, 0.75, 0.95, 1.15, and 1.35 respectively, the turn-off characteristics is shown in Fig. 17. Due to the allowable high negative gate voltage of Si IGBT, its turn-off driving voltage $V_{DR\_IGBT-}$ can be set higher, so the change of turn-off current spike is not obvious when the absolute value of turn-off driving voltage $V_{DR\_IGBT-}$ is larger than 6 V. At the same time, the Si IGBT's driving circuit has no obvious effect on other loss, so the turn-off loss does not change significantly with the driving circuit parameters. In general, the turn-off driving parameters of Si IGBT must first ensure that $R_{G2}$ does not exceed the maximum value, and then set a large turn-off voltage to reduce the current spike. Here, the turn-off driving parameters of Si IGBT is (10.7 Ω, − 6.5 V), and the damping ratio of the driving circuit is 1.15.

### 2) TURN-OFF DRIVING PARAMETERS OF SIC MOSFET

For the driving parameters of SiC MOSFET, increasing the turn-off driving resistance $R_{G1}$ can reduce d$v$/d$t$ more effectively than increasing the turn-off driving voltage $V_{DR\_MOS-}$, but it will cause larger $E_{off\_MOS}$. Considering the comprehensive turn-off loss $E_{off}$, $R_{G1}$ should not be too large.

Similarly, increasing the turn-off driving voltage $V_{DR\_MOS-}$ can reduce $E_{off\_IGBT}$, but the allowable negative gate voltage of SiC MOSFET is lower and the turn-off oscillation caused by switching speed is more serious, so it is difficult to change the turn-off driving voltage significantly.

In order to select the optimal combination of driving parameters, $V_{GS(max)-}$ is set to –3 V, and when $L_{G1}$ is 42 nH, the driving circuit's damping ratio is set to 0.64, 0.74, 0.84, 0.94, and 1.04 respectively, the turn-off characteristics is shown in Fig. 18. Since the allowable negative gate voltage of SiC MOSFET is very low, 16 Ω driving resistance is required to suppress the turn-off oscillation and prevent the gate voltage from exceeding $V_{GS(max)-}$. When the driving parameters can ensure the gate reliability, increasing $R_{G1}$ will make the SiC MOSFET's turn-off loss $E_{off\_MOS}$ increase significantly, while making the loss $E_{off\_IGBT}$ decrease at the same time. The experimental results show that the optimal combination of SiC MOSFET's driving parameters is (18 Ω, −2 V), and the damping ratio of the driving circuit is 0.94.

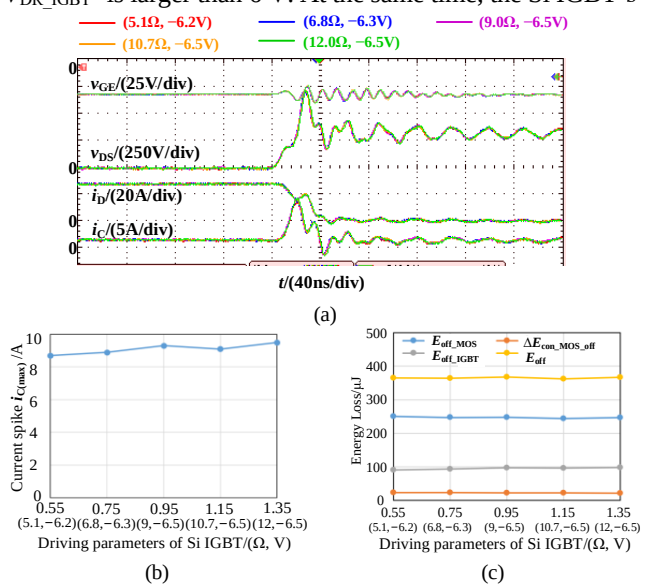



**FIGURE 17. Experimental results under different Si IGBT's turn-off driving parameters. (a) Turn-off waveform. (b) Turn-off current spike. (c) Turn-off loss.**

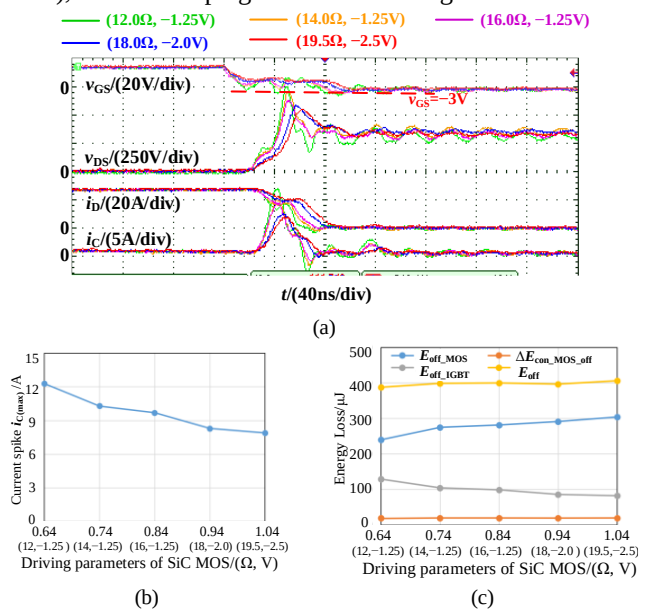



**FIGURE 18. Experimental results under different Si IGBT's turn-off driving parameters. (a) Turn-off waveform. (b) Turn-off current spike. (c) Turn-off loss.**

## V. CONCLUSIONS

The turn-off current spike of SiC/Si hybrid switch is formed by the remnant carriers in the carrier storage area of Si IGBT bearing the high d*v*/d*t* during the turn-off process. In this paper, the influence factors and rules of turn-off current spike are evaluated, and a new turn-off current spike suppression method is proposed to weaken the current spike and optimize the turn-off loss. Through the double pulse experiment, the influence of Si IGBT's type, turn-off delay time and driving parameters on the turn-off current spike is verified. Combined with the principle of optimal loss, the optimal parameters are given to verify the effectiveness of the turn-off current spike suppression method. When the hybrid switch is composed of SiC MOSFET (SCT3060AL) and Si IGBT (IKW40N60H3), the optimal turn-off delay time is set to 0.5 μs. According to the Si IGBT's driving parameters, in order to ensure the gate reliability and reduce the turn-off current spike, the turn-off negative voltage of −6 V should be set first. For the SiC MOSFET's driving parameters, in order to ensure the gate reliability, the damping ratio greater than 0.84 should be set first, and then the design should be carried out in combination with other driving parameters.

## REFERENCES

[1] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang and Y. Zhang, "Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1181-1196, Feb. 2019.

[2] W. Zhou and X. Yuan, "Experimental evaluation of SiC MOSFETs in comparison to Si IGBTs in a soft-switching converter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 5, pp. 5108-5118, Sept.-Oct. 2020.

[3] R. Wang, L. Tan, C. Li, T. Huang, H. Li and X. Huang, "Analysis, design, and implementation of junction temperature fluctuation tracking suppression strategy for SiC MOSFETs in wireless high-power transfer," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 1193-1204, Jan. 2021.

[4] C. Wei, J. Shao, B. Agrawal, D. Zhu and H. Xie, "New surface mount SiC MOSFETs enable high efficiency high power density Bi-directional on-board charger with flexible DC-link voltage," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, 2019, pp. 1904-1909.

[5] H. Sheng, Z. Chen, F. Wang and A. Millner, "Investigation of 1.2 kV SiC MOSFET for high frequency high power applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Palm Springs, CA, USA, 2010, pp. 1572-1577.

[6] Y. Cui, M. S. Chinthavali, F. Xu and L. M. Tolbert, "Characterization and modeling of silicon carbide power devices and paralleling operation," in *Proc. IEEE Int. Symp. Ind. Electron.*, Hangzhou, China, 2012, pp. 228-233.

[7] Y. M. Jian, G. C. Hua, F. X. Yang, and F. C. Lee, "Soft-switching of IGBT's with the help of MOSFET's," in *Proc. VPEC Power Electron. Seminar*, Blacksburg, VA, USA, Sep. 1992, pp. 77–84.

[8] Z. Li e*t al.*, "A novel gate driver for Si/SiC hybrid switch for multi-objective optimization," *IET Power Electron.*, vol. 14, no, 2, pp. 422-431, Oct. 2020.

[9] Z. Peng *et al.*, "Adaptive gate delay-time control of Si/SiC hybrid switch for efficiency improvement in inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3437-3449, March 2021.

[10] A. Deshpande and F. Luo, "Design of a silicon-WBG hybrid switch," in *Proc. IEEE 3rd Workshop on Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 296-299.

[11] Z. Li *et al.*, "Optimal control strategies for SiC MOSFET and Si IGBT based hybrid switch," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, San Antonio, TX, USA, 2018, pp. 1717-1721.

[12] M. Rahimo *et al.*, "Characterization of a silicon IGBT and silicon carbide MOSFET cross-switch hybrid," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4638-4642, Sept. 2015.

[13] R. A. Minamisawa, U. Vemulapati, A. Mihaila, C. Papadopoulos and M. Rahimo, "Current sharing behavior in Si IGBT and SiC MOSFET cross-switch hybrid," *IEEE Electron Device Lett.*, vol. 37, no. 9, pp. 1178-1180, Sept. 2016.

[14] U. R. Vemulapati, A. Mihaila, R. A. Minamisawa, F. Canales, M. Rahimo and C. Papadopoulos, "Simulation and experimental results of 3.3kV cross switch "Si-IGBT and SiC-MOSFET" hybrid," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs*, 2016, pp. 163-166.

[15] A. Q. Huang, X. Song and L. Zhang, "6.5 kV Si/SiC hybrid power module: An ideal next step?," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Chicago, IL, USA. 2015, pp. 64-67.

[16] X. Song and A. Q. Huang, "6.5kV FREEDM-Pair: Ideal high power switch capitalizing on Si and SiC," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, Geneva, Switzerland, 2015, pp. 1-9.

[17] C. Zeng et al., "Comparison of SiC Synchronous rectification and schottky diode in voltage source inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Portland, OR, USA, 2018, pp. 1903-1906.

[18] A. Deshpande and F. Luo. "Practical design considerations for a Si IGBT + SiC MOSFET hybrid switch: parasitic interconnect influences, cost, and current ratio optimization." *IEEE Trans. Power Electro.*, vol. 34, no. 1, pp. 724-737, Jan. 2019.

[19] F. Yuan *et al.*, "Sizing selection optimization of SiC/Si hybrid switch in DC/DC buck converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Portland, OR, USA, 2018, pp. 6160–6164.

[20] Y. Wei, D. Woldegiorgis, R. Sweeting and A. Mantooth, "Four control freedoms AGD for hybrid SiC MOSFET and Si IGBT application," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Phoenix, AZ, USA, 2021, pp. 2211-2216.

[21] Z. He, Z. Li, J. Yu, X. Jiang and J. Wang, "Multi-objective optimization control strategy for SiC/Si hybrid switches," in *Proc. IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, USA, 2019, pp. 4558-4561.

[22] Z. He, Z. Li, F. Yuan, C. Zeng, X. Jiang and J. Wang, "Active thermal control of SiC/Si hybrid switch," in *Proc. IEEE Int. Power Electron. Appl. Conf. Expo.*, Shenzhen, China, 2018, pp. 1-4.

[23] X. Peng, J. Wang, Z. Peng, Z. Liu, M. Li and Y. Dai, "Study on the CM EMI characteristics of Si/SiC hybrid switch based converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Orleans, LA, USA, 2020, pp. 2565-2569.

[24] H. Qin, D. Wang, Y. Zhang, D. Fu and C. Zhao, "Characteristics and switching patterns of Si/SiC hybrid switch," in *Proc. PCIM Asia, Int. Exhib. Conf. Power Electron., Intell. Motion, Renewable Energy Manage.*, Shanghai, China, 2017, pp. 1-6.

[25] H. Qin, R. Wang, Q. Xun, W. Chen and S. Xie, "Switching time delay optimization for "SiC+Si" hybrid device in a phase-leg configuration," *IEEE Access*, vol. 9, pp. 37542-37556, Jan. 2021.

[26] Z. Li, J. Wang, B. Ji and Z. J. Shen, "Power loss model and device sizing optimization of Si/SiC hybrid switches," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8512-8523, Aug. 2020.

[27] Z. Peng *et al.*, "A variable-frequency current-dependent switching strategy to improve tradeoff between efficiency and SiC MOSFET overcurrent stress in Si/SiC-hybrid-switch-based inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4877-4886, April 2021.

[28] L. Ou *et al.*, "An EMI suppression strategy for Si/SiC hybrid switch based single-phase inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Detroit, MI, USA, 2020, pp. 3548-3551.

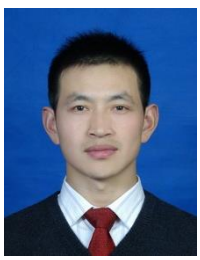
[29] Z. Li *et al.*, "Active gate delay time control of Si/SiC hybrid switch for junction temperature balance over a wide power range," *IEEE Trans. Power Electro.*, vol. 35, no. 5, pp. 5354-5365, May 2020.

**Haihong Qin** (Member, IEEE) was born in Jiangsu Province, China, in 1977. He obtained his Bachelor's degree in Aviation Electrical and Electronic Engineering, Master's Degree, and Doctorate in Power Electronics and Motion Control from Nanjing University of Aeronautics and Astronautics, in 1998, 2002, and 2007, respectively. He joined the Aero-power Sci-tech Center in Nanjing University of Aeronautics and Astronautics in 2007. Currently, he is an associate professor of the Department of Electrical Engineering in Nanjing University of Aeronautics and Astronautics. His research interests include power electronics and motion control and applications of wide bandgap devices in more electric aircraft.

**Sixuan Xie** was born in Zhejiang Province, China, in 1998. She received the B.S. degree from the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, in 2020, where she is currently pursuing the M.S. degree. Her research interests include power electronics and wide band-gap devices and its applications.

**Zhenhua Ba** was born in Henan Province, China, in 1999. He received the B.S. degree from the College of Mechanical and Electrical Engineering and Vehicle Engineering of Chongqing Jiaotong University, in 2022. He is currently pursuing the M.S. degree in the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include power electronics and wide band-gap devices and its applications.

**Xiang Liu** was born in Guangdong Province, China, in 1998. He received the B.S. degree from the College of Automation Engineering, Guangdong University of Technology, in 2021. He is currently pursuing the M.S. degree in the College of Automation Engineering, Nanjing University of Aeronautics and Astronautics. His research interests include power electronics and wide band-gap devices and its applications.



**Wenming Chen** was born in 1981 in China. He received his B.S. degree in College of Automation Engineering from Nanjing University of Aeronautics and Astronautics in 2005. From 2005 to 2018, he is working as a technical teacher in College of Automation Engineering in Nanjing University of Aeronautics and Astronautics. Since 2019, he is the laboratory technical director of the department of Electrical Engineering in Nanjing University of Aeronautics and Astronautics. He is responsible for experimental and testing technical guidance. His current research interests include the testing of wide band-gap devices and power electronic devices.

**Dafeng Fu** was born in 1977 in China. He received his B.S. degree in College of Automation Engineering from Nanjing University of Aeronautics and Astronautics in 2002. From 2002, he is working as a lecturer in College of Automation Engineering in Nanjing University of Aeronautics and Astronautics. Since 2018, he is the vice director of the department of Electronics Engineering in Nanjing University of Aeronautics and Astronautics. His current research interests include the design and testing of power electronic apparatus.

**Qian Xun** (Graduate Student Member, IEEE) received the B.Eng. degree from Hohai University, in 2012, and the M.Sc. degree from the Nanjing University of Aeronautics and Astronautics, China, in 2015. She is currently pursuing the Ph.D. degree with the Chalmers University of Technology, Sweden. She worked as a Lecturer with Huzhou University, China, for a period of two years. Her research interests include modeling and simulation of fuel cell electric vehicle, control and energy management of energy storage systems, power electronics, and motion control as well as wide band-gap devices.