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A Wideband and Highly Efficient Circulator Load Modulated Power Amplifier Architecture

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***Abstract*—A complete theoretical analysis is presented for a highly efficient power amplifier (PA) architecture based on a non-reciprocal combiner. The architecture consists of two amplifier branches and a microwave circulator acting as the output combiner, referred to as the circulator load-modulated amplifier (CLMA). The continuous-mode (CM) design technique has been further exploited for the CLMA to demonstrate the wideband capabilities of the architecture. The analysis reveals that the CLMA performs active load modulation to maintain high PA efficiency performance across a wide bandwidth and large output power dynamic range. As a proof of concept, a CLMA demonstrator circuit based on gallium nitride (GaN) transistors and a microwave circulator, is designed and characterized with continuous-wave and modulated-signal measurements. The implemented CLMA prototype circuit experimentally demonstrates Doherty-like efficiency enhancement over a large bandwidth covering 2.1 to 3.5 GHz. In measurements, the prototype exhibits a drain efficiency of 46.7-57.5% at peak output power and 35.6–50.6% at 7-dB output power back-off level, within the design bandwidth. When tested with a 60-MHz multi-carrier orthogonal frequency-division multiplexing (OFDM) signal having a 7-dB peak-to-average power ratio (PAPR), an average efficiency of 48.5% with better than 47.5-dBc adjacent channel leakage ratio (ACLR) is achieved after applying digital pre-distortion (DPD).**

***Index Terms*—Active load modulation, circulator, continuous-mode (CM), Doherty, energy efficiency, gallium nitride (GaN), power amplifier, non-reciprocity, wideband.**

I. Introduction

THE increasing demand for data throughput has resulted in a continuous evolution of modern communication systems to adopt more spectrally efficient modulation schemes. This inevitably results in modulated signals with a large peak-to-average power ratio (PAPR). In addition to that, the energy efficiency of the system is extremely critical because its power consumption corresponds to a large part of the overall mobile network operational cost and environmental impact. Moreover, excessive power consumption increases the system complexity considerably since cooling equipment is often required to deal with heat dissipation. Thus, efficiency enhancements will translate to large energy savings and simplified thermal management [1].

Consequently, active load-modulated power amplifier (PA) architectures have been proposed to improve the PA efficiency at significantly backed-off output power levels. During several decades of research on active load-modulated PAs, the outphasing PA [2] and the Doherty PA [3] architectures have been extensively analyzed and studied. In outphasing PAs, two branches of constant-envelope amplifiers are phase modulated and then combined to achieve linear transmission and back-off efficiency enhancement. However, it often requires extensive digital pre-distortion (DPD) separately on the two PA branches. Moreover, outphasing PAs require Chireix compensation reactances to realize its efficiency enhancement, which typically limits the PA bandwidth. The Doherty PA, on the other hand, has relatively low complexity and moderate linearity performance. However, the Doherty PA has inherent bandwidth limitations, primarily imposed by the quarter-wavelength impedance inverter at the output. Moreover, the bandwidth limitation is also highly constrained by the need for precise phase delay alignment between its two amplifier branches for proper load modulation and power utilization.

To resolve these fundamental problems, several PA architectures with high efficiency and wide bandwidth performance have been proposed recently. A distributed efficient power amplifier (DEPA) was introduced in [4]. This architecture mitigates the inherent bandwidth limiting factors caused by impedance inversion and load modulation in a Doherty PA. It is achieved by distributing multiple auxiliary sub-amplifiers along a broadband multisection impedance transformer, which makes the DEPA capable of large bandwidth and high efficiency at a deep power back-off level. However, the large number of auxiliary sub-amplifiers used in the DEPA increases its circuit complexity and combiner loss significantly. Another highly efficient and wideband PA architecture, named load modulated balanced amplifier (LMBA), was proposed in [5]. The LMBA comprises a balanced amplifier with two quadrature hybrids at the input and output. Besides, a third amplifier is utilized in the LMBA to inject signals to the isolated port of the output quadrature hybrid. A generic three-port combiner synthesis theory, which includes the LMBA and all the PA architectures that contain three amplifier branches, was proposed in [6]. Essentially, the working principle of the LMBA can be categorized as the Doherty-like linear operation [5] or the sequential-type operation [7], [8]. Compared to the Doherty PA, the LMBA-type architectures have a larger bandwidth since the quadrature coupler is inherently more

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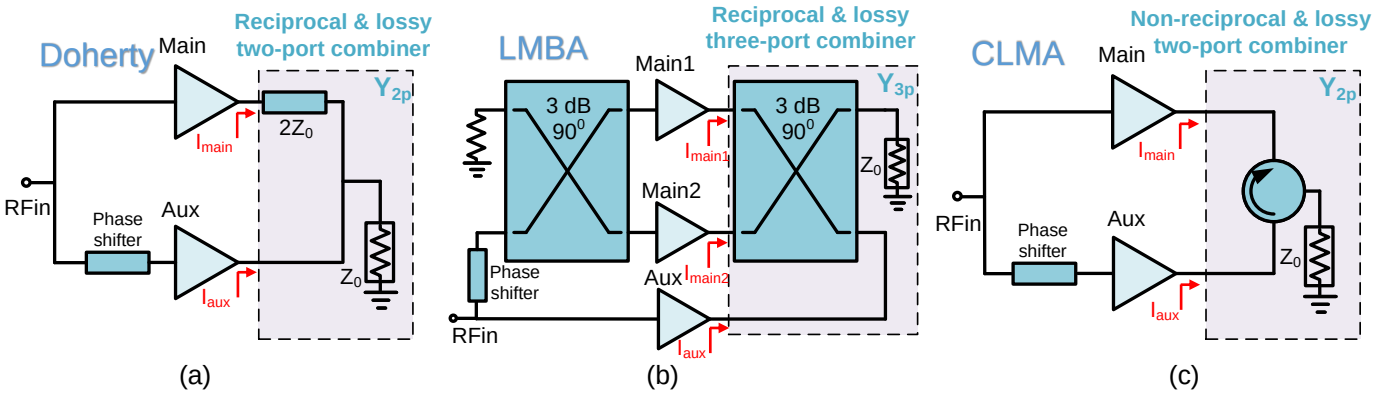

Fig. 1. Active load modulated power amplifier architectures. (a) The Doherty PA, (b) the load-modulated balanced amplifier (LMBA), and (c) the circulator load-modulated amplifier (CLMA).

wideband than the one provided by the standard Doherty PA. In recent work, the authors proposed a novel active load modulation PA architecture called the circulator load modulated amplifier (CLMA) [9], which was further developed into a sequential-type CLMA [10], [11]. This topology utilizes only two active devices and a non-reciprocal combiner, specifically a circulator, and can maintain high efficiency over a large output power dynamic range. The availability of wideband, low-loss microwave circulators makes the CLMA well-suited for wideband applications. In addition to the advantage of requiring only a single transistor for the main PA, the CLMA architecture is particularly useful when an isolator is to be integrated between the PA and the antenna. Therefore, the CLMA represents a promising alternative to previously proposed load-modulated PA architectures.

In this paper, we extend our previous work [9] by presenting a thorough theoretical analysis of the CLMA architecture. The analysis derives the drive profiles of the main and auxiliary amplifiers, based on the non-reciprocal combiner characteristic. In particular, the theory and relation between load modulation and current scaling ratio are expanded by further analysis under ideal transistor assumptions. Thereafter, the reconfigurable back-off efficiency of the CLMA is demonstrated with closed-form analytical expressions to further broaden the design space. Moreover, a continuous mode (CM) output matching network is used for the broadband operation of the CLMA architecture. To validate the bandwidth capabilities of the proposed topology and design theory, a wideband CLMA prototype is designed, implemented, and characterized using both continuous-wave (CW) and modulated signals. The design is based on equally-sized gallium nitride (GaN) transistors and a microwave circulator. It should be noted that the design procedure is adaptable and scalable to different frequency bands, processes, and output power levels. The state-of-the-art performance in terms of back-off efficiency and bandwidth of the CLMA indicates its potential for use in future wireless applications.

This paper is organized as follows. Section II provides a brief overview of active load modulation PA architectures, followed by a complete theoretical analysis of the operational principle of the CLMA. This includes closed-form equations, efficiency reconfigurable behavior, and gain characteristics of the CLMA under various drive profiles. In Section III, we present a detailed comparison of the theoretical performance of the Doherty PA and the CLMA. Section IV focuses on the CLMA prototype circuit design, including the wideband design methodology used, design space limitations, simulation results, and design tradeoffs. Experimental results for both continuous-wave (CW) and modulated signal measurements are presented in Section V, and the prototype design is also benchmarked against recently reported active load-modulated GaN HEMT PAs. Finally, the main conclusions from this work are presented in Section VI.

II. Circulator Load Modulated Amplifier

The active load-modulated PA architectures typically consist of several sub-amplifiers with certain drive profile relations and an output combiner. The theoretical analysis often assumes a representation where the load is merged with the combiner into a lossy combiner network [6]. The Doherty PA, LMBA, and CLMA architectures are presented in Fig. 1. The three PA architectures all have main amplifiers, whose current increases linearly with the input drive voltage. They also have auxiliary amplifiers, which are turned off in the lower drive level, and turned on after the back-off drive level. However, it can be noticed that the drive profile relations and combiner parameters are different for the three cases, which when combined uniquely define each of the PA architectures. The Doherty output combiner is based on the quarter-wavelength transformer, while the output combiner of the LMBA is a quadrature hybrid. Moreover, it should be stressed that only the CLMA combiner is non-reciprocal, which is a key difference compared to the Doherty PA and LMBA case. In its most simplified form, the CLMA architecture comprises a class-B biased main amplifier, an auxiliary amplifier biased in class-C mode, and a circulator-based output combiner network as presented in Fig. 2 [9]. The fundamental operating principle of the CLMA architecture can be described as follows: An auxiliary amplifier injects power into the output of the main amplifier through the circulator, thereby modulating its load impedance to maintain high efficiency at both peak power and power back-off. Due to the inherent non-reciprocal property of

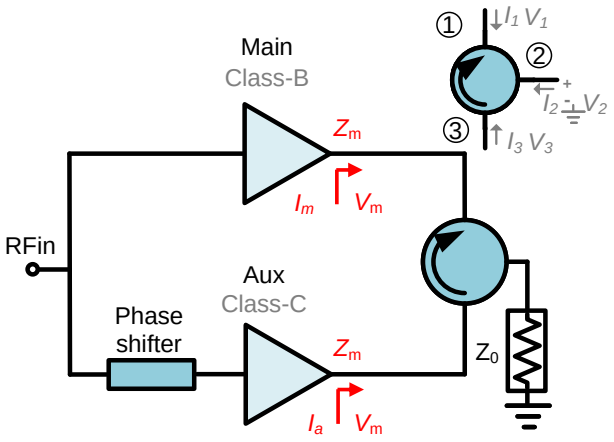

Fig. 2. Block diagram of the circulator load modulated amplifier and block diagram of an ideal circulator used for analysis of the CLMA architecture.

the circulator, the powers injected by the main and auxiliary amplifiers are both fully delivered to the load. Moreover, the impedance seen by the auxiliary amplifier is maintained constant due to the high isolation from the main to the auxiliary port in the circulator. In this section, the basic operating principle of the CLMA is revisited and analyzed with an ideal circulator, as shown in Fig. 2. Then, the reconfigurable efficiency behavior of the CLMA is demonstrated, under various current drive profiles. Furthermore, the boundary conditions and design space limitations are illustrated.

To analyze the operation principle of the CLMA, it is vital to first study the circulator. As it is well known, the scattering parameters of an ideal circulator, which are depicted in Fig. 2, can be expressed as

$$\mathbf{S}_{\text{circ}} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}. \tag{1}$$

It is then straightforward to convert the three-port scattering parameters ($\mathbf{S}_{\text{circ}}$) to admittance parameters. The operational mechanism of the CLMA can thereafter be analyzed using the three-port admittance parameter matrix of the ideal circulator. Note that this formulation assumes that the port currents, I_n, flow into the corresponding port of the circulator, and the voltages V_n are referenced to the common ground connection. The port currents and voltages are therefore related by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = Y_0 \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \tag{2}$$

where $Y_0 = 1/Z_0$ is the characteristic admittance of the circulator. The main (connected at port 1) and auxiliary (connected at port 3) amplifiers can be represented as current sources in the analysis, having magnitudes I_m and I_a, respectively. Thus, $I_1 = I_m$, $I_3 = I_a e^{j\theta}$, where θ is the output current phase delay between the main and auxiliary amplifier branches. In addition, the output port (port 2) is terminated with a resistive load matched to the characteristic impedance of the circulator Z_0, so $V_2 = -Z_0 I_L$.

Substituting the above equations into the three-port admittance matrix from (2), the resulting three equations can be solved to obtain the expressions for the impedance seen by the main and auxiliary amplifiers at their output, denoted as Z_m and Z_a, respectively, as follows

$$Z_m = Z_0 \left(1 - 2\frac{I_a e^{j\theta}}{I_m}\right), \tag{3}$$

$$Z_a = Z_0. \tag{4}$$

Equation (3) reveals that the load impedance seen by the main amplifier can be dynamically modulated by the magnitude and output phase delay of the auxiliary current. It should be remarked that the impedance seen by the auxiliary amplifier remains constant to the characteristic impedance of the circulator, according to (4). Moreover, the relationship between the currents is given by

$$I_L = I_m - I_a e^{j\theta}. \tag{5}$$

The power delivered to the load is therefore given by

$$\begin{aligned} P_L &= \frac{1}{2} Z_0 \Re\left\{I_L\right\}^2 \\ &= \frac{1}{2} Z_0 \left(I_m^2 - 2 I_m I_a \cos\left(\theta\right) + I_a^2 \cos\left(\theta\right)^2\right) \end{aligned} \tag{6}$$

The power generated by the main and auxiliary amplifiers can be expressed as

$$\begin{aligned} P_m &= \frac{1}{2} I_m^2 Z_0 \Re\left\{1 - 2\frac{I_a e^{j\theta}}{I_m}\right\} \\ &= \frac{1}{2} Z_0 \left(I_m^2 - 2 I_m I_a \cos\left(\theta\right)\right) \end{aligned} \tag{7}$$

$$P_a = \frac{1}{2} Z_0 \Re\left\{I_a e^{j\theta}\right\}^2 = \frac{1}{2} Z_0 I_a^2 \cos\left(\theta\right)^2 \tag{8}$$

Consequently, it can be noticed that $P_L = P_m + P_a$, which indicates that the power generated by the main and auxiliary amplifiers is fully transferred to the load.

A. Drive Profiles and Boundary Conditions

To further investigate the theoretical performance of the CLMA architecture, its main and auxiliary amplifiers are represented by ideal piece-wise voltage-controlled linear current sources, having fundamental output currents I_m and I_a that depend on the normalized input voltage β as

$$I_m = \beta i_{m,M} \tag{9}$$

$$I_a = \begin{cases} 0, & 0 \le \beta \le \beta_B \\ \left(\dfrac{\beta - \beta_B}{1 - \beta_B}\right) i_{a,M}, & \beta_B \le \beta \le 1 \end{cases} \tag{10}$$

where $i_{m,M}$ and $i_{a,M}$ are the maximum current from the main and auxiliary amplifiers, respectively, and β_B is the normalized input drive voltage at the back-off level. Note that all higher harmonic components are assumed to be short-circuited, corresponding to the ideal class-B operation.

To fully determine the operation of the CLMA and ensure a proper load modulation presented to the main amplifier, the current ratio (α) between the current of the auxiliary and main amplifiers should be related by

$$\alpha = \frac{I_a}{I_m} = \frac{\beta - \beta_B}{2}. \tag{11}$$

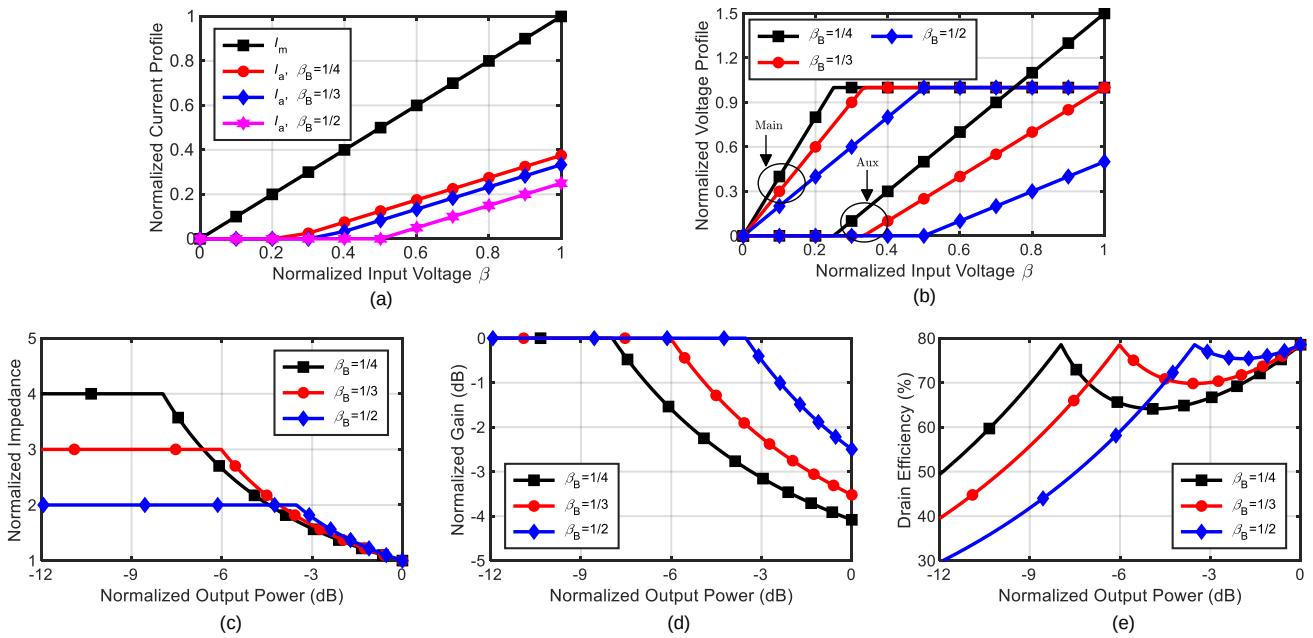

Fig. 3. (a) Normalized amplitude of the fundamental currents and (b) normalized amplitude of the fundamental voltage from the circulator load modulated amplifier versus normalized input drive voltage, for β_B = 1/4, 1/3, and 1/2. (c) Normalized optimal load impedance of the main amplifier from the circulator load modulated amplifier, (d) normalized gain of the circulator load modulated amplifier, and (e) drain efficiency of the circulator load modulated amplifier, versus normalized output power, for β_B = 1/4, 1/3, and 1/2.

Note that the output voltage from the main amplifier should be kept constant at its full voltage swing $V_{m,M}$ throughout the high power region (when $\beta_B < \beta \leq 1$) to guarantee high-efficiency operation. Furthermore, to fulfill the power conservation laws at both peak and back-off power levels, the output power from the main and auxiliary amplifiers should be related by

$$P_{m,M} + P_{a,M} = \gamma P_{m,B}, \tag{12}$$

$$\gamma = \frac{(\beta_B + 1)^2}{4\beta_B^2}, \tag{13}$$

where $P_{m,M}$ and $P_{a,M}$ are the peak output power from the main and auxiliary amplifiers, respectively, $P_{m,B}$ is the back-off output power of the main amplifier, and γ is the output power back-off level. The output maximum voltage swing from the auxiliary amplifier $V_{a,M}$ can thereby be derived with (9)-(13) as

$$V_{a,M} = \left(\frac{1-\beta_B}{2\beta_B}\right) V_{m,M}, \tag{14}$$

where $V_{m,M}$ is the maximum voltage swing of the main amplifier. Similarly, the overall gain of the CLMA can be expressed as

$$G = \frac{(1+\beta_B)^2}{4}. \tag{15}$$

The current and voltage profiles of the CLMA with respect to the normalized input voltage (β) are shown in Fig. 3(a) and 3(b), respectively. As seen in Fig. 3(a), the peak current required from the auxiliary amplifier is lower than that of the main amplifier. Furthermore, a higher value of the current ratio (α) leads to higher efficiency at deeper power back-off levels. It is also worth noting that the maximum voltage swing of the auxiliary amplifiers varies with different back-off levels.

B. *Efficiency Reconfigurability*

In the previous section, the current and voltage drive profiles of an ideal CLMA architecture are determined. Therefore, assuming both main and auxiliary amplifiers with the ideal class-B efficiency, their corresponding RF output power and DC supply power can be derived as

$$P_{m,RF} = \frac{1}{4} V_m \beta i_{m,M}, \tag{16}$$

$$P_{m,DC} = \frac{1}{\pi} V_{m,M} \beta i_{m,M}, \tag{17}$$

$$P_{a,RF} = \frac{1}{4} V_a \left(\frac{\beta - \beta_B}{1-\beta_B}\right) |\alpha| i_{m,M}, \tag{18}$$

$$P_{a,DC} = \frac{1}{\pi} V_{a,M} \left(\frac{\beta - \beta_B}{1-\beta_B}\right) |\alpha| i_{m,M}. \tag{19}$$

Combined with (9)-(14), the efficiency of the CLMA can be expressed as

$$\begin{aligned} \eta &= \frac{P_{m,RF} + P_{a,RF}}{P_{m,DC} + P_{a,DC}} \\ &= \begin{cases} \dfrac{\pi}{4}\beta, & 0 \leq \beta \leq \beta_B \\ \dfrac{\pi}{4}\left(\dfrac{\beta^2 + \dfrac{k\,(\beta_B - \beta)}{\beta_B - 1}}{\beta_B + k}\right), & \beta_B < \beta \leq 1 \end{cases} \end{aligned} \tag{20}$$

where

$$k = \frac{(\beta_B - \beta)^2}{4\beta_B}. \tag{21}$$

The theoretical performance of the CLMA is presented in Figs. 3(c)-3(e), where the load modulation, normalized gain,

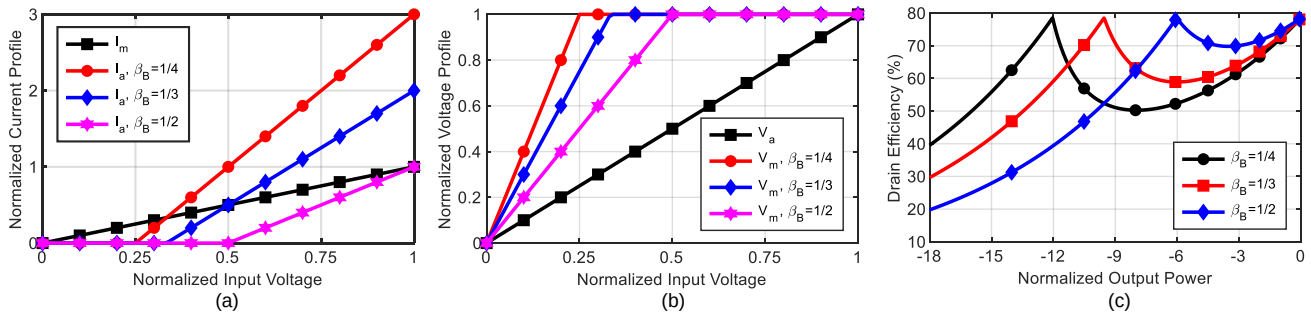

Fig. 4. (a) Normalized amplitude of the fundamental currents and (b) normalized amplitude of the fundamental voltage from the Doherty PA versus normalized input drive voltage, for β_B = 1/4, 1/3, and 1/2. (c) Drain efficiency of the Doherty PA, versus normalized output power, for β_B = 1/4, 1/3, and 1/2.

TABLE I
COMPARISON OF DOHERTY PA AND CLMA.

Parameter (linear value)	Doherty PA	CLMA (This work)
Power back-off level (γ)	$\frac{1}{\beta_B^2}$	$\frac{(\beta_B+1)^2}{4\beta_B^2}$
Relative auxiliary size (α)	$\frac{1}{\beta_B}-1$	$\frac{(1-\beta_B)}{2}$
Gain compression	1	$\frac{(1+\beta_B)^2}{4}$
Voltage swing ($\frac{V_{a,M}}{V_{m,M}}$)	1	$\left(\frac{1-\beta_B}{2\beta_B}\right)$
Parallel loss	$\frac{V_{a,M}^2}{4R_{off}}$	0
Offset line required	Yes	No

and drain efficiency are plotted versus the normalized output power. Note that the maximum voltage for the auxiliary amplifier varies with different back-off levels, which agrees with (14). An auxiliary amplifier with different drain bias is therefore required to obtain the best optimal performance. It should be noticed that, for the case of $\beta_B = 1/3$, the main and auxiliary amplifiers have a symmetrical drain bias. Moreover, it should be stressed that the ideal CLMA suffers from gain compression. As a remark, the LMBA also presents a similar nonlinear behavior. The theoretical analysis and performance presented in this section illustrate how a simple combination of the main and auxiliary amplifiers, together with correct driving conditions and the non-reciprocal circulator combiner, results in enhanced efficiency performance at a deep output power back-off level.

III. COMPARISON OF CIRCULATOR LOAD MODULATED AMPLIFIER AND DOHERTY PA

In Section II, it is shown that the impedance seen by the main amplifier of the CLMA is load-modulated by the active current injection from the auxiliary amplifier. In addition, the power generated by both the main and auxiliary amplifiers can be fully recovered at the CLMA output port. Therefore, the CLMA can potentially be a suitable alternative to two-way back-off efficiency-enhanced PA architectures. This section presents a detailed comparison between CLMA and the Doherty PA, being the most widely used two-way PA architecture in base stations. The design parameters of both architectures are compared and summarized in Table I.

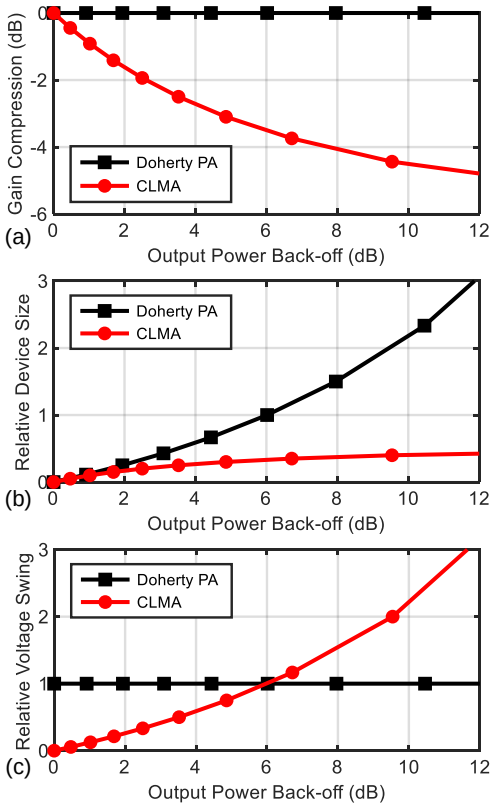

Fig. 5. (a) Gain compression, (b) relative device size, and (c) relative voltage swing versus the high-efficiency back-off power levels.

Fig. 4 shows the current and voltage drive profiles and the efficiency profile of a Doherty PA at various back-off levels (β_B). Fig. 5 plots the gain profile, relative device size ratio, and relative voltage swing against the high-efficiency output power back-off levels. It can be seen that the CLMA architectures suffer from gain compression, while the Doherty PA is linear. In addition, for large back-off levels, the relative device size ratio between the main- and auxiliary amplifiers becomes large for the Doherty PA while remaining small for the CLMA. However, the relative voltage swing of the CLMA becomes very large at high back-off levels. To counteract this asymmetry in bias voltages, the DC supply voltage of the main and auxiliary amplifiers should be chosen to under-utilize the transistor.

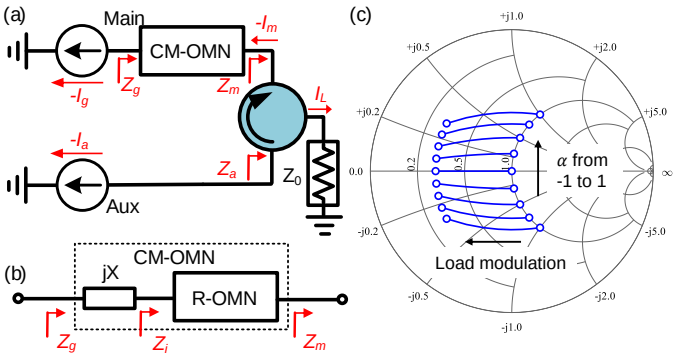

Fig. 6. (a) Ideal block diagram of the continuous-mode CLMA, (b) the equivalent network of the continuous-mode output matching network, and (c) load modulation trajectory at the main current generator plane (Z_g)

IV. Wideband CLMA Prototype Design

The analysis in the previous sections demonstrates the fundamental operational principles of the CLMA architecture, in comparison with the Doherty PA. In this Section, we extend the analysis of the CLMA architecture to wideband design- and practical implementation considerations. The implementation of the broadband output matching networks will be in particular focus. First, the continuous-mode (CM) design technique for realizing high-efficiency broadband matching is revisited, then a general procedure for the design of a practical CLMA is demonstrated and applied through the design of a wideband CLMA prototype based on GaN HEMT transistors. Finally, the simulated results of the prototype are presented.

A. Wideband Continuous-mode Output Matching Network

A theoretical block diagram of a CM CLMA is shown in Fig. 6(a). In this configuration, the active devices are represented by ideal current generators. In addition, an output matching network at the main amplifier branch is required not only to exploit the CM operation for the wideband design but also to provide the proper phase delay between the two amplifier branches, therefore allowing to the exploitation of the novel high-efficiency architecture over a larger bandwidth. To illustrate the load modulation in CM CLMA [12], the class B/J continuum PA operation modes are used. Assuming that the optimal class B impedance of the main amplifier at the current generator plane, Z_g, is R_{opt} at saturation, the corresponding impedance of the continuous class B/J mode can be expressed as $Z_{g,S} = R_{opt}(1+j\alpha)$ [13]. For high back-off efficiency, a larger impedance is necessary at the back-off level. Thus, the back-off impedance can be expressed as $Z_{g,B} = (R_{opt}/\beta)(1 + j\alpha)$. To satisfy the load condition at the back-off level, the CM output network should match Z_0 to $(R_{opt}/\beta)(1 + j\alpha)$. To simplify the analysis of the CM load modulation process, an equivalent network consisting of a real-to-real output matching network (R-OMN) and a series reactance component is used to represent the CM output matching network [12], as shown in Fig. 6(b). Consequently, the impedance at the intermediate terminal, Z_i, should be $Z_{i,B} = R_{opt}/\beta$ and $Z_{i,S} = R_{opt}(1-j(1/\beta-1)\alpha)$, at back-off and peak power levels, respectively, to provide the same CM impedance at the current generator plane of the main amplifier. As a result, the reflection coefficient of the intermediate port at saturation can be expressed as

$$\Gamma_{i,S} = \frac{(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j\arctan\alpha}}{2+(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j\arctan\alpha}}, \tag{22}$$

Note that the R-OMN is matched at both ports at the back-off level. Assuming that the R-OMN is a lossless and reciprocal network with a phase shift of ϕ [6], the reflection coefficient at the circulator port at saturation can be expressed as

$$\Gamma_{m,S} = \frac{(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j(\arctan\alpha-2\phi)}}{2+(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j\arctan\alpha}}. \tag{23}$$

From the current relationship at the main and auxiliary amplifiers' current generator plane, as given in (11), the normalized auxiliary current at the circulator port can be derived, taking into account the CM output matching network. Based on (3), the corresponding $Z_{m,S}$ can then be calculated. A detailed derivation is provided in the Appendix, and the resulting expression for $\Gamma_{m,S}$ is

$$\Gamma_{m,S} = \frac{(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j(\theta-\phi)}}{2+(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j\arctan\alpha}}. \tag{24}$$

According to (23) and (24), in order to achieve the required carrier CM impedance at saturation, the following phase relationship should be satisfied

$$\theta = \arctan(\alpha) - \phi. \tag{25}$$

It should be noted from equation (25) that the CM load modulation can be achieved by the proper selection of the phase of the auxiliary current. The CM CLMA load modulation trajectories at the main generator plane are therefore shown in Fig. 6(c). In addition, the CM output matching network should be designed to satisfy the second harmonic impedance condition of the corresponding CM to ensure high-efficiency performance at the back-off level [14].

B. Practical CLMA Design Procedure

The analysis in previous sections assumes that both main and auxiliary transistors are represented by ideal current sources. In reality, the parasitic and nonlinear effects of real transistors are significant at microwave frequencies, and their operation deviates from that of ideal current sources. Therefore, this section focuses on the practical implementation of the CLMA architecture. A step-by-step flowchart of the design procedure is presented in Fig. 7. Details of each step are illustrated below.

Step 1: Based on the required delivered output power, the size of the main- and auxiliary transistors from CLMA can be decided. A back-off level (β_B) should then be selected depending on the peak-to-average-power ratio (PAPR) of the transmitted communication signal. In addition, the selection of the gate bias for the main amplifier should be made taking into account the trade-offs between the overall gain, linearity, and efficiency performance of the CLMA.

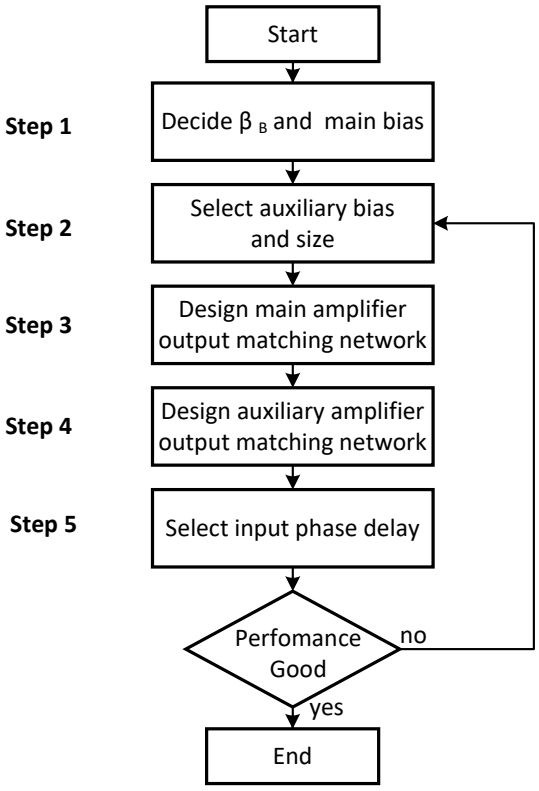

Fig. 7. Design procedure of a practical circulator load modulated amplifier.

Step 2: Select the gate bias for the auxiliary amplifier. The selection of the class-C gate bias may require several iterations in order for the auxiliary amplifier to turn on at the desired back-off power level over the designed bandwidth. Moreover, the auxiliary transistor size should be selected carefully considering the fundamental peak current relationship between the main and auxiliary amplifiers from the CLMA, as illustrated thoroughly in Section II. It is worth mentioning that compared to the peak fundamental current from a class-B biased transistor, a smaller peak fundamental current is presented by an equally sized transistor that is biased in class-C mode [15]. This implies that in many cases identical device sizes of the main and auxiliary amplifiers can be utilized for the CLMA architecture.

Step 3: Design the CM output matching network of the main amplifier. The CM output matching network should be designed to match the high-efficiency CM impedance at the back-off power level (β_B) to the characteristic impedance of the circulator (Z_0). The parasitic and packaging components are included in the network design to achieve the required CM impedance at the current generator plane. The specific parasitic and packaged components are obtained from the de-embedded transistor model [16]. It should be emphasized that the specific circuit structure of the CM output matching networks has no effect on the operation of the CLMA. To achieve maximized back-off efficiency, the optimal phase shift between the main and auxiliary branches is determined at various frequencies. The detailed design procedures that are extensively covered in previous publications [17]–[19] have been followed.

Step 4: Design the output matching network of the auxiliary amplifier. The gate bias and transistor size of the auxiliary amplifier are selected already in Step 2. The auxiliary output matching network should be further designed to deliver a proper output power to fulfill the desired fundamental current relationship between the main and auxiliary amplifiers. Note that, when selecting the auxiliary output impedance, trade-offs can be made for the auxiliary transistor to deliver a lower output power with higher efficiency performance since the efficiency and output power load-pull contours are separated. Afterward, the optimal output impedance from the auxiliary transistor should be matched to the characteristic impedance of the circulator across the desired operating frequency range [20].

Step 5: Select a proper phase delay between the main- and auxiliary amplifier branches. First, the input matching and stabilization networks should be designed to make sure the device is stable and provides decent gain performance. It is then vital to select the phase delay for the load modulation to function correctly across the desired bandwidth.

C. Prototype Circuit Design

To validate the proposed theory, a CLMA prototype circuit is implemented according to the systematic design procedure presented above. Gallium Nitride (GaN) packaged transistors (CGH40010F) from Wolfspeed are adopted as the active devices for both the main and auxiliary amplifiers. A commercial microwave circulator from Quest Microwave (SM2040C09) is selected to act as the output combiner due to its broadband capability, low insertion loss, and high isolation. All transmission lines are EM simulated using Keysight Momentum. Models provided by Modelithics are employed for all the lumped elements to guarantee good agreement between measurements and simulations. The CLMA prototype, which is implemented on a 20-mil Rogers 4350B substrate, is designed to operate with enhanced back-off efficiency performance over the frequency range from 2.1 to 3.5 GHz. Fig. 8 shows the circuit schematic of the implemented CLMA prototype.

The main amplifier operates in Class-B mode, with a nominal gate bias of $V_{\text{GG-m}} = -3$ V and a drain bias of $V_{\text{DD-m}} = 28$ V. Under this bias condition, the optimal load impedance of the main amplifier can be estimated as $R_{\text{opt-m}} = 32\ \Omega$ at the intrinsic plane, according to the de-embedded load-pull simulated model of the transistor [16]. For the auxiliary amplifier, the nominal gate bias is set to $V_{\text{GG-a}} = -7$ V, and the drain supply voltage is chosen to be $V_{\text{DD-a}} = 25$ V. Note that to achieve enhanced efficiency at the power back-off level with identical CG2H40010F transistors for both the main and auxiliary amplifiers, a slightly reduced drain supply voltage of the auxiliary amplifier is used to guarantee a proper load modulation ratio. The measured input return loss, isolation, and insertion loss of the microwave circulator are plotted versus frequency in Fig. 9.

The output matching network of the main amplifier is designed, following the procedure explained in the previous section, to transform the optimal back-off terminations to match the circulator characteristic impedance across the design

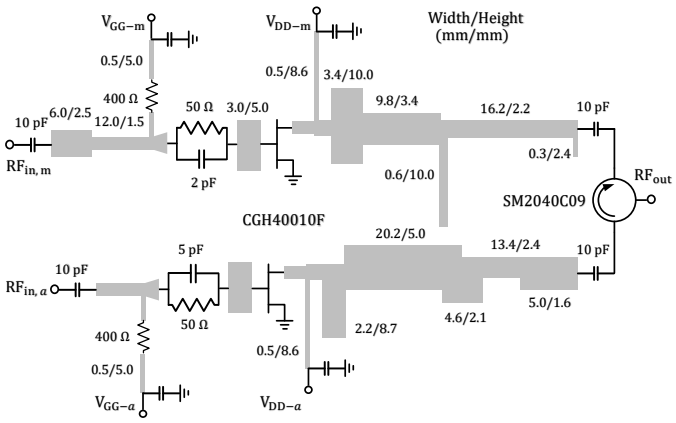

Fig. 8. Circuit schematic of the proposed circulator load modulated amplifier.

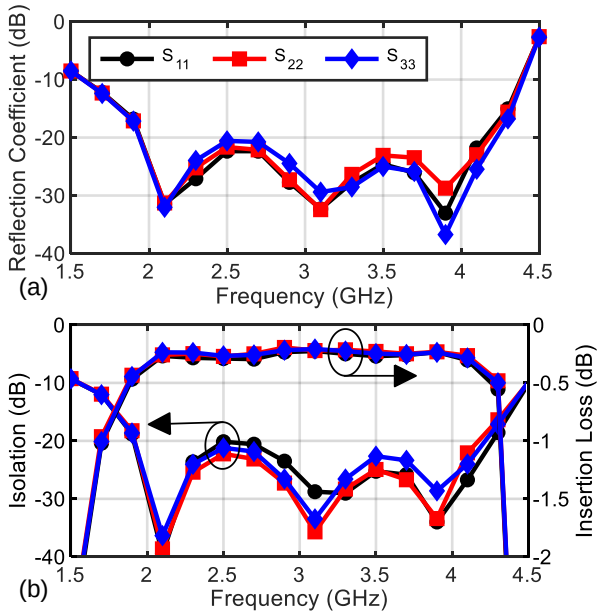

Fig. 9. (a) Measured reflection coefficient and (b) measured isolation and insertion loss of the microwave circulator.

bandwidth. Load-pull simulations are used to extract the extrinsic fundamental and harmonic impedance. The designed CM output matching network is shown in Fig. 10(a) along with an equivalent output parasitic circuit model of the packaged CGH40010F transistor [16]. A de-embedded network with parasitic and packaged elements is used in the practical output-matching design to achieve the required CM impedance condition at the intrinsic plane. The matching results for the main amplifier are presented in Fig. 10(b) on the Smith chart, which shows that both the fundamental and second harmonic matching results are close to the ideal CM operation. To ensure proper power delivery at the auxiliary port of the circulator, a preliminary simulation is performed, which also identifies a suitable active device size for the auxiliary amplifier. Note that the auxiliary amplifier is biased in deep class-C mode, thus its peak fundamental current is smaller than that of a nominal class-B biased main amplifier for equally sized transistors [15]. Therefore, identical device sizes for both

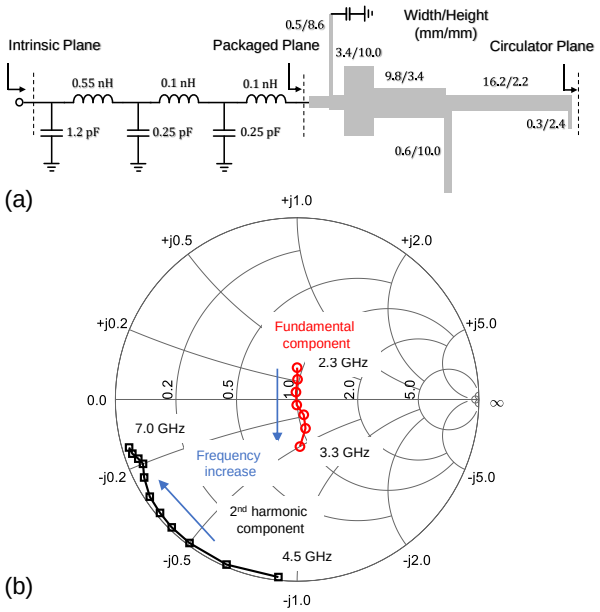

Fig. 10. (a) Continuous-mode output matching network with the equivalent parasitic and packaged model of the CGH40010F transistor. (b) Simulated matching results of the output network with a reference impedance of R_{opt}/β.

amplifiers can be employed in the prototype. Finally, the auxiliary output matching network is designed to transform the optimal impedance for the requested delivered power to match the characteristic impedance of the circulator.

The input matching networks for both the main and auxiliary amplifiers are designed based on the source impedance extracted from the source-pull simulation. To ensure amplifier stability, a 50 Ω resistor and a 2.0 pF capacitor are connected in parallel at the gate terminal of the main amplifier, while a 50 Ω resistor and a 5.0 pF capacitor are used for the gate of the auxiliary transistor. These components are selected to provide broadband stabilization over the operating frequency range. In addition, a 10-pF capacitor is included for DC blocking.

D. Simulated Results

The entire circuit topology and detailed parameters of the biasing and matching networks are presented in Fig. 8. EM simulation of all transmission line structures is conducted using Keysight ADS Momentum. The load-pull and source-pull are performed with harmonic balance simulations using the nonlinear transistor model provided by the vendor. During the design, both manual tuning and optimization are used with large-signal simulations, adopting the transistor nonlinear model, to obtain a good impedance-matching performance over the desired frequency band. The harmonics, especially the second harmonic, have been monitored to avoid detrimental conditions for power and efficiency [18].

Figs. 11(a) and 11(b) show the simulated fundamental components of the main and auxiliary versus the normalized input drive voltage at the CLMA prototype's center operating frequency of 2.8 GHz. The fundamental current and voltage relationships between the main and the auxiliary amplifiers agree well compared with that from the ideal CLMA circuit, as

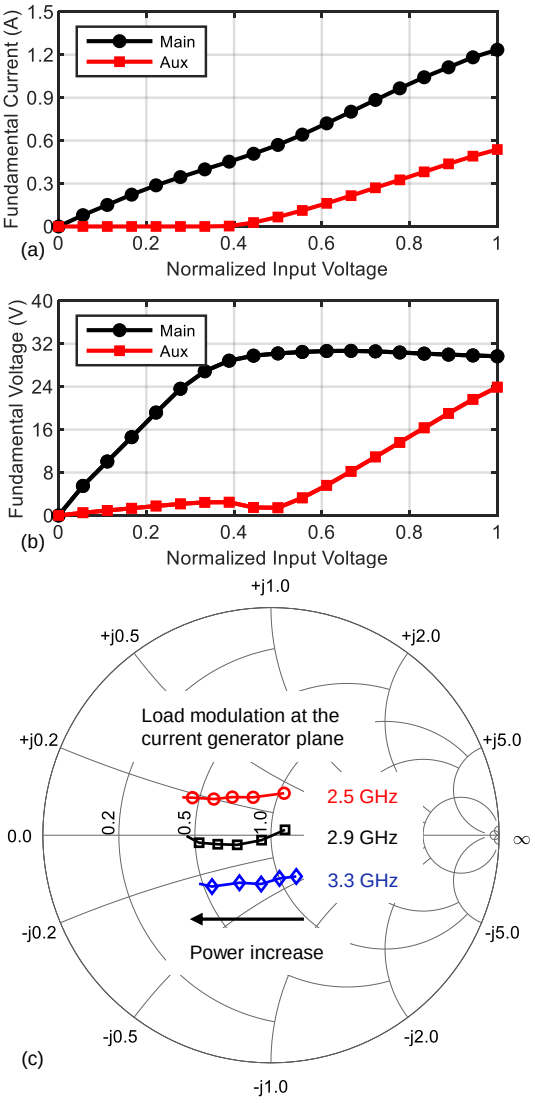

Fig. 11. (a) Simulated fundamental currents and (b) fundamental voltages of the CLMA's main and auxiliary amplifier at the intrinsic plane of the transistor at 2.8 GHz. (c) Simulated load modulation trajectories at the main amplifier's intrinsic plane.

shown in Figs. 3(a) and 3(b). Moreover, the fundamental load modulation trajectories at the main intrinsic plane at several operating frequencies are shown in Fig. 11(c). It can be seen that the simulated results of the load modulation are close to the ideal ones, but there are also small deviations at different power levels and frequencies, which are mainly caused by the non-ideal circulator.

In Fig. 12 and 13, the simulated performance of the proposed CLMA prototype circuit is demonstrated with different operating frequencies within the designed bandwidth from 2.1 GHz to 3.5 GHz. A peak drain efficiency of 54.1%–74.7% is achieved by the CLMA prototype with a saturated output power of 42.5–43.5 dBm. Furthermore, an efficiency of 42.7%–55.4% is obtained at the 6-dB output power back-off level. It can be observed that the realized CLMA demonstrator circuit achieves excellent efficiency performance over a large output power dynamic region across a 1.4 GHz bandwidth.

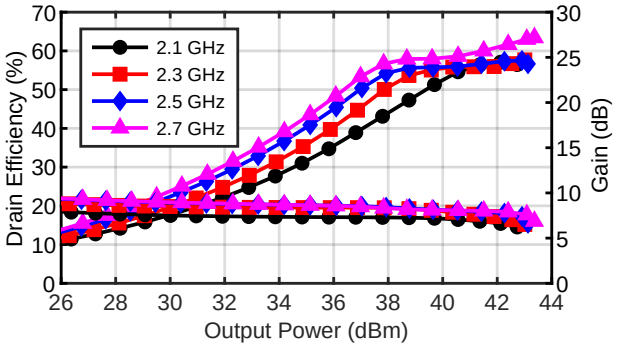

Fig. 12. Simulated drain efficiency and gain versus output power of the CLMA prototype from 2.1 to 2.7 GHz.

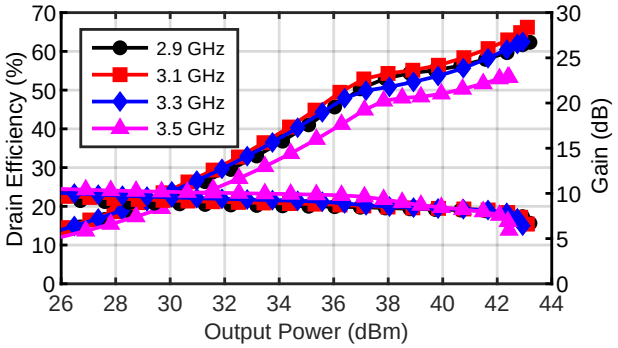

Fig. 13. Simulated drain efficiency and gain versus output power of the CLMA prototype from 2.9 to 3.5 GHz.

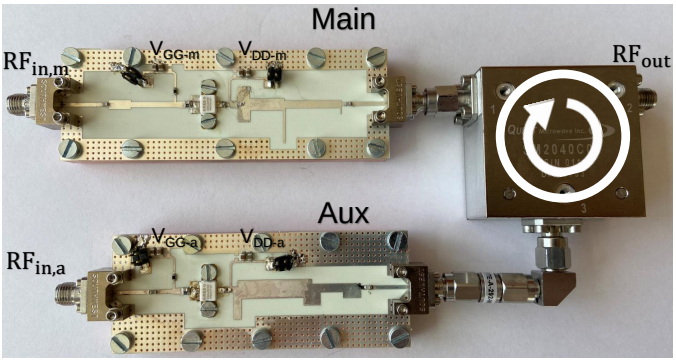

Fig. 14. Photograph of the fabricated CLMA prototype circuit.

V. Measurement Results

A photograph of the fabricated CLMA prototype is shown in Fig. 14. Both continuous-wave (CW) and modulated signal measurements are used to characterize the fabricated prototype circuit. The gate and drain bias of the main amplifier are set to be -3 V and 28 V, respectively, with a quiescent drain current of 36 mA. The drain voltage of the auxiliary amplifier is set to 25 V and the auxiliary gate bias voltage is set to -6.5 V. A 3-dB Wilkinson power splitter and an adjustable phase shifter are employed at the input of the auxiliary amplifier to set the optimal phase delay at each of the measured frequencies. Fig. 15 shows the optimal phase shift between the main and auxiliary branches at different frequencies for maximized

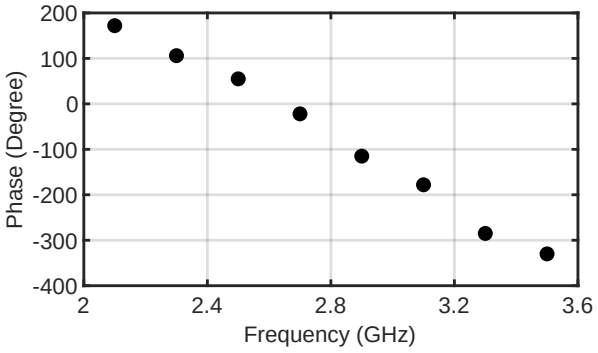

Fig. 15. Optimal phase shift between the main and auxiliary branches across designed frequencies for maximized back-off efficiency.

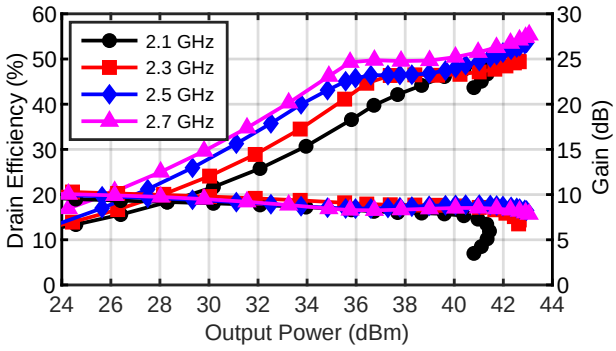

Fig. 16. Measured drain efficiency and gain versus output power of the CLMA prototype from 2.1 to 2.7 GHz.

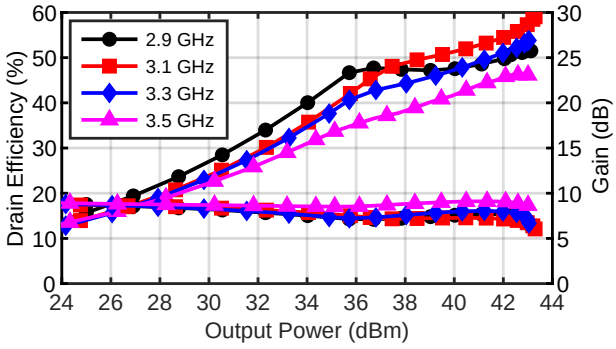

Fig. 17. Measured drain efficiency and gain versus output power of the CLMA prototype from 2.9 to 3.5 GHz.

back-off efficiency. The plot shows that the optimal phase shift varies nearly linearly with frequency, making it easy to achieve using a transmission line at the input. During the measurements, the CW and modulated signals are both generated by a vector signal generator, and the output power is measured with a power meter and spectrum analyzer, together with a low-pass filter included to prevent harmonics from entering the power meter. Moreover, a broadband linear driver amplifier is used to drive the CLMA prototype circuit with enough input power.

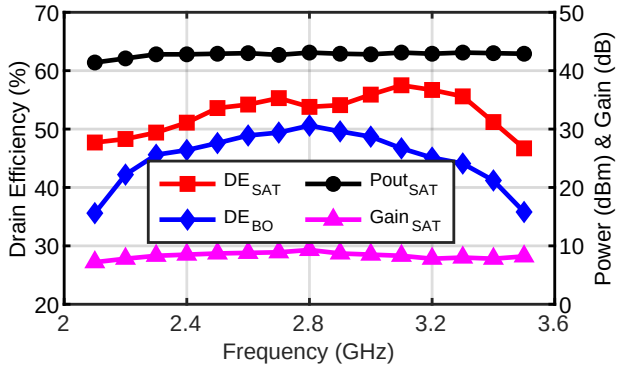

Fig. 18. Measured drain efficiency at peak and 7-dB back-off power level, saturated output power, and gain versus frequencies across 2.1 to 3.5 GHz.

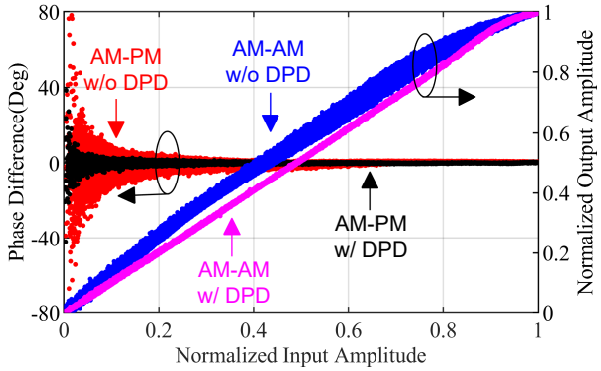

Fig. 19. Measured AM-AM and AM-PM characteristics when using a 20-MHz 7-dB PAPR OFDM signal at 2.8 GHz, with and without DPD.

A. *Continuous-wave Measurements*

The implemented CLMA is measured under the excitation of a single-tone CW signal from 2.1 to 3.5 GHz. Fig. 16 and 17 presents the measured drain efficiency and gain performance versus the output power. It can be observed that Doherty-like back-off efficiency enhancement behavior is achieved by the prototype within the designed frequency band. The broadband performance of the fabricated CLMA prototype is further illustrated in Fig. 18, which presents the measured drain efficiency at different output power levels, the saturated output power, and the gain versus the operating frequency. The saturated output power stays between 41.4-43.1 dBm across the bandwidth. It should be stressed that the prototype shows a very flat saturated output power of 42.7–43.1 dBm over a 1-GHz bandwidth, which verifies the wideband large-signal capability. Moreover, the PA achieves a drain efficiency of 46.7%–57.5% and 35.6%-50.6% at the peak and 7-dB back-off output power level, respectively, throughout the entire operating frequency band.

B. *Modulated-signal Measurements*

To evaluate the linearity and efficiency performance of the proposed CLMA under the modulated signal stimulus, 20- and 60-MHz orthogonal frequency-division multiplexing (OFDM) signals with 7-dB PAPR are employed to perform

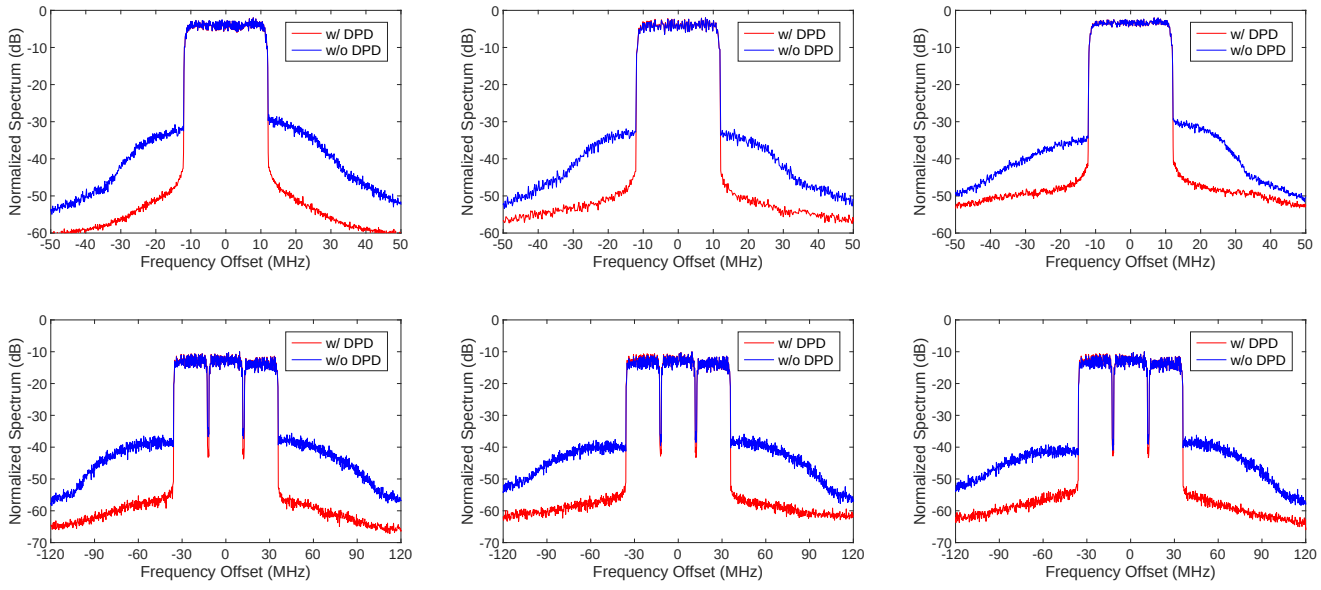

Fig. 20. Measured normalized power spectral density for 20-MHz and 60-MHz 7-dB PAPR OFDM signals, with and without DPD at (a) 2.3 GHz, (b)2.8 GHz, and (c) 3.3 GHz.

TABLE II
COMPARISON WITH STATE-OF-THE-ART LOAD MODULATED PAS.

Ref. / Year	Architecture	Freq (GHz)	BW (GHz)	Pmax (dBm)	OPBO (dB)	DE @Pmax (%)	DE @OPBO (%)	Gain (dB)	Signal BW (MHz)	PAPR (dB)	DE @Pave (%)	ACLR (dBc)
[21] 2019	2-way Outphasing	2.00	N.A.	43.0	9.0	72.0	61.0	10.0	20	8.5	60.0	-47.7
[22] 2022	Sym. 2-way Doherty	1.60-1.95	0.35	42.7-43.5	9.0	64.6-70.9	62.5-67.5	12.0-12.6	5	9.6	N.A.	-22.0
[6] 2021	Sym. 3-way Doherty	2.14	N.A.	45.3	10.0	69.0	55.0	8.6	100	8.5	54.5	-45.7
[23] 2021	Asym. 3-way Doherty	0.55-0.90	0.35	41.3-42.9	12.0	54.0-71.5	50.4-58.0	7.0-9.6	50	11.5	54.3	-47.6
[4] 2019	DEPA	1.80-3.8	2.00	44.3-46.5	8.0	42.0-62.0	41.0-51.0	7.6-10.8	10	8.0	39.0-50.0	-52.5
[12] 2020	RF-Input CM-LMBA	1.45-2.45	1.0	45.6-46.7	6.0	67.1-77.9	51.2-64.4	11.2-13.4	100	8.0	40.0-48.6	-44.3--49.0
[7] 2020	Sequential LMBA	3.05-3.55	0.5	42.3-43.7	8.0	60.8-74.8	46.8-60.7	9.5-10.3	80	10.0	49.9	-45.2
[8] 2022	Sequential ALMBA	1.70-3.00	1.3	42.0-43.0	10.0	63.0-81.0	50.0-66.0	8.0-13.0	20	9.5	50.0-56.0	-27.0--31.0
[10] 2022	Sequential CLMA	2.00-3.00	1.0	42.0-43.5	8.0	55.0-68.0	46.0-53.0	N.A.	N.A.	N.A.	N.A.	N.A.
This Work	**CLMA**	**2.10-3.50**	**1.4**	**41.4-43.1**	**7.0**	**46.7-57.5**	**35.6-50.6**	**8.6-10.8**	**60**	**7.0**	**43.8-48.5**	**-45.1--47.5**

the measurement. The generalized memory polynomial model is applied for digital pre-distortion (DPD) [24]. Fig. 19 reports the measured AM/AM and AM/PM performance with and without DPD, under the 20-MHz 7-dB PAPR signal excitation at 2.8 GHz.

The measurement is first conducted with 20-MHz OFDM signals. As shown in Fig. 20, the measured adjacent channel leakage ratios (ACLR) of the CLMA without DPD are –26.8/–27.6/–25.2 dBc at 2.3/2.8/3.3 GHz, respectively. After DPD correction, the ACLR is improved to –50.1/–50.3/–49.7 dBc at 2.3/2.8/3.3 GHz. Approximately 36 dBm average output power is achieved at these three frequencies after DPD, with an average drain efficiency of 47.4%, 50.1%, and 44.8%, respectively. The test is further conducted with 60-MHz OFDM signals. The measured ACLR is improved from –24.9/–25.7/–24.2 to –46.3/–47.5/–45.1 at 2.3/2.8/3.3 GHz after DPD, with an average drain efficiency of 45.4%, 48.5% and 43.8%, respectively.

C. Performance Comparison

The prototype PA performance is summarized and compared with recently reported state-of-the-art PAs with back-off efficiency enhancement, as shown in Table I. Compared with other published high-efficiency PAs, the proposed CLMA

exhibits excellent wideband efficiency performance at both saturation and power back-off levels. Although our CLMA prototype exhibits slightly degraded efficiency compared to the referenced LMBA, we attribute this to two main factors. Firstly, the CLMA prototype operates at higher frequencies and wider bandwidth (2.1-3.5 GHz). Secondly, the circulator used in the CLMA prototype incurs a higher loss than the one used in the LMBA. In summary, this work further advances the performance of wideband load-modulated PAs and presents the CLMA as a viable approach to further push the bandwidth–efficiency tradeoff.

VI. Condlusion

This article presents, for the first time to the authors' knowledge, a wideband circulator load-modulated amplifier. Furthermore, a unified theory of the CLMA architecture is derived. The non-reciprocal output combiner in the CLMA naturally reduces the interaction between the active devices and relaxes the auxiliary turn-off conditions, thereby minimizing the effect of parallel loss. With broadband and low-loss microwave circulators, the CLMA can perform highly efficient amplification over a large bandwidth. As a proof of concept, a prototype CLMA circuit is designed and fabricated using packaged GaN devices. The PA achieves distinct back-off efficiency enhancement across 2.1 to 3.5 GHz, verifying the wideband performance. The PA prototype also shows very good linearity performance with competitive average efficiency and output power values with modulated signals, while meeting the requirements of modern wireless communication standards. The CW and modulated signal measurement results show a large potential of the CLMA technique as a viable alternative to other back-off efficiency-enhanced PA architectures.

Appendix
Solutions to the Main reflection coefficient

In Section IV-A, a theoretical block diagram of a CM CLMA is presented, as shown in Fig. 6(a), with the class B/J continuum used as an example. To simplify the analysis of the CM load modulation process, an equivalent network comprising a real-to-real output matching network (R-OMN) and a series reactance component is employed to represent the CM output matching network, as depicted in Fig.6(b). Using equation (3), $Z_{m,S}$ can be calculated when $I_{m,S}$ and $I_{a,s}$ are obtained. As a result, $\Gamma_{m,S}$ can be derived.

Equation (11) gives the current relationship between the main and auxiliary amplifiers in the absence of the output matching network. Note that the CM output matching network serves to provide a specific impedance transformation ratio of $T = Z_0\beta/R_{opt}$. Consequently, the normalized auxiliary current at saturation can be expressed as

$$I_{a,S} = \frac{1}{2T}\left(1-\beta\right), \tag{26}$$

The CM output matching network can be expressed as the cascading of two ABCD matrices: one for the R-OMN and the other for the series reactance component jX. As a result, it is possible to derive the normalized main current as follows

$$I_{m,S} = \frac{1}{\sqrt{N(1+\alpha)}}\left(e^{j\phi} - j\left(1-\beta\right)\left(1+j\alpha\right)sin(\phi)\right). \tag{27}$$

According to (26) and (27), the $\Gamma_{m,S}$ can be derived as

$$\Gamma_{m,S} = \frac{(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j(\theta-\phi)}}{2+(\beta-1)\sqrt{1+\alpha^2}\cdot K}, \tag{28}$$

where

$$K = e^{j(\theta-\phi)} - e^{j(\arctan\alpha-2\phi)} + e^{j\arctan\alpha}.$$

Note that when

$$\theta = \arctan\alpha - \phi, \tag{29}$$

the $\Gamma_{m,S}$ can be further simplified as

$$\Gamma_{m,S} = \frac{(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j(\arctan\alpha-2\phi)}}{2+(\beta-1)\sqrt{1+\alpha^2}\cdot e^{j(\arctan\alpha)}}. \tag{30}$$

Acknowledgment

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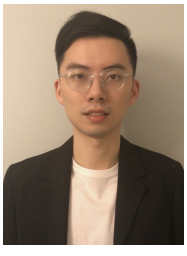

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