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ORIGINAL RESEARCH

Linear broadband interference suppression circuit based on GaN monolithic microwave integrated circuits

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Abstract

This paper presents simulation and measurement results of a 2–4 GHz octave bandwidth interference suppression circuit. The circuit accomplishes the function of a tunable frequency notch through an interferometer architecture. The relative delay in the interferometer paths is varied with GaN monolithic microwave integrated circuit tunable delay lines. The delay is adjusted by varying the drain voltage of cold-FET connected high electron mobility transistors acting as varactors. Two types of periodically-loaded delay lines are compared: a uniform and a tapered design. A simple theoretical study, relating the delays and amplitudes in the interferometer circuit branches, is developed to inform the design. Two interference suppression hybrid circuits are implemented, and measurements demonstrate a 25–40 dB notch across the 2.24–4 GHz range for the uniform delay line, and 2.32–4.13 GHz for the tapered design. The return loss for both designs remains below 10 dB. Measurements with two tones spaced 0.5 and 1 GHz for varying tone power are performed to quantify suppression. The circuit can handle an input power of 37 dBm and maintains performance with two simultaneous 25 dBm tones spaced 0.5 GHz apart. Linearity is characterised with 10 MHz two-tone measurements, and the circuit demonstrates a 3rd-order intercept input power larger than 30 dBm for control biases above −12 V.

KEYWORDS

analogue circuits, delay lines, field effect MMIC, gallium compounds, interference suppression, notch filters

1 | INTRODUCTION

Broadband receivers are susceptible to interference, and a large interfering signal can saturate the low noise amplifier (LNA), mixer, or analogue to digital converter. Generally, interference suppression circuits are intended to reduce either an in-band interfering signal, including self-interference, or out-of-band interfering signals. Self-interference methods are detailed in Ref. [1] and often rely on pre-determined knowledge of the system transfer function which determines the tapped feedback parameters [2]. For suppressing out-of-band interference, especially relevant for broadband receivers, a possible solution is electronically-tunable passive filters. These are extensively reported in the literature, for example, Refs [3–5], but can be lossy and/or bulky. A general overview of many types of interference suppression circuits for reconfigurable front ends is given in Ref. [6], including analogue finite impulse response (FIR) filters, which have been implemented in CMOS [7, 8] and GaAs [9], designed for use as equalisers in optical communication systems. The CMOS implementations usually have switched delay lines or switched capacitor banks, often referred to as N-path filters, which can be used in both in-band self [10] and out-of-band interference [11, 12], and are limited in input power handling, for example, 80 mW in Ref. [8]. A similar idea has been used in RFID for broadband leaking carrier suppression, where an analogue FIR filter is used to approximate the leakage channel in amplitude and phase across a wide band to effectively suppress the leaking carrier signal and its noise components [13]. Direct-conversion mixer-first receivers have been used for selecting a subsection of the system RF bandwidth in a passive homodyne software defined radio system [14], carrier aggregated LTE system [15], and a

10 MHz LTE system [16]. However, these require more complex and power-hungry digital backends, and noise is higher since there is no LNA before the mixer. On the other hand, feed-forward designs leverage benefits of narrow filtering at IF frequencies with better sensitivity than mixer-first topologies by splitting the signal after, or in parallel with, an LNA [17–19]. Digital cancelation can provide a large degree of suppression but still requires linear operation of receiver frontends and ADCs to work [20]. Therefore analogue linear suppression circuits can provide the necessary coarse suppression to make digital cancelation feasible.

The analogue interference suppression circuit (AISC) presented here and shown in Figure 1 performs the function of a tunable, absorptive bandstop filter and can be inserted between the antenna port and LNA of a receiver. A comparison of different bandpass and bandstop topologies is given in Ref. [21]. Substrate integrated waveguide evanescent mode cavity resonators in Ref. [22] are tuned using piezoelectric actuators, and a 44 mm × 40 mm bandstop filter is demonstrated covering 1.57–3.18 GHz with a 10 dB fractional bandwidth from 1% to 2.4%. Another example in Ref. [23] is a varactor-tuned bandstop/bandpass filter from 1.9 to 2.6 GHz with a −25 dB rejection and a bandstop bandwidth tunable from 45 to 160 MHz, with an insertion loss of 5.6 dB. A micro-electro-mechanical systems (MEMS)-tuned 12–20 GHz cavity bandstop filter with an −10 dB rejection bandwidth of 155–266 MHz and better than 40 dB rejection across tuning is shown in Ref. [24], and in Ref. [25], a 3–6 GHz MEMS-tuned bandstop cavity filter has a passband insertion loss better than 0.37 dB and greater than 60 dB rejection. These MEMS-tuned cavity filters have areas of 17 mm × 30.6 mm and 17 mm × 41 mm.

Here, we describe an AISC for out-of-band interference suppression in wideband receivers. The circuit is a two-branch hybrid interferometer with a variable delay line implemented as a GaN monolithic microwave integrated circuit (MMIC), shown in Figure 1. When two simultaneous signals at different frequencies in the 2–4 GHz octave band are incident at the input, a notch can be placed at one of the frequencies by controlling the voltage on the variable delay line. The attenuator and extra delay in Path 2 ensure destructive interference at the output. The implementation of varactors as pinched-off high electron mobility transistors (HEMTs) in a wide bandgap semiconductor (GaN) and the omission of active transistors results in improved linearity and power handling. In this case, the power handling is limited by the output power combiner and the large-signal performance of the variable capacitors in the delay line. This means that this design using GaN MMICs can operate at higher powers than other continuously tunable filters. Additionally, the AISC topology does not rely on resonators and can be miniaturised through full integration.

In the next section, the design and characterisation of two high-power capable variable true-time delay MMICs is described. In Section 3, a simple analytic approach for analysing the circuit is presented, along with the interferometer hybrid circuit design. Section 4 compares the measured and simulated tunable notch behaviour. Measurements of power handling and linearity characterisation in terms of input-referenced third order intercept point (IIP3) are performed, showcasing the advantages of the architecture.

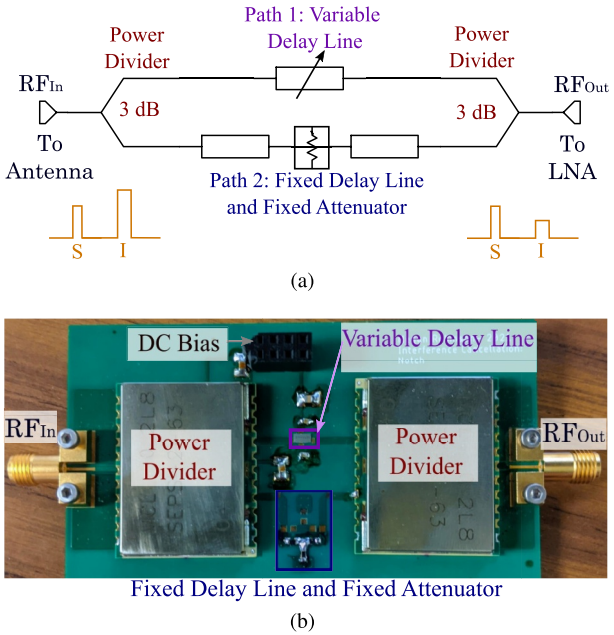

FIGURE 1 (a) Labelled block diagram of an AISC. (b) Photograph of the printed circuit boards showing surface mount reflectionless 3-dB couplers, the uniform delay line GaN MMIC in Path 1, and fixed delay lines (total delay of 433 ps) and attenuator (1.28 dB) in Path 2. A similar board is fabricated for the tapered delay line MMIC, with a different delay (463 ps) and attenuation (1.35 dB) in Path 2. The size of the board is 8.5 cm by 5 cm. AISC, analogue interference cancelation circuit. MMIC, monolithic microwave integrated circuit.

2 | VARIABLE DELAY LINE DESIGN AND PERFORMANCE

Next, we describe the design and performance of the uniform and tapered variable delay line MMICs. The circuit diagram of a loaded-line variable delay is shown in Figure 2a, where the variable capacitors are varactor diodes. The photographs in Figure 2b,c show the two MMICs designed in the WIN Semiconductors NP15 GaN on SiC process. The varactor diodes are implemented from depletion-mode HEMTs, as detailed next.

2.1 | Variable GaN HEMT capacitors

Most varactors in GaN are implemented based on the gate-to-channel capacitance of a HEMT structure, where separate drain and source contacts are either omitted in the layout [26, 27] or shorted together [28]. Since the capacitance variation occurs for a relatively small voltage swing, the linearity is poor but can be improved by using an anti-serial connection [29].

The variable capacitance in this work is implemented as a cold-FET topology by using a standard HEMT device, as shown in Figure 3. The gate is biased at −20 V for pinch-off, and the varactor is formed by the output capacitance of the

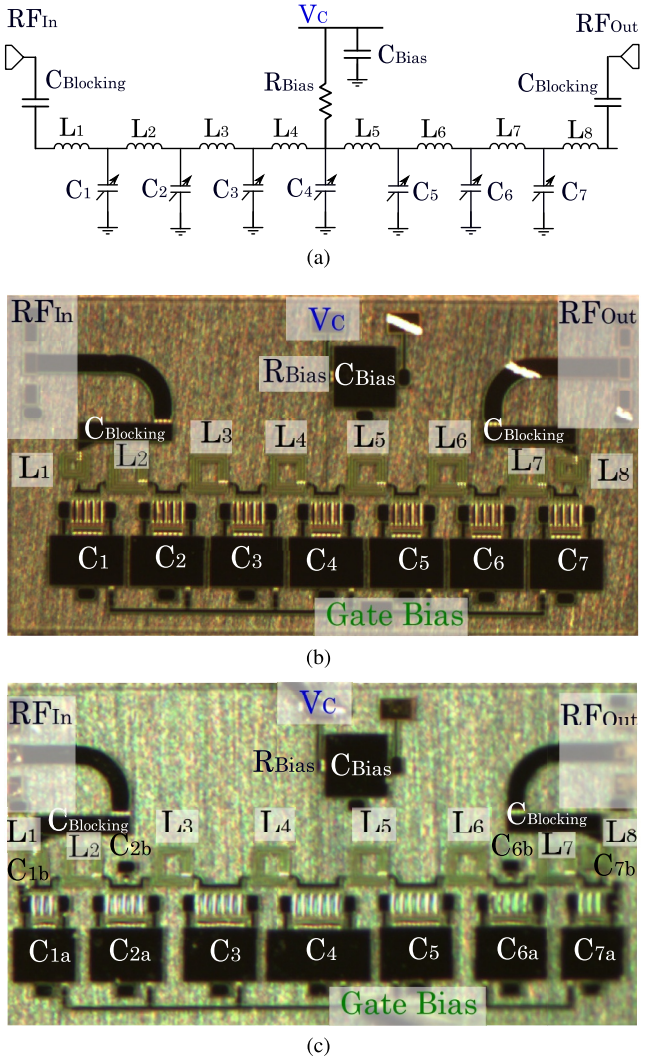

FIGURE 2 (a) Circuit schematic of a tunable true-time artificial transmission-line delay, consisting of inductors and variable capacitors. (b and c) Photographs of the uniform and tapered delay lines, respectively. Note the different sizes of transistors in (c). The chips are 1.6 mm × 3.0 mm in area.

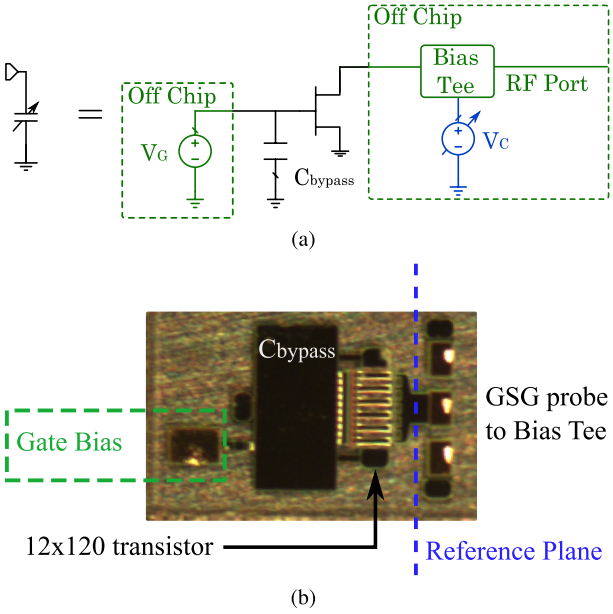

FIGURE 3 (a) Circuit schematic of the variable capacitor showing the gate bias and drain control bias circuits. (b) Photograph of a single 12 × 120-μm device used to extract the capacitance from a one-port measurement calibrated to the reference plane shown in a dashed line.

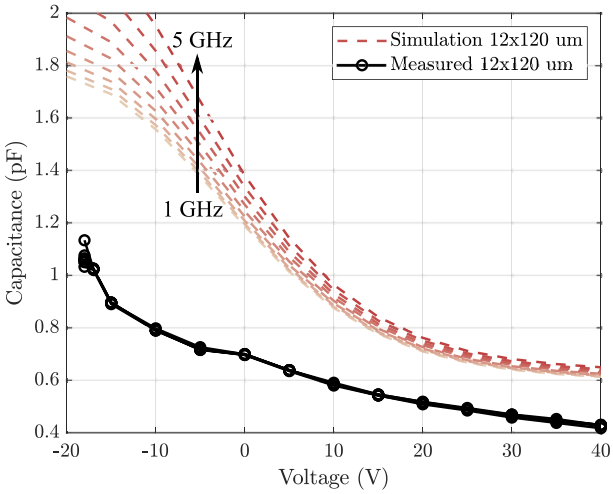

FIGURE 4 A comparison of measured (black line with symbols) and simulated (red dashed lines) tunable capacitor extracted from one-port measured and simulated data. Both are performed from 1 to 5 GHz, showing little frequency variation in the measured data.

cold HEMT. To adjust the capacitance, the drain bias voltage is varied between −20 and +40 V. This topology has a larger relative capacitance range of 2.4:1 for the measured fabricated capacitors compared to 1.7:1 for the diode-connected transistor in simulation. While this topology adds complexity through the requirement of a secondary bias voltage and the bypass capacitor, it expands the tuning bias voltage range from 2 V (−3 to −1 V) to 60 V (−20 to +40 V). The wider tuning voltage provides improved linearity and high power performance, which we investigate in Section 4.2.

The non-linear HEMT model in the WIN process is extracted for amplifier design, so we expect the model to only predict trends when the transistors are in a varactor configuration. Therefore, a separate variable capacitor with a 12 × 100-μm HEMT is fabricated for characterisation and comparison with the non-linear model. The capacitor is measured using an on-wafer SOLT calibration kit and the measured capacitance extracted from a S_{11} measurement. The comparison with non-linear simulations is shown in Figure 4. The red curves are extracted capacitance values from a 1–5 GHz one-port simulation for the 12-finger device, while the measured capacitance is plotted in a solid black line and has a smaller value and range, indicating that the non-linear foundry model over-estimates the drain-to-source capacitance in heavy pinch-off conditions. Additionally, the measured device starts drawing current at $V_C = -18$ V due to reverse conduction in the channel, which does not occur in simulation.

2.2 | Variable delay line MMICs and characterisation

Using the HEMT variable capacitors as in Figure 3, two artificial transmission-line delays are designed (Figure 2). The uniform line has seven equal 8 × 122 μm HEMT capacitors. For a control voltage variation from −20 to +40 V, the simulated capacitance range is 0.4–1.3 pF. The inductor values for a 50 Ω line are 2.1 nH, and a Tee unit cell is implemented, so that the edge inductors (L_1 and L_8) are 1 nH.

The tapered impedance line is designed to have a larger group delay variation for the same minimum return loss. When tuning only a single reactance element of an artificial transmission line, it is impossible to vary the delay without affecting the characteristic impedance and hence the return loss of the line. For the tapered line, we employ a larger capacitance variation in the centre (capacitors C_3, C_4, and C_5) than at the edge elements, such that the impedance variation at the edge elements is smaller than in the centre, as summarised in Table 1. Similar to a tapered transmission line, the gradual change in the impedance of the artificial transmission line results in a lower return loss at the edges of the tuning range for the same overall impedance variation.

To implement a lower capacitance variation with the same total capacitance at the edge elements, the smaller varactor cells for C_{1a}, C_{2a}, C_{6a}, and C_{7a} are placed in parallel with fixed capacitors C_{Xb}, as shown in Figure 2c. The inductors used for the tapered line are identical to those in the uniform line. The resulting characteristic impedance is plotted for each cell of the simulated artificial transmission line of both types in Figure 5 for seven different control voltages. Note that we compute the impedance based on the average of the inductance values adjacent to the capacitors, which leads to the lower impedances for the first and last elements of the uniform line. Note that the impedance of the tapered line varies less for the end elements (40–58 Ω) compared to the uniform line (35–63 Ω), resulting in improved return loss. Recomputing the characteristic impedances for the measured capacitance values (Table 1), there is an increase in impedance, but the general trend of less impedance variation at the input and output ports of the tapered line holds.

The fabricated delay lines were measured on-wafer with an external SOLT calibration substrate. Figure 6 shows simulated *S*-parameters for both lines compared to the measured results from 1 to 5 GHz. The match remains below −8.2 and −12 dB for the uniform and tapered lines, respectively, in both simulations and measurements. As expected, the tapered line has less variation in the impedance match over the voltage tuning range. The transmission coefficient remains approximately constant with tuning voltage in measurement, although simulations show significant variation. Figure 7 displays the simulated and measured group delay, showing a variation of 230–350 ps and 260–385 ps at 3 GHz for the uniform and tapered delay lines, respectively. The group delay variation is less than 35 ps across the 2–4 GHz range for the tapered line and is <25 ps for the uniform delay line.

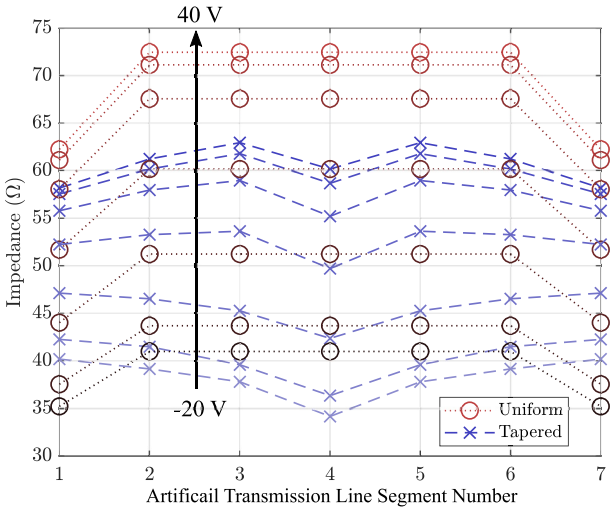

FIGURE 5 Characteristic impedance of each line segment of the simulated uniform and tapered artificial transmission lines at 3 GHz plotted for control voltages of −20 to +40 V with steps of 10 V.

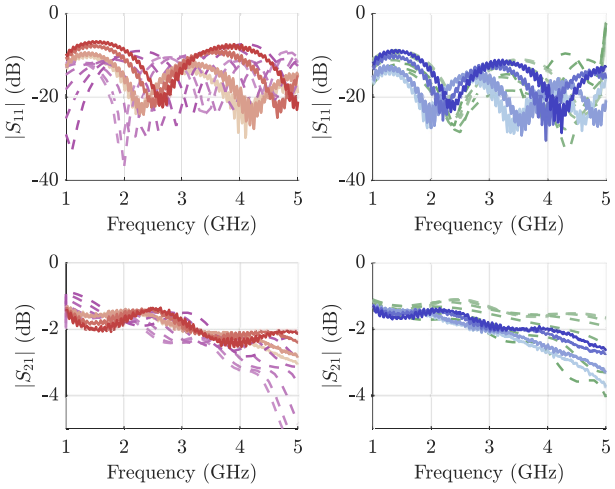

FIGURE 6 Measured (solid) and simulated (dashed) $|S_{11}|$ (top) and $|S_{21}|$ (bottom) for the uniform (left) and tapered (right) tunable delay line MMICs. MMIC, monolithic microwave integrated circuit.

Capacitor	Device size	Simulated capacitance (pF)	Measured capacitance (pF)
C_1 & C_7	6 × 108 μm	0.46–0.93	0.31–0.57
C_2 & C_6	10 × 110 μm	0.51–1.4	0.51–0.95
C_3 & C_5	12 × 106 μm	0.6–1.4	0.38–0.91
C_4	12 × 120 μm	0.63–1.5	0.43–1.02

TABLE 1 Capacitance values of tapered delay line.

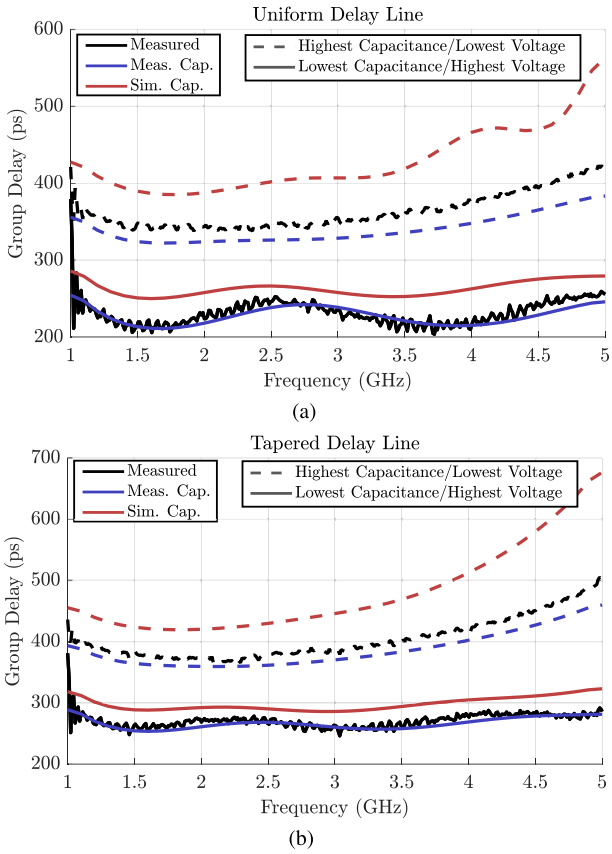

FIGURE 7 Measured (black), simulated with the measured capacitance (blue), and simulated with the simulated capacitance (red) group delay for the uniform (a) and tapered (b) tunable delay-line MMICs, for a control voltage variation of −20 V (dashed) and +40 V (solid). MMIC, monolithic microwave integrated circuit.

3 | INTERFERENCE SUPPRESSION CIRCUIT DESIGN

The AISC from Figure 1a is first analysed theoretically by using some assumptions, as described below. The results of this simple theory are used to guide two designs using non-linear circuit simulations. The fabricated prototypes shown in Figure 1b are then characterised.

3.1 | Simplified AISC theory

Figure 8 defines the parameters used in the simplified analysis. The input signal to the interferometer $\underline{S}_{in}$ passes through a power divider where it is split into components $\underline{S}_1(f) = S_1(f)e^{j\theta_1(f)}$ and $\underline{S}_2(f) = S_2(f)e^{j\theta_2(f)}$. The signals are then delayed in the two paths. The signal in Path 1 attenuates and is delayed as a function of the control voltage V_c, resulting in signal $\underline{A}_1$ at the input of the combiner:

$$\underline{A}_1 = A_1 e^{\phi_1} = \alpha_1(f, V_c) S_1(f) e^{j\theta_1(f) - j2\pi f \tau_1(V_c)} \quad (1)$$

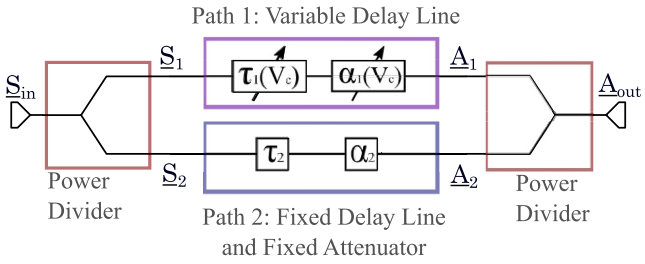

FIGURE 8 Circuit diagram of the interferometer, showing the input signals ($\underline{S}_{in}$, $\underline{S}_1$, and $\underline{S}_2$), delays ($\tau_1(V_c)$ and τ_2), attenuation ($\alpha_1(V_c)$ and α_2) and output signals ($\underline{A}_{out}$, $\underline{A}_1$ and $\underline{A}_2$).

where α_1 and τ_1 are the amplitude and delay of Path 1, respectively. Similarly, the signal $\underline{A}_2$ at the input of the combiner in Path 2 is

$$\underline{A}_2 = A_2 e^{\phi_2} = \alpha_2(f) S_2(f) e^{j\theta_2(f) - j2\pi f \tau_2} \quad (2)$$

where the amplitude α_2 and delay τ_2 are fixed. At the output of the combiner, the total signal becomes

$$\underline{A}_{out} = A_1 e^{\phi_1} + A_2 e^{\phi_2} \quad (3)$$

where we assume a perfect lossless in-phase combiner. Any amplitude or phase imbalance can be included in the frequency response of the input power divider without loss of generality. The output signal can be written as

$$\underline{A}_{out} = A_1 e^{\phi_1} \left(1 + \frac{A_2}{A_1} e^{\phi_2 - \phi_1}\right) \quad (4)$$

and its amplitude is

$$|\underline{A}_{out}| = A_1 \cdot \sqrt{1 + \left(\frac{A_2}{A_1}\right)^2 + 2\frac{A_2}{A_1}\cos(\phi_2 - \phi_1)}, \quad (5)$$

where the phases can be expressed as $\phi_i = \theta_i - 2\pi f \tau_i$. The phase difference is now

$$\phi_2 - \phi_1 = \Delta\theta - 2\pi f \Delta\tau, \quad (6)$$

where $\Delta\theta = \theta_2 - \theta_1$ and $\Delta\tau = \tau_2 - \tau_1$. Figure 9 shows a plot of $|\underline{A}_{out}|/|\underline{S}_{in}|$ as a function of normalised frequency f/f_N, where f_N is the centre frequency of the notch, for different ratios (A_1/A_2). We observe that perfect cancelation occurs at $f = f_N$ corresponding to $\phi_2 - \phi_1 = \pi$ and for an amplitude ratio of $A_2/A_1 = 1$. Deviating from this amplitude ratio results in a wider and shallower notch but does not change the frequency of maximum cancelation. Therefore, the effects of amplitude imbalance can be separated from the frequency response.

For $A_1 = A_2 = \frac{1}{2}$, the output magnitude is

$$|\underline{A}_{out}| = \frac{1}{2}\sqrt{2 + 2\cos(\phi_2 - \phi_1)}, \quad (7)$$

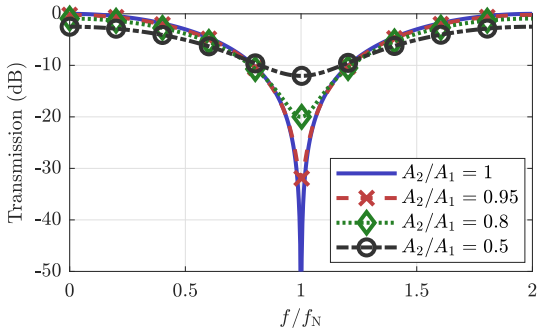

FIGURE 9 Transmission magnitude $|A_{out}|/|S_{in}|$ as a function of f/f_N when $A_1 = 1/\sqrt{2}$ for different amplitude ratios A_2/A_1.

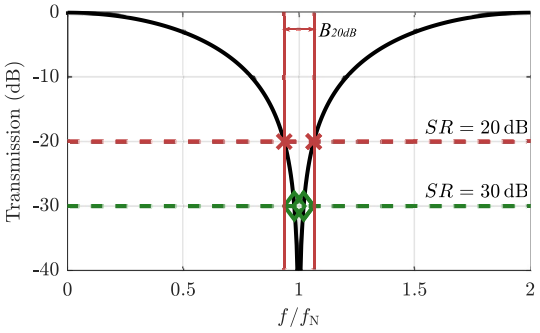

FIGURE 10 Transmission magnitude $|A_{out}|/|S_{in}|$ compared to f/f_N and output of the notch circuit when $A_1 = 1/\sqrt{2}$ and $A_2/A_1 = 1$. The 20 and 30 dB suppression ratio is shown in dashed lines. The notch bandwidth is shown with the symbols 'x' and '◊' for the 20 and 30 dB cases, respectively.

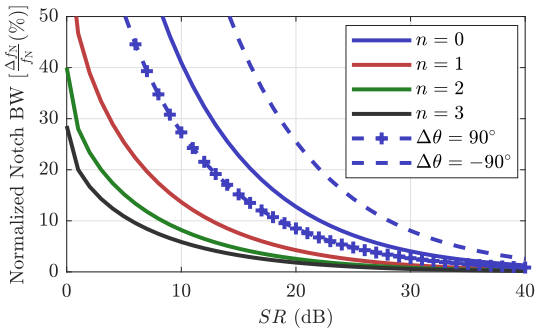

FIGURE 11 Normalised notch bandwidth compared to SR when $\Delta\theta = 0$ for the first notch ($n = 0$), second notch ($n = 1$), third notch ($n = 2$), and forth notch ($n = 3$). The dashed lines show the effects of a $\pm 90°$ phase shift to the $n = 0$ notch.

with a notch occurring periodically according to

$$\phi_2 - \phi_1 = 2n\pi - \pi, \quad \forall n \in \mathbf{Z}. \tag{8}$$

Replacing ϕ_i from Equation (6), the frequency of maximum cancelation can be expressed as

$$f_N = \frac{\pi + \Delta\theta}{2\pi\Delta\tau} + \frac{n}{\Delta\tau}, \quad \forall n \in \mathbf{Z}. \tag{9}$$

We note that notches occur periodically with a spacing of $1/\Delta\tau$. The phase difference between paths $\Delta\theta$ shifts them in frequency, while the delay difference between paths $\Delta\tau$ scales the frequency separation between notches and the position of the first notch.

To find the bandwidth of the notch, we define a suppression ratio SR in dB, and assume $SR = 20$ and 30 dB in Figure 10. The bandwidths for the two cases (depicted with the symbols 'x' and '◊' in Figure 10) are related to the delay difference $\Delta\tau$, the suppression ratio (SR) and the centre frequency of the notch. In general, it is straightforward to solve for the bandwidth given a specific suppression ratio:

$$B = 2\left(f_N - \frac{\Theta_{SR} + \Delta\theta}{2\pi\Delta\tau}\right), \tag{10}$$

and

$$\Theta_{SR} = \cos^{-1}\left[\left(\frac{2}{10^{SR/10}}\right) - 1\right]. \tag{11}$$

Using Equation (9) we compute the normalised notch bandwidth as

$$\frac{B}{f_N} = \frac{2\pi - 2\Theta_{SR}}{2n\pi + \pi + \Delta\theta}, \quad \forall n \in \mathbf{Z}. \tag{12}$$

The normalised notch bandwidth for a given suppression ratio depends on the phase shift $\Delta\theta$ and the notch index n but not on $\Delta\tau$, as illustrated in Figure 11. For the same suppression ratio, a larger n leads to a narrower notch, a feature that is generally desirable in notch filters. Additionally, a fixed positive phase shift, $\Delta\theta$ can reduce the notch bandwidth, as shown for the $n = 0$ case in dashed lines in Figure 11. However, there is a tradeoff between the notch bandwidth and the tuning range of the filter, as investigated next.

3.2 | Tuning bandwidth

The useful tuning range of the notch centre frequency f_N is limited by the frequency of the next higher-order notch, illustrated in Figure 12. The possible notch frequencies for four notch orders are shown in Figure 12a, illustrating that for $n = 0$ (blue) and for $\Delta\tau = 167$ ps, there is a notch at 3 GHz. When tuning the delay to 0.5 ns, the second-order notch appears. Figure 12b shows that the first notch tunes lower in frequency as the delay is increased, and the second notch appears at the initial first notch frequency for a delay of 0.5 ns. The plots assume that there is no considerable dispersion of $\Delta\theta(f)$. If the dispersion is linear, it can be mathematically included in the time delay of one of the paths.

To quantify the tuning, Equation (9) can be rewritten as

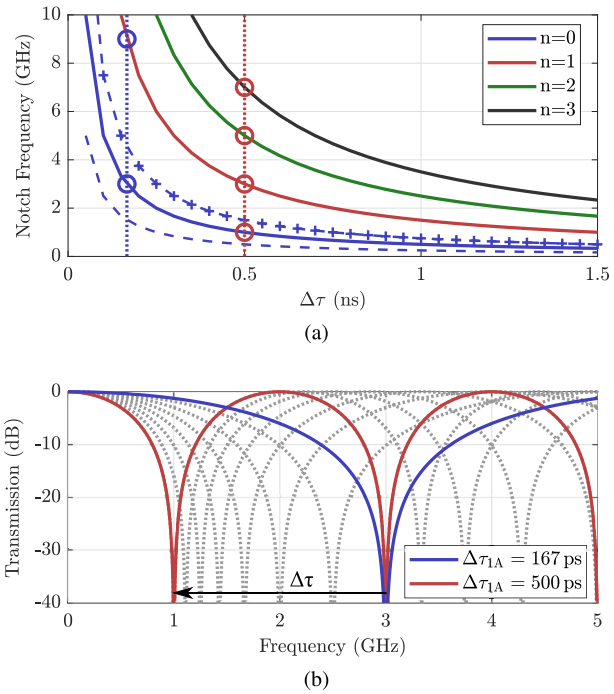

FIGURE 12 (a) Notch frequency f_N compared to $\Delta\tau$. It is shown in terms of GHz and ns, however, the entire graph scales even to Hz and s. (b) The magnitude versus frequency for $\Delta\tau = 0.167$ ns, and $\Delta\tau = 0.5$ ns, the cross section indicated by the dashed blue line and the dashed red line in (a).

$$f_{Nn} = \frac{2\pi n + \pi + \Delta\theta}{2\pi(\Delta\tau)}, \quad \forall n \in \mathbf{Z} \tag{13}$$

The ratio between neighbouring notch frequencies becomes

$$\frac{f_{N(n+1)}}{f_{Nn}} = \frac{(2n+3)\pi - \Delta\theta}{(2n+1)\pi - \Delta\theta}. \tag{14}$$

When $\Delta\theta(f) = 0$, the first notch ($n = 0$) tuning ratio is

$$\frac{f_{N1}}{f_{N0}} = \frac{3}{1}. \tag{15}$$

In summary, the simplified theory is useful for providing design guidelines as follows:

- The depth of the notch depends on the balance of the gains in the two branches. As expected, if the gain is equal for a 3-dB splitter/combiner, the notch depth is the largest and degrades to 12 dB for a 3-dB gain ratio.
- The notch fractional bandwidth is related to the suppression ratio and is the lowest for the first notch. For example, for $SR = 20$ dB, the bandwidth of the first notch ($n = 0$) is 12.7%, while that of the third notch ($n = 2$) is 2.5%.
- The notch tuning range is inversely proportional to the relative delay change. The first notch frequency has the most variation for small changes in delay, for example, a delay change of 125 ps results in frequency tuning from 2 to 4 GHz. Higher order notches require more delay change for the same relative frequency change, for example, for $n = 2$, $\Delta\tau = 625$ ps for the same frequency change.
- Introducing a relative phase shift between the two branches of the interferometer can increase the tuning frequency range at the expense of the normalised notch bandwidth, shown in dashed lines in Figures 11 and 12.

3.3 | Design and fabrication

The 2–4 GHz tunable notch designs have a 2:1 tuning ratio, which means that the $n = 0$ null has to be chosen so that only one notch is present in the tuning band. For $n = 0$ in Equation (9), we obtain the delays at the two edges of the frequency band, $\Delta\tau_1$ and $\Delta\tau_2$, for $\Delta\theta = 0$, as follows:

$$\Delta\tau_1 = 250\,\text{ps} \quad \text{and} \quad \Delta\tau_2 = 125\,\text{ps}. \tag{16}$$

To achieve this with the uniform and tapered lines, with 230–350 ps and 270–390 ps delays, fixed delays of 478 and 518 ps are needed, respectively. There are two additional effects: dispersion of phase and attenuation. To determine which of the two is dominant, the attenuation is kept constant at 2 dB in simulations and, as a result, the tuning range decreased from 2–4 GHz to 2–3.25 GHz. In this case, the fixed delay is reduced to 453 and 480 ps, for the uniform and tapered lines, respectively, to re-centre the notch at 3 GHz. The responses with the measured *S*-parameters of the delay lines, keeping other components ideal, are shown in Figure 13.

For the circuit implementation of Figure 1, the fixed delay lines are achieved with microstrip 50-Ω transmission lines. The fixed attenuation is 1.28 and 1.34 dB for the uniform and tapered delay-line circuits, respectively, and is determined from the loss in Paths 1 and 2 in Figure 1. Surface-mount three-port dividers/combiners (MiniCircuits SEPS-2-63+) that operate from 0.68 to 6 GHz are chosen and have a high power handling capability of 5 W. The combiners are well isolated and therefore assure that the AISC will behave like an absorptive filter. The MMICs are epoxied directly on the 2-layer 20-mil 4350B Rogers' substrate and bonded to the 50-Ω microstrip traces. The fixed attenuator is achieved by a Tee network of surface-mount 0603 resistors, with series resistors of 3.6 and 4.3 Ω, and parallel resistors of 330 and 360 Ω for the uniform and the tapered delay-line circuits, respectively. The bias/control lines have blocking capacitors.

4 | MEASURED PERFORMANCE

The hybrid circuit from Figure 1 is characterised experimentally. Following small-signal measurements, the linearity of the circuits is characterised using 2-tone measurements. The current consumption of the chip is less 0.01 mA during normal operation, but when $V_C < -19$ V the conduction current can

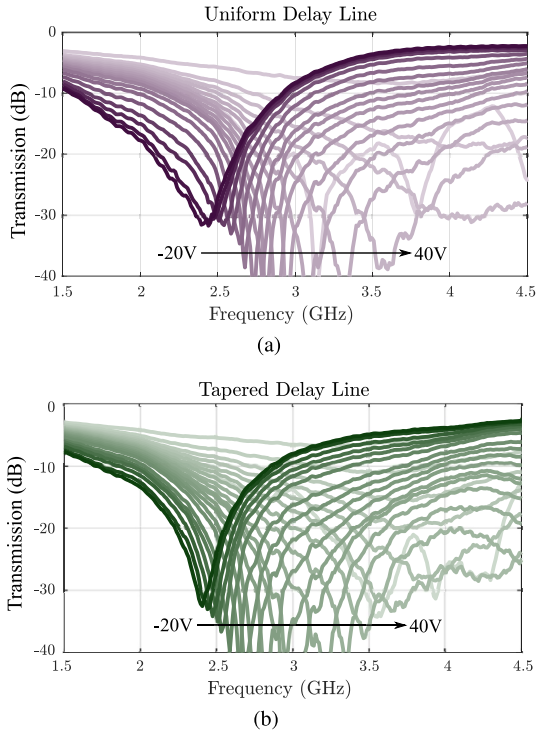

FIGURE 13 Simulated tuning of the notches from 2 to 4 GHz using the measured frequency-varying loss and time delay of the two MMICs in an ideal interferometer circuit, for (a) the uniform and (b) tapered delay lines. MMIC, monolithic microwave integrated circuit.

reach 1 mA. Therefore the calculated power consumption ranges from 10 μW to 20 mW.

4.1 | Small-signal simulations and measurements

Small-signal simulations are performed with measured MMIC delay line *S*-parameters, and including 0.1 nH bond-wire inductances at input and output. Manufacturer-provided *S*-parameters for the resistors and dividers are used in the simulations. Figure 14 shows $|S_{11}|$ with a comparison to measurements of the full circuits. A similar comparison is shown for $|S_{21}|$ in Figure 15. The notches tune over 2.24–4 GHz for the uniform line AISC and 2.32–4.13 GHz for the tapered line AISC. The attenuation at the desired notch frequencies is greater than −30 dB. The uniform-line circuit shows deeper notches with variable depth across frequency, while the tapered-line circuit exhibits a consistent notch depth over the tuning range. We define the insertion loss of the circuit, IL_{LOW}, as the loss at the lowest notch frequency, when the notch is set to the highest frequency. A similar insertion loss IL_{HIGH} can be defined for the complementary case. For the uniform-line AISC, IL_{LOW} = 5.01 dB and IL_{HIGH} = 4.48 dB, while the tapered-line AISC measures IL_{LOW} = 6.16 dB and IL_{HIGH} = 5.31 dB. Note that the notch depth degrades for control voltages below −18 V, due to the HEMT varactors starting to conduct, increasing the loss.

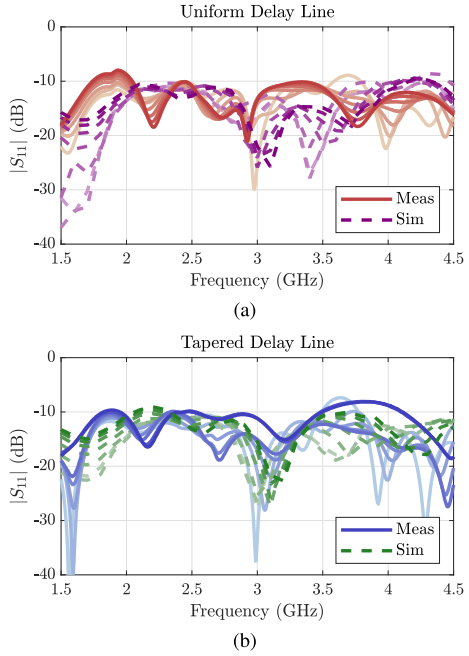

FIGURE 14 Measured (solid) and simulated (dashed) $|S_{11}|$ for the interferometer circuits with uniform (a) and tapered (b) MMIC delay lines over the −20 to +40 V control voltage range in 10 V steps. MMIC, monolithic microwave integrated circuit.

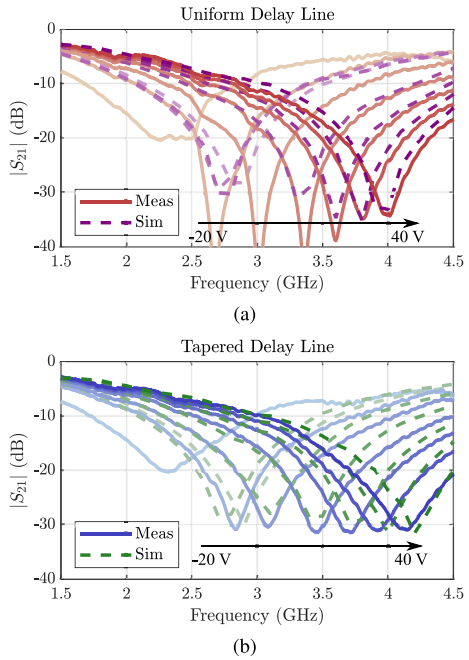

FIGURE 15 Measured (solid) and simulated (dashed) $|S_{21}|$ for the interferometer circuit with uniform (a) and tapered (b) MMIC delay lines over the −20 to +40 V control voltage range in 10 V steps. MMIC, monolithic microwave integrated circuit.

4.2 | Non-linear characterisation

Since the GaN interference suppression circuit is the first component in the received chain after the LNA, it is important

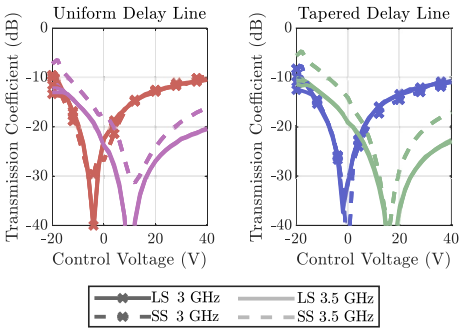

FIGURE 16 Large signal measurements (solid line) for 25 dBm input power per tone, compared to small-signal S-parameters (dashed line). The $|S_{21}|$ is shown for the uniform (left) and tapered (right) tunable delay line MMIC circuits with simultaneous large signal tones at 3 and 3.5 GHz. MMIC, monolithic microwave integrated circuit.

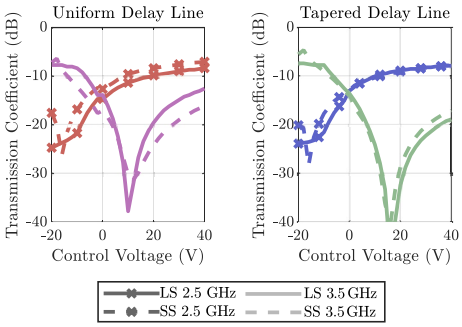

FIGURE 17 Large signal measurements (solid line) for 25 dBm input power per tone, compared to small-signal S-parameters (dashed line). The $|S_{21}|$ is shown for the uniform (left) and tapered (right) tunable delay line MMIC circuits with simultaneous large signal tones at 2.5 and 3.5 GHz. MMIC, monolithic microwave integrated circuit.

to characterise its linearity. The first step is to verify that the circuit operates under large signal input. Figure 16 shows a comparison of the small and large-signal transmission coefficient for two simultaneous 25 dBm tones spaced 500 MHz apart. Very similar results are obtained for other tone frequencies across the band at the same spacing. For a larger tone spacing of 1 GHz, Figure 17 shows the same comparison. The notch performance remains very similar between the small signal and large signal measurements.

A two-tone measurement is next performed with P_{in} = 22–26 dBm in each tone with a 10 MHz tone spacing. Figure 18 shows the measured results and calculated third order intercept point (IP3) at 3 GHz for −20, 10, and 40 V control voltages along with the control voltage associated with the 3 GHz notch, −2 and, −4 V for the tapered and uniform delay lines, respectively. Note that for the control voltage corresponding to the notch, the fundamental output signal amplitude is reduced due to the notch effect. However, the non-linear components created by the varactors in the variable delay line branch of the interferometer do not cancel and hence the IMD3 products are unaltered, resulting in a lower IIP3 for that control setting.

Figure 19 shows the IIP3 as a function of control voltage for tones centred at 2.5, 3, and 3.5 GHz, with the notch control

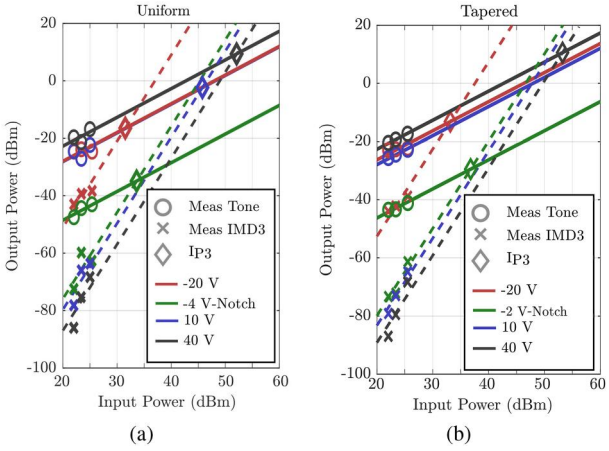

FIGURE 18 The measured signal and third order mixing product with the calculated third order intercept point at 3 GHz for −20, 10, and 40 V control voltages, as well as for control voltages associated with the 3 GHz notch for the for the (a) uniform (−4 V) and (b) tapered (−2 V) analogue interference suppression circuits, respectively.

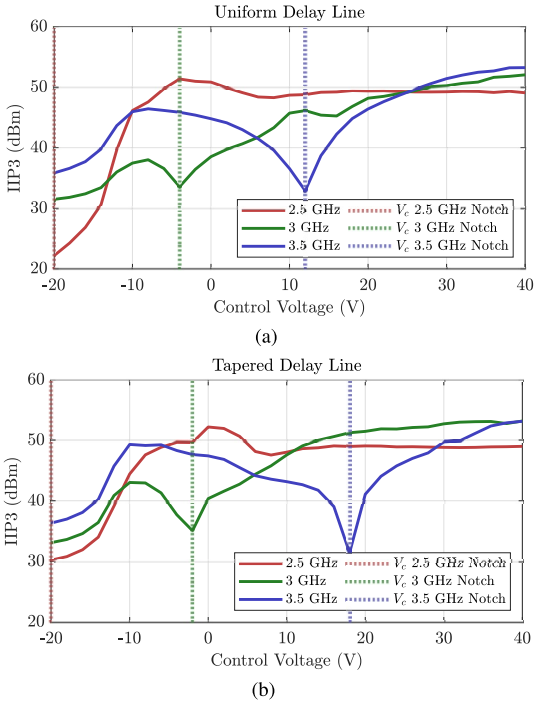

FIGURE 19 Measured IIP3 of a 10 MHz spaced two tone signal centred at 2.5, 3, and 3.5 GHz for the uniform delay line (a) and tapered delay line (b).

voltages labelled for the three frequencies. Similar results are obtained at other frequencies within the octave. Note the degradation in linearity for low control voltages between −20 and −10 V due to reverse conduction in this bias region in large-signal operation. The total IIP3 observed in Figure 19 is therefore the superposition of the increased nonlinearity for low control voltages and the linear effect of the notch attenuation.

Finally, the power handling of the circuit is tested by increasing the input power up to 5 W. After this, the small-signal S − parameters are remeasured with no observable change.

TABLE 2 Comparison with prior work in tunable bandstop filters.

Ref.	Tuning range (GHz)	Voltage range (V)	Suppression (dB)	Notch bandwidth (MHz)	Insertion loss (dB)	Size (mm × mm)	Power handling	IIP3 (dBm)
[30]	1.8–2.2	−1.2 to −0.2	35	50	-	1.2 × 1.2	-	-
[31]	3.5–6.5	0 to 17	11	550	<1	4.8 × 2.9	0.1 dBm	10
[32]	1.2–2.6	0 to 65	40	140	<0.8	37 × ?	-	>25
[25]	3–6	-	60	-	0.37	41 × 17	-	-
[22]	1.57–3.18	0 to 90	47	50	<2	45 × 45	-	-
[33]	0.5–2	1.3 to 27.4	30	200	-	-	-	-
[34]	1.8–2	−20 to 0	50	200	<2	-	-	-
[23]	1.9–2.6	0 to 15	25	45–160	5.4	40 × 23	-	-
[35]	0.5–2.5	0 to 28	25	500	-	23 × ?	-	-
[36]	4–6.4	2.8 to 9	16–30	1700	-	38 × 38	-	-
Uniform (AISC)	2.2–4	−20 to 40	35	1000	5.01	85 × 50	37 dBm	>30
Tapered (AISC)	2.3–4.1	−20 to 40	30	1000	6.16	85 × 50	37 dBm	>30

Abbreviation: AISC, analogue interference suppression circuit.

5 | CONCLUSION

In summary, we present the design of a broadband analogue interference suppression hybrid circuit implemented with GaN MMIC tunable delay lines, which can help prevent the saturation of wideband receiver front-end components caused by strong interferers. Table 2 compares tunable bandstop filters in a similar frequency range, highlighting quantities usually missing in literature, namely the power handling and linearity of the AISCs. The few reported values are significantly lower, for example, in Ref. [31], a maximum voltage of 1.6 V_{pp} on the MEMS is reported, which corresponds to 0.1 dBm of input power; the authors in Ref. [17] state 2.6 dBm for a feedforward integrated LNA design.

The interferometer circuit topology is analysed using a simplified theory that takes into account dispersion and predicts the trends observed in non-linear simulations and measurements. Two types of periodically-loaded GaN MMIC delay lines using HEMT varactors are compared: a uniform and a tapered design. Measurements demonstrate a 25–40 dB notch across the 2.5–4 GHz range (46% fractional bandwidth) for the uniform delay line and a constant 30-dB notch for the tapered design with improved return loss exceeding 12 dB, thus acting as an absorptive filter. Measurements with two tones spaced 0.5 and 1 GHz for varying tone power are performed to quantify suppression, and the two-tone third order intercept exceeds 30 dBm for tuning voltages above −12 V. The circuit can form a notch with up to 2 W of total input power.

The implemented tunable notch hybrid circuit does not have any gain and would thus increase the noise figure of the receiver as with any lossy filter. However, since the delay lines are implemented in a MMIC, gain stages can easily be integrated as demonstrated in a GaAs MMIC at X-band in Ref. [37], which improves noise in the figure. This X-band GaAs MMIC is fully integrated with Lange couplers used for the input power divider and output power combiner on chip. This approach could be done for the 2–4 GHz band with a larger chip size. Additionally, the output combiner is the limitation for power handling as it must be able to absorb the power of the suppressed signal. For this reason, an on-chip Lange coupler in conjunction with an off-chip resistor could improve power handling and reduce the size of the circuit. This approach can also be extended to multiple simultaneous notches by additional parallel paths, and a tuning speed below a microsecond can easily be achieved.

AUTHOR CONTRIBUTIONS

Megan C. Robinson: Conceptualization; data curation; formal analysis; investigation; methodology; validation; visualization; writing – original draft. **Zoya Popović**: Conceptualization; funding acquisition; resources; supervision; validation; writing – original draft. **Gregor Lasser**: Conceptualization; funding acquisition; methodology; project administration; supervision; validation; writing – review & editing.

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CONFLICT OF INTEREST STATEMENT

The authors have no conflict of interest to disclose.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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