THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Low-Power HEMT LNAs for Quantum Computing

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Gothenburg, Sweden, 2023

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Technical Report No. 462
ISSN 1652-0769
This thesis has been prepared using LaTeX.

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Printed by Chalmers Reproservice
Gothenburg, Sweden, September, 2023

'I have no special talents. I am only passionately curious' - Albert Einstein

Abstract

The rapid development of quantum computing technology predicts much more qubits to handle in the detection, readout, and amplification of qubits than in today's system. Due to the limited cooling capability of the dilution refrigerator, the current low-noise amplifiers (LNAs) are in need of ten to hundred times reduced dc power consumption yet with lowest noise temperature at qubit readout frequencies, typcially 4-12 GHz. Cryogenic indium phosphide (InP) high electron mobility transistor (HEMT) LNAs, are the standard qubit amplifier at 4 K in today's superconducting quantum system. However, the power consumption of current InP HEMT LNAs is still too high for future quantum system up-scaling.

A small-signal noise model of a 100-nm gate-length InP HEMTs has been characterized and extracted at 4 K ambient under low-power bias down to 1 μW. The extracted low-power small-signal noise models revealed fast degradation points of drain voltage bias for RF and noise performance.

The design goals of the cryogenic LNA were tailored for a superconducting qubit readout application based on the extracted low-power small-signal noise model of the InP HEMT for optimum noise and power consumption trade-off. A cryogenic InP HEMT hybrid LNA operating in the 4-6 GHz frequency range at 200 μW with an average noise temperature of 2.0 K has been designed, fabricated and successfully demonstrated, validating the extracted model and design methodology.

An epitaxially-optimized InP HEMT was modeled with the low-power methodology. The comparison of the small-signal noise model parameters to the standard InP HEMT showed improved transconductance, matching, and noise at the same bias power. The demonstrated three-stage cryogenic 4-6 GHz LNA equipped with an optimized HEMT as the first stage achieved 2.0 K average noise temperature at 100 μW dc power dissipation, representing a new state-of-the-art. This licentiate thesis has presented experimental evidence that there is large potential in reducing dc power in the cryogenic InP HEMT LNA for qubit readout which can be important for the planned up-scaling in future quantum computing.

Keywords: Cryogenic, quantum computing, qubit, low-power, low-noise amplifier, InP HEMT.

List of Publications

This thesis is based on the following publications:

[A] **Yin Zeng**, Jörgen Stenarson, Peter Sobis, Niklas Wadefalk, Jan Grahn, "A 100-μW 4–6 GHz Cryogenic InP HEMT LNA Achieving an Average Noise Temperature of 2.6 K". Published in *34th Asia-Pacific Microwave Conference* (pp. 13-15). IEEE, Dec, 2022.

[B] **Yin Zeng**, Jörgen Stenarson, Peter Sobis, Niklas Wadefalk, Jan Grahn, "Sub-mW Cryogenic InP HEMT LNA for Qubit Readout". Accepted for publication in *IEEE Transactions on Microwave Theory and Techniques*, Aug. 2023.

[C] **Yin Zeng**, Jörgen Stenarson, Peter Sobis, Jan Grahn, "100-μW Cryogenic HEMT LNAs for Quantum Computing". Accepted by *18th European Microwave Integrated Circuits Conference*, Sept. 2023.

Contents

CHAPTER 1

Introduction

1.1 Low-power HEMT LNAs for quantum computing

The high electron mobility transistor (HEMT) low-noise amplifier (LNA) is one of the crucial components in superconducting quantum computers. The quantum processor relies on microwave components at 4-12 GHz [1]. Since the qubit represents a signal power of typically -120 dBm, microwave amplification of qubits becomes critical. In Fig. 1.1, a schematic of a typical qubit handling is presented. The first stage amplifier is a superconducting Josephson parametric amplifier (JPA) or traveling wave parametric amplifier (TWPA). Parametric amplifiers are quantum-noise limited and dissipates nearly zero dc power at 10 mK ambient temperature [2]. Following the superconducting amplifier, the second stage amplifier is the HEMT LNA at the 4 K stage [3], [4]. After around 10 dB loss of the cable, a room-temperature amplifier is followed, to provide amplification before the digitizer [4], [5].

The HEMT LNA in Fig. 1.1 is the focus of this thesis. When the HEMT LNA is used as the second stage amplifier after the parametric amplifier, a

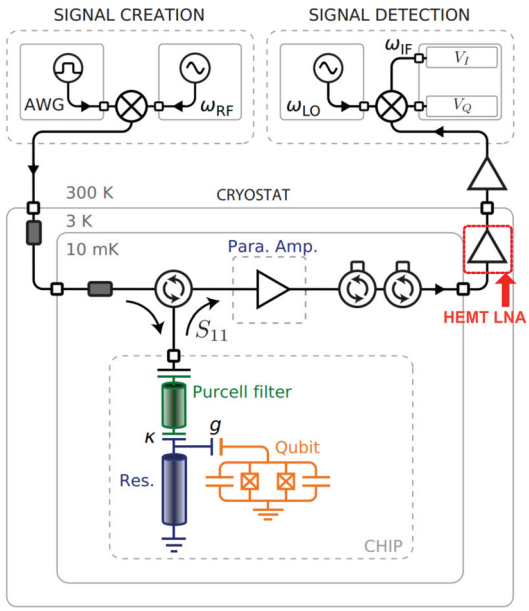

Figure 1.1: Simplified schematic of a representative experimental setup used for dispersive qubit readout. This figure is modified from [5].

$\leq$2 K noise temperature for the HEMT LNA is needed to sustain low enough noise for the readout chain [3]. The HEMT LNA can be also used as the first stage amplification for qubits readout in fast multiplexing architecture [6].

Even though superconducting quantum computers today with fewer than 1000 qubits [7] already demonstrated supremacy in certain areas [8], a full error correction that would unlock the complete power of quantum computing requires scaling up the qubit amount to approximately one million [9]. Due to the limited cooling power of the dilution refrigerator that sustains the superconducting environment, such a massive increase of qubits poses a significant demand to improve the power consumption of HEMT LNAs. Therefore, achieving high-quality qubit readout in large quantities requires the development of cryogenic HEMT LNAs that dissipate 10-100 times less dc power than currently available solutions while still maintaining sufficient gain and noise performance required in quantum systems [10].

1.2 Cryogenic LNAs

The HEMT LNAs used for qubit readout are direct descendants of cryogenic LNAs developed for radio astronomy. Since the first cryogenic LNA was realized by Dr. Sander Weinreb based on GaAs metal–semiconductor field-effect transistor (MESFET) in 1980 [11], the FET-based cryogenic LNA was quickly adopted to replace the parametric amplifiers used in radio astronomy front end for better gain, linearity, bandwidth, and stability [2]. After Mimura's HEMT invention [12], the GaAs HEMT was first employed for cryogenic LNA in radioastronomy and satellite communication, owing to the significant noise reduction provided by HEMT's two-dimensional electron gas (2DEG) [13]. Today, the InP HEMT LNA maintains leadership in noise performance, showcasing a three-stage cascaded LNA with 1.2 K average noise temperature at 5 GHz with 4.2 mW dc power dissipation, which is only 5 times the quantum-noise limit [14].

Studies have been carried out to improve the noise performance of InP HEMTs under low-power bias. By the investigation of InP HEMT channel contents, a 2.9 K average noise temperature has been achieved by a cryogenic 4-8 GHz LNA employing 65 % indium channel InP HEMT with 300 μW power consumption at 5 K [15], [16]. In another study, the spacer thickness of the InP HEMT epi-structure was optimized to produce a 4-8 GHz cryogenic LNA with 1.4 K average noise with 6.1 mW power consumption [17].

The standard InP HEMT technology has been challenged by SiGe heterojunction bipolar transistors (HBT) for its potential to be integrated with complementary metal-oxide semiconductor (CMOS) processes and high gain [3], [18]. By investigating the model behavior of SiGe HBT under ultra-low power bias, a 1.8-3.6 GHz cryogenic amplifier based on a commercial foundry process (BiCMOS8HP) demonstrated 5 K average noise temperature at 290 μW dc power consumption [19]. Furthermore, the cryogenic noise performance of SiGe HBTs was optimized by altering the Ge doping profile to reach lower noise and better matching quality that produced a 4-8 GHz cryogenic LNA with 3.2 K average noise temperature at 1 mW power consumption [20]. Recently, a reconfigurable SiGe HBTs cryogenic LNA has been reported to achieve 4.3 K average noise from 3 to 6 GHz with a tunable bandwidth and 1.8 mW dc power consumption [21]. Despite the significant performance improvements, the SiGe HBT cryogenic LNAs do not surpass InP HEMT technology in terms of noise and low-power performance, in part limited by the generation of shot

noise in the reverse-biased base-collector junction of the HBT.

As an alternative to semiconductor-based cryogenic LNAs for qubit readout, a TWPA was recently proposed to be operated at 4 K [22]. The TWPA demonstrated 1.9 K average noise temperate from 3.5 to 5.5 GHz with 100 μW power consumption. However, due to limited dynamic range, low gain, and high cost of the TWPA, the InP HEMT cryogenic LNA is still the preferred choice for qubit readout at 4 K.

1.3 Thesis scope and outline

As mentioned above, future massive up-scaling in quantum computing calls for HEMT LNAs at 4 K with much less dc power than today and still with excellent noise performance. When operating with power levels much below 1 mW, semiconductor-based cryogenic LNAs with a noise temperature below 2.0 K for qubit readout is yet to be realized. This thesis claims that extremely low-power HEMT LNAs can be engineered with much smaller dc power consumption than found in today's quantum readout circuits. The trade-off between noise performance, bandwidth, and power consumption in the InP HEMT has been tailored to meet the superconducting qubit readout requirements.

In Chapter 2 of the thesis, a small-signal noise model of InP HEMT down to 1 μW is outlined to determine the best bias strategy for noise and performance trade-off in cryogenic LNA design [Paper A and B]. A two-bias strategy is described for noise extraction at low power. In Chapter 3, the requirements for qubit readout application with respect to the cryogenic HEMT LNAs are discussed and analyzed with the extracted model from Chapter 2 [Paper B]. Futhermore, Chapter 3 presents the design, fabrication, and measurement of a new state-of-art cryogenic HEMT LNA for qubit readout [Paper B]. In Chapter 4, an epitaxially optimized InP HEMT in the LNA is tested. It is found that the optimized HEMT has a large influence on the cryogenic HEMT LNA low-power performance [Paper C]. Finally, the results from this licenciate thesis are concluded in Chapter 5. Future research work to advance HEMT LNAs in superconducting quantum computing is proposed.

CHAPTER 2

Characterization and modeling of low-power HEMT for LNAs in quantum computing

Accurate modeling of small-signal and noise characteristics is crucial for designing RF circuits at low-power conditions. For cryogenic LNA design, the model extraction relies on experimental data measured at 4 K, which is often unavailable for transistor models. Scalable small-signal noise models at cryogenic temperature have been developed for the InP HEMT down to 5 mW/mm [23], [24]. However, this level is not sufficient for designing cryogenic LNA with a total dc power consumption much less than 1 mW.

To fully utilize the RF and noise performance of the transistor in a cryogenic LNA designed for very low power, this chapter presents an investigation of a cryogenic model for InP HEMTs down to 1 μW. The developed cryogenic small-signal noise model paves the way for the realization of LNAs requested for future large-scale quantum computing systems.

2.1 InP HEMT technology

The transistor used for the model extraction and circuit design was a 100-nm gate-length and 4×50 μm gate-width InP HEMT [25]. This transistor size is well-known to yield sufficient dc and RF device performance for cryogenic LNA designs in today's qubit readout circuits [26]. The epitaxial layer structure from top to bottom was 20 nm InGaAs cap followed by 3 nm InP etch stopper, 8 nm InAlAs barrier, silicon δ-doping (5×10^{12} cm^{-2}), 3 nm InAlAs spacer, 15 nm InGaAs channel with 65% indium content and 500 nm InAlAs buffer layer. The channel electron mobility and sheet carrier concentration was 12000 cm^2/Vs and 3.6×10^{12} cm^{-2}, respectively.

The dc characterization was performed at 4 K environment in a Lakeshore model CRX-4K cryogenic probe station. In Fig. 2.1 (a), the drain current I_d versus drain-source voltage V_{ds} showed a peak drain current of 900 mA/mm at $V_{ds} = 0.5$ V with an on-resistance R_{on} of 0.33 Ω·mm. The transfer characteristic of the InP HEMT is plotted in Fig. 2.1 (b). The threshold gate-source voltage V_{gs} for the device was -0.25 V and the maximum extrinsic transconductance $g_{m,o}$ reached 1.8 S/mm at $V_{ds} = 0.7$ V.

The magnitude of gate current I_g presented in Fig. 2.1 (c) was in the order of 0.1 μA/mm for V_{ds} up to 0.7 V, indicating satisfactory control of the gate leakage path [25], [27]. An elevated level of the I_g will negatively influence the final LNA noise performance [28].

The minimum noise temperature T_{min} of the HEMT is well-known to appear at the bias for minimum $\sqrt{I_d}/g_{m,o}$ [27], plotted in Fig. 2.1 (d). A smaller value of $\sqrt{I_d}/g_{m,o}$ means that at a lower drain current, the transistor provides higher transconductance. Thus, a lower $\sqrt{I_d}/g_{m,o}$ leads potentially to better noise performance at low-power bias, as discussed in [15]. The minimum $\sqrt{I_d}/g_{m,o}$ value 0.22 $\sqrt{\mathrm{V \cdot mm/S}}$ is observed at $I_d = 16$ mA/mm. This $\sqrt{I_d}/g_{m,o}$ performance is comparable to the state-of-the-art InP HEMT specifically optimized for low-power operation (0.21 $\sqrt{\mathrm{V \cdot mm/S}}$ at 10 mA/mm) [16].

The lower the subthreshold swing (SS), the higher $g_{m,o}/I_d$ the HEMT can achieve. Hence, the SS can determine the potential noise performance at low power consumption bias [29]. The SS of the InP HEMT characterized is plotted in Fig. 2.1 (e), from which 18 mV/dec SS can be observed nearly independent from V_{ds}. For comparison, state-of-the-art InP HEMT is 14 mV/dec at 5 K [15] and the lowest experimental values of FETs reported is 11 mV/dec at 4.2 K [30]. The data in Fig. 2.1 (d) and Fig. 2.1 (e) therefore suggest the

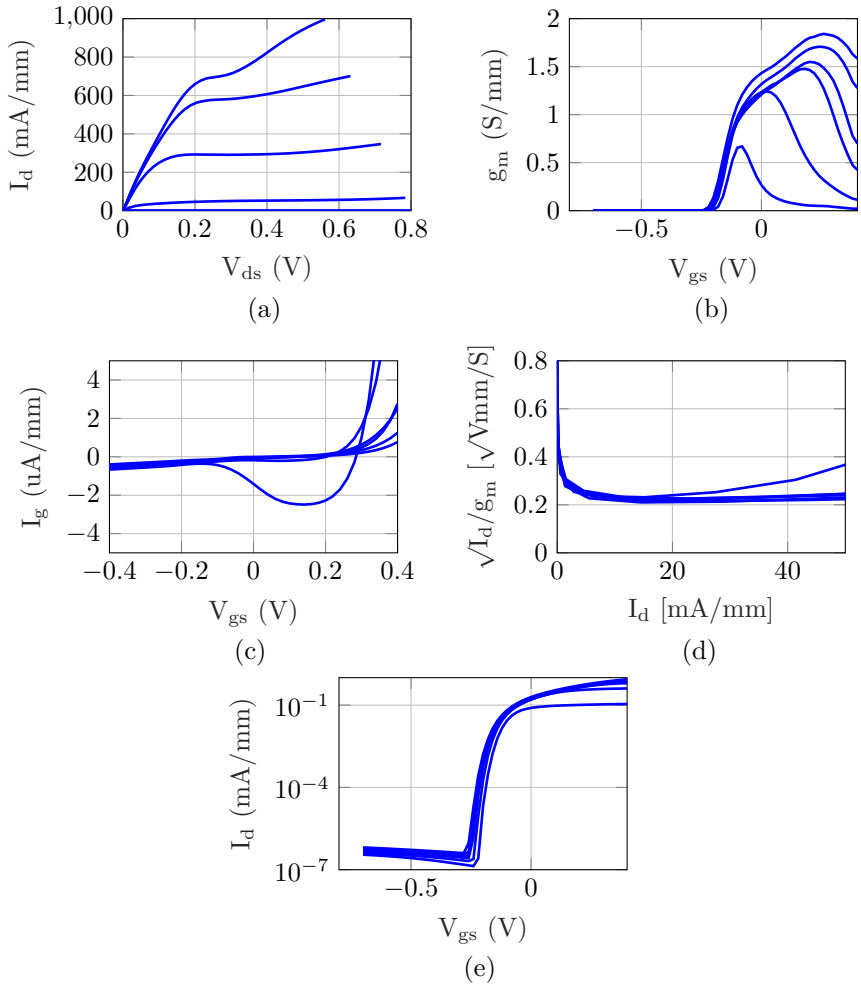

Figure 2.1: DC characterisation at 4 K of 4×50 μm InP HEMTs used in circuit design. (a) I_d versus V_{ds} where V_{gs} is from -0.5 V to 0.5 V in steps of 0.2 V. V_{ds} is from 0.05 to 0.8 V in steps of 0.15 V for (b) $g_{m,o}$ versus V_{gs}; (c) I_g versus V_{gs}; (d) the $\sqrt{I_d}/g_m$ versus I_d; and (e) SS plot where I_d versus V_{gs} plot in log scale. [From Paper B]

potential of the InP HEMTs to be used for low-power cryogenic LNA circuit application.

2.2 Cryogenic small-signal noise model at low power

In superconducting quantum computing that demand low power consumption for large-scale systems, a comprehensive understanding of the HEMT model used in LNA design for qubit readout is crucial. This knowledge enables trade-offs in circuit design to meet the qubit readout requirements at low power. In this licentiate thesis, the small-signal noise model used to simulate the HEMT was based on Pospieszalski's noise model [28]. This model assigns the fitting parameters equivalent drain temperature T_d and gate temperature T_g to resistance and conductance, respectively, in a equivalent circuit model of the HEMT; See Fig 2.2. The small-signal noise model in this thesis adapted a mature small-signal equivalent circuit model for the HEMT, both at room temperature and cryogenic ambient studied in this work [31]. The parameters of this small-signal equivalent models were extracted from the S-parameters measured of the HEMT at targeted low-power biases at 4 K ambient temperature.

In Pospieszalski's noise model, T_g is set to be close to the ambient temperature. In contrast, T_d, which accounts for the hot electrons in the channel, is usually much higher than the ambient temperature.

Using Pospieszalski's noise model, the minimum noise temperature T_{min} that can be achieved by the HEMT under a certain bias is expressed by

$$T_{min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g g_{ds} T_d} \tag{2.1}$$

where R_t is the sum of the gate resistance R_g, the intrinsic gate-source resistance R_i and the source resistance R_s. g_{ds} denotes the intrinsic output conductance of the applied drain voltage. The intrinsic cut-off frequency f_T is described by [32]

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd}) \cdot (1 + \frac{R_s + R_d}{R_{ds}}) + g_m C_{gd}(R_s + R_d)} \tag{2.2}$$

where C_{gs} and C_{gd} are the intrinsic gate-source and gate-drain capacitance,

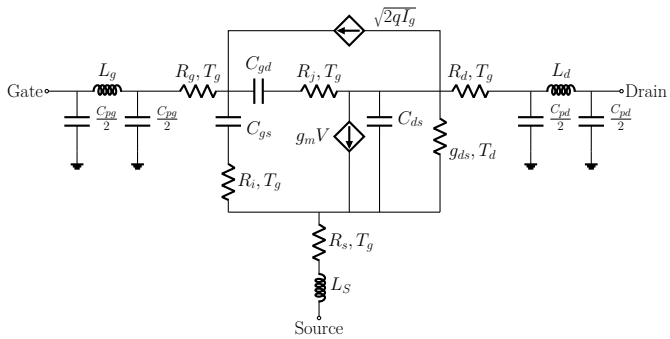

Figure 2.2: Equivalent small-signal and noise model of the InP HEMT. [From Paper B]

respectively, R_d is the drain resistance, and R_{ds} is the inverse of g_{ds}. g_m is the intrinsic transconductance.

The T_{min} are thus bias-dependent and have a close relationship with the extracted small-signal equivalent circuit parameters.

HEMT small-signal model parameters at low power

In this thesis, on-wafer measurements of the InP HEMT's S-parameters at 4 K were recorded using a Rohde Schwarz ZVA67 vector network analyzer with a maximum frequency range of 67 GHz. The InP HEMTs, same as described in Sec. 2.1, were tested at different V_{ds} and I_d levels, with dc power varying from 1 μW to 600 μW. Given that the magnitude of I_g was only a few tens of nA, the contribution of the gate current to the overall dc power consumption was considered negligible.

Fig. 2.3 depicts the comparison between the measured and simulated S-parameters of the InP HEMT at 4 K for dc power of 1, 40, and 600 μW, up to 40 GHz. The simulated data was generated using the extracted small-signal parameters. A good agreement is observed between the measured and simulated S-parameters for all dc power levels. This confirms the accuracy and effectiveness of the extracted small-signal model over a wide range of dc bias powers.

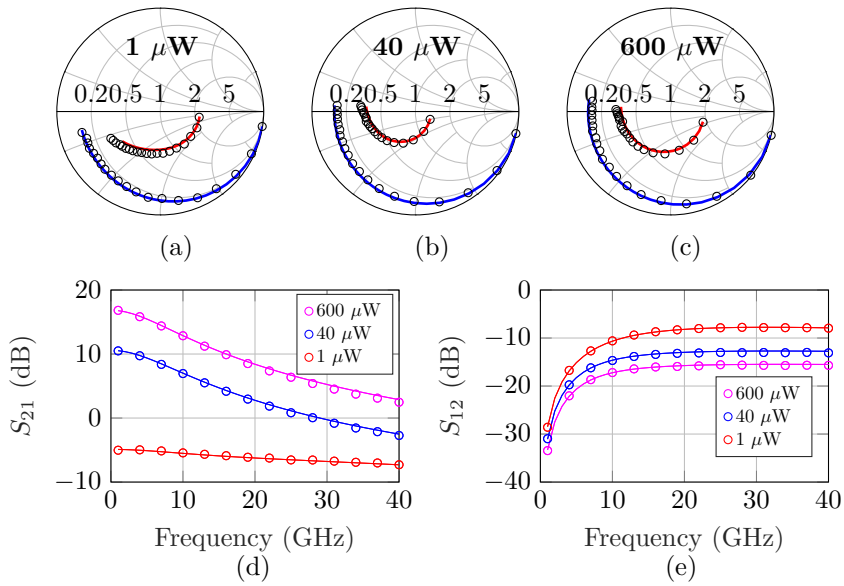

Figure 2.3: Comparison of measured (circles) and simulated (solid) S-parameters from 0.01 to 40 GHz of a 4×50 μm gate width and 100 nm gate-length InP HEMT at 4 K for different ULP levels. S_{11} (red line) and S_{22} (blue line) plotted in Smith chart with bias power at (a) 1 μW (V_{ds} = 0.01 V, I_d = 0.1 mA) (b) 40 μW (V_{ds} = 0.04 V, I_d = 1 mA), and (c) 600 μW (V_{ds} = 0.3 V, I_d = 2 mA). (d) S_{21} and (e) S_{12} for 600, 40, and 1 μW. [From Paper B]

Fig 2.4 presents extracted g_m, C_{gs}, C_{gd}, and g_{ds} versus V_{ds} for different I_d at 6 GHz. As illustrated in Fig 2.4 (a), the dependence of g_m on I_d is strong, with a roll-off starting at V_{ds} of 0.05 V. The mean g_m values prior to roll-off are 50, 75, 160, 330, and 530 mS/mm for I_d of 0.1, 0.15, 0.4, 1, and 2 mA, respectively, indicating a nearly linear relationship with I_d. This roll-off intensifies for current biases exceeding 0.4 mA. When sweeping the V_{ds} from saturation to the triode region (0.3 V to 0.01 V) while keeping I_d fixed, g_m initially remains constant due to increased V_{gs} compensating for the reduced influence of V_{ds}. However, upon reaching low V_{ds} values, it is evident that the insufficient number of channel carriers for effective V_{gs} modulation results in a decrease in g_m.

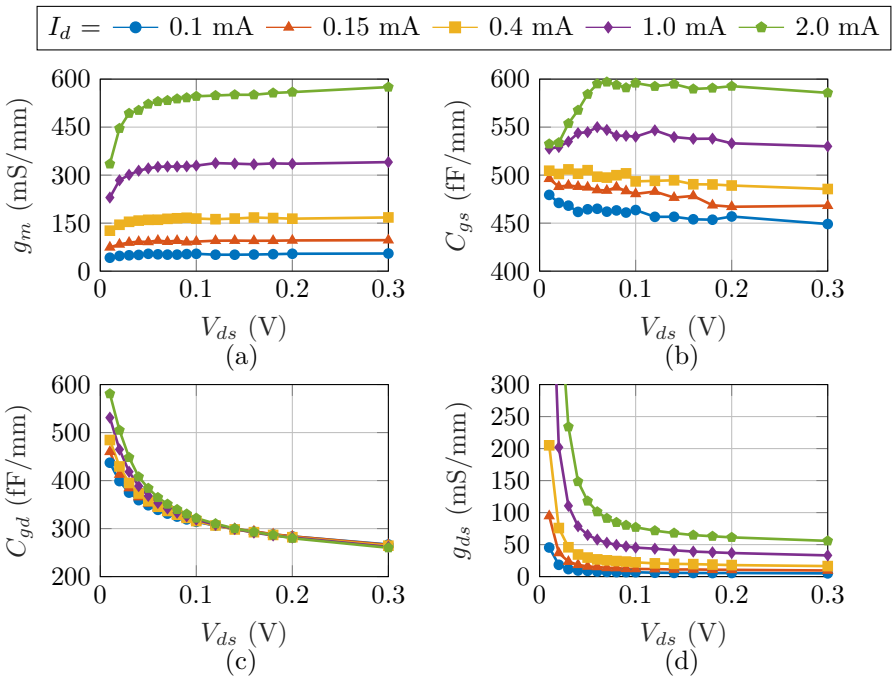

Figure 2.4: Extracted (a) intrinsic g_m, (b) C_{gs}, (c) C_{gd}, (d) g_{ds} as a function of Vds at 6 GHz of a 4×50 μm gate width and 100 nm gate-length InP HEMT at 4 K with I_d bias from 2 mA down to 0.1 mA. [From Paper B]

The C_{gs} behavior in Figs 2.4 (b) exhibits a similar pattern to the g_m for I_d values of 1 mA or higher. For I_d values of 0.4 mA or lower, C_{gs} undergoes a minor increase as V_{ds} decreases. This can be explained by the interplay between the overlapping effect of V_{ds} and V_{gs} on C_{gs} at a constant I_d. When V_{ds} was lowered, an increased V_{gs} needed to sustain the fixed I_d enhanced the channel's carrier concentration and slightly raised C_{gs}. On the other hand, a reduction in V_{ds} resulted in a more uniform 2DEG carrier distribution, decreasing the carrier density at the source side and subsequently lowering C_{gs}. At high current bias (and high V_{gs}), the channel carrier concentration reaches saturation, causing the influence of low V_{ds} to become dominant, leading to

a decrease in C_{gs}. Conversely, at low drain current where V_{gs} is low and the channel is not fully open, it is expected that the increase in V_{gs} at lower V_{ds} will outweigh the decrease in V_{ds}, resulting in an increase in C_{gs}.

C_{gd} in Figs 2.4 (c) displays no substantial I_d dependency for V_{ds} greater than 0.1 V. However, when V_{ds} is below this bias, C_{gd} escalates 2 to 6 times more swiftly, depending on I_d. The C_{gd} increase can be attributed to the reduction of the depletion region of the 2DEG at the drain side.

The extracted g_{ds} values exhibit an increase with higher I_d, as plotted in Figure 2.4 (d). When V_{ds} enters triode region (0.03 to 0.07 V), the HEMT channel behaves as a voltage-controlled resistor and small fluctuations in V_{ds} result in significant current variations. This phenomenon explains the observed increase in g_{ds}.

The extracted small-signal model parameters reveal evident trends when the InP HEMT is biased at low power. All parameters exhibit relatively weak responses to a decrease in V_{ds} until reaching a value of around 0.05 V for the measured InP HEMT. This observation suggests that the InP HEMT can preserve its microwave performance even at exceptionally low power in cryogenic conditions, a characteristic desired for large-scale qubit readout. Slightly below $V_{ds} = 0.05$ V, g_m drops sharply, accompanied by a rise in g_{ds} and the overall intrinsic capacitance. Based on Eqs. (2.1) and (2.2), a rapid deterioration in f_T and T_{min} is anticipated.

HEMT noise model and extraction at low power

In Pospieszalski's model, all noise parameters and associated gain of the transistor are based on small-signal equivalent circuit model parameters, T_g, and T_d. Gate leakage noise is modeled as a shot noise source, as depicted in Fig.2.2, with noise current $\sqrt{2 \cdot q \cdot I_g}$. The I_g values are measured during the S-parameter measurements at each bias point. For the targeted second stage amplification of qubit readout at 4 K, T_g is set to 10 K to account for potential self-heating in the device [27], [33]–[35]. With the extracted small-signal equivalent circuit model parameters of the InP HEMT under different biases, T_d can be extracted by fitting the simulated noise of the HEMT model to the measured noise results.

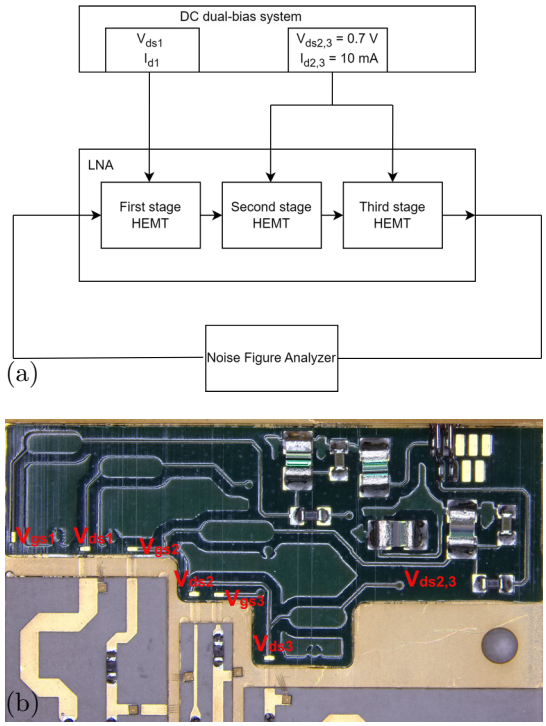

Figure 2.5: (a) Schematic of the dual-bias noise extraction method [From Paper B]. I_{d1} and $I_{d2,3}$ are adjusted by gate voltage of each stage: V_{gs1}, V_{gs2}, and V_{gs3}, which are denoted in (b) top view of the fabricated dc bias printed circuit board (PCB) circuit.

Dual-bias strategy for low power noise model extraction

Due to insufficient gain and low noise signal levels, on-wafer noise measurements for HEMTs at cryogenic temperatures suffer from low accuracy. Thus, an indirect noise parameters extraction method using a hybrid amplifier equipped with the HEMTs was adapted [14], [36]. The InP HEMTs were mounted in a three-stage 4-8 GHz LNA with the same gate and drain bias for all stages for noise measurement and T_d fitting. Such a procedure results in much higher signal-to-noise ratio as required by the noise figure analyzer (NFA). In this work where the low-power regime was of particular interest, the hybrid LNA

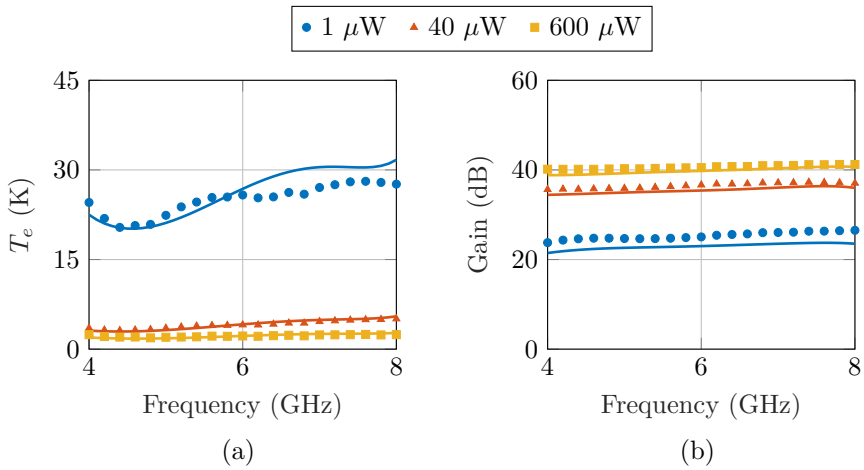

Figure 2.6: Comparison of measured (symbols) and modeled (solid lines) (a) noise and (b) gain of the 4-8 GHz LNA used for T_d extraction at 4 K for the first stage HEMT biased at 1 μW (V_{ds1} = 0.01 V, I_{d1} = 0.1 mA), 40 μW (V_{ds1} = 0.04 V, I_{d1} = 1 mA), and 600 μW (V_{ds1} = 0.3 V, I_{d1} = 2 mA). The second and third HEMT stages were biased with $V_{ds2,3}$ = 0.7 V, $I_{d2,3}$ = 10 mA; See Fig. 2.5.

method still suffered from insufficient gain for accurate T_d extraction. This was solved by replacing the common bias for the HEMTs in the LNA with a dual-bias design. In this way, gain for the LNA could be preserved also at very low dc power in the HEMT down to 1 μW. The dual-bias circuit was implemented in the LNA to supply V_{gs} and V_{ds} independently for the first stage, as well as the second and third stages, respectively. See Fig 2.5. The first-stage InP HEMT was biased as in the S-parameter measurement. In contrast, the second and third InP HEMTs were biased at previously extracted and modeled bias point for high gain and low noise (V_{ds} = 0.475 V and I_d = 5 mA). Fig 2.6 shows the noise and gain measurements and simulations of the LNA over the frequency range of 4 to 8 GHz at three bias powers (1 μW, 40 μW, and 600 μW) for the first stage InP HEMT. The LNA with the dual-bias solution can sustain more than 20 dB gain when the first stage InP HEMT is biased at 1 μW. The measured equivalent noise T_e at 1 μW is around 20 K. The agreement between simulated and measured data for both gain and noise

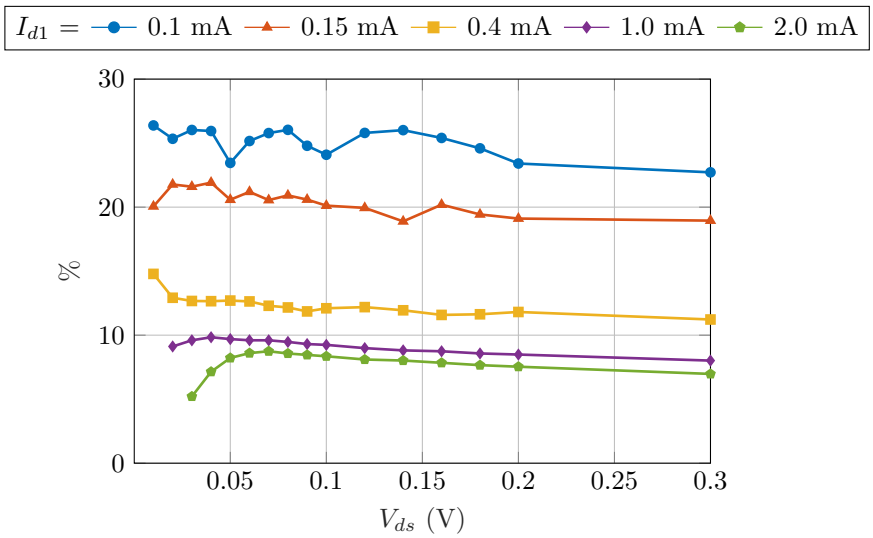

Figure 2.7: Simulated percentage of second and third-stage noise contribution to the total LNA noise versus first stage InP HEMT V_{ds} for different I_{d1}.

is excellent for 40 and 600 μW bias. The agreement is slightly worse for 1 μW bias, which can be attributed to measurement uncertainty due to lower gain and non-uniformity between HEMTs especially at low power.

For a meaningful low-power T_d extraction, the measured total noise should be highly correlated with the noise contribution from the first stage transistor. By setting T_d, T_g and ambient temperature T_a of the first stage HEMT and input matching network to zero in the simulator (AWR Microwave Office), the contribution of the subsequent stages can be obtained. The simulated equivalent noise T_e percentage of the second and third stages to the overall T_e of the LNA at 6 GHz are plotted versus V_{ds} of the first stage InP HEMT for different I_{d1} in Fig 2.7. Despite the increasing noise contribution for lower first stage I_{d1}, the first stage InP HEMT still contributes more than 70% noise temperature even at $I_{d1} = 0.1$ mA. As a result, the indirect procedure for measuring noise of the first InP HEMT in a three-stage LNA can be used with sufficient gain and hence noise accuracy even when biasing this first stage at a dc power of only 1 μW (first stage InP HEMT $V_{ds} = 0.01$ V).

HEMT noise model parameters at low power

The extracted T_d, noise parameters, and associated gain of the InP HEMT at 6 GHz are presented versus V_{ds} for different I_d under a 4 K ambient temperature in Fig. 2.8.

In Fig. 2.8 (a), the extracted T_d values are shown. A decrease in I_d results in a proportional reduction in T_d, confirming the widely accepted observation [37] that T_d exhibits a nearly linear relationship with I_d. From a device physics perspective, T_d represents the amount of fluctuations among channel electrons [38]. It is expected that electron scattering diminishes with reduced dc power in the channel, which explains the decline in T_d with lower V_{ds} bias.

Using Eq. (2.1), T_{min} was calculated from the extracted T_d and small-signal model parameters. In Fig. 2.8 (b), T_{min} of the InP HEMT is depicted. As I_d increases, T_{min} improves and saturates beyond 1 mA. When V_{ds} is above 0.05 V, T_{min} stays constant or even slightly decreases with a lower V_{ds}. According to Eqs. (2.1) and (2.2), the increase in T_{min} below the critical V_{ds} around 0.05 V is primarily due to the deterioration of the small-signal model parameters, as T_d is a monotonically decreasing function for I_d below 2.0 mA. Consequently, the small-signal behavior in Fig. 2.4 serves as a useful indicator for T_{min} performance, in particular under low-power conditions. The observed slightly decrease in T_{min} with lower V_{ds} before 0.05 V is mainly due to the fact that the positive impact of the reduced T_d outweighs the negative impact of the degradation in small-signal model parameters.

From Fig. 2.8 (b), the optimal bias point for achieving the lowest T_{min} with minimal dc bias power can be determined for the InP HEMT at 4 K. In a single-stage analysis of HEMT LNA design, the overall noise performance must take other noise parameters into account in relation to impedance matching:

$$T_e = T_{min} + T_0 \frac{R_n}{\Re Z_{opt}} |Z_s - Z_{opt}|^2 \tag{2.3}$$

where T_0 is the reference temperature (290 K), R_n is the noise resistance, Z_s is the source impedance, and Z_{opt} is the optimal impedance for noise matching. To achieve the minimum T_e across the entire bandwidth of the cryogenic LNA, the impact of R_n and Z_{opt} is crucial.

In a multi-stage HEMT LNA, the associated gain G_{assoc} for each stage must be considered [39]. The parameter N is introduced as an invariant to account for the combined effect of R_n and $\Re(Z_{opt})$, as defined in [40]:

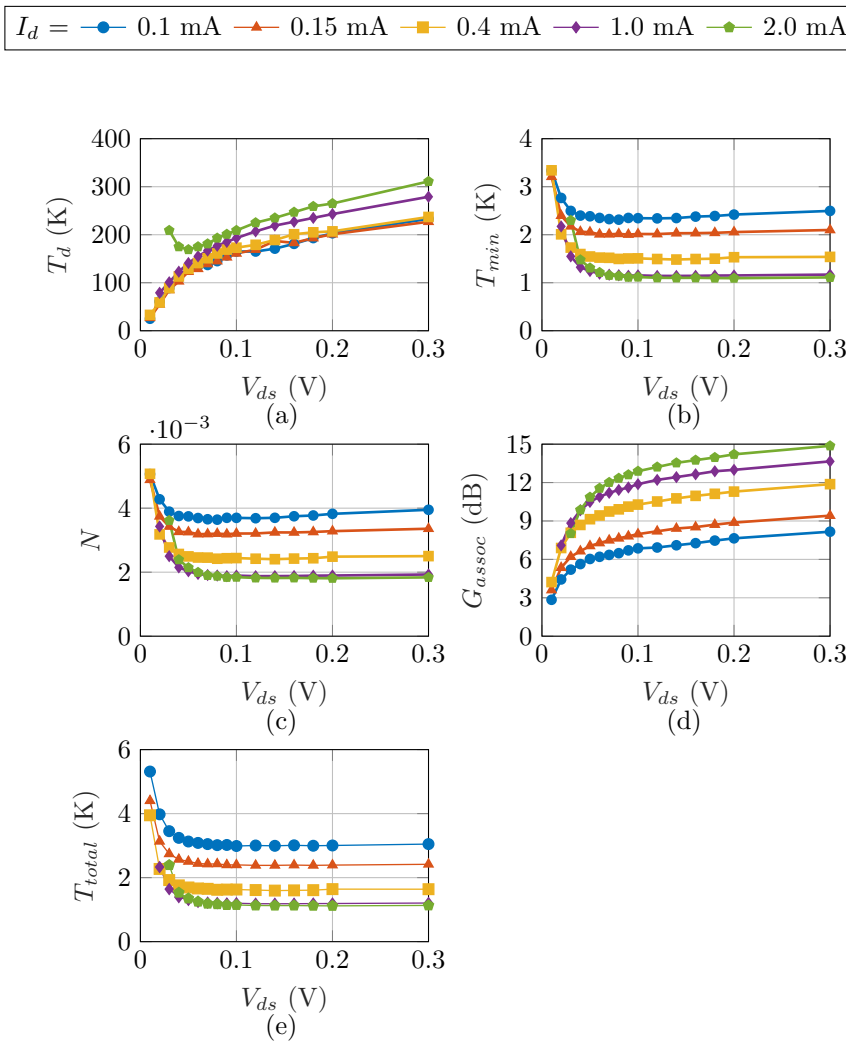

Figure 2.8: Extracted (a) T_d, (b) T_{min}, (c) N, (d) G_{assoc}, and (e) T_{total} as a function of V_{ds} at 6 GHz for a 4×50 μm gate width and 100 nm gate-length InP HEMTs at 4 K with I_d biased from 2 mA down to 0.1 mA.

$$N = \frac{R_n}{\Re(Z_{opt})} \tag{2.4}$$

At frequencies much lower than f_T, N is proportional to T_{min} [28]. This is confirmed in Fig. 2.8 (c) where N displays the same trend as T_{min} in Fig. 2.8 (b). Below $V_{ds} = 0.05$ V, N rapidly increases for all I_d values, causing the InP HEMT to become more sensitive to noise mismatch.

As depicted in Fig. 2.8 (d), the G_{assoc} declines for lower I_d values. Similar to other noise parameters, G_{assoc} decreases gradually with reduced V_{ds} and drops off sharply when reaching the critical point at $V_{ds} = 0.05$ V. It is noteworthy that at a dc power of only 40 μW ($V_{ds} = 0.04$ V; $I_d = 1$ mA), the InP HEMT still maintains a G_{assoc} of 10 dB at 6 GHz.

To study the influence of G_{assoc} in the cascade noise analysis, a modified noise measure M_{opt} is introduced. Compared to the original definition of noise measure [41], available gain and T_n is replaced by G_{assoc} and T_{min}:

$$M_{opt} = \frac{T_{min}}{T_0} \frac{1}{1 - \frac{1}{G_{assoc}}} \tag{2.5}$$

The total noise temperature (T_{total}) of an infinite number of cascade stages is

$$T_{total} = T_0 \cdot M_{opt} \tag{2.6}$$

The T_{total} is plotted in Fig. 2.8 (e), which exhibits a pattern similar to that of T_{min}. However, the critical V_{ds}, where performance degrades, slightly increases from 0.05 to 0.07 V. This is due to the rapid decrease of G_{assoc} with V_{ds} compared to T_{min}. The T_{total} constitutes a more stringent condition compared to T_{min} for choosing the first stage HEMT minimum bias. The projected Z_{opt} in the Smith chart in Fig. 2.9 shows that the lower the bias power, the further away Z_{opt} is from the origin of the Smith chart, emphasizing the challenge in impedance matching between noise and bandwidth at low power.

In summary, a cryogenic small-signal noise model for the InP HEMT reaching a dc power of 1 μW was presented. It was found that noise parameters and G_{assoc} were strongly influenced by I_d. The impact of V_{ds} on noise parameters is relatively insignificant above $V_{ds} = 0.05$ V. Below this, noise performance and G_{assoc} rapidly deteriorate. Thus, maintaining V_{ds} above this level can help prevent noise degradation, serving as a key guideline for optimizing low power in cryogenic HEMT LNA design. The behavior observed in the InP

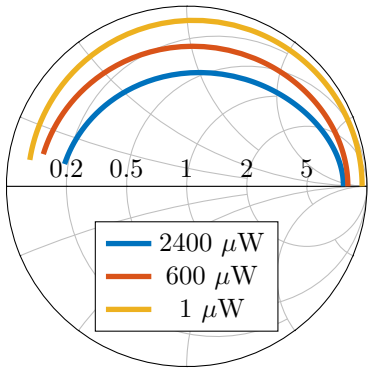

Figure 2.9: The extracted Z_{opt} at 4 K of a 4×50 μm gate width and 100 nm gate-length InP HEMT with bias power of 2.4 mW (V_{ds} = 0.475 V, I_d = 5 mA), 600 μW (V_{ds} = 0.3 V, I_d = 2 mA), and 1 μW (V_{ds} = 0.01 V, I_d = 0.1 mA) at 4 K in the Smith chart. The data is plotted up to 40 GHz

HEMT small-signal noise model under cryogenic conditions at low power indicates the feasibility of attaining low noise levels while also maintaining a reduced dc bias power. However, potential challenges related to wide-band matching and gain could arise. The next chapter will address these issues by detailing the analysis and implementation of a low-power LNA specifically tailored for qubit readout applications, based on the investigated small-signal noise model presented in this chapter.

CHAPTER 3

Low-power HEMT LNA design for qubit readout

Utilizing the extracted cryogenic ULP small-signal noise model of the InP HEMT in Chapter 2, low-power optimization of the HEMT LNA for qubit readout becomes possible. This implies a trade-off between noise and low-power performance for the HEMT LNA. The analysis in Chapter 2 tells us that low-power design also means a decrease in G_{assoc} and poor matching conditions for the HEMT. Finally, the low-power optimization must meet the system requirements in qubit amplification with respect to gain, bandwidth, and linearity.

In this chapter, the design objectives of the low-power HEMT LNA for qubit readout will be analyzed, taking into account the quantum system constraints. The HEMT small-signal noise model developed in Chapter 2 will be applied in the design of a tailored hybrid LNA to achieve the optimal balance between noise performance and power consumption. A suspended transmission line structure in the designed LNA is implemented in a cryogenic vacuum environment to meet the high impedance requirement for noise matching. The measured results of the LNA will be compared with electromagnetic (EM) and circuit schematic co-simulation results. The realized LNA at low power shows state-of-the-art noise performance making it interesting for qubit readout in

future quantum computing.

3.1 Design analysis for qubit readout

In Chapter 1, the HEMT LNA in a qubit experimental setup was described. The HEMT LNA is located as the second amplifier after the parametric amplifier at the 4 K stage which provides 1 to 1.5 W cooling capacity. Several isolators are put in between the parametric amplifier and HEMT LNA to prevent noise from the HEMT LNA's input from reaching the fragile qubits [2], [4], [10]. In some experiments, the HEMT LNA is employed as first stage amplifier at 4 K, i.e without parametric amplifier, to amplify the qubit resonator with sufficient readout fidelity [6].

In qubit readout systems, present (commercial) HEMT LNAs are normally optimized for minimum noise, with a typical T_e ranging between 1.5 and 2 K and a gain of around 40 dB [3]. The HEMT LNA has a bandwidth of 4-8 GHz and consumes dc power on the order of 5-10 mW [1], [26].

Amplifier linearity is an essential design parameter since each LNA handles simultaneous qubit readout. The line-width and frequency separation between each readout signal can be designed to be below 11 MHz and 160 MHz, respectively [42]. In an ideal scenario, the available frequency band should be fully utilized for qubit readout signal separated with the smallest possible frequency distancing. Assuming each qubit occupies a 2 MHz bandwidth, the ideal capacity for a 4-8 GHz cryogenic LNA is 2000 qubits. Utilizing the full 4 GHz bandwidth for qubit readout increases the input linearity requirement by +33 dB compared to an LNA used for single qubit readout. If the preceding stage parametric amplifier achieves an output 1 dB compression point P1dB of around -90 dBm [43], the input P1dB for the HEMT LNA should be at least higher than -57 dBm. In reality, the qubit handling capability across a given bandwidth in the HEMT LNA is considerably smaller, due to many practical limitations.

In superconducting quantum computing, the readout process is designed not to directly interact with the qubit, but instead to probe using a superconducting resonator. This is called dispersive readout. This allows the readout system to acquire information about the state of the qubit while effectively minimizing unwanted "back-action" effects on the qubit [5]. Top part of Fig. 3.1 shows the equivalent circuit representation of a dispersive read-

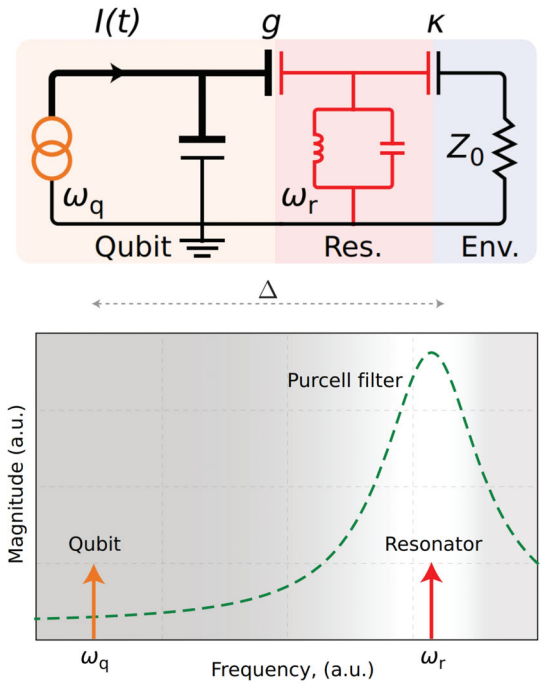

Figure 3.1: Top: circuit representation of qubit (ω_q) coupling to environment load with a readout resonator (ω_r) in-between. Bottom: Transmission spectrum of the resonator frequency and qubit frequency. The purcell filter (green dashed line), enhancing fast readout and mitigating qubit decay, is not denoted in the top figure. [5]

out. A resonator is situated between the qubit and the readout environment load (50 Ω). The resonator placement serves two functions: firstly, it shields the qubit from potential decay, and secondly, it introduces a detuning that shifts the readout frequency away from the native qubit frequency ω_q. As illustrated in Fig. 3.1 bottom part, the qubit resonator readout frequency, ω_r, is distanced from ω_q by a frequency detuning Δ:

$$\omega_r = \omega_q \pm \Delta \tag{3.1}$$

Here, $\omega_r/2\pi$ and $\Delta/2\pi$ range from typically 4-8 GHz [1] and 0.5-1.5 GHz [10], respectively. ω_r can be engineered over a wide frequency range in qubit

resonator fabrication. This suggests that the 4-8 GHz working bandwidth requirement for the HEMT LNA can be traded off versus other design parameters such as dc power. State-of-the-art TWPA [44] uses 3.5-5.5 GHz and JPA [45] uses 4.6-4.8 GHz for qubit readout. Provided that the low-power LNA allows for an increase in the feasible number of qubit readouts within the limited cooling power capability, the bandwidth of the LNA can therefore be reduced for lower dc power consumption. The small-signal noise model in Chapter 2 shows that such a trade-off must be carefully balanced with gain and matching when running the HEMT at low power.

To design a low-power cryogenic LNA optimized for superconducting qubit readout, the following priorities must be taken into consideration:

1. Reducing the LNA's power consumption below 1 mW [1].

2. Maintaining adequate noise performance (($\leq$ 2 K) for qubit readout.

3. Ensuring sufficient linearity ($\geq$ -60 dBm) of the LNA to support the maximum number of qubit readouts.

3.2 Design and implementation of low-power LNA for qubit readout

In this thesis, a design goal of the low-power LNA for qubit readout was to consume less than 200 μW dc power, which is much less than the current 5-10 mW used today [1]. The noise temperature of the low-power LNA was targeted to 2 K which meet the requirement for qubit readout at 4 K ambient temperature [3]. As a trade-off for the low-bias power, the targeted gain and working bandwidth were set to be above 20 dB and 4-6 GHz. This is due to the high sensitivity of the matching difficulty and associated gain of the HEMT to bias power revealed by the extracted model versus power in Chapter 2.

In this thesis, the developed HEMT LNA utilized hybrid technology for optimal noise performance. This approach allows for low-loss matching and easy prototyping, advantages that MMIC technology currently does not offer. A common-source topology was applied for low noise, high gain, high isolation, including the capability to use inductive source degeneration. From experience, a transistor size with a 4$\times$50 μm gate-width was chosen for the

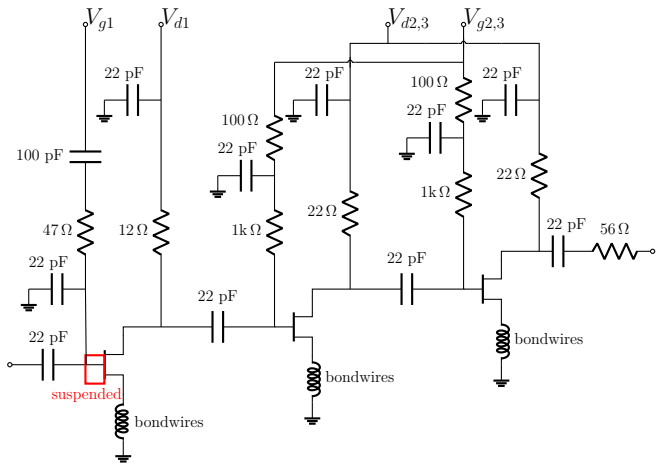

Figure 3.2: Circuit schematic of the designed 4-6 GHz cryogenic HEMT LNA. The red frame represents the suspended transmission line. [From Paper B]

InP HEMT technology, as its gate impedance is more readily matched at C band frequencies.

The simplified circuit schematic of the LNA can be seen in Fig. 3.2. Based on the cascade noise equation by Friis [39], the first-stage HEMT is anticipated to contribute the most noise, provided the first stage HEMT has adequate gain. Considering the rapid degradation of the InP HEMT's G_{assoc} (Fig.2.8 (d)) and Z_{opt} (Fig.2.9) at a reduced dc bias, it is reasonable to bias the first-stage HEMT at higher power compared to the second and third-stage HEMT. The dual-bias dc system described in Fig. 2.5 was integrated into the LNA module. To sustain a G_{assoc} higher than 10 dB, the first HEMT stage was biased with V_{d1} = 0.08 V and I_{d1} = 1.5 mA, corresponding to 90 μW (V_{ds} = 0.06 V and I_d = 1.5 mA) on the InP HEMT, with a 12 Ω stability resistor in series with the bias line. The second and third stages were biased with $V_{d2,3}$ = 0.08 V and $I_{d2,3}$ = 1 mA, respectively, with a 22 Ω stability resistor. The corresponding dc power for each InP HEMT of second and third-stages was 30 μW (V_{ds} and I_d were 0.06 V and 0.5 mA) respectively.

To reduce the noise contribution of the second and third-stage HEMTs, it was critical to match the first-stage HEMT for the lowest noise with a sufficient gain. To achieve the simultaneous matching of noise and gain for the first-stage HEMT, the inductive source degeneration technique that can alter input

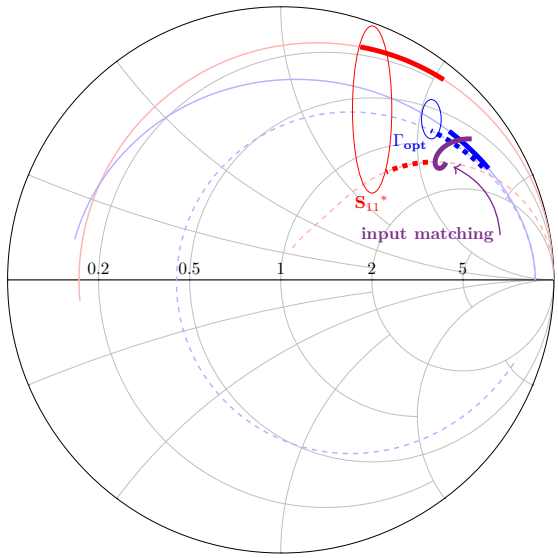

Figure 3.3: Simulated Γ_{opt} and conjugate S_{11} at 4 K of a 4×50 nm gate-length and 100 nm gate-width InP HEMT biased at $V_{ds} = 0.06$ V and $I_d = 1.5$ mA up to 40 GHz. The dashed lines represent Γ_{opt} and S_{11} for the HEMT with two 1.6 mm long bond wires connected at the source using the inductance degeneration technique. The S_{22} of the input matching circuit was plotted at the purple solid line. The targeted frequency band from 4 to 6 GHz is marked in bold line.

impedance was applied. The introduced inductance is expected not to heavily influence the Γ_{opt}. However, the inductance will negatively affect available gain. The trade-off has been optimized to achieve lowest noise and highest gain in the simulation. The inductive source degeneration for the first-stage HEMT matching was implemented by two 1.6 mm bond wires connecting the source pad to the ground plane. Fig.3.3 demonstrates the simulated input matching using the inductive source degeneration in the Smith chart. The introduced source inductance adjusted the conjugate S_{11} much closer to the middle of the Smith chart. Meanwhile, the source degeneration only slightly influenced Γ_{opt} within the targeted 4-6 GHz frequency band. As a result, this approach brought the input impedance and Γ_{opt} closer together, making it easier to achieve simultaneous matching.

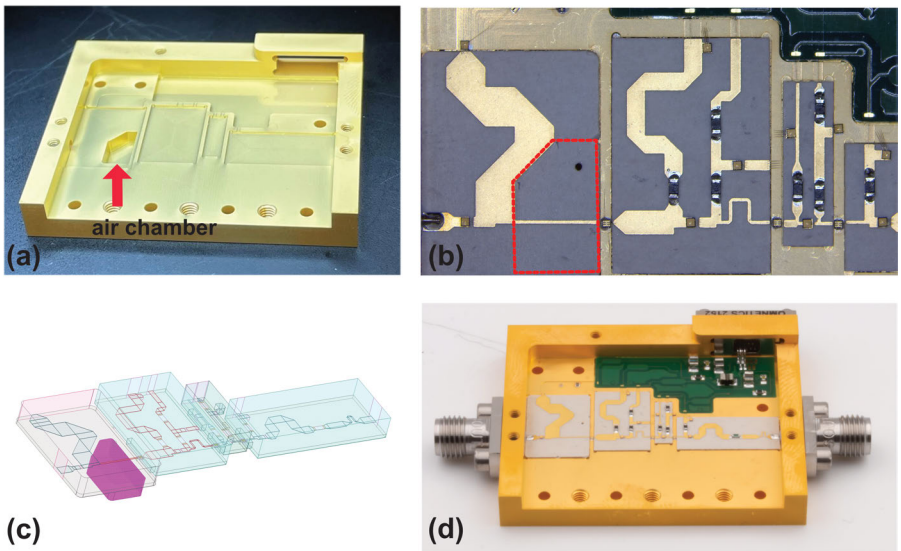

Figure 3.4: (a) The open chassis showing the air chamber for the suspended transmission line in the input matching network [From Paper A]. (b) Top view of the RF PCBs, the dashed line areas shows the suspended transmission line of the input matching network and venting aperture. (c) Ansys HFSS EM simulation model of the designed 4-6 GHz LNA. (d) The gold-plated open module with mounted RF and DC PCBs. The size of the full module is 34.9 mm × 42.5 mm × 3 mm [From Paper A].

A suspended transmission line was implemented to provide the high impedance needed for the input matching network, shown as the purple solid line in Fig. 3.3. The suspended transmission line provided 277 Ω impedance at 5.5 GHz. It was realized using a 2 mm deep air chamber beneath the substrate in the circuit package, shown as Fig 3.4 (a). Since the LNA is usually tested and used in the vacuum condition for cryogenic temperature, a venting aperture was designed to provide an airway that prevented the negative pressure to tear up the PCB above the air chamber, illustrated in Fig 3.4 (b). The structure of suspended line, venting aperture, and chassis chamber has been optimized with the EM simulation in Ansys HFSS, as shown in Fig 3.4 (c).

The second and third-stage HEMT both used four 0.2 mm source bond wires as inductive source degeneration to mitigate the matching difficulty.

The second stage HEMT is matched for higher gain compared to the first stage, and the third stage HEMT is matched solely for maximum gain. At the output matching stage, a 56 Ω series resistor was used to enhance the LNA stability. The designed LNA exhibited unconditional stability in the circuit simulation [46].

All matching PCBs used in the LNA were constructed using a 0.381 mm thick Duroid 6002 substrate with 0.0012 loss tangent and 2.94 relative permittivity. The RF circuit PCBs and dc bias PCB were fabricated and packaged in a gold-plated aluminum chassis with SMA coaxial RF connectors and connected with bond wires. Fig. 3.4 (d) shows the open chassis of the fabricated three-stage hybrid HEMT LNA.

3.3 Measurement results and discussion

The fabricated HEMT LNA circuit was characterized at 4 K for noise temperature, small-signal gain, return loss, and P1dB.

Using a Y-factor method with an in-house 20 dB cold attenuator at 4 K [47] and a 4-8 GHz LNA connected at the output to maintain a high signal-to-noise ratio for optimal measurement accuracy, the noise temperature and gain of the fabricated LNA module were measured by an Agilent N8975B noise figure analyzer. A noise measurement uncertainty of ± 0.3 K and measurement repeatability of ± 0.1 K were estimated [41].

At a total dc power of 200 μW with V_{d1} = 0.08 V and I_{d1} = 1.5 mA, and $V_{d2,3}$ = 0.08 V and $I_{d2,3}$ = 1 mA, the simulated and measured gain and noise of the fabricated cryogenic LNA at 4 K are presented in Fig. 3.5. The good agreement between the measured results and simulations validates the extracted small-signal and noise model parameters at low power. The average gain across the target frequency band is 23.1 dB. Additionally, the measured LNA's average noise temperature $T_{e,avg}$ is 2.0 K, with a minimum value of 1.7 K at 5.7 GHz. The measured 2.0 K noise temperature of the LNA reached the threshold necessary for qubit readout [3]. In some scenarios of qubit readout, LNA gain exceeding 20 dB is needed to compensate for losses from 4 K to 300 K. A higher gain can be achieved either by incorporating an additional stage in the HEMT LNA or by adding a LNA at the 77 K stage in the qubit readout chain.

Fig. 3.6 shows the dc power sweep of the fabricated cryogenic LNA, ranging

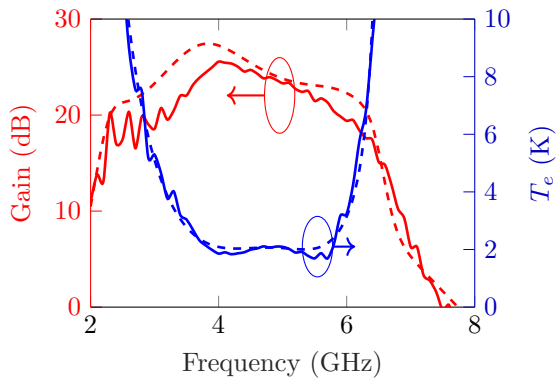

Figure 3.5: Simulated and measured gain and noise under cryogenic environment (4 K) for the designed 200 μW InP HEMT LNA (V_{d1} = 0.08 V and I_{d1} = 1.5 mA, and $V_{d2,3}$ = 0.08 V and $I_{d2,3}$ = 1 mA)). The red solid line is measured gain performance and the red dashed line is simulated gain performance. The blue solid line is the measured noise temperature and the blue dashed line is the simulated noise temperature. [From Paper B]

from 48 μW to 600 μW. The behavior of the $T_{e,avg}$ with reduced bias power is similar to that of T_{min} shown in Fig. 2.8 (d). The decrease in gain at lower power is due to the degraded G_{assoc} in the lower V_{ds} range, as illustrated in Fig. 2.8 (d). When reduced to 100 μW dc power, the LNA reaches an average gain of 22.5 dB and a $T_{e,avg}$ of 2.6 K, with a minimum value of 2.0 K at 5.7 GHz. The best noise performance occurs at 600 μW, with a $T_{e,avg}$ of 1.6 K and a minimum value of 1.4 K at 5.7 GHz, and an average gain of 33.6 dB. A higher bias power at the first stage brings the $T_{e,avg}$ closer to T_{min} for the designed bandwidth, indicating a relaxation of the trade-off between noise performance and bandwidth, which is predicted by the extracted small-signal noise model in Chapter 2.

Using a Keysight N52478 PNA-X network analyzer, the S-parameters and P1dB were measured at 4 K. The measured average S_{11} of the designed LNA biased at 200 μW from 4-6 GHz is -8.9 dB, with the lowest value being -13.5 dB. Given the 60 dB isolation from isolators between the parameteric amplifier and the HEMT LNA [4], S_{11} becomes less crucial in the qubit readout system. The average S_{22} is -18.7 dB.

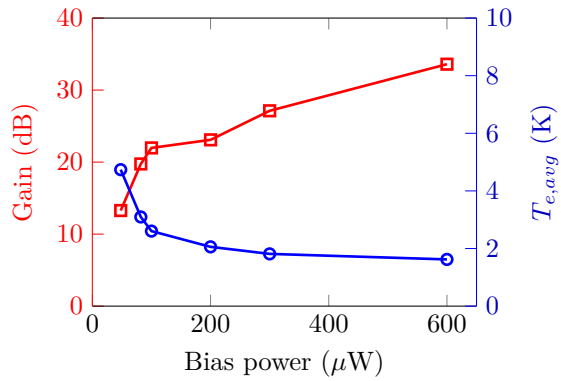

Figure 3.6: Measured average gain (red square line) and noise temperature (blue circle line) as a function of the total dc power from 48 to 600 μW for the 4-6 GHz LNA at 4 K. Bias points are 48 μW ($V_{ds1} = 0.04$ V, $I_{d1} = 0.6$ mA, and $V_{ds2,3} = 0.04$ V, $I_{d2,3} = 0.6$ mA), 82 μW ($V_{ds1} = 0.05$ V, $I_{d1} = 1$ mA, and $V_{ds2,3} = 0.04$ V, $I_{d2,3} = 0.8$ mA), 100 μW ($V_{ds1} = 0.06$ V, $I_{d1} = 1$ mA, and $V_{ds2,3} = 0.05$ V, $I_{d2,3} = 0.8$ mA), 200 μW ($V_{ds1} = 0.08$ V, $I_{d1} = 1.5$ mA, and $V_{ds2,3} = 0.08$ V, $I_{d2,3} = 1$ mA), 300 μW ($V_{ds1} = 0.1$ V, $I_{d1} = 2$ mA, and $V_{ds2,3} = 0.1$ V, $I_{d2,3} = 1$ mA) and 600 μW ($V_{ds1} = 0.2$ V, $I_{d1} = 2$ mA, and $V_{ds2,3} = 0.1$ V, $I_{d2,3} = 2$ mA), respectively.

Fig. 3.7 depicts the input and output P1dB values of the fabricated amplifier. The measured average output P1dB values at 100, 200, and 600 μW dc power are -30.6, -23.2, and -19.1 dBm, respectively. The corresponding average input P1dB values are -53.0, -49.0, and -50.2 dBm, which are sufficient to support more than 2000 qubit readout simultaneously based on analysis in Section 3.1. Notably, even with one-order less dc bias power, the input P1dB of the designed LNA remains comparable to the typically utilized LNA for qubit readout, which is around -52 dBm [26].

In summary, a low-power HEMT LNA has been designed and optimized based on the requirements analysis for its application in the quantum computing readout system. The LNA was a three-stage cascade hybrid design with a suspended transmission line for high-impedance matching required at low power. Based on the measurement results, the LNA successfully achieved its design objectives in terms of noise, power consumption, gain, and dy-

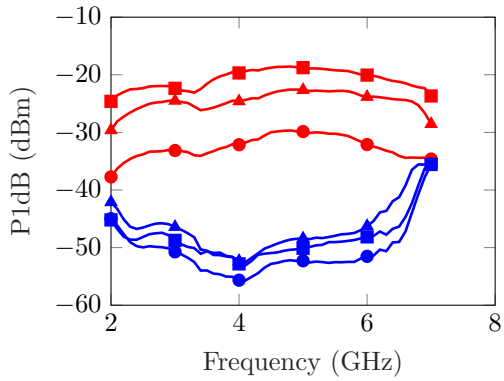

Figure 3.7: Measured input and output P1dB of the fabricated LNA circuit at 4 K for various dc power. The blue lines are input P1dB and the red lines are output P1dB. Circle, triangle and square lines represent bias power of 100, 200, and 600 μW, respectively.

namic range, aligning with the requirements for qubit readout. The measured noise temperature and gain of the fabricated LNA were found to be in good agreement with simulations, which validated the efficiency of the extracted low-power small-signal noise model for the InP HEMT. The LNA demonstrated qubit readout threshold noise with low power consumption, achieving an $T_{e,avg}$ of 2.0 K with only 200 μW dc power. To the best of the author's current knowledge, no other semiconductor-based LNA designed for qubit readout frequencies has achieved a 2.0 K noise temperature with power consumption below 2 mW [1], [3], [26]. The significant decrease in dc power consumption and high input P1dB demonstrated by the HEMT LNA in this licentiate thesis highlights the circuit's potential for future large-scale quantum systems.

CHAPTER 4

A low-power LNA for qubit readout using an optimized InP HEMT

In this chapter, the low-power small-signal noise modeling methodology from Chapter 2 will be applied to a novel InP HEMT where the epitaxial structure has been optimized for even lower transistor noise than in Chapter 2. A new InP HEMT model was compared with the standard InP HEMT model derived in Chapter 2. The optimized InP HEMT was tested in the first stage of the low-power 4-6 GHz LNA designed for qubit readout described in Chapter 3. The LNA measurement results were compared with the results in Section 3.3. It will be shown that the optimized InP HEMT can be successfully applied for the LNA in this work to advance state-of-the-art noise performance towards 100 μW dc power consumption. This shows the potential for low-power HEMT LNAs for qubit readout circuitry in future massive quantum computing.

4.1 Optimized HEMT technology for low power

The standard InP HEMT, whose epitaxial structure has been described in Section 2.1, is denoted as HEMT A. The optimized InP HEMT is denoted as

HEMT B. The epitaxial structure of HEMT B is described in [17]. A primary distinction between the HEMTs was small adjustments of the epitaxial layer thickness between gate and channel in the device. Compared to HEMT A, the spacer thickness of HEMT B was changed from 3 to 5 nm and its barrier thickness from 8 to 4 nm. When used in the cryogenic 4-8 GHz hybrid LNA, HEMT A achieved $T_{e,avg}$ of 1.7 K at a dc power of 12.3 mW. On the other hand, the LNA employing HEMT B exhibited a $T_{e,avg}$ of 1.4 K while consuming only 6.1 mW dc power [17]. The optimized spacer thickness leads to better channel confinement which shows potential for better noise performance at low power. The quest in this thesis was to evaluate the optimized HEMT B in the model and design approach used for sub-mW LNAs based on HEMT A in Chapter 2 and 3.

4.2 Comparison of small-signal noise models

Cryogenic low-power small-signal noise modeling in Chapter 2 has been applied to HEMT B for dc bias points ranging from 0.05 to 0.1V for V_{ds} and I_d = 1 mA, corresponding to a HEMT bias power of 50 to 100 μW. The selected dc bias range was just before the small-signal parameters of HEMT A began to deteriorate rapidly, according to the extracted model in Chapter 2. This chosen bias range allowed for optimizing power consumption while preserving the noise performance of the HEMT. Fig. 4.1 presents the small-signal model parameters for HEMT A and B at 4 K. The small-signal parameters include g_m, C_{gs}, C_{gd}, g_{ds}, and calculated f_T as a function of V_{ds} at an I_d of 1 mA for both HEMTs. The g_m of both HEMT A and B remains relatively unaffected by the variation of V_{ds}. HEMT B's average g_m is 445 mS/mm, which is 36% higher than HEMT A. Conversely, C_{gs} and C_{gd} for both HEMTs are quite similar, as a result of their identical device geometries. The C_{gs} and C_{gd} for both HEMTs do not respond to changes in this V_{ds} interval. In contrast, g_{ds} of HEMT B is around 20% higher than that of HEMT A. Both HEMTs exhibit a slight increase in g_{ds} with a decrease in V_{ds}. The f_T, taking all small-signal parameters into account, appears to marginally decline when V_{ds} decreases from 0.1 to 0.05 V. f_T of HEMT B is 32% higher than HEMT A, primarily due to the difference in g_m, as indicated by Eq. (2.2). Within the examined low-power range, the small-signal model parameters that exhibit notable differences between HEMT A and B are the channel-related parameters g_m and

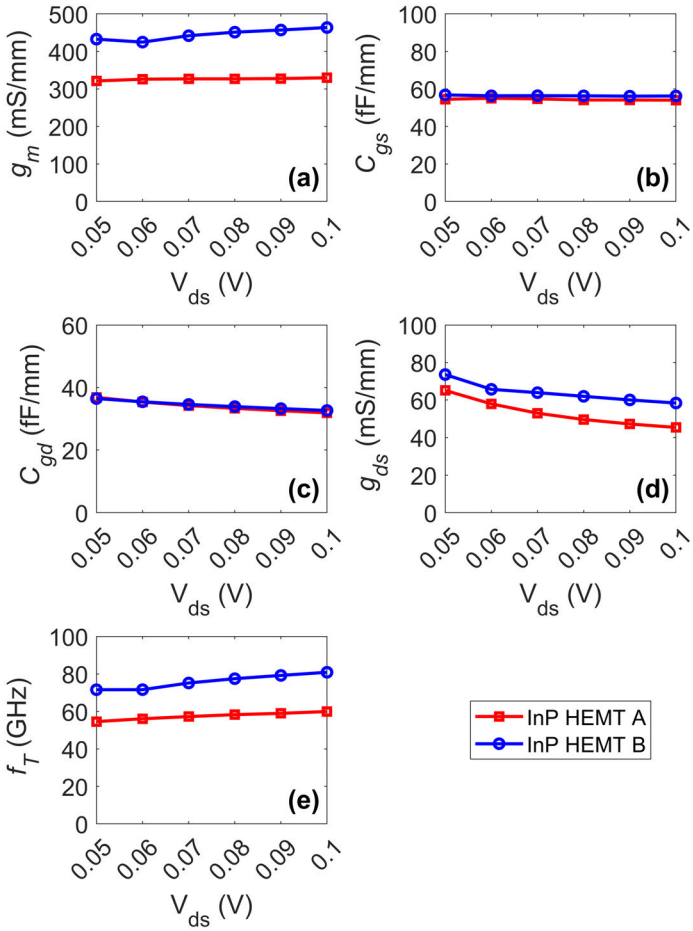

Figure 4.1: Small-signal model parameters (a) g_m, (b) C_{gs}, (c) C_{gd}, (d) g_{ds}, and (e) f_T as a function of V_{ds} at 6 GHz for HEMT A and B at 4 K. I_d = 1 mA.

g_{ds}. This distinction can be accounted for by the optimized spacer thickness that leads to better confinement of the two-dimensional electron gas in the cryogenic HEMT channel [17], [35].

Fig. 4.2 illustrates the extracted T_d, the product of g_{ds} and T_d, T_{min}, N,

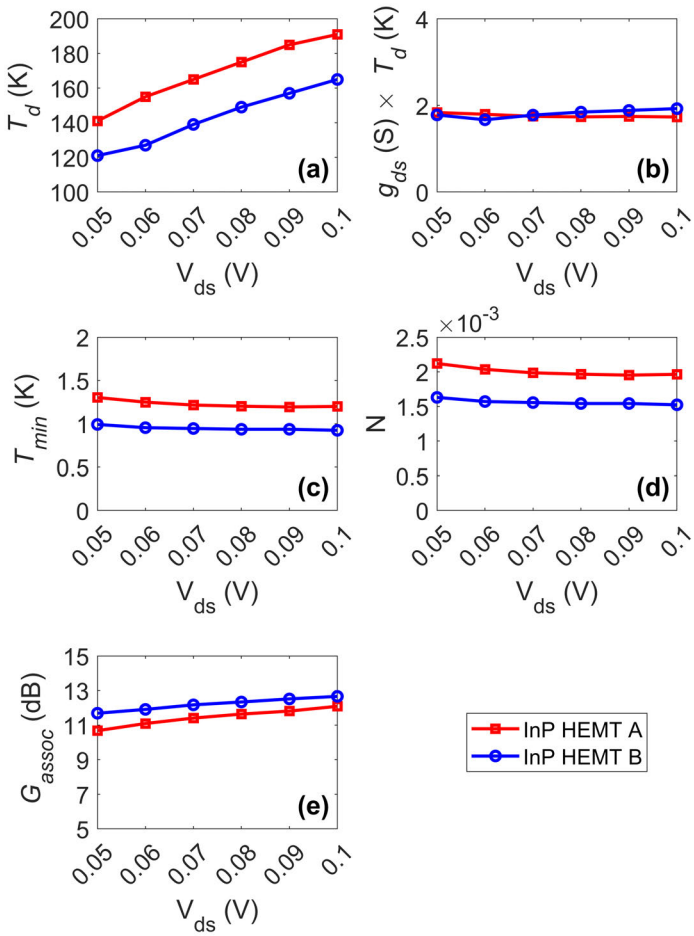

Figure 4.2: Noise-model parameters (a) T_d, (b) product of g_{ds} and T_d, (c) T_{min}, (d) N, and (e) G_{assoc} as a function of V_{ds} at 6 GHz for HEMT A and B at 4 K. $I_d = 1$ mA.

and G_{assoc} at 6 GHz as a function of V_{ds} at an I_d of 1 mA for both HEMTs at 4 K. As V_{ds} decreases from 0.1 to 0.05 V, T_d exhibits a declining pattern, indicating that the channel temperature reduces with less dc power applied. HEMT A has a 10% higher average T_d compared to HEMT B. Nevertheless,

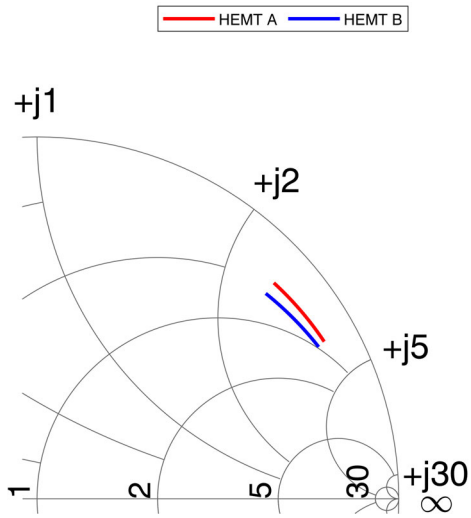

Figure 4.3: The extracted Γ_{opt} from 4 to 6 GHz for HEMT A (red solid line) and B (blue solid line) at 4 K. $I_d = 1$ mA and $V_{ds} = 0.05$ V. [From Paper C]

the product of T_d and g_{ds} for both HEMTs is quite similar. Consequently, the lower T_d advantage for HEMT B to reach lower T_{min} is offset by its increased g_{ds}. The average T_{min} for HEMT B is 0.95 K, which is 30% lower than HEMT A (1.23 K). The reduced T_{min} of HEMT B can therefore be ascribed to its higher g_m (and effectively f_T) values.

In Fig. 4.2 (d), HEMT A appears more sensitive to mismatch than HEMT B, showing a 30% elevated N value. Due to the variance in g_m, HEMT B exhibits a slightly higher G_{assoc} compared to HEMT A, as plotted in Fig. 4.2 (e).

The Γ_{opt} for the noise match at 4-6 GHz for both HEMTs is shown in the Smith chart in Fig.4.3. Relative to HEMT A, HEMT B's Γ_{opt} lies closer to the center of the Smith chart, which is attributed to HEMT B's higher g_m [28]; See Fig.4.1 (a).

Fig. 4.4 presents the simulated T_e when matching the input and output of the two HEMT models to 50 Ω without any matching network at 6 GHz. The T_e for a 50 Ω port impedance serves as an initial approximation for the quality of matching, taking all noise model parameters into account. Although the

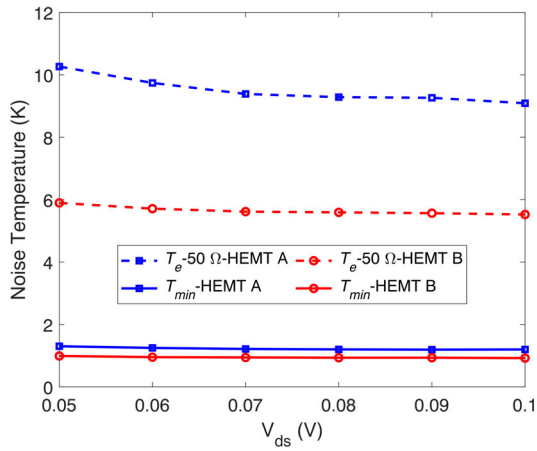

Figure 4.4: The simulated T_e at 6 GHz for HEMT A and B to match both input and output to 50 Ω situation. The T_{min} at 6 GHz of both HEMTs are plotted for comparison. $I_d = 1$ mA. [From Paper C]

average T_{min} for HEMT A and B differs by only 0.28 K, their average T_e over V_{ds} displays a 3.8 K difference. This indicates a more favorable trade-off between noise and bandwidth for HEMT B as opposed to HEMT A when operating at low power.

4.3 Measurement results and comparison

The impact from HEMT A or HEMT B on the noise performance at low power is demonstrated using the 4-6 GHz cryogenic LNA designed for qubit readout in this thesis; See Chapter 3. As the initial stage of the LNA is vital in defining overall noise performance, the first stage of the LNA was used to evaluate HEMT A and HEMT B. The performance of LNA A, which employed HEMT A for all three stages, was reported in Section 3.3. LNA B is identical to LNA A but for the first stage where HEMT B replaced HEMT A.

Both LNAs were characterized under 100 μW bias ($V_{d1} = 0.06$ V and $I_{d1} =$ 1 mA, and $V_{d2,3} = 0.05$ V and $I_{d2,3} = 0.8$ mA). The corresponding first-stage HEMT bias power was 50 μW ($V_{ds} = 0.05$ V and $I_d = 1$ mA). As shown in Fig.4.5, the measured $T_{e,avg}$ for LNA A and LNA B was 2.6 K and 2.0 K,

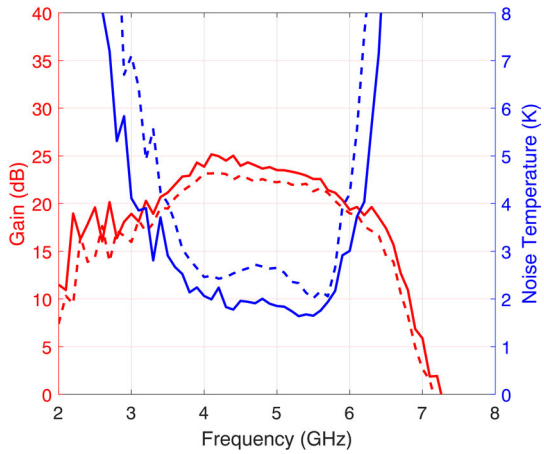

Figure 4.5: Measured gain and noise for the 4-6 GHz HEMT LNAs at 4 K under 100 μW dc power consumption. The dashed lines represent LNA A, and the solid lines LNA B. The blue color represents the noise temperature and the red color the gain. [From Paper C]

respectively. The 23% decrease in $T_{e,avg}$ for LNA B compared to LNA A was mainly due to the increase in g_m and the reduction in T_d for HEMT B compared to HEMT A. The average gain for LNA A and LNA B was 22.5 dB and 23.2 dB, respectively. The improved average gain for LNA B compared to LNA A was due to the greater G_{assoc} of HEMT B compared to HEMT A; See Fig.4.1(b). The measured input P1dB for LNA B was -53 dBm, which was the same as LNA A. The P1dB was mostly limited by the output stage HEMT, which was identical for the two LNAs. The average S_{11} of LNA B for 4-6 GHz was -7.2 dB, which was 0.9 dB improvement compared to LNA A.

The improved noise performance, gain, and input matching of LNA B compared to LNA A at low power aligns with predictions made by the small-signal noise model comparison in section 4.2. This reinforces that the epitaxially optimized HEMT B, boasting a superior g_m, offers a more advantageous trade-off between noise performance and bandwidth compared to HEMT A.

4.4 State-of-the-art comparison

The performance of LNAs presented in this chapter and Chapter 3 has been compared with state-of-the-art cryogenic amplifiers operating at low dc power in frequency bands targeted for qubit readout, as shown in Table 4.1. A new figure-of-merit (FOM) modified from [20] is proposed where $T_{e,avg}$ is replaced by $T_{e,avg,total}$:

$$FOM = \frac{f_h}{f_l} \times \frac{hf_0}{kT_{e,avg,total}} \times \frac{1}{P_{dc}} \tag{4.1}$$

where

$$T_{e,avg,total} = T_{e,avg} + \frac{T_{e,avg}}{G} + \frac{T_{e,avg}}{G^2} + \frac{T_{e,avg}}{G^3} + ... = T_{e,avg} \times \frac{G}{G-1} \tag{4.2}$$

and f_h, f_l, and f_0 represent the upper-band, lower-band, and central frequency within the designed bandwidth, respectively; P_{dc} denotes the total dc power for the LNA; G is the average gain of LNA. The FOM represent maximum to minimum frequencies scaled by the inverse of both the average number of added photons and the total dc power consumption. The gain is involved by $T_{e,avg,total}$ that represents the total average noise temperature with infinite number of cascaded LNAs.

Table 4.1 categorizes amplifiers by device technology and ranks them based on their FOM, starting with the highest values. Among the semiconductor-based LNAs, the InP HEMT based LNAs still represent the lowest noise temperature working with minimal dc power consumption, leading to the highest FOM. Although MMIC designs have benefits for mass production, hybrid designs still show better performance. This is due to the design flexibility of the hybrid, especially the ability to use low-loss substrates and other strategies for optimal matching. SiGe HBT-based LNAs are notable for their considerable gain at low power and has the advantage as a silicon technology to be integrated with CMOS. However, the SiGe-HBT LNAs have not achieved top-tier noise performance and is not sufficient on its own for qubit amplification. CMOS LNAs, using refined circuit typologies made possible by mature processes, have been optimized for cryogenic environment and designed for qubit readout. However, compared to InP HEMT and SiGe HBT LNAs, CMOS LNAs exhibit much higher noise and power consumption. Lastly, the TWPA operating at 4 K has below 2.0 K $T_{e,avg}$ with 100 μW dc consumption, which is

Table 4.1: Comparison of state-of-the-art cryogenic LNAs for qubit readout frequencies.

Ref.	Amplifier type	Device Technology	Freq. (GHz)	T_{eavg} (K)	G (dB)	dc power (mW)	FOM ($10^{-2}mW^{-1}$)
[22]	MMIC	TWPA	3.5-5.5	1.9	18	100	178.7
[15]	Hybrid	InP HEMT	4-8	4.1	20.0	112	124.2
[15]	Hybrid	InP HEMT	4-8	2.8	27.0	300	68.5
[48]	Hybrid IC	InP HEMT	0.3-14	3.5	41.6	12000	38.1
[14]	Hybrid	InP HEMT	4-8	1.6	44.0	4200	8.57
[35]	Hybrid	InP HEMT	4-8	1.2	42.0	7800	5.7
[49]	Hybrid IC	InP HEMT	4-12	8.1	26	12000	1.2
[50]	MMIC	InP HEMT	4-8	3.8	23.7	770	19.6
[50]	MMIC	InP HEMT	4-8	2.7	31.0	7780	2.7
[49]	MMIC	InP HEMT	4-12	11.6	22	41000	0.2
[51]	MMIC	InP HEMT	4-12	22.5	27	20900	0.2
[52]	Hybrid IC	SiGe HBT	0.1-3	4.6	30.5	1000	48.5
[20]	Hybrid	SiGe HBT	4-8	3.2	27.5	1000	18.0
[19]	Hybrid IC	SiGe HBT	4-8	8.0	30.0	760	9.5
[21]	MMIC	SiGe HBT	3-6	4.3	36.0	1800	5.58
[53]	MMIC	CMOS	6-8	≈ 39.0	≈ 50.0	4200	0.3
[54]	MMIC	CMOS	4.2-9.2	≈ 12.7	≈ 33.0	21000	0.3
[55]	MMIC	CMOS	3.9-5.3	10.2	36.5	23100	0.1
This work, LNA B	Hybrid	InP HEMT	4-6	2.0	23.2	100	**180.5**
This work, LNA A	Hybrid	InP HEMT	4-6	2.6	22.5	100	138.5
This work, LNA A	Hybrid	InP HEMT	4-6	2.0	23.1	200	90.0
This work, LNA A	Hybrid	InP HEMT	4-6	1.6	33.6	600	37.5

a true challenger for InP HEMT cryogenic LNAs. However the TWPA suffers from lower gain and linearity with higher cost and fabrication complexities that restricts its usage.

LNA A in this thesis with 100 μW bias power exhibits the highest FOM among the listed semiconductor solutions. It achieves 2.0 K $T_{e,avg}$ for qubit readout with 200 μW bias power. On the other hand, LNA B presented in this study reaches 2.0 K $T_{e,avg}$ with 100 μW bias power. To our knowledge, this represents the most efficient power consumption for a transistor-based LNA achieving 2.0 K threshold noise performance for qubit readout. When benchmarked against the TWPA at 4 K, LNA B has nearly the same noise and dc power consumption with higher gain and linearity. The performance combined with cost-effectiveness, makes the LNA B strong competitor for qubit readout in future large-scale quantum computing system. Furthermore, the next iteration employing optimized InP HEMTs across all LNA stages is

expected to deliver even more superior results.

CHAPTER 5

Conclusions and future work

5.1 Conclusions

This thesis has developed the HEMT modeling and circuit design methodology for a cryogenic LNA operating below 1 mW. The circuit design targeted the readout of superconducting qubits in a quantum computer. A HEMT LNA consuming 100 μW dc power has been demonstrated with 23.2 dB average gain and 2.0 K noise temperature. This represents a new state-of-the-art for qubit readout using semiconductor-based amplification at 4 K.

First, a 100-nm gate-length InP HEMT was characterized for its noise and RF performance at dc biases down to 1 μW. A dual-bias strategy ensured accurate noise extraction at low dc bias for the HEMT. The extracted model revealed that $V_{ds} = 0.05$ V defined a lower limit for maintaining noise performance at reduced power. The model enabled the first-ever design and optimization of an InP HEMT LNA for qubit readout at such low power.

Secondly, the superconducting qubit readout system was discussed regarding its requirement for the HEMT cryogenic LNA. Tailored design goals were set based on the extracted model and application requirements. A suspended transmission line structure was realized in cryogenic vacuum environment to

achieve high impedance for noise match at low-power bias of the InP HEMT. The design method resulted in a 4-6 GHz cryogenic LNA that attained 2.0 K $T_{e,avg}$ threshold performance for qubit readout with 200 μW dc power consumption.

Finally, the 4-6 GHz cryogenic HEMT LNA in Chapter 3 was tested with an InP HEMT slightly modified in the thicknesses of the epitaxial layers. The improvement of model parameters of the new HEMT was analyzed with respect to the standard HEMT. The enhancement in g_m was the reason for superior noise performance meaning easier matching conditions for the HEMT. The LNA using the optimized InP HEMT as the first stage reached 2.0 K $T_{e,avg}$ with 100 μW bias power, which is a new state-of-the-art performance with even higher FOM than a superconducting TWPA operated at 4 K [22].

5.2 Future work

Based on the demonstration of this study, the author believes the following topics can be interesting for future studies:

- **Demonstration of HEMT LNAs with optimized InP HEMT for 6-8 GHz.** The 4-6 GHz LNA employing epi-optimized InP HEMT for the first stage demonstrated large improvement in performance. It is promising to have 6-8 GHz LNA with similar enhanced low-power performance to cover the upper half of commonly used qubit readout frequencies.

- **Test the low-power cryogenic LNA in the qubit readout chain.** It is reported that the qubit can be negatively influenced by the thermal disspation from the HEMT LNA at 4 K [56]. The low-power cryogenic HEMT LNA with more than one-order power consumption improvement can be tested in the qubit readout chain to further verify this claim. The experiment can pave the way for better integration in qubit readout system.

- **Develop pulsed operation for low-power cryogenic HEMT LNA.** The low-power cryogenic HEMT LNA can be operated under pulse operation due to the pulse nature of qubit readout [5]. A pulsed HEMT LNA can greatly reduce the LNA's average power consumption without sacrificing RF and noise performance. The dynamic response of the

HEMT and LNA needs to be investigated for implementation of pulsed operation of the cryogenic HEMT LNA.

- **High performance InP MMIC LNA.** The developing InP-on-Si technology is promising for fabrication of high-performance and low-power MMICs in much larger volumes than today. The potential to be integrated with CMOS technology will enable more advanced circuit topology to overcome matching difficulties. The MMIC solution can provide larger volumes and higher integration for the whole readout chain.

Acknowledgments

I'd like to express deep gratitude to everyone who supported me and made this work possible.

My heartfelt thanks go to my main supervisor, Professor Jan Grahn, for his support, encouragement, and invaluable discussions throughout this journey.

I'm also thankful to my co-supervisors from Low Noise Factory AB (LNF), Dr. Jörgen Stenarson and Dr. Peter Sobis. Jörgen's guidance in the measurement lab has been invaluable, revealing the true essence of engineering problem-solving. Peter was always supportive, helping me with HFSS and circuit fabrication, and we had many good discussions.

I want to thank Professor Jan Stake, my examiner, for creating a positive scientific atmosphere at the Terahertz and Millimetre Wave Laboratory (TML), and for his consistent encouragement.

A special thank goes to Niklas Wadefalk, CEO of LNF, for enriching my understanding in circuit design, providing access to LNF's resources, and helping polish my manuscripts. Dr. Sumedh Mahashabde and Dr. David Niepce, both from LNF, have inspired me with their expertise in quantum computing. I'm thankful to Johan Embretsén, Production Manager at LNF, for seamlessly coordinating measurements and fabrication timings; and to Hannes Hanhineva, Senior Production Technician at LNF, for helping me assembly the circuits with excellent skills.

I appreciate that Junjie Li for providing me her state-of-the-art InP HEMT. I want to send my regards to Dr. Andrei Vorobiev from TML, for helping me understanding semiconductor physics behind my observations, Professor Serguie Cherednichenko for fruitful discussion and helping me many times on the cryogenic probe station, and Dr. Yu Yan for giving me help hand for finding lab components!

I want thank to Hangxi Li from Quantum Technology Laboratory (QTL) for discussing quantum computer architecture with me and invite me to present my work at QTL group meeting, so I can get precious feedback from Professor Per Delsing and Dr. Giovanna Tancredi.

To my friends on the 6th floor of MC2, thanks for your help and the fun times we had. Last but not least, I want to thank my families for your priceless love and support.

This work was supported by the Sweden's innovation agency (Vinnova) in the Strategic Innovation Program Smartare Elektroniksystem and by the

GHz-ChaseOn Bridge Centre at Chalmers University of Technology.

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