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Ionotronic WS_2 memtransistors for 6-bit storage and neuromorphic adaptation at high temperature

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Inspired by massive parallelism, an increase in internet-of-things devices, robust computation, and Big-data, the upsurge research in building multi-bit mem-transistors is ever-augmenting with different materials, mechanisms, and state-of-the-art architectures. Herein, we demonstrate monolayer WS_2-based functional mem-transistor devices which address nonvolatility and synaptic operations at high temperature. The ionotronic memory devices based on WS_2 exhibit reverse hysteresis with memory windows larger than 25 V, and extinction ratio greater than 10^6. The mem-transistors show stable retention and endurance greater than 100 sweep cycles and 400 pulse cycles in addition to 6-bit (64 distinct nonvolatile storage levels) pulse-programmable memory features ranging over six orders of current magnitudes (10^{-12}–10^{-6} A). The origin of the multi-bit states is attributed to the carrier dynamics under electrostatic doping fluctuations induced by mobile ions, which is illustrated by employing a fingerprint mechanism including band-bending pictures. The credibility of all the storage states is confirmed by obtaining reliable signal-to-noise ratios. We also demonstrate key neuromorphic behaviors, such as synaptic plasticity, near linear potentiation, and depression, rendering it suitable for successful implementation in high temperature neuromorphic computing. Furthermore, artificial neural network simulations based on the conductance weight update characteristics of the proposed ionotronic mem-transistors are performed to explore the potency for accurate image recognition. Our findings showcase a different class of thermally aided memories based on 2D semiconductors unlocking promising avenues for high temperature memory applications in demanding electronics and forthcoming neuromorphic computing technologies.

npj 2D Materials and Applications (2023)7:63 ; https://doi.org/10.1038/s41699-023-00427-8

INTRODUCTION

The amount of digital data generated by humans, which can be quantified in terms of the number of bits produced yearly, is continuously expanding and is projected to exceed 100 zettabytes by 2023. To effectively manage the massive amount of data and global memory requirements, the upcoming nonvolatile memory (NVM) technologies must furnish multi-bit ultra-high-density storage capacity with a significant extinction ratio, endurance, retention, and low energy consumption[1]. Two-dimensional (2D) layered materials, consisting of atomically thin layers, possess a plethora of exotic properties and have emerged as the leading contenders for the upcoming generation of electronic devices[2]. Specific attention given to the layered transition metal dichalcogenides (TMDCs)[3], has created numerous prospects for developing low-power electronics, cutting-edge memory device arrays[4,5] and smart computing architectures[6] with desirable miniaturization. Recently, there has been an intensive exploration of NVMs based on 2D materials and their heterostructures[7]. These NVMs utilize revolutionary device architecture and unusual mechanisms to overcome the limitations of conventional flash memory based on silicon. Opto-electronically controlled floating gate (FG) and charge trap based devices can produce high operation speed, and low power memory characteristics[8–17]. Nevertheless, it is difficult to develop high-capacity multi-bit generation that can work at elevated temperatures. Recent report by Li et al. propose MoS_2/hBN/MoS_2/GDYO/WSe_2 heterostructure as an active layer to generate 8 memory states[18] whereas, Lai et al. use top FGM with stacked MoS/hBN/2D-RPP to produce 22 distinct memory states[19]. Furthermore, the production of such memory devices necessitates cumbersome state-of-the-art methodologies, which require accurate deposition of various semiconductor layers, and multiple lithography processes, culminating in intricate mem-transistors with numerous floating metals and oxide layers. As the yearning for energy conservation is more prevalent than ever, advancing the scale-down of circuits beyond Moore's law will mandate the exploration of 2D materials based architectures[20].

On the contrary, the electrolyte-gated transistors show analog switching performance with superior storage capacity benefited from their ion-gating mechanism over electrostatic charge trap phenomena, making them viable candidates for brain-inspired computation and logic-in-memory applications[21–25]. Post stimulation, the diffusive dynamics of mobile ions (such as Li^+, Na^+) possess linear and symmetric weight updates of the discrete multilevel states, making them more effective than FGM-based arrays in processing artificial neural networks (ANNs)[26–28]. Despite the recent development of synaptic ion-gated transistors, multi-bit memory based on ion gating mechanisms is still lacking. With the increasing spatial density of FET arrays on a solitary wafer, integrated circuits (ICs) of superior performance can attain an operating temperature as high as 450 K[29]. Therefore, understanding and leveraging the properties of 2D materials-based devices is crucial for their high-temperature potential applications in harsh environments such as aerospace industries, military, automotives, sensors, well logging, oil refinery etc[30]. However, no

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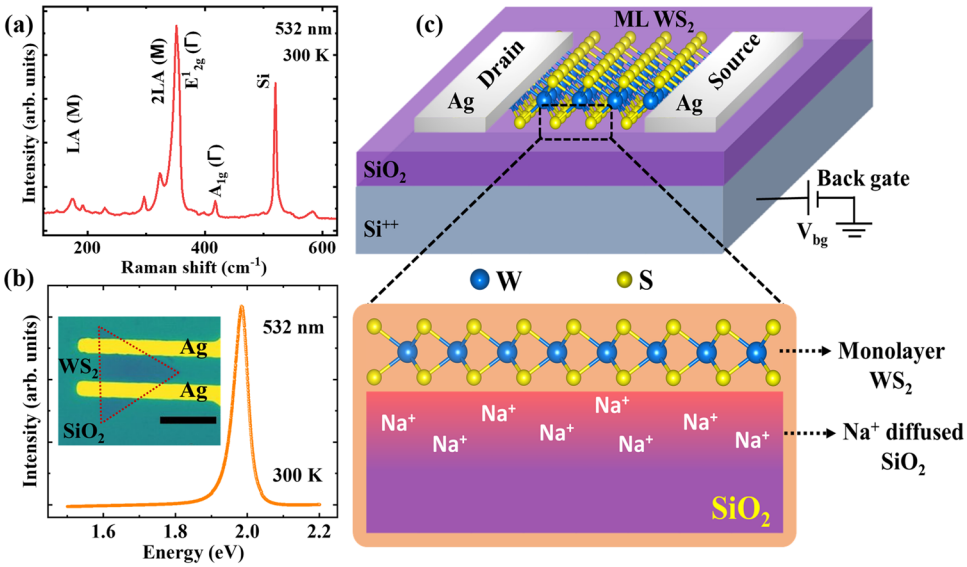

Fig. 1 Structural characterization and device architecture of ion-gated WS_2 transistors. a Room temperature Raman spectrum of as-grown ML WS_2 supported by SiO_2 (285 nm)/Si substrate. **b** The photoluminescence spectrum confirms the monolayer nature of WS_2. Inset shows the optical micrograph (top view) of a WS_2 transistor with silver (Ag) metal as drain/source electrodes (Scale bar is 10 μm). **c** Schematic representation of the ML WS_2-based device model with necessary electrical contacts. The magnified cross-sectional view at the WS_2/SiO_2 interface illustrates the diffusion of Na^+ ions inside SiO_2.

consensus has been reported to address stable multilevel memory switching at elevated temperatures. Unfortunately, the use of liquid electrolytes severely demarcates the integration density of devices and limits their applicability to high-temperature environments[22,24]. As a result, it is imperative to introduce multi-level memories with eccentric synaptic functionalities that can enable simpler device architectures, thermally-stable reliable switching, and enhanced throughput.

In this context, we have proposed and demonstrated monolayer (ML) WS_2 mem-transistor with robust device architecture and reduced dimensionality for multi-bit nonvolatile memory applications at high temperatures (~425 K). The WS_2 based mem-transistor manifests endurance properties greater than 100 sweep and 400 pulse cycles, high switching ratios, non-volatility with stable retention and efficient conductance modulation. The memory behavior is attributed to the interfacial electrostatic doping effect of channel material through active cation migration under the applied gate field. Furthermore, the three-terminal device exhibits more than 64 distinct memory states, making it a potential candidate for 6-bit memory operations. The multi-bit memory operations in our device show exceptional pulse control of charge injection and release, providing a complete yet straightforward strategy to achieve large-scale data storage capabilities in WS_2 mem-transistors. Moreover, key synaptic behaviors such as excitatory post-synaptic current (EPSC), long-term potentiation/depression (LTP/LTD) are demonstrated at elevated temperatures using various pulse schemes. We further utilize ionotronic non-volatile conductance weights to establish excellent pattern recognition accuracy approaching software limit of ~98% during ANN training of MNIST datasets. Our results showcase a different class of thermally-driven memories based on 2D semiconductors, representing a leap forward for developing high density memories and future neuromorphic computing technologies operating at high-temperatures.

RESULTS AND DISCUSSION

Fabrication of ion-gated WS_2 transistors

The ML WS_2 is synthesized via a salt-assisted chemical vapor deposition (CVD) technique[31], wherein the synthesis parameters are fine-tuned to achieve large-scale triangular domain growth with high crystallinity, as shown in Supplementary Fig. 2 and facilitate the diffusion of mobile ions (Na^+) into the SiO_2 gate dielectric (for detailed information, refer to "Methods"). As-grown samples are characterized with Raman spectroscopy at room temperature, utilizing a 532 nm excitation wavelength. The WS_2 exhibits two prominent Raman active modes, namely E^1_{2g} and A_{1g}, as illustrated in Fig. 1a, corresponding to the in-plane vibration of W and S atoms and the out-of-plane vibrations of the S atoms, respectively. The frequency difference ($\Delta\omega \leq 61 cm^{-1}$) between them indicates the ML nature of the as-grown WS_2 samples[32]. Figure 1b displays the photoluminescence (PL) spectrum with a very sharp and intense luminescence at 1.96 eV, which further confirms the high optical grade quality of salt-assisted CVD-grown ML WS_2[33]. The inset shows the optical micrograph (top view) of a WS_2 transistor with silver (Ag) metal as drain/source electrodes (for details, see Supplementary Fig. 2). Figure 1c depicts the schematics of the device architecture with necessary electrical contacts where the back gate is facilitated by heavily doped silicon (Si^{++}). The WS_2/SiO_2 interface is portrayed in a separate magnified cross-sectional cartoon where Na^+ ions are shown to be diffused inside the SiO_2 near the interface region. Recently, Kaushik et al. report the adsorption of lighter impurities such as Na^+ ions, on the SiO_2 surface during NaCl-aided CVD growth[34]. These Na^+ ions get diffused inside the SiO_2 upon high-temperature annealing which can be employed to realize a solid-state ion-gated medium in our case, similar to electrolyte/ionic liquid-gated transistors[22,23].

Thermally-driven hysteresis evolution

The temperature-dependent dual sweep transfer characteristics are conducted under high vacuum (10^{-6} mbar) after annealing the device at 200 °C for 36 h. Annealing is found to be crucial to reduce contact resistances without degrading the device performance, as reported earlier[35]. Figure 2a, b depicts the evolution of hysteresis curves for temperatures ranging from 275 to 425 K during a gate voltage sweep range of ±50 V. The black and red arrows represent forward and backward sweep directions and the threshold voltage differences between them indicate the memory window (ΔV_{th}). Initially at 275 K, the nature of the hysteresis is

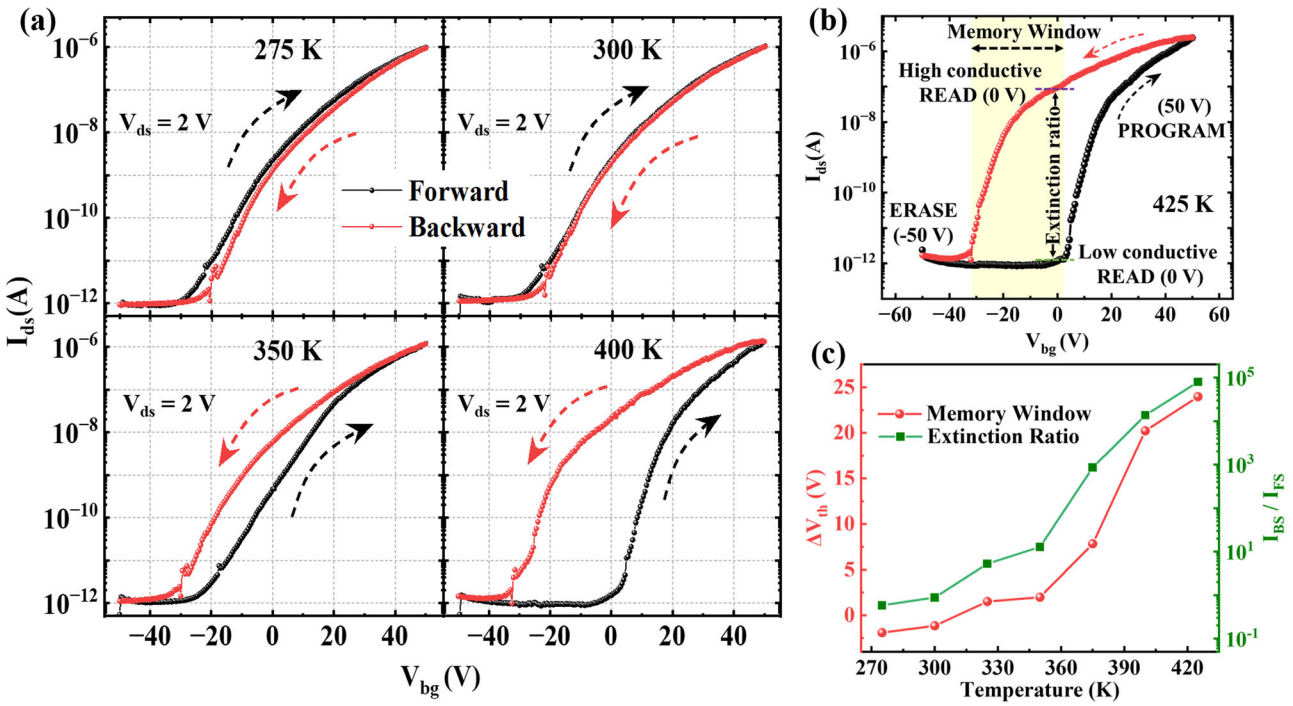

Fig. 2 Temperature-dependent hysteresis evolution. a The dual sweep transfer characteristics at temperatures ranging from 275 to 400 K. The black and red arrows represent forward and backward sweep direction, respectively and nature of the hysteresis loop. **b** Dual sweep reverse hysteretic transfer curves with memory window of 25 V and extinction ratio of ~10^5 is demonstrated at 425 K for gate voltage sweep range of ±50 V. The PROGRAM, ERASE, and READ operation regime are also demonstrated. **c** The relation between memory window ($\triangle V_{th}$) and current switching ratios (I_{BS}/I_{FS}) with temperature at zero gate voltages during dual sweep measurements.

found to be clockwise (CW), while at room temperature, the forward and backward sweeps overlap with each other collapsing the hysteresis completely. Interestingly, upon increasing the temperature to 350 K, an anti-clockwise (ACW) hysteresis loop is evolved which inflates further with elevated temperatures. It is worth to mention that, at 425 K the memory window is increased to as high as 25 V with extinction ratio (I_{BS}/I_{FS}) rises to the orders of 10^5 at zero gate bias. The hysteresis curves at 325 and 375 K along with temperature dependent mobility variations are shown in Supplementary Fig. 3, which are consistent with the thermally-driven hysteresis evolution in our case. Moreover, in Fig. 2b, we demonstrate the potential application of thermally-assisted reverse hysteresis in nonvolatile memory operations. The memory characteristics can be obtained by utilizing specific regions of the transfer curves to define the PROGRAM, ERASE, and READ operations. During the forward sweep, the ERASE operation can be executed by applying a gate voltage of −50 V, followed by a low conductive READ operation at $V_{bg} = 0$ V. Similarly, by applying a high positive gate voltage of 50 V, we can PROGRAM our memory device to achieve a higher conductance state, which can be subsequently READ at $V_{bg} = 0$ V during backward sweep. Recently, the temperature dependent hysteresis crossover/inversion has been reported in ML and few-layer MoS_2[36,37]. However, the nature and origin of the hysteresis loops and their proposed mechanisms are very different from the results we observed in our case. For example, in the article by He et al.[36], the hysteresis loop contains two different regions, i.e., anti-clockwise loop below $V_{bg} = 0$ V and clockwise loop above $V_{bg} = 0$ V, which also limits the extinction ratio to ~10^2. Also, the origin of such hysteresis is attributed to carrier injection from Si into SiO_2 with minimal role of channel MoS_2. However, in our case, the device attains a single large anticlockwise hysteresis with extinction ratio of ~10^6 and the memory is governed by the dielectric/channel interfacial physics. Figure 2c represents the progression of memory windows and extinction ratios as a function of temperature. Both the parameters show systematic and significant enhancements when compared with their respective room temperature values. Here we want to emphasize that our recent findings on CVD (without NaCl) grown ML MoS_2 shows a high temperature clockwise hysteresis behavior owing to the accelerated charge trapping/detrapping, however, the anticlockwise hysteresis is only observed in NaCl-assisted CVD grown MoS_2[38]. This further confirms the Na^+ driven ion-gating induced large reverse hysteresis in our NaCl-assisted CVD grown WS_2 based transistors. For the sake of completeness, we also perform the output characteristics for different gate voltages in our devices which are shown in Supplementary Fig. 4.

Operation mechanism of Ionotronic memory

In conventional WS_2 transistors, a relatively high surface-to-volume ratio necessitates an inescapable exposure of the atomically thin channel to the oxide trap/defect states, which induce clockwise hysteresis and high threshold voltage instabilities, leading to reliability issues[39]. Nonetheless, the substantial hysteresis generated during the dual sweep and pulsed gate operations in most 2D transistor devices has been meticulously utilized for nonvolatile (which encompass 2D flash memory, magnetic random access memory, resistive random access memory) and volatile (such as dynamic random access memory, semi-floating gate transistor) memory applications[1]. However, in our case, temperature modulated hysteresis collapse and switch from clockwise to anti-clockwise hysteresis indicates ion-gating induced charge transfer and charge storage[25]. The increased kinetic energy of Na^+ inside SiO_2 at high temperatures generates an efficient ion gating over conventional dielectric gating for transistor applications[28]. To shed light on the effect of Na^+ ions on hysteresis, we propose a fingerprint mechanism as depicted in Fig. 3a–d, that adequately illustrates the evolution of hysteresis with temperature, providing the possibilities to attain thermally stable nonvolatile memory states in ML WS_2. The upper and lower panel shows the cross-sectional schematic view of the WS_2/Na^+ diffused

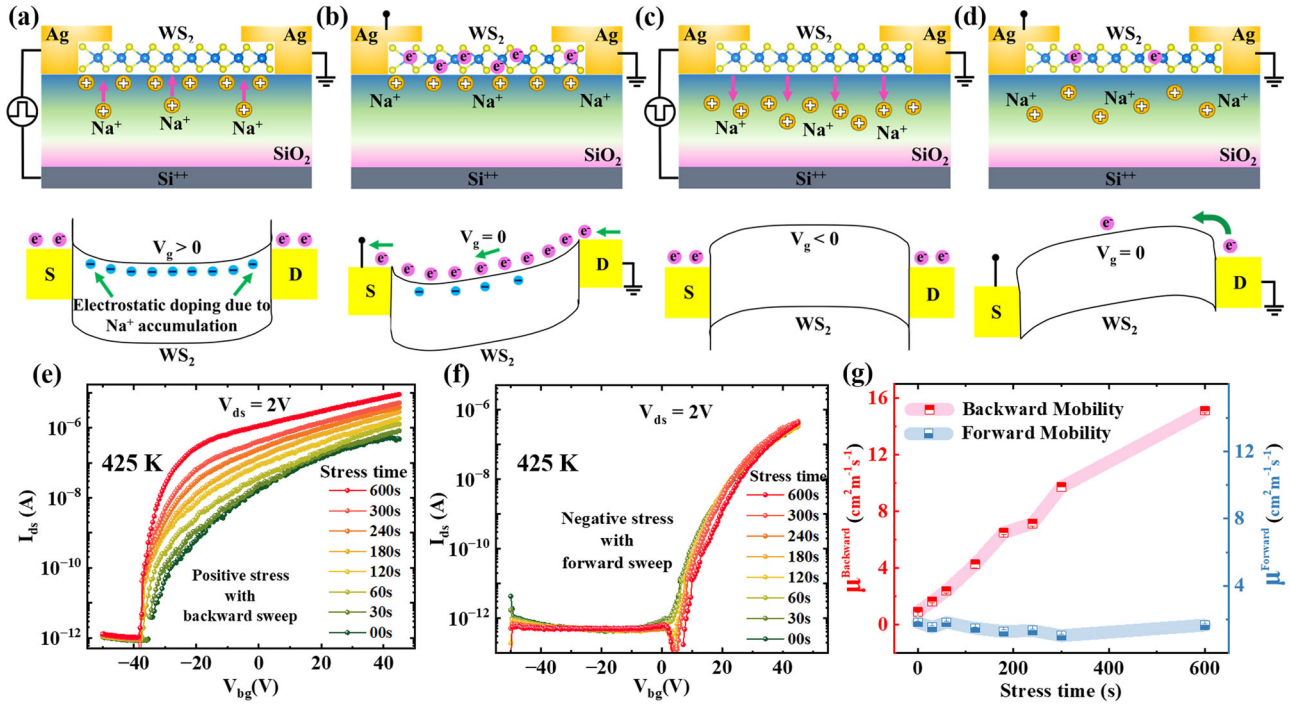

Fig. 3 Operation mechanism of Ionotronic memory. The cross-sectional schematic view of the WS_2 mem-transistor (upper panel), Energy band diagram of source-channel-drain (lower panel) for **a** PROGRAM, **b** High Conductive Read, **c** ERASE, and **d** Low Conductive Read operations. For Read operations, the bias voltage V_{ds} is fixed at a finite voltage (in our case, 2 V) to measure the drain current values after PROGRAM/ERASE. The PROGRAM operation is facilitated by the Na^+ accumulation at the WS_2/SiO_2 interface, whereas in the ERASE operation, the depletion of the ion layer reduces the effective electrostatic doping resetting the device to the original state. The green arrows in the energy band diagrams indicate the direction of the flow of currents through the channel. Effect of **e** Positive (+50 V) and **f** Negative (−50 V) stress under different stress times of ML WS_2 mem-transistor. **g** Mobilities extracted from forward and backward transfer curves vs. stress time, at $V_{ds} = 2$ V.

SiO_2 interface and energy band diagram of source-channel-drain, respectively during various programming operations. Applying a positive gate-source voltage induces a drift of mobile Na^+ ions, causing them to move towards the WS_2 channel. This accumulation beneath the interface, illustrated in Fig. 3a, results in the buildup of spatial charges near the interface. This accumulation has the effect of further electrostatically doping the WS_2 channel, an operation referred as 'PROGRAM'. The added n-doping of WS_2 reduces its energy band below the Fermi level of Ag, creating an easily accessible pathway for conduction electrons to tunnel through.

Figure 3b illustrates the schematic for the "High Conductive Read" operation with a bias voltage (V_{ds}) of 2 V at $V_{bg} = 0$ V. Following the "PROGRAM" operation, the collected Na^+ ions progressively enhance the drain current, reaching around ~10^{-6} A even in the absence of gate voltage during the backward sweep. The corresponding band diagram highlights the increased carrier concentration within the WS_2 channel under the conditions of the "High Conductive Read" state. The Na^+ ions accumulated at the interface exhibit high retention due to their low probability of returning to their original state, even after removing the external electric field, resulting in band lowering and hence high conductance of the WS_2 channel. Thus it can only be depleted by employing a highly negative V_{bg}, an "ERASE" operation. In such cases, the Na^+ ions migrate away from the interface and towards the opposite direction, facilitated by the electrostatic polarization effect. The "ERASE" operation increases the barrier width at the Schottky junction, as displayed in Fig. 3c. A further "Read" operation can furnish low current values up to ~10^{-12} A, akin to the case of an undoped WS_2 channel. The schematic representation of Fig. 3d illustrates low carrier channel densities with corresponding band bending in the "Low Conductive Read" operation. Hence, by administering a positive or negative gate voltage of approximately ±50 V, the doping concentration of the WS_2 channel can be tuned, resulting in a subsequent modification of its resistivity.

Considering the intricate dynamics of Na^+ ions during gating, it is imperative to scrutinize the impact of gate bias stress in our ML WS_2 mem-transistors. Specifically, to induce positive (negative) gate bias stress, a uniform gate voltage of 50 V (-50 V) was applied for a defined duration before measuring the transfer characteristics. As demonstrated in Fig. 3e, the transfer curve gradually shifts upwards with prolonged positive gate bias stress durations. The maximum output current (I_{ds}^{max}) with different hold times is also charted in Supplementary Fig. 5 to elucidate the gate bias stress on our memory devices. It can also be noted that the maximum current augments linearly with increasing stress durations. Interestingly, the transfer curves remain unaltered for mounting negative gate bias stress durations as shown in Fig. 3f. Considering the fact that the Na^+ are mobile in few nm range inside the diffused SiO_2 region, the ions cannot be pushed away to the gate/dielectric interface, unlike the case of single ion conductor[40]. Therefore, we expect the formation of a weaker negatively charged depletion layer at the channel/dielectric interface on the application of negative gate voltage which will have a negligible impact on the device performance. The values of mobilities obtained from multiple transfer curves with various positive and negative stress durations are determined and presented in a graph against the duration of stress in Fig. 3g. It is observed that the positively stressed mobility values vary linearly with increasing stress durations, unlike the case for negatively stressed mobility values. We have also estimated the carrier doping densities of ~10^{12} cm^{-2} for different stress time durations. It may also be noted that the doping concentrations in

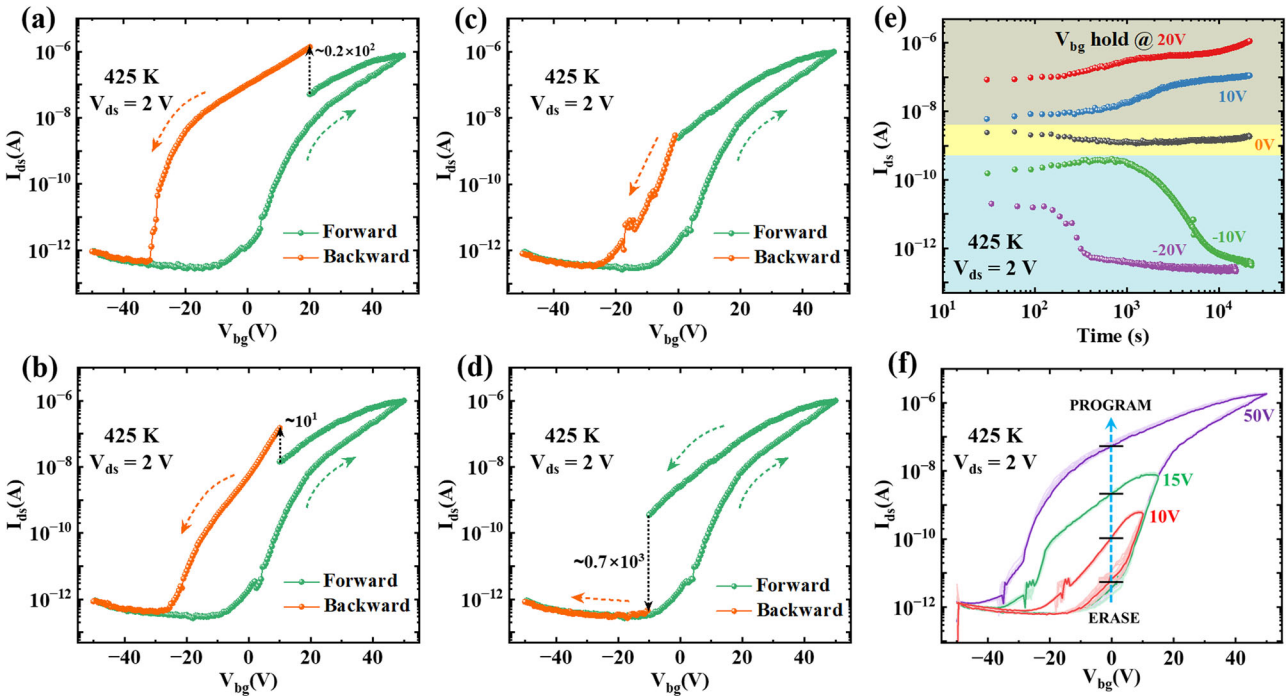

Fig. 4 Influence of hold voltage on hysteretic behavior. The effect of hold voltage on the hysteretic behavior is demonstrated. Initially, the gate voltage is swept from the negative to positive voltage range, and during the backward sweep, it is halted at a specific intermediate voltage called $V_{bg}{}^{hold}$: **a** 20 V, **b** 10 V, **c** 0 V, and **d** −10 V. Then, the current progression is recorded over a period exceeding 20,000 s. After the hold, the sweep is resumed, and the gate voltage returns to the negative range. The hysteresis curve is indicated in green color before the hold and is represented by orange after the delay. **e** The I_{ds} vs. time measured during the hold phase of the experiments demonstrated in (**a**–**d**). **f** Dual sweep transfer curves leading to distinct PROGRAM states by varying V_{bg} amplitudes.

our WS_2 mem-transistors increases with increasing positive stress times as shown in Supplementary Fig. 5.

The existence of hysteresis in the transistor current suggests a dynamic characteristic, which we investigate in Supplementary Fig. 6 by measuring transfer curves with varying sweep rate and range. It may be deduced that since this is an analog memory, changing the voltage sweep range and step size will have an impact on the extinction ratio and hysteresis window because the effective program time will change drastically. We observe an interesting trend by varying the sweep rate from 2 V/s to 0.1 V/s and the range from ±20 V to ±50 V. As the sweep range (rate) is increased (decreased), the current jump observed in the forward sweep becomes more significant. However, a considerable increase in the overall current level is observed toward a lower sweep rate in the backward sweep case, indicating the existence of distinct time scales for different segments of the hysteresis curve. To further probe the dynamics, we terminate the backward sweep at an intermediate gate voltage ($V_{bg}{}^{hold}$) and closely observe the time-dependent fluctuations of I_{ds} over a specific time interval prior to recommencing the sweep as shown in Fig. 4a–d when we hold at 20 V, the drain current increases by approximately ~10^2, whereas holding at 10 V for 20,000 s can elevate the current level to the order of ~10. In contrast, holding at negative $V_{bg}{}^{hold}$ can decrease the current level. Furthermore, Fig. 4e displays the temporal evolution of the current achieved at distinct $V_{bg}{}^{hold}$ levels. Upon halting at a positive $V_{bg}{}^{hold}$, a gradual increase in the drain current is witnessed over a prolonged time period. However, holding at $V_{bg}{}^{hold} = 0$ V, we observe no significant alterations in drain current values after the holding period, indicating zero gate bias as an ideal condition for READ voltage. For the negative $V_{bg}{}^{hold}$, the current exhibits a remarkably rapid decrease in a time frame that is several orders of magnitude shorter. These findings are in sharp contrast to the transient analysis reported earlier, where no current rises were observed for any $V_{bg}{}^{hold}$ cases[36]. Additionally, we showcase an alternative trial by altering the V_{bg} sweep amplitudes to accomplish discrete PROGRAM states. As depicted in Fig. 4f, a rise in the positive V_{bg} from 10 V to 50 V leads to an increase in the hysteresis window and extinction ratios, with the expectation of achieving diverse PROGRAM states. While conducting a dual sweep, we execute retention measurements at $V_{bg} = 0$ V to observe the loss of carriers over time. However, the satisfactory retention behavior of over 10^4 for various PROGRAM states, as demonstrated in Supplementary Fig. 7, exemplifies the exceptional dynamic behavior of charge injection and release of our ion-gated WS_2 mem-transistor.

Robustness of nonvolatile memory in ion-gated transistors

The WS_2-based mem-transistors are subjected to endurance tests, wherein more than 100 hysteresis cycles with varying sweep rates are performed. As shown in Fig. 5a, the tests reveal that our memory device sustains high on/off ratios without significant decay, demonstrating its superior memory capacity and reliability. In addition, we have extracted the forward and backward mobilities and the threshold voltage shifts (ΔV_{th}), of the WS_2 channel from the transfer curves acquired at a sweep rate of 0.5 V/s, which have been briefly summarized in Supplementary Fig. 8. The mobilities and ΔV values of 100 hysteresis cycles demonstrate the reliability of these memory devices, with minimal fluctuation bands. Transfer curves have been obtained for eight different devices to establish stability amidst device-to-device variations. The extracted parameters, encompassing extinction ratios and memory windows (ΔV) of different devices, are depicted in Fig. 5b. The large extinction ratios observed in these ionotronic memory devices concur with the previous reports based on the floating gate and electrolyte-gated mem-transistors[13,19,25]. An additional performance index of a durable memory device is its retention behavior over an extended duration. In this particular case, the retention characteristics following PROGRAM (a pulse of +50 V, 4 s)

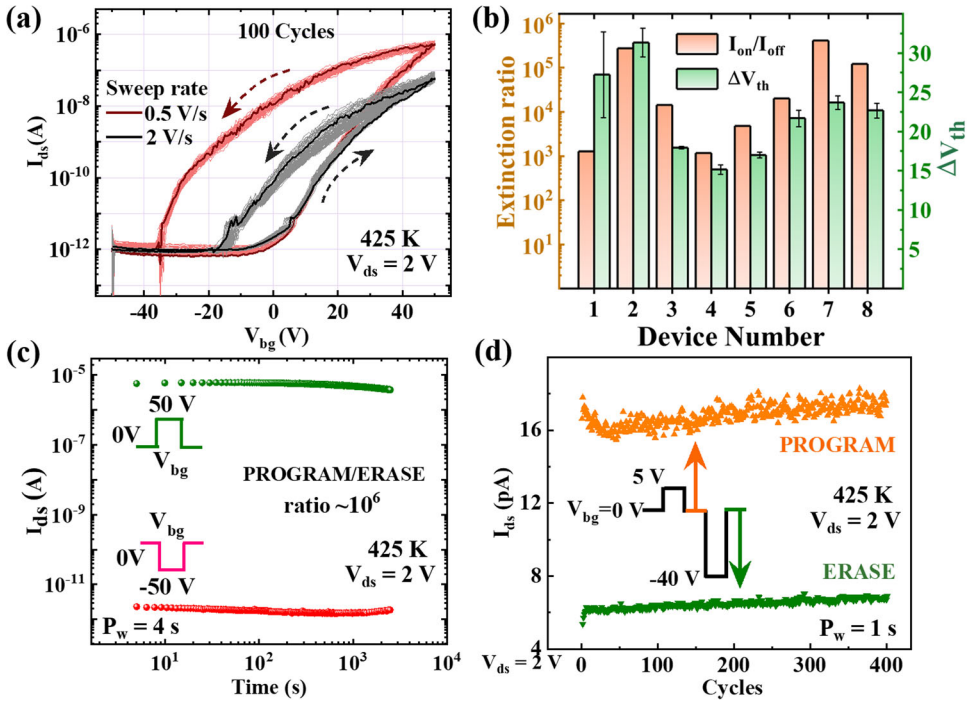

Fig. 5 Robustness of nonvolatile memory in ion-gated transistors. a The endurance tests of 100 dual sweep hysteresis cycles for varied sweep rates. The gate voltages are swept from −50 V to +50 V and back to again −50 V. Transfer curves (black) of faster sweep rates introduce a stable extinction ratio of $10^{2,}$ whereas the Transfer curves (black) of slower sweep rates provide a stable I_{on}/I_{off} ratio of 10^4. **b** Extracted parameters, i.e., I_{on}/I_{off} ratios (orange) and memory windows (ΔV) (green) of transfer curves from 8 different devices illustrating device-to-device variations (the error bars represent the standard error of the mean). **c** Retention characteristics of the device after PROGRAM (pulse of +50 V, 4 s) and ERASE (pulse of −50 V, 4 s) operations for 2000 s. **d** The ionotronic memory device over 400 cycles of operations showing endurance characteristics of the programmable waveforms at (0 V, 1 s) READ pulse (orange) succeeded by a (5 V, 1 s) PROGRAM pulse. After that, an ERASE pulse of (–40 V, 1 s) is supplied, and another READ pulse (green) for 1 s is followed. The orange (green) triangles represent High (low) conductive READ currents in each cycle.

and ERASE (a pulse of −50 V, 4 s) operations have been illustrated in Fig. 5c. Our device exhibits an stable extinction ratio exceeding 10^6 after 2000 s at elevated temperatures, thereby opening up opportunities for practical device applications in innovative nonvolatile memories. Building memory devices that can operate at high temperatures offers numerous challenges, including the shortened data retention time resulting from increased thermal screening[41]. Additionally, an augmented carrier trapping and de-trapping leads to significant off-state currents, which results in lower on/off ratios[30]. To our knowledge, no report on such high-temperature retention characteristics with a larger extinction ratio is available. Furthermore, we investigate the programmable cyclic endurance of the device by applying alternating positive and negative pulses. The applied periodic waveform includes a PROGRAM (5 V, 1 s) pulse, followed by a READ (0 V, 1 s) pulse, and then an ERASE (–40 V, 1 s) pulse followed by another similar READ pulse, as shown in Fig. 5d. The high/low conductive READ currents remain nearly invariant even after subjecting the devices to 400 periodic cycles, indicating the exceptional endurance properties of these memory devices. Here, the mechanism involved in the 2D WS_2 nonvolatile memory devices opens up broader possibilities to use 2D semiconductors for robust data storage applications.

Dynamic response and paradigm of multibit storage

Multibit memories, featuring the capacity to stockpile over a solitary bit of data within a single device, have been widely acknowledged as an effective mechanism to amplify the data retention ability in forthcoming miniaturized electronics. To examine the dynamic response of our memory device, we alter the V_{bg} pulses in a programmable operation, fluctuating between ±40 V for a duration of 1 s, as depicted in Fig. 6a. The switching process between READ states subsequent to each PROGRAM/ERASE cycle is accomplished via the attrition of Na^+ ions in the vicinity of the WS_2/SiO_2 interface. At the same time, the drain is grounded, and the source is biased at 1 V. The device is first set to the OFF state (~10^{-10} A) by implementing a high negative gate voltage ($V_{bg} = -40$ V) pulse. To activate the device, a positive voltage pulse of 40 V for 1 s causes attrition of charges in the WS_2 channel, signified by the ~10^{-6} A current surge. Upon resetting the gate voltage to 0 V, the device persists in a high conductive READ level with a steady OFF current of ~10^{-8} A. The imposition of a similar negative pulse of -40V for 1 s restores the initial OFF state (~10^{-10} A), also called a low conductive READ state. To attain a storage capacity of n-bits, a mem-transistor must comprise no less than 2^n distinct storage levels[42]. These devices can be exploited for a 2-bit storage potential that mandates 4 data levels. Figure 6b depicts four V_{bg} operations implemented to configure our mem-transistor into 4 data states (“00,” “10,” “01,” “11”). The V_{bg} pulses denoted by “00” and “11” correspond to the pulses employed to establish the device into binary “ERASE” and “PROGRAM” states, respectively. However, the V_{bg} pulses for collecting the “01” and “10” state are combinational, consisting two successive pulses of (-40 V, 1 s) and (40 V, 1 s) and vice versa. These operations generate two additional intermediate PROGRAM states with stable READ currents traversing four orders of current magnitudes across the spectrum. The conservation of the corresponding READ states is additionally probed for 2000 s at a steady drain-source bias of 2 V, as depicted in Fig. 6b. By scrutinizing their time-dependent behavior, it can be inferred that ion-gated transistors based on 2D

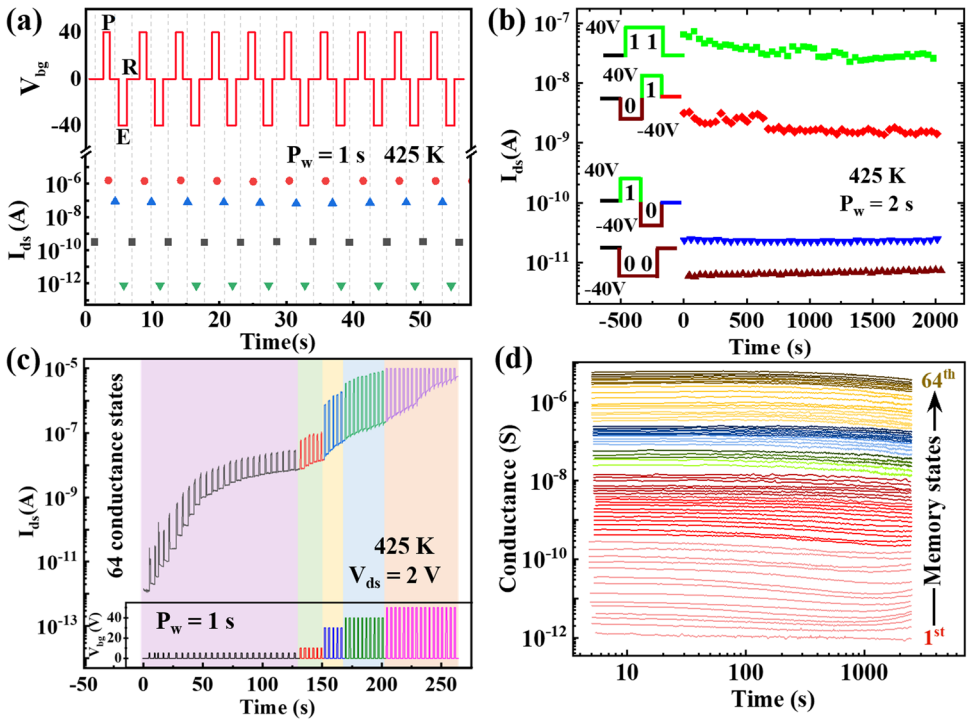

Fig. 6 The dynamic response of ML WS_2 mem-transistors based multibit storage capabilities. a Switching between PROGRAM (P, high current, device ON, red circles) and ERASE (E, low current, device OFF, green triangles) states (lower panel) induced by the application of alternating V_{bg} pulses (±40 V,1 s), upper panel. The READ (R) operations are performed by using $V_{bg} = 0$ V. The high (low) conductive READs are blue triangles (black squares). **b** V_{bg} pulses used for programming the mem-transistor into 4 distinguishable storage states ("00," "01," "10," "11"), i.e., a 2-bit memory device. Retention characteristics of 4 states are also shown for 2000 s at $V_{bg} = 0$ V and $V_{ds} = 1$ V. **c** Transient drain current memory operations by using a combinational gate pulse of various amplitudes, i.e., 5 V, 10 V, 30 V, 40 V, and 50 V, displaying over 64 distinct current levels. **d** The retention of 64 conductance states for more than 1000 s, taken at $V_{bg} = 0$ V, $V_{ds} = 2$ V.

Table 1. Comparison list of memory parameters of various multibit memory device configurations using 2D materials and heterostructures.

Device structure	Active material	Extinction ratio	Retention (s)	Memory states (# of bits)	High temperature application	Ref.
Ionotronic transistor	CVD-grown WS_2	10^6	$>10^3$	64 (6 bit)	150 °C	This work
FGM	MoS_2/hBN/MoS/GDYO/WSe_2	10^7	$>10^4$	8 (3 bit)	–	18
FGM	MoS_2/hBN/2D-RPP	10^4	$>10^3$	22 (4 bit)	–	19
FGM	MoS_2/hBN/Gr	10^2	$>10^4$	4 (2 bit)	–	51
CTM	MoS_2/hBN/GDY/Gr	10^6	$>10^4$	6 (2 bit)	–	17
CTM	MoS_2/GDY	10^8	$>10^4$	10 (3 bit)	–	16
OM	MoS_2/BP/MoS_2	10^7	$>10^4$	11 (3 bit)	–	15
FGM	SnS_2/h-BN/Gr	10^6	$>10^3$	50 (5 bit)	–	14
Tribo-tronic	MoS_2/hBN/MoS_2	10^5	$>10^3$	14 (3 bit)	–	52
FGM	MoS_2/hBN/Gr	10^6	$>10^4$	13 (3 bit)	–	13
CTM	MoS_2/SWCNT network	10^6	$>10^3$	10 (3 bit)	–	11
OM CTM	MoS_2/hBN/Gr	10^6	$>10^4$	18 (4 bit)	–	12
CTM	MoS_2/PbS	2	$>10^4$	4 (2 bit)	–	10
Memristor	Gr/$MoS_{2-x}O_x$/Gr	10	$>10^4$	–	340 °C	53
OM	MoS_2/plasma-treated SiO_2	4700	$>10^4$	8 (3 bit)	–	9
OM	MoS_2/cPVP/AuNPs	10^7	$>10^4$	8 (3 bit)	–	8
Transistor	Plasma-treated MoS_2	10^3	$>10^4$	8 (3 bit)	–	42

FGM floating gate memory, *CTM* charge trap-based memory, *OM* optoelectronic memory, *GDYO* graphdiyne oxide, *2D-RPP* two-dimensional Ruddlesden–Popper perovskite, *Gr* graphene, *GDY* graphdiyne, *SWCNT* single-walled carbon nanotube, *cPVP* crosslinked poly(4-vinylphenol), *AuNP* metallic gold nanoparticle.

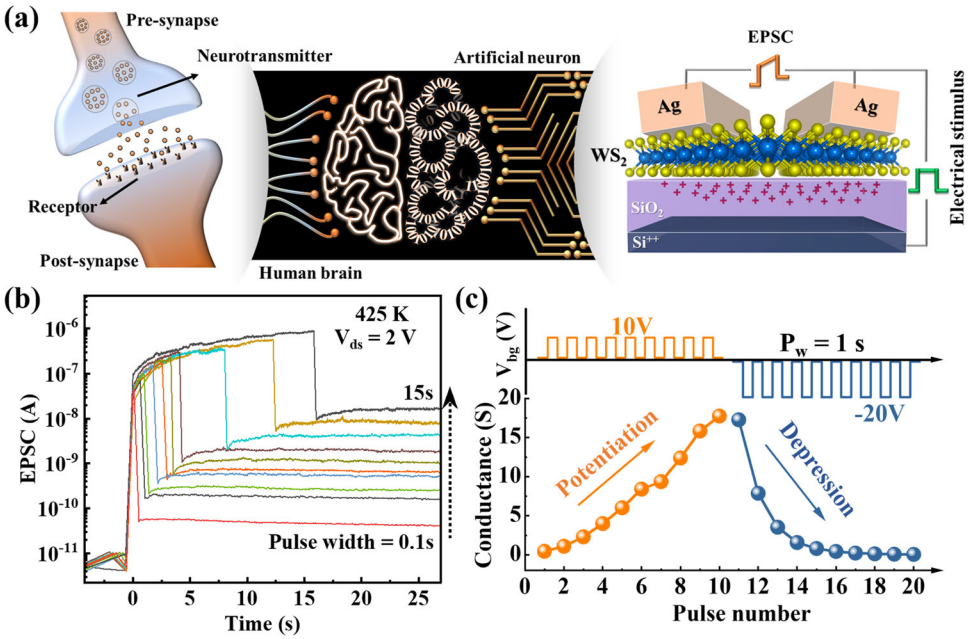

Fig. 7 Synaptic characteristics of ionotronic WS_2 mem-transistors. a Schematic illustration of human and artificial brain synaptic elements. (left: biological synapse operation by pre-synaptic and post-synaptic neurons and right: artificial synapse operation by using the proposed ion-gated WS_2-based mem-transistors). **b** Excitatory postsynaptic current (EPSC) stimulated by gate voltages with an amplitude of 40 V and different duration times (0.1–15 s) showing long-term plasticity. **c** Emulating long-term potentiation (LTP) and depression (LTD) with consecutive identical pulses of (10 V, 1 s), and (-20 V, 1 s), respectively.

materials can cater to the pressing need for high-temperature multi-level storage devices.

The extinction ratios and retention capabilities of these ionotronic WS_2 mem-transistors signify the potential of multibit memory with exceptional storage capacities. Although floating-gate multibit memories based on 2D materials, such as MoS_2, manifest high switching ratios exceeding 10^6, the ungovernable laws of the charge trapping mechanism lead to a restricted storage capability with less than 16 storage levels (4 bits)[17,18]. Nevertheless, the electrolyte-gated transistors exhibit enhanced conductance modulation due to their ion-gating mechanism compared to the electrostatic charge trap phenomena, rendering them suitable contenders for high storage densities[43,44]. We execute several voltage operations to demonstrate the multibit storage potential of our solid-state ion-gated WS_2 mem-transistors. Initially, the device is subjected to repetitive stimulation by a gate pulse of (5 V, 1 s) duration. The phenomenon observed is the gradual increase in storage current with increasing the number of pulses indicating the persistent accumulation of charge carriers in WS_2. Furthermore, we utilize combinational gate pulses of various amplitudes, including 5 V, 10 V, 30 V, 40 V, and 50 V, as depicted in Fig. 6c. This approach yielded 65 distinct storage currents, spanning over six orders of magnitude of current levels, thereby revealing the potential for 6-bit data storage capabilities in our ion-gated WS_2 mem-transistors compared to existing literature[11–17]. Our results, combined with recent studies on multibit memory that use two- and three-terminal device configurations on 2D materials and heterostructures, have been consolidated in Table 1. The table highlights various memory parameters such as retention, extinction ratios, and thermal stabilities.

Notably, our study presents, the capability of achieving such high data storage states (>6 bits) with intriguing memory characteristics at high temperatures (425 K) using NaCl-assisted CVD-grown ML WS_2. Figure 6d depicts the stable nonvolatile retention characteristics of 64 storage states, even after 1000 s of programming using combinational gate pulses. We explicitly observe 64 levels spread across six orders of current, with discernible gaps between consecutive levels. To further confirm the credibility of all the storage states, we calculated the signal-to-noise ratio (SNR) as illustrated in Supplementary Fig. 9. All the computed ratios surpass the critical limit of SNR = 1, anticipating the validity of the 6-bit ionotronic memory in the present study. Furthermore we have estimated a low energy consumption of <1 pJ in case of our WS_2 mem-transistors by modulating several conductance states at pA range. The operation speed can be further improved by using lighter ions such as Li^+ and the programming voltage range can be reduced with a top gate architecture. The device's unwavering dependability and thermal stability can be attributed to the highly effective conductance modulation through ion-gating. Such reliable multi-bit data storage is highly desirable in high performance neuromorphic computing applications[45].

Neuromorphic adaptation with proposed WS2 based mem-transistors

The robust multi-bit storage of our proposed WS_2 mem-transistors, provides an upper hand in achieving reliable neuromorphic computing at high temperatures, as most previous literatures on ion-gated synaptic transistors are based on room temperature neuromorphic performances[7,22–27]. The proposed WS_2 mem-transistor operating at 425 K can be treated as an artificial synapse, and the structural analogy with a biological synapse is illustrated in Fig. 7a. In biological synapses, the information transmits between presynaptic and postsynaptic neurons by sending neurotransmitters across the synapse to dock with receptors on the postsynaptic neuron. If enough neurotransmitters dock with the receptors, a signal is sent down that neuron to generate excitatory post-synaptic current (EPSC). Similarly, in the case of our artificial synaptic device, the gate acts as the presynapse to input modulatory signals through Na^+ diffused SiO_2, while the drain electrode serves as the postsynapse to measure the EPSC from the WS_2 channel.

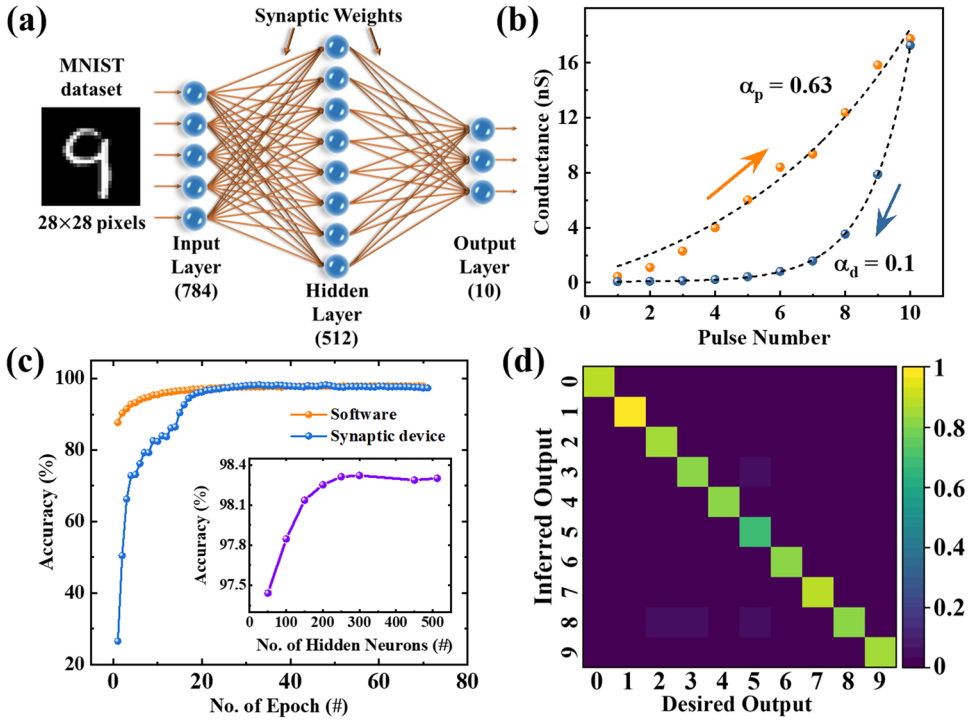

Fig. 8 Hand-written digital image recognition of WS_2 memory devices using ANN. a The schematic of a three-layer ANN structure consisting of the input layer (784 nodes), hidden layer (512 nodes), and output layer (10 nodes) for recognition of MNIST images. **b** The nonlinearity factors (α_p and α_d) are extracted from LTP and LTD characteristics. **c** The recognition accuracy of our synaptic device with respect to training epoch. Software limit is shown for comparison. Inset shows the relation between accuracy with increasing nodes in hidden layers. **d** Confusion matrix showing the digit classification results for hand-written MNIST training datasets. The diagonal form represents most of the digits are correctly classified.

To probe the high-temperature neuromorphic characteristics of WS_2 mem-transistors, sequential voltage pulses of equivalent magnitudes (40 V) and diverse time scales (from 0.1 to 15 s) are exerted on the gate electrode as an external action potential at 425 K. The corresponding excitatory postsynaptic current (EPSC) is measured at a fixed V_{ds} of 2 V. As shown in Fig. 7b, positive voltages applied to the gate terminal significantly increase synaptic weights due to the accumulation of Na^+ ions at the SiO_2/WS_2 interface. The EPSCs exhibit an incremental peak value as the duration of the voltage pulses increases in a manner similar to that of biological excitatory synapses[6]. Moreover, a linear correlation is observed between the duration of the pulse width and the EPSC response, as depicted in Supplementary Fig. 10. Furthermore, we observe negligible decay in post-stimulated read currents attributed to the robust non-volatile EPSC response at 425 K from these ion-gated WS_2 mem-transistors. Long-term potentiation (LTP) and depression (LTD), essential for implementations of ANNs in neuromorphic learning, are also emulated at high temperatures by tuning the conductance states of our ionotronic memory devices with repetitive presynaptic stimulation pulses. As depicted in Fig. 7c, the potentiation triggered using successive voltage pulses of 10 V exhibits near linear synaptic weight changes even at elevated temperatures, which entails the robust ion-gating mechanism in our case. Similarly, a depression characteristic is emulated by employing a series of voltage pulses of −20 V, illustrating an inhibitory post-synaptic current behavior. In this process, we anticipate decumulations of Na^+ back to the original state under negative gate bias.

On the basis of excellent memory capabilities with key synaptic performances, we explore the potency of our WS_2 based memory devices for accurate image recognition by conducting ANN simulations using the open-source Pytorch package[46]. In this approach, a three-layer neural network is constructed to train and test the hand-written MNIST data sets, as shown in Fig. 8a[47]. The input, hidden, and output layers are fully connected through 784 × 512 × 10 synaptic weights. The 784 input neurons correspond to the 28 × 28 pixels input MNIST image, whereas the 10 output neurons correspond to the digit ranging from "0" to "9." Moreover, The multi-bit memory states of our ionotronic device are treated as synaptic weights during the training of 60,000 data sets. Figure 8b shows the nonlinearity factors of LTP and LTD characteristics which are extracted using the following equation[48]

$$G = \begin{cases} \left(\left(G_{Max}^{\alpha} - G_{Min}^{\alpha}\right) \times \omega + G_{Min}^{\alpha}\right)^{1/\alpha} & if\ \alpha \neq 0 \\ G_{Min}^{\alpha} \times \left(G_{Max}/G_{Min}\right)^{\omega} & if\ \alpha = 0 \end{cases} \quad (1)$$

where G_{Max} and G_{Min} represent maximum and minimum conductances, ω is an internal variable and α_p, α_d are nonlinearity coefficients of potentiation and depression, respectively. In our case, the nonlinearity coefficients obtained from the fitted LTP and LTD curves are 0.63 and 0.1 for potentiation and depression, respectively, consistent with near-ideal device cases ($\alpha = 1$). These values are key metrics for evaluating the high classification accuracy rate in neural network simulations. The backpropagation algorithm updates the synaptic weights in our ANN module with cross-entropy loss as the cost function at zero bias condition. A nonlinear rectified linear unit (ReLU) activation function is during information propagation from one layer to another. Each training session is repeated 5 times for 70 epochs, and the mean accuracy is plotted against the number of epochs. As displayed in Fig. 8c, the validation accuracy reached over 90% after training for 20 epochs establishing an excellent recognition rate using our proposed memory devices. Moreover, the maximum accuracy approaches the computational limit of ~98%, which delineates excellent neuromorphic adaptation with superior near-ideal synaptic characteristics in our case, which are also consistent with previous reports[49,50]. The inset shows the improvement of test

accuracy with an increasing number of neurons in hidden layers at a specific epoch. Similar trends are also observed in previous literatures stating the early convergence of our test results with increasing hidden neurons[49]. To further support the high accuracy obtained in our pattern recognition task, we have computed the confusion matrices shown in Fig. 8d. The resulting confusion matrix can be used to evaluate the performance of our ANN model in terms of output class separability. The diagonal elements denote the normalized ANN model predictions that match the true labels in the test data. The observed high diagonal and low off-diagonal values clearly indicate the class separation capability of our device-based ANN implementation. The proposed ion-gated WS_2 mem-transistors in this work offer potential avenues for employing other 2D materials in high-temperature multifunctional nonvolatile memories with extensive storage capacities and future neuromorphic computing applications.

In summary, we demonstrate a mem-transistor device based on ML WS_2 that addresses more than 64 storage states (6 bits) and synaptic operations, emulating biomimetic plasticity. The direct salt-assisted synthesis of ML WS_2 on SiO_2/Si^{++} substrate using a cost-effective CVD method has the potential for scalability. In addition, it is advantageous to directly fabricate three-terminal 2D memory devices with robust ion-gating mechanisms and device functionalities. The Na^+ diffused SiO_2 can be treated as an ionic gating medium instead of dielectric gating at high temperatures due to the thermal activation of mobile Na^+ ions. Using band-bending characteristics, we employ a fingerprint mechanism to address the carrier dynamics under electrostatic doping fluctuations induced by local ion movements. The WS_2-based ionotronic memory is equipped with endurance tests (>400 pulse cycles), 10^5 extinction ratio with stable retention, low device-to-device variations, and 64 distinct nonvolatile storage levels with reliable signal-to-noise ratios using combinational pulses. It also leverages the high-temperature potential memory applications in harsh electronics as demanded in aerospace, military, and automotive industries. We also demonstrate the excitatory postsynaptic current with varying time scales, near linear potentiation, and depression for successful implementation in ANNs. We anticipate that the simple and cost-effective synthesis and fabrication methods presented in this work would substantially enhance the distinctive attributes of WS_2 and other emerging layered 2D materials, thus representing potential for their advancement as scalable memory solutions. The associated bio-inspired synaptic capability delineates a viable path to constructing next-generation 2D mem-transistors towards advanced computing platforms at high temperatures.

METHODS

Growth of ML WS_2

The ML WS_2 is synthesized using a salt-assisted CVD technique in a single-zone tube furnace (Carbolite 1200) with a 2-inch diameter quartz tube, as shown in Supplementary Fig. 1. In this specific experiment, high purity NaCl (99%, SRL) and WO_3 (99.998%, Alfa Aesar) powders are used as metal precursors and sulfur (99.995%, Alfa Aesar) powder is used as a chalcogen source. These precursors are placed in separate alumina boats. The SiO_2 (285 nm)/Si (1×1 cm^2) substrate is cleaned using the ultrasonication method with acetone, isopropyl alcohol, and de-ionized (DI) water, followed by drying with pressurized dry N_2 (99.999%) to eliminate any moisture. Before placing the cleaned substrate face down on the boat with the precursors, the precursor (WO_3+NaCl) height is adjusted to minimize the distance between the precursor and growth substrate to 3 mm, to channelize the sulfur feeding during the growth period. The boat containing the growth substrate and precursors is then moved to the center of the furnace, while the boat containing sulfur is placed upstream. The tube is initially pumped down to 0.2 mbar, and then purged three times with 500 sccm of high-purity Ar (99.999%) to eliminate any oxygen contaminants inside the tube. The system is heated to 900 °C at a ramp speed of 30 °C/min using Ar (75 sccm) as the carrier gas. The pressure inside the tube is maintained at 500 mbar throughout the 10 min growth time. Finally, the system is cooled down rapidly to ambient temperature by partially opening the furnace.

Raman and PL spectroscopy

The Raman spectra are collected with a confocal micro-Raman spectrometer (Renishaw Invia) using a laser excitation wavelength of 532 nm in a backscattering configuration employing an ~100x (NA = 0.8) objective. The laser power on the sample was kept low to avoid local heating. The laser exposure time on the sample is kept fixed for 10 s with 2 accumulations. However, to obtain PL spectra, the exposure time is reduced to 1 s to avoid local heating during the spectral acquisition.

Device fabrication

The ML WS_2 based mem-transistors are fabricated by using a photolithography (Heidelberg μPG 101) system. Initially, the salt-assisted CVD grown WS_2 samples on SiO_2/Si substrate are coated with a positive photoresist (ma-p-1205) by a spin coater (SUSS Microtech) and then baked at 80 °C for 1 min. Under the inspection of a high-resolution microscope, the contact patterns of several channel lengths are exposed on the ML WS_2 flakes with a 405 nm laser in photolithography. The exposed patterns are developed with an alkaline solution (1:4, NaOH:DI water) for 1 min. The sample is then mounted on a thermal evaporation chamber for the deposition of the silver (Ag) electrode followed by dissolution of residual resists in acetone for 10 min, known as lift-off process. The heavily p-doped silicon functioned as the gate electrode and 285 nm SiO_2 functioned as the gate dielectric. Before taking all the electrical measurements for this work, the devices are annealed at 200 °C for 36 h in a high vacuum (~10^{-6} mbar) condition.

Electrical characterization

The fabricated device is mounted on a cryogenic four-probe station (Lake Shore) to probe the top and bottom electrodes. The chamber is maintained at a high vacuum of ~10^{-6} mbar during all the measurements. For electrical characterization, a semiconductor parameter analyzer system (Keithley 4200A-SCS) is used. A high-speed pulse generator module 4220-PGU and measurement unit 4225-PMU integrated within Keithley 4200 system are used for electrical pulse characterization. In order to prevent photo-excitation of charge carriers, all experiments are performed in dark conditions.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Received: 19 May 2023; Accepted: 31 August 2023;
Published online: 09 September 2023

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ACKNOWLEDGEMENTS

S.S., G.K.P., and R.P. thank the Science and Engineering Research Board for partial financial support (CRG/2020/006190). The authors acknowledge the use of the Micro-Raman facility at the central research facility (CRF) of KIIT Deemed to be University, Bhubaneswar.

AUTHOR CONTRIBUTIONS

The project was conceptualized by S.S. and S.K.M. and S.S. supervised the project. S.K.M. and R.P. carried out the CVD growth, device fabrications. S.K.M. performed Raman and PL experiments. S.K.M. and R.P. carried out temperature-dependent transport measurements. S.K.M. and M.C.S. analyzed the experimental data. S.K.M., G.K.P., P.K.S., S.P.D., and S.S. carried out formal analysis and scientific discussions. S.K.M. wrote the manuscript with input from all the authors. The final manuscript was reviewed by all the authors.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41699-023-00427-8.

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