Thesis for the Degree of Doctor of Philosophy

Efficient and Wideband Load Modulated Power Amplifiers for Wireless Communication

Han Zhou

CHALMERS

Microwave Electronics Laboratory
Department of Microtechnology and Nanoscience – MC2
Chalmers University of Technology
Gothenburg, Sweden 2023

Efficient and Wideband Load Modulated Power Amplifiers for Wireless Communication

Han Zhou

ISBN 978-91-7905-941-5

Doktorsavhandlingar vid Chalmers tekniska högskola
Ny serie nr 5407
ISSN 0346-718X

Chalmers University of Technology
Department of Microtechnology and Nanoscience – MC2
Microwave Electronics Laboratory
SE-412 96 Gothenburg, Sweden
+46(0)31-772 1000

Printed by Chalmers Digitaltryck
Gothenburg, Sweden 2023

Abstract

The increasing demand for mobile data traffic has resulted in new challenges and requirements for the development of the wireless communication infrastructure. With the transition to higher frequencies and multi-antenna systems, radio frequency (RF) hardware performance, especially the power amplifier (PA), becomes increasingly important. Enhancing PA energy efficiency and bandwidth is vital for maximizing channel capacity, reducing operational costs, and facilitating integration.

In the first part of the thesis, the bandwidth limitations of the standard two-way Doherty PA are discussed. A comprehensive analysis is provided and the frequency responses of different Doherty combiner networks are presented. Furthermore, a Doherty combiner network is proposed, notable for its inherent broadband frequency and its capacity to account for the influence of output parasitics and packaged components from the active devices. The introduced Doherty combiner network is experimentally verified by a wideband gallium nitride (GaN) Doherty PA operating over $1.6 - 2.7$ GHz.

In the second part of the thesis, an analytically based combiner synthesis approach for the three-stage Doherty PA is proposed and presented. A compact output combiner network, together with the input phase delays, is derived directly from transistor load-pull data and the PA design requirements. The technique opens up new design space for three-stage Doherty PAs with reconfigurable high-efficiency power back-off levels. The utility of the proposed technique is demonstrated by the implementation of a 30-W GaN three-stage Doherty PA prototype at 2.14 GHz. Measurements show that a drain efficiency of 68% and 55% is exhibited at 6- and 10-dB back-off power, respectively.

In the third part, a new PA architecture named the circulator load modulated amplifier (CLMA), is proposed. This architecture utilizes active load modulation for achieving enhanced back-off efficiency. Two active devices are incorporated in this innovative architecture, and a non-reciprocal circulator-based combiner is leveraged. Following this, the sequential CLMA (SCLMA) is introduced, characterized by its ability to enhance back-off efficiency without the necessity of load modulation. GaN demonstrator circuits for both CLMA and SCLMA architectures, whether with dual-input or RF single-input, are designed and fabricated, with excellent performance being measured.

The thesis contributes novel design techniques and architectures to enhance PA efficiency and bandwidth. These findings pave the way for energy-efficient and adaptable RF transmitters in future wireless communication systems.

Keywords: Combiner synthesis, CLMA, Doherty, energy efficiency, GaN, load modulation, microwave, power amplifier, RF, SCLMA, wideband.

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] **H. Zhou**, H. Chang, and C. Fager, "Doherty Power Amplifier Combiner Network for Improved Bandwidth and Efficiency," submitted to *IEEE Transactions on Microwave Theory and Techniques*, Sep. 2023.

[B] **H. Zhou**, J.-R. Perez-Cisneros, B. Langborn, T. Eriksson, and C. Fager, "Design of a Compact GaN Power Amplifier With High Efficiency and Beyond Decade Bandwidth," *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 12, pp. 1439-1442, Dec. 2022.

[C] **H. Zhou**, J.-R. Perez-Cisneros, S. Hesami, K. Buisman, and C. Fager, "A Generic Theory for Design of Efficient Three-Stage Doherty Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 2, pp. 1242-1253, Feb. 2022.

[D] **H. Zhou**, J.-R. Perez-Cisneros, B. Langborn, T. Eriksson, and C. Fager, "A Wideband and Highly Efficient Circulator Load Modulated Power Amplifier Architecture," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 8, pp. 3117-3129, Aug. 2023.

[E] **H. Zhou**, H. Chang, and C. Fager, "Design and Analysis of a RF-input Doherty-like Circulator Load Modulated Amplifier," submitted to *IEEE Microwave and Wireless Components Letters*, Sep. 2023.

[F] **H. Zhou**, H. Chang, and C. Fager, "RF-input Sequential Circulator Load Modulated Amplifier with Extended Efficiency Range," Manuscript.

[G] **H. Zhou**, J.-R. Perez-Cisneros, and C. Fager, "Wideband Sequential Circulator Load Modulated Amplifier with Back-Off Efficiency Enhancement," *IEEE European Microwave Conference*, Milan, Italy, Oct. 2022.

Other Publications

The content of the following papers partially overlaps with the appended papers or is out of the scope of this thesis.

[a] E. Liu***** **H. Zhou***, C. Fager, and H Wang, "A 25 – 40 GHz Three Way Power Amplifier with No Main PA Load Modulation Achieving Broadband Deep Power Back-Off Efficiency Enhancement," submitted to *IEEE International Solid-State Circuits Conference (ISSCC)*, 2024.

***** Equally-Credited Authors (ECAs)

[b] **H. Zhou**, J.-R. Perez-Cisneros, and C. Fager, "Circulator Load Modulated Amplifier: A Non-Reciprocal Wideband and Efficient PA Architecture," *IEEE MTT-S International Microwave Symposium (IMS)*, Atlanta, GA, USA, Jun. 2021.

[c] **H. Zhou**, H. Chang, and C. Fager, "Symmetrical Doherty Power Amplifier with High Efficiency and Extended Bandwidth," accepted for presentation at *IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, Aveiro, Portugal, Nov. 2023.

[d] J. Haider, **H. Zhou**, P. Saad, R. Hou, and C. Fager, "Design and Validation of a Concurrent Dual-Band 1.84/2.65 GHz GaN Doherty Power Amplifier," accepted for presentation at *IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, Aveiro, Portugal, Nov. 2023.

[e] V. Åberg, **H. Zhou**, C. Fager and L. Svensson, "RF PA Predistortion using Non-Linear RF-DACs," *IEEE Nordic Circuits and Systems Conference*, Oslo, Norway, Oct. 2022.

[f] P. Saad, **H. Zhou**, J.-R. Perez-Cisneros, R. Hou, C. Fager and B. Berglund, "Doherty Load Modulation Based on Non-Reciprocity," *IEEE European Microwave Conference*, London, United Kingdom, Apr. 2022.

[g] J.-R. Perez-Cisneros, **H. Zhou**, C. Fager and K. Buisman, "Emulation of Non-Reciprocity applied in Load-Modulated Power Amplifier Architectures using Single Amplifier Load-Pull Measurements," *IEEE European Microwave Conference*, London, United Kingdom, Apr. 2022.

Thesis

[h] **H. Zhou**, "Theory and Design of Efficient Active Load Modulation Power Amplifiers," Chalmers University of Technology, Gothenburg, Sweden, Nov. 2021.

As part of the author's doctoral studies, some of the work has previously been published in [h]. Text, figures, and tables from [h] may therefore be fully or partially reproduced in this thesis.

Notations and Abbreviations

Notations

C_{ds}	Device drain-source capacitance
f	Frequency
ω	Angular frequency
α	Current ratio
β	Normalized input voltage level
β_{B}	Normalized input voltage at the back-off level
γ_{B}	Output power at the back-off levels
η	Drain efficiency
φ	Input current phase delay
θ	Phase delay or transmission line electrical length
I_{m}	Main amplifier output current
$i_{\mathrm{m,M}}$	Maximum current from the main amplifier
I_{a}	Auxiliary amplifier output current
$i_{\mathrm{a,M}}$	Maximum current from the auxiliary amplifier
V_{m}	Main amplifier output voltage
V_{a}	Auxiliary amplifier output voltage
V_{ds}	Drain-source voltage
VGG	Gate bias of transistors
VDD	Drain bias of transistors
P_{DC}	DC power
P_{L}	Power delivered to the load termination
$P_{\mathrm{del,M}}$	Delivered power at the peak power level
$P_{\mathrm{del,B}}$	Delivered power at the back-off power level
R_{L}	Load resistance
R_{opt}	Optimal load resistance
$\Re$	Function that gives the real part of a complex number
y_{4P}	Four-port admittance parameters
Z_{2P}	Reciprocal and lossy two-port output combiner
Z_{3P}	Reciprocal and lossy three-port output combiner
λ	Wavelength

Abbreviations

ACLR	Adjacent Channel Leakage Ratio
ALM	Active Load Modulation
Aux	Auxiliary
CLMA	Circulator Load Modulated Amplifier
CW	Continuous Wave
CM	Continuous-Mode
DEPA	Distributed Efficient Power Amplifier
DLM	Dynamic Load Modulation
DPA	Doherty Power Amplifier
DSM	Dynamic Supply Modulation
DPD	Digital Predistortion
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
GaN	Gallium Nitride
LMBA	Load Modulated Balanced Amplifier
LTE	Long Term Evolution
OFDM	Orthogonal Frequency Division Multiplexing
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
RF	Radio Frequency
SCLMA	Sequential Circulator Load Modulated Amplifier
SLMBA	Sequential Load Modulated Balanced Amplifier
Si	Silicon
CMOS	Complementary Metal-Oxide Semiconductor

Contents

Chapter 1

Introduction

1.1 Motivation

The development of wireless communication technology has changed people's daily lives significantly. Before this technological revolution, many aspects of our day-to-day interactions were bound by physical constraints and distances. Now, with the click of a button, vast oceans are bridged, and distant continents feel like next-door neighbors. The pandemic, an unforeseen and unparalleled challenge, has had a strong impact and influence on the world's socio-economic landscapes. It has not only disrupted routines and norms but also fundamentally altered the way individuals, communities, and even nations interact and function. Ever since the pandemic, many traditional physical activities transitioned to online platforms. Whether it was attending international conferences, engaging in academic workshops, or simply catching up with friends, the virtual realm became the new norm. In [1], it was shown that even though employees are being encouraged to return to the office after the pandemic era, over 40% still choose to work remotely, full-time or several days a week. Faster and more reliable communication is, therefore, expected to be a desire for more and more individuals and societies.

In 2021, a 3-fold growth in global mobile data traffic was observed when compared to the year 2018. With respect to the global population, this growth represented 51% in 2018 and continued to reach 66% penetration in 2023 [1, 2]. Furthermore, a tripling of data traffic from 2023 to 2028 is anticipated [3], as depicted in Figure. 1.1. By the end of 2023, a noticeable shift in mobile data traffic was documented. The contribution of the fifth-generation system (5G) to this traffic reached 15 percent, a significant rise from the 9 percent recorded in the previous year. This evolving trend in 5G utilization suggests a rapid adoption rate and underscores the growing reliance on this technology. Looking forward, projections indicate a continued upward trajectory. The share of 5G in mobile data traffic is anticipated to soar, reaching an estimated 66 percent by the year 2028 [3]. This substantial trend can be attributed largely to the ubiquitous connectivity facilitated by devices like smartphones and tablets, as well as innovations like the Internet of Things, smart homes and cities, autonomous vehicles, wearable technology, and more.

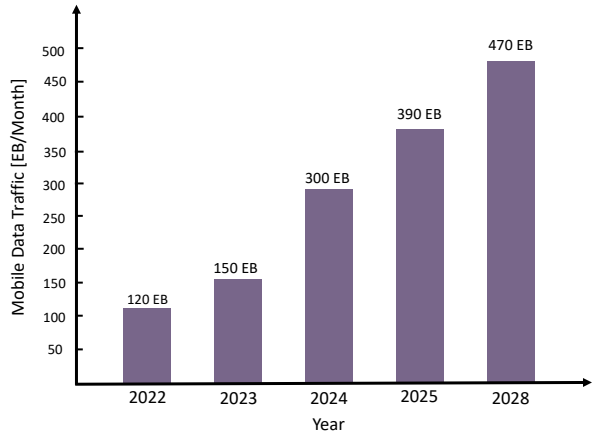


Figure 1.1: Projection of global mobile data traffic [3]

As the demand for mobile data traffic escalates, the development of wireless communication infrastructure faces various challenges [4–8]. Central to this is the performance of microwave transmitters, the cornerstone of any radio base station and link equipment. There are two main performance aspects of the microwave transmitter to enable high capacity, low cost, and high speed of the wireless connections [5]: energy efficiency and bandwidth. Energy efficiency is perhaps the most important property of the transmitter because its power consumption corresponds to a large part of the overall mobile network operational cost [9]. Moreover, higher power consumption of transmitters increases the system complexity considerably since cooling equipment is often required to deal with heat dissipation. The cooling equipment draws a significant amount of power, which further multiplies the energy consumption because of low efficiency. Meanwhile, bandwidth performance is another important attribute. The scarcity of the frequency spectrum and the need for frequency planning has resulted in a widespread of carrier frequencies, therefore it is preferable if the transmitter can cover more frequency bands to reduce the system complexity and cost.

The essential building block of all mobile microwave transmitters is the power amplifier (PA). Its primary function is to amplify the signal power, thereby achieving the necessary system performance to ensure the desired signal coverage. Importantly, it should be emphasized that PAs constitute the most energy-intensive components within radio base stations, typically accounting for 50% to 80% of the total energy consumption [9–11]. Therefore, the critical performance aspects mentioned earlier, namely energy efficiency and bandwidth, have a profound influence on the PA designs.

1.2 Power Amplifier Design Challenges

The growing need for greater data throughput in modern wireless communication systems necessitates the utilization of more complex modulation schemes. Consequently, this results in communication signals characterized by a high peak-to-average-power ratio (PAPR). To deal with these high-PAPR communi-

cation signals, PAs should be designed to deliver high efficiency across a large range of output power levels [6, 12].

Furthermore, it is crucial for PAs to possess the capability to operate across larger bandwidths to accommodate various signal bandwidths and diverse frequency bands. As the demand for higher communication data rates continues to grow, it becomes increasingly important for PAs to inherently support wideband operation. This inherent wideband capability ensures their efficiency remains consistent across an expanding signal frequency range. A strategic decision must be made: either deploy distinct PAs for each frequency band or opt for a more streamlined approach with fewer, yet highly versatile, broadband PAs to minimize transmitter complexity. This underscores the necessity for PAs to possess wideband capabilities capable of accommodating a wide range of carrier frequencies.

The linearity performance of the PA is another crucial attribute. The in-band distortion compromises the quality of the transmitted signal, subsequently degrading the overall communication performance within its dedicated frequency band. Conversely, out-of-band spectral regrowth poses its own set of challenges, potentially leading to unintended interference with other wireless systems operating in adjacent frequency bands. Contemporary communication systems, especially the fourth-generation (4G) and 5G systems, impose stringent linearity criteria concerning spectral regrowth and in-band distortion. However, when a PA operates at its peak efficiency, it often exhibits pronounced nonlinearity. As a remedy, linearization techniques, especially digital pre-distortion (DPD), are frequently employed to improve the linearity of the PA while preserving high power and efficiency [13, 14].

1.3 Efficiency Enhancement Techniques

As previously emphasized, to efficiently transmit high-PAPR communication signals, PAs should be designed to ensure high efficiency over a large output dynamic range. Over the years, substantial efforts have been dedicated to researching strategies to enhance PA efficiency, particularly at its power back-off levels. Essentially, two predominant types of efficiency-enhancement architectures have emerged: supply modulation and load modulation.

1.3.1 Supply Modulation

The supply modulation PA operates on the principle of reducing the drain supply voltage when the output power is backed off, thereby maintaining high efficiency over a large output dynamic range. In this architecture, an additional control path, working in conjunction with the PA path, dynamically modulates the supply voltage of the PA path based on the signal envelope. L. Kahn first introduced the concept of envelope modulation in 1952 with the envelope elimination and restoration (EER) technique [15]. Characterized as a polar transmitter, in EER, the PA receives a phase-only modulated input signal, while the modulation of the supply voltage introduces the amplitude modulation to the output signal. Building upon this foundation, the envelope tracking (ET) technique was developed in 1983 by A. Saleh and D. Cox [16]. Unlike its predecessor, ET feeds both phase and amplitude to the PA. Simultaneously, the

supply voltage is modulated dynamically in sync with the envelope variation of the input signal. The ET technique is the most widely adopted form of supply modulation nowadays. Notably, the efficacy of supply modulation PAs is largely constrained by the characteristics of its envelope amplifier. Factors such as bandwidth, efficiency, and dynamic range of the envelope amplifier directly influence the performance of supply modulation PAs.

1.3.2 Load Modulation

The load modulation technique can be divided into two types of architectures. One is referred to as dynamic load modulation [17, 18], where tunable elements, such as switches or varactors, are used to modulate the load impedance of the PA as the signal envelope varies. The other is referred to as active load modulation. Unlike dynamic load modulation, the active load modulation utilizes active current injection to modulate the load impedance. The active load modulation architectures employ multiple PAs that interact with each other through an output combiner network to enhance the PA back-off efficiency. Two of the most common active load modulation architectures are the outphashing and Doherty PA. The outphasing PA, originally introduced by H. Chireix in 1935 [19], uses two nonlinear outphased amplifiers with constant envelopes to achieve load modulation. The Doherty PA, which was first proposed by W. Doherty in 1936 [20], relies on the active current injection from the main (Main) and auxiliary (Aux) amplifiers, together with a static phase delay between them, to realize the load modulation. The Doherty PA is constructed using an analog input power splitter, appropriate phase delays, gate bias settings for the sub-amplifiers, and an output combiner network. With its simplified design and the absence of the need for dual/multiple inputs or external control circuitry, the Doherty PA stands out as a widely adopted architecture, setting it apart from others such as the outphasing PA or the dynamic load modulation PA.

The combination of efficiency enhancement and relatively simple circuit implementation has made the Doherty PA by far the most attractive architecture in cellular base stations [21, 22]. However, the Doherty PA does have its drawbacks, notably a restricted radio frequency (RF) bandwidth, which is attributed to the transistor parasitics and the combiner network [23]. Additionally, as the back-off level increases, it has been observed that the efficiency of the Doherty PA degraded between its peak and back-off power levels. Addressing these challenges, recent innovations have given rise to several promising PA architectures with high efficiency and wideband operations. These include the distributed efficient power amplifier (DEPA), introduced in [24], and the load modulated balanced amplifier (LMBA) proposed in [25], the sequential LMBA (SLMBA), as first presented in [26, 27] etc.

In general, various active load modulation architectures offer distinct advantages and present unique challenges when compared to each other. A common challenge shared among all these architectures is the need to develop a practical method for generating current profiles with minimal complexity. Additionally, there is a shared goal of creating an efficient combiner with low signal loss, wide bandwidth, and compact form factor, among other desirable attributes.

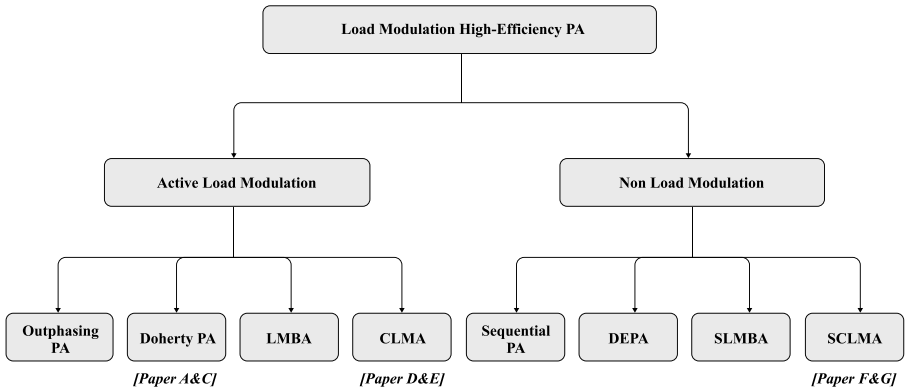


Figure 1.2: Thesis contribution and outline in block diagrams.

1.4 Thesis Scope and Outline

This thesis focuses on the theory, design, and practical implementation of high-efficiency PAs, with a particular emphasis on their application in transmitting modern communication signals with a large PAPR. It introduces novel operational modes, circuit topologies, and design methods, with a primary focus on the load modulation category of PA efficiency enhancement techniques, as illustrated in Figure 1.2. Overall, the thesis presents promising approaches for enhancing performance in high-efficiency PAs, including improvements in back-off efficiency, bandwidth, compactness, and design methodology.

In Chapter 2, the bandwidth limitations inherent in the standard two-way Doherty PA are discussed. It offers a thorough analysis, contrasting various two-way Doherty PA configurations. The chapter then illustrates a generic combiner synthesis method and its potential to improve the efficiency of class B/C Doherty setups. Following this demonstration, the frequency responses of different Doherty combiner networks are illustrated. Moreover, the chapter introduces a Doherty combiner network with inherent broadband frequency and capability to account for the influence of output parasitics and packaged components originating from the active devices, as elaborated in [Paper A & B].

Chapter 3 introduces and reviews the operation of the three-stage Doherty PA, in order to cope with the evolving demands of modern communication signals with increasingly higher PAPR. Based on [Paper C], we present a comprehensive theory for the design of a three-stage Doherty PA. A load-pull-based three-port combiner synthesis method is introduced. This method paves the way for the design of an ultra-compact, low-loss combiner network for the three-stage Doherty PAs. Experimental measurements from our proof-of-concept prototype confirm the capability of the fabricated circuit to provide profound power back-off efficiency enhancements with an ultra-compact combiner network.

Chapter 4 proposes a novel PA architecture named the CLMA, which utilizes active load modulation to achieve back-off efficiency enhancement. First presented in [Paper b], this innovative architecture incorporates two active devices and leverages a non-reciprocal circulator-based combiner. The operational principles are elaborated in detail, leading to the design of a wideband demonstrator circuit with dual-input and continuous-mode (CM)

matching, as presented in [Paper D]. Additionally, a single RF-input CLMA has been fabricated and characterized, demonstrating promising results, as shown in [Paper E].

Chapter 5 discusses the inherent bandwidth constraints of the active load-modulated PA architectures, especially when considering deep power back-off scenarios. This chapter also traces the evolutionary trajectory of PA architectures that aim to boost back-off efficiency without relying on load modulation. Building on foundational principles and the previously introduced CLMA architecture, a novel sequential CLMA (SCLMA) architecture is proposed. To validate this proposed concept, two demonstrator circuits are presented: one, as detailed in [Paper G], demonstrates a dual input topology with wideband performance; the other, presented in [Paper F], emphasizes a single RF input with efficiency enhancement during deep back-off scenarios.

Chapter 6 concludes the thesis and discusses future work.

Chapter 2

Two-Way Doherty Power Amplifiers

In the previous chapter, it was mentioned that many PA architectures have been proposed to enhance the PA back-off efficiency, and thereby improve the average efficiency of microwave transmitters with modern communication signals. Among those architectures, the Doherty PA is established as one of the most adopted architectures deployed in cellular base stations.

This chapter aims to present a comprehensive analysis and comparison of different two-way Doherty PA configurations. We will then illustrate the black-box combiner synthesis method and its potential to enhance the efficiency of class B/C Doherty configurations. Following this, the frequency responses of the Doherty combiner network, derived using this method, will be illustrated. A subsequent discussion will address their associated trade-offs. Furthermore, we introduce a Doherty combiner network with inherent broadband frequency and the ability to account for the influence of output parasitic and packaged elements arising from the active devices.

2.1 Conventional Doherty PAs

The two-way Doherty PA was first introduced in 1936 [28]. Figure 2.1 illustrates the fundamental configuration of this classical implementation, which consists of an output combiner with a quarter-wavelength ($\lambda/4$) transformer and a 90-degree input phase delay. The essence of Doherty's operation lies in load modulation at the output plane of its Main amplifier, achieved through the active current injection from the Aux amplifiers. Typically, this modulation entails operating the Main amplifier in class-B mode and the Aux amplifier in class-C mode. At lower drive levels, the Aux amplifier remains off. As the drive level increases, the Aux amplifier gradually enters conduction, leading to a progressive rise in the magnitude of the current.

Figure 2.1 illustrates the commonly adopted conventional two-way Doherty PA configuration, where the Main and the Aux amplifiers are combined via a $\lambda/4$-transmission line with a characteristic impedance $Z_{\mathrm{T}} = R_{\mathrm{opt}}$ at the output of the Main amplifier and connected to a load $R_{\mathrm{L}} = \beta_{\mathrm{B}} R_{\mathrm{opt}}$ with R_{opt}being

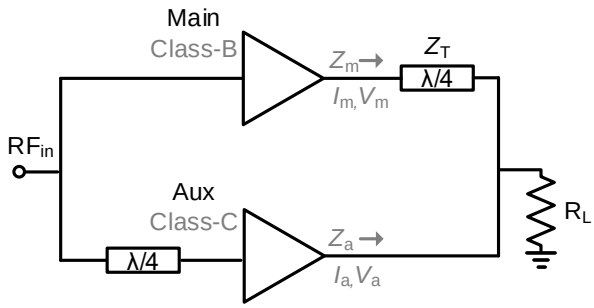
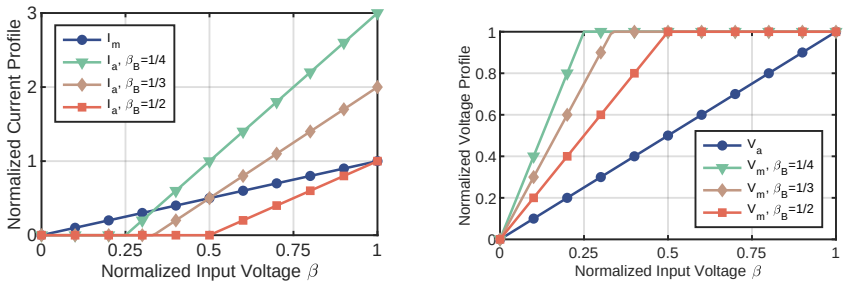
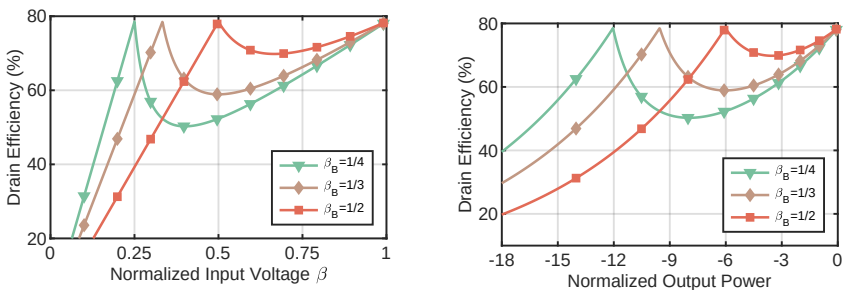


Figure 2.1: The conventional two-way Doherty PA.



(a) **(b)**

Figure 2.2: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the two-way Doherty PA versus normalized input voltage, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) **(b)**

Figure 2.3: Drain efficiency of the two-way Doherty PA versus (a) normalized input voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.

the optimum class-B load impedance. Meanwhile, the input consists of a power splitter and another $\lambda/4$ transmission line at the Aux amplifier branch to provide the equal phase delay through the two amplifier paths.

Figure 2.2 presents the current and voltage drive profiles of the Main and Aux amplifiers from the conventional two-way Doherty PA with different back-off levels (β_{B}). The current profiles are normalized to the maximum saturated current and the voltage profiles are normalized to the drain-source bias voltage (V_{ds}). From Figures 2.2 and 2.3, it is evident that enhancing the high-efficiency back-off power level of a two-way Doherty PA requires an increased Aux

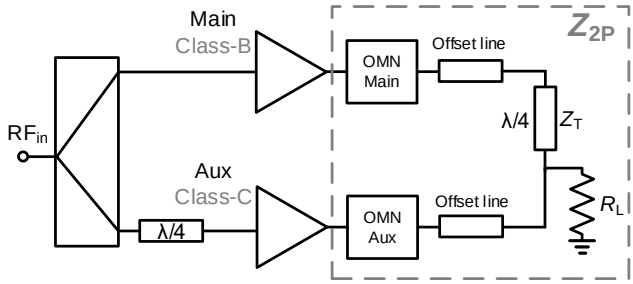


Figure 2.4: Typical realization of a conventional two-way Doherty PA.

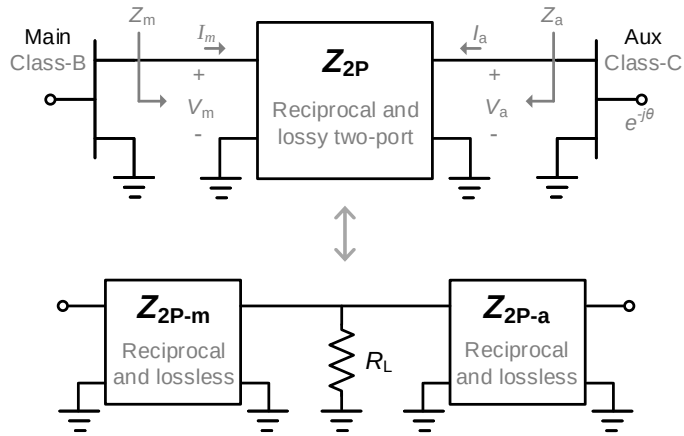


Figure 2.5: Block diagram of the conversion from the reciprocal lossy two-port combiner network to the reciprocal lossless three-port network terminated with a resistive load.

current. In its standard form, the two-way Doherty PA [20], demonstrates efficiency improvements at the 6-dB output power back-off level and demands identical fundamental currents from both Main and Aux amplifiers at the peak drive level [29–36]. In contrast, the asymmetrical two-way Doherty PA, as described in [37–39], typically employs Aux amplifiers of varying sizes to facilitate the extension of the high-efficiency output power back-off range. It is crucial to recognize that the fundamental operating principle underlying the N-way Doherty PA [40] is the same as that of the asymmetrical two-way Doherty PA. The only difference is that the N-way Doherty PA uses multiple Aux amplifiers to achieve a higher Aux current, thereby increasing the high-efficiency back-off range. It should be stressed that, as presented in Figure 2.3, the asymmetrical two-way Doherty PA exhibits a significant drop in efficiency in the regions between the efficiency peaking points, especially for large output power back-off levels. To address this problem, the three-stage Doherty PA will be demonstrated and analyzed in Chapter 3.

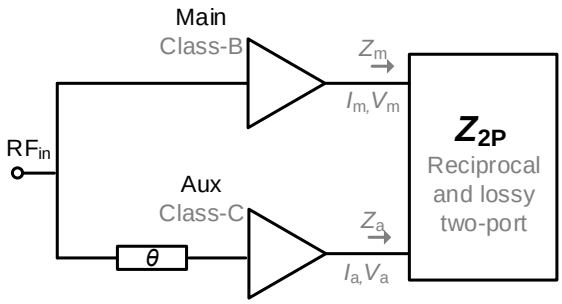


Figure 2.6: Block scheme of the generalized two-way Doherty PA. The lossy and reciprocal two-port output combiner network is denoted as $\mathbf{Z_{2P}}$.

2.2 Black-Box Doherty PA Designs

2.2.1 Overview

The passive output combiner network is a critical component of Doherty PA as it governs the interaction between different amplifier paths and the resulting modes of PA operation. This network also plays a significant role in enhancing the back-off efficiency range and enabling carrier and modulation bandwidths. Figure 2.4 shows a typical realization of a conventional two-way Doherty PA, where additional offset lines and matching networks at the output of the Main and Aux amplifiers are often adopted to accommodate the non-ideal behavior of realistic transistors at microwave frequencies. By simply comparing Figure 2.1 with Figure 2.4, it is clear that the implementation of the Doherty PA plays an important role in its overall performance.

To fully utilize the transistor capabilities, in [41], the black-box combiner synthesis method was proposed to synthesize Doherty combiner networks by specifying the desired output load impedance from large-signal load-pull data. An analytical approach was then used to determine the phase shifts, lossless combiner networks, and an external load resistor, which opens up new design space, as illustrated in Figure 2.5. The combiner synthesis approach was further expanded for improving Doherty linearity [42] and increasing Doherty PA-antenna integration [43, 44] in a microwave transmitter. Additionally, the combiner synthesis approach is well-suited for millimeter-wave integrated circuit designs due to its lower insertion loss and compactness [45–47]. Nevertheless, it is worth noting that the adoption of the black-box approach in Doherty PA design has predominantly been confined to narrow-band applications.

2.2.2 Theory

A generic configuration of the two-way Doherty PA is illustrated in Figure 2.6, comprising a Main amplifier and an Aux amplifier. These amplifiers are combined via a passive output combiner, paired with an input phase shifter to ensure a proper phase delay between the two branches. The fundamental working principle of the two-way Doherty PA lies in modulating the load impedance seen by the class-B biased Main amplifier. This modulation is accomplished via active current injection from the class-C biased Aux amplifier.

Therefore high efficiency can be maintained over a large range of output power.

For the evaluation of the generic two-way Doherty PA, we assume that the Main and Aux transistors are modeled as ideal piece-wise voltage-controlled linear current sources with zero knee voltage. Under this assumption, higher harmonic components are short-circuited, and only the fundamental component is considered, corresponding to the ideal class-B operation. The same drain bias and upper drain voltage limit are used for both the Main and Aux amplifiers. Note that the above assumptions are adopted in the subsequent theoretical analysis throughout the entire thesis.

The Main and Aux amplifiers are represented by current sources having fundamental output currents I_{m} and I_{a}, respectively, that depend on the input voltage drive level ($0 \leq \beta \leq 1$) as

$$I_{\mathrm{m}} = \beta i_{\mathrm{m,M}} \tag{2.1}$$

$$I_{\mathrm{a}} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{\mathrm{B}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B}}}{1 - \beta_{\mathrm{B}}}\right) i_{\mathrm{a,M}} \cdot e^{-j\theta}, & \beta_{\mathrm{B}} \leq \beta \leq 1 \end{cases} \tag{2.2}$$

where $i_{\mathrm{m,M}}$ and $i_{\mathrm{a,M}}$ are the maximum fundamental current from the Main and the Aux amplifiers, respectively.

Furthermore, the analysis also assumes a representation where the load is initially merged with the Doherty output combiner into a reciprocal and lossy two-port combiner network. The realization of the actual combiner network involves a conversion from the lossy two-port network into a lossless three-port network terminated with a purely resistive load. The impedance parameters of the reciprocal and lossy two-port combiner, $\mathbf{Z_{2P}}$, are derived using ideal current source models. The voltages and currents at the output of the Main and Aux amplifiers are related through $\mathbf{Z_{2P}}$ as

$$\begin{bmatrix} V_{\mathrm{m}} \\ V_{\mathrm{a}} \end{bmatrix} = \mathbf{Z_{2P}} \begin{bmatrix} I_{\mathrm{m}} \\ I_{\mathrm{a}} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{12} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{\mathrm{m}} \\ I_{\mathrm{a}} \end{bmatrix} \tag{2.3}$$

where $Z_{12} = Z_{21}$ since the network is reciprocal.

The amplitude of the output voltage from the Main amplifier should be kept constant and equal to its drain-source bias voltage V_{ds} all over the higher power region (when $\beta_{\mathrm{B}} < \beta \leq 1$) to guarantee full utilization of its voltage swing capability, thereby ensuring high-efficiency operation. Assuming that the optimal impedance of the Main amplifier is R_{opt}, the optimal impedance of the Aux impedance is R_{opt}/α, where $\alpha = i_{\mathrm{a,M}}/i_{\mathrm{m,M}}$ is the current ratio between the Main and Aux amplifiers. It is then possible to obtain the impedance parameters of the output combiner, $\mathbf{Z}_{\mathrm{2P}}$ as

$$\begin{cases} Z_{11} = \dfrac{R_{\mathrm{opt}}}{\beta_{\mathrm{B}}} \\ Z_{12} = Z_{21} = \left(1 - \dfrac{1}{\beta_{\mathrm{B}}}\right)\left(\dfrac{R_{\mathrm{opt}}}{\alpha}\right) e^{j\theta} \\ Z_{22} = \left(\dfrac{1}{\beta_{\mathrm{B}}} + \alpha e^{-j2\theta} - 1\right)\left(\dfrac{R_{\mathrm{opt}}}{\alpha^2}\right) e^{j2\theta} \end{cases} \tag{2.4}$$

The condition requiring that the lossy and reciprocal two-port network be convertible into a lossless and reciprocal three-port network, while the third port is terminated by a resistive load, imposes a particular constraint [41]:

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\}. \tag{2.5}$$

Additionally, the output power dynamic range γ can be defined as

$$\gamma = \frac{P_{\text{del,M}}}{P_{\text{del,B}}} \tag{2.6}$$

where $P_{\text{del,M}}$ is the maximum delivered power and $P_{\text{del,B}}$ is the back-off power level where the second efficiency peak occurs. It is then important to mention that, to satisfy the law of power conservation, the relation between the current ratio and the output power dynamic range should be

$$\gamma = \frac{1+\alpha}{\beta_{\text{B}}}. \tag{2.7}$$

Based on the given boundary condition, the expression of θ can be determined as

$$\theta = k\pi \pm \arcsin\sqrt{\frac{\beta_{\text{B}}\left(\alpha - \beta_{\text{B}} + 1\right)}{1-\beta_{\text{B}}^2}} \tag{2.8}$$

where k represents any integer number.

It is crucial to emphasize that the analytical expression for θ reveals the presence of two distinct solution sets for achieving Doherty load modulation. Notably, the choice of $k = 1$ is particularly advantageous, as it contributes to a more compact combiner design. The parameters associated with the generic two-port network $\mathbf{Z}_{\text{2P}}$ mentioned earlier can be adapted to different Doherty drive profiles. The configuration of the combiner network, which is derived based on these parameters, results in varying values for θ. For a more comprehensive understanding and design formulas related to generic combiner synthesis, one can refer to [41, 48].

2.2.3 Discussion

In Doherty PA configurations, it is widely recognized that the Aux amplifier, when operating in class-C mode, yields a reduced fundamental current component compared to its class-B-biased Main amplifier counterpart [49]. This requires feeding a higher input power to the Aux amplifier. Such a scenario leads to an uneven input splitter, thereby escalating the complexity of the circuit and causing an overall reduction in gain. Consequently, employing identical amplifier cells in conjunction with a fixed combiner network would result in degraded gain and thus power added efficiency (PAE) performance.

To provide a thorough analysis of the performance of a two-way class B/C Doherty PA, Figure 2.7 illustrates two cases characterized by a reduced Aux current ($\alpha = 0.8$). In both cases, it is assumed that the input power is equal and the transistor size remains identical. As shown in the figure, Case I presents the theoretical performance of the two-way conventional Doherty PA when $\beta_{\text{B}} = 0.5$ and $\alpha = 0.8$. This illustration indicates that the reduced auxiliary

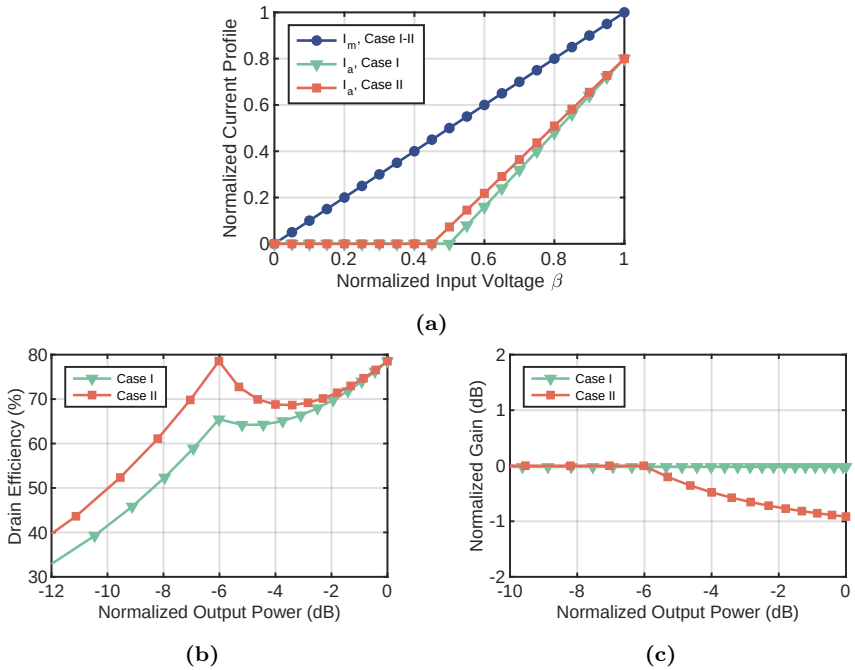


Figure 2.7: Comparison between the conventional (Case I) and black-box (Case II) Doherty PA. (a) The current drive profiles, (b) the ideal efficiency, and (c) the normalized power gain versus the output back-off power level.

current correlates with a drop in back-off efficiency. To maintain high back-off efficiency with $\alpha = 0.8$, the black-box Doherty approach is employed, as shown in Case II. A θ value of $\pi/3$ and $\beta_{\mathrm{B}} = 0.45$ are calculated using equations (2.7) and (2.8). Consequently, Case II can consistently sustain high efficiency at a 6 dB back-off power level.

In essence, the black-box Doherty PA methodology can uphold a predetermined high-efficiency back-off level. This proves advantageous, especially in a class B/C Doherty configuration where the peak Aux current is reduced compared to the Main current. Nevertheless, this approach encounters gain compression, leading to a decline in linearity. Furthermore, its bandwidth performance is also compromised, and this aspect will be discussed in more detail in the subsequent sections.

2.3 Wideband Doherty PAs

2.3.1 Overview

The Doherty PA bandwidth extension has been a focal point in research over the past decade [50]. Various theories and design methodologies have been introduced to enhance the bandwidth capability of Doherty PAs. In general, the bandwidth constraints of Doherty PAs are primarily caused by two factors: the transistor parasitics and the frequency response of the Doherty combiner.

To address the issue of transistor parasitics, researchers have widely em-

ployed parasitic compensation strategies alongside absorption networks. These techniques, as illustrated in [30, 51, 52], aim to alleviate the challenges posed by the device parasitics. The frequency capability enhancement of the Doherty PA, on the other hand, demands a redesign of the Doherty combiner. This is due to the inherent bandwidth restrictions that result from the load modulation network. The difficulty of this challenge lies in reducing the transformation ratio of the Doherty impedance inverter [53]. To address this, researchers have introduced two main categories of methods.

The first category involves employing asymmetrical drain bias voltages for the Main and Aux amplifiers [54–56]. This approach ensures that the load impedance of the Main amplifier becomes frequency-independent at back-off power levels. However, it does come at the cost of reduced power utilization due to the substantial voltage difference between the Main and Aux transistors.

The second category of methods focuses on engineering solutions to broaden the frequency response of the Doherty combiner. These solutions encompass various techniques, such as post-matching structures with low-order impedance inverters [31], complex combining loads [57], transformer-less load modulation networks [58], CM operation [59], and integrated compensating reactance [32]. These techniques aim to optimize the impedance-matching condition while considering the output parasitic effects of the Doherty PA. Despite the progress achieved with these methods, the fundamental frequency limitation of the Doherty PA persists due to the inherent constraints of the load modulation network structures.

In an attempt to overcome this limitation, a Doherty load modulation network was introduced in previous work [60–62]. This novel approach utilizes three $\lambda/4$ transmission lines, effectively breaking the inherent bandwidth limitations of the load modulation network. However, a primary challenge associated with this method is the significant efficiency variations within the operating bandwidth, primarily driven by the effects of parasitics and packaged elements from the high-power packaged gallium nitride (GaN) transistors.

2.3.2 Combiner Frequency Response Analysis

The parameters for the black-box combiner network can be derived to solve for different Doherty drive profiles. When these parameters are employed, the resulting Doherty combiner network demonstrates varying values for θ. Specifically, when

$$\beta_{\mathrm{B}} = \frac{1}{1+\alpha} \tag{2.9}$$

the solutions for θ are calculated to be $\pi/2$ and $3\pi/2$, based on equation (2.8), given that $k = 1$. Figure 2.8 illustrates three specific combiner examples. It is worth noting that for $\theta = \pi/2$, the Doherty combiner network (A) represents the conventional Doherty configuration. Conversely, when $\theta = 3\pi/2$, the combiner network (C) is composed of three $\lambda/4$ transmission lines, corresponding to the network introduced in [60–62]. Meanwhile, Combiner B serves as an example for intermediate θ values that deviate from $\theta = \pi/2$ and $\theta = 3\pi/2$. It should be stressed that Combiner B represents the solution when synthesizing the combiner for maximized back-off efficiency with a class B/C Doherty PA possessing a reduced current ratio [63, 64].

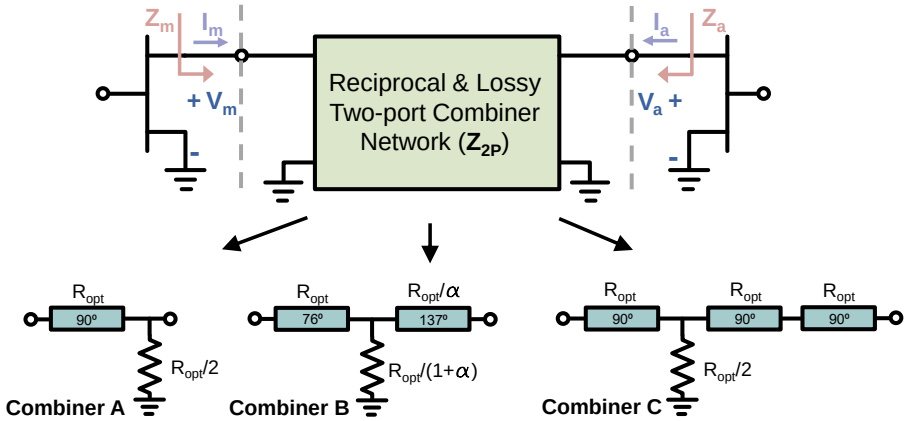


Figure 2.8: Illustration of the Doherty combiner synthesis technique with three explicit example combiner networks.

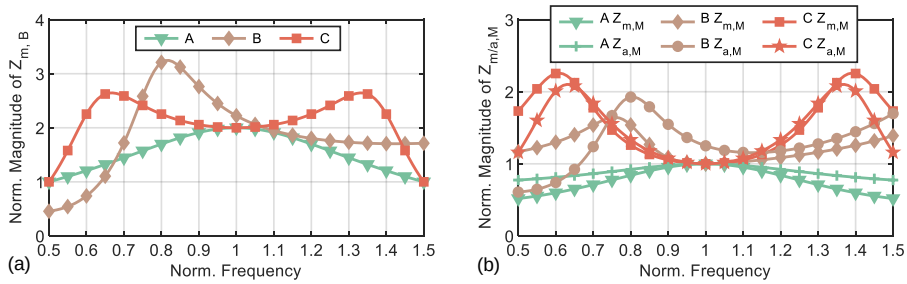


Figure 2.9: Impedance magnitudes seen by the main and auxiliary amplifiers with the Doherty Combiner A-C at (a) the back-off power level and (b) the maximum power level.

The frequency response for the three types of Doherty combiner networks is depicted in Figure 2.9. This illustrates the magnitude of impedances at the outputs of both the Main and Aux amplifiers as a function of the normalized frequency, at both back-off and peak power levels. The plot shows that Combiners A and B possess a narrower bandwidth than Combiner C. It can be noticed that Combiner B clearly demonstrates an asymmetrical response with respect to frequency, both at back-off and peak power levels, underscoring its significant frequency dependence.

To summarize, for a symmetrical class B/C Doherty configuration, Combiner B, with θ obtained from (2.8), is the optimal topology for achieving maximized back-off efficiency. However, its drawbacks include gain compression and pronounced frequency dependence, which limit its suitability for broadband and linear applications. Notably, the bandwidth capability of Combiner C surpasses that of Combiner A [60–62]. This establishes Combiner C as the preferred Doherty combiner for broad bandwidth implementations.

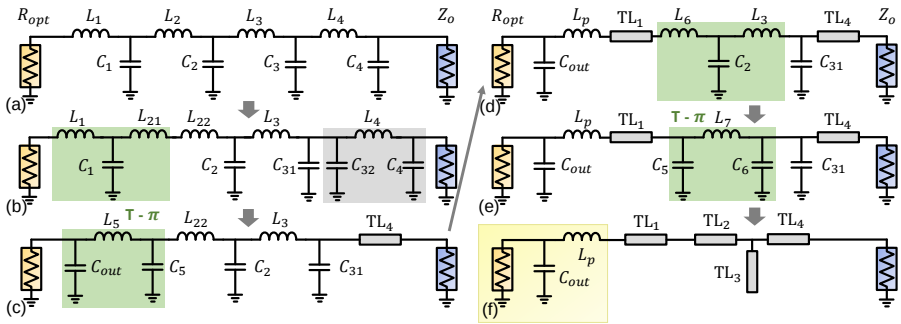


Figure 2.10: The modified low-pass matching network includes transistor output parasitic and packaged elements.

2.3.3 Combiner Practical Implementations

Transistor output equivalent model

It is essential to emphasize that the output characteristics of a packaged GaN transistor can be effectively represented by a current source with a shunt capacitor (C_{ds}) and a series inductor (L_{p}). For strategies involving wideband matching, the matching network needs to match from the system characteristic impedance to the optimal impedance (R_{opt}) of the active device [65]. Additionally, it should properly absorb the active device's parasitic capacitance and packaged inductance. An illustrative design example can be found in [Paper B]. This example employs a filter-based matching network [66–69] to one that absorbs transistor parasitics and packaged elements, leading to an exceptionally broad bandwidth. Considering these factors, it is vital that the Doherty combiner network can properly mitigate the effects of the parasitic capacitor C_{ds} and the packaged inductor L_{p} over the target design frequency.

Tee-line combiner network

In [Paper A], it is shown that the Tee-line network can effectively represent a $\lambda/4$ transmission line. Based on this insight, we adopted this topology for the outputs of both the Main and Aux amplifiers. This choice leads to a Doherty combiner configuration comprised of two Tee-line-based networks with an additional $\lambda/4$ transmission line, as shown in Figure. 2.11. Apart from the broad bandwidth capabilities inherent to this topology, the Tee-line-based combiner network offers the added advantage of direct drain biasing for the active device. This is facilitated by the shunt transmission line connection to the ground, leading to a more compact design. Furthermore, the proposed Tee-line-based Doher combiner network is able to effectively absorb the transistor parasitic capacitance and packaged inductance as illustrated in Figure 2.12.

2.3.4 Circuit Realization and Results

To validate the proposed Doherty combiner network, in [Paper A], we constructed a prototype circuit based on the theoretical framework and design methodology discussed earlier. For the active devices employed for both the

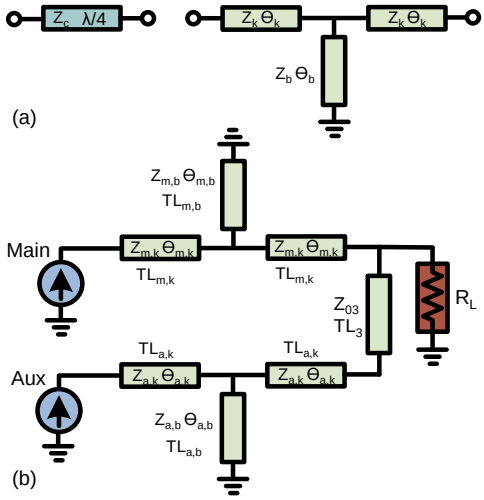


Figure 2.11: (a) Topology representation of the Tee-line network, equivalent to a $\lambda/4$ transmission line. (b) Illustration of the Tee-line-based Doherty combiner network.

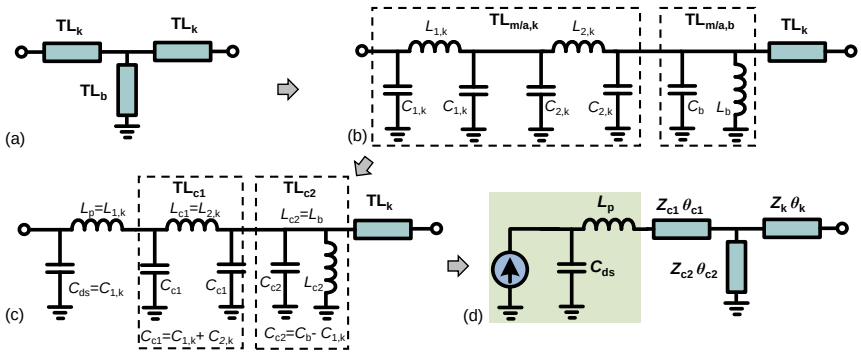


Figure 2.12: Introduced Tee-line-based topology for Doherty combiners. (a) and (b) Approximating transmission lines using Π networks. (c) Reorganizing inductors and capacitors to absorb transistor parasitic capacitors and packaged inductors. (d) Capacitor merging and splitting for transmission line modeling.

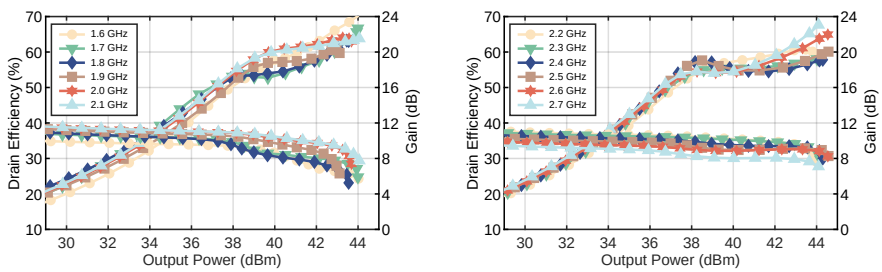


Figure 2.13: Simulated drain efficiency and gain versus output power of the wideband Doherty PA prototype from (a) 1.6 to 2.1 GHz and (b) 2.2 to 2.7 GHz.

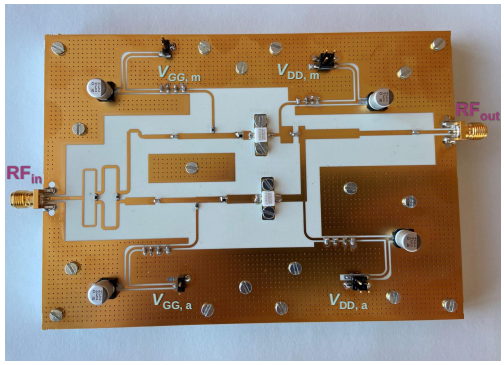


Figure 2.14: Photograph of the fabricated Doherty PA prototype circuit in [Paper A].

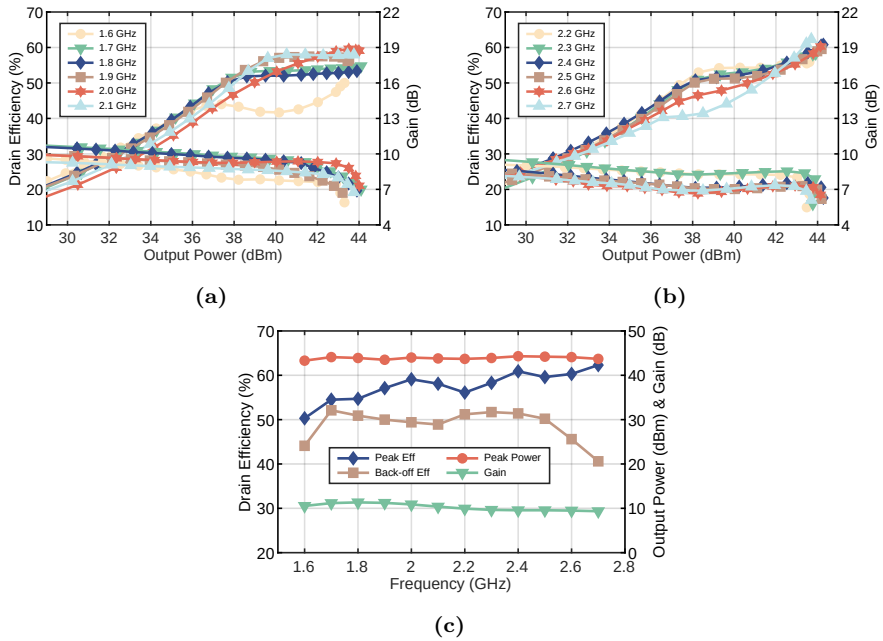


Figure 2.15: Measured drain efficiency and gain versus output power of the wideband Doherty PA prototype from (a) 1.6 to 2.1 GHz and (b) 2.2 to 2.7 GHz. (c) Measured drain efficiency at peak and 6-dB back-off power level, peak output power, and gain versus frequencies across 1.6 to 2.7 GHz.

Main and Aux amplifiers, we selected the GaN HEMT packaged transistors (CGH40010F) from Wolfspeed. The simulated performance of the designed Doherty PA prototype circuit is demonstrated in Figure 2.13, across the design bandwidth ranging from 1.6 GHz to 2.7 GHz.

The fabricated Doherty PA is shown in Figure. 2.14, with a physical dimension of 120 mm × 80 mm. To effectively manage heat during its operation, the PA is mounted on a copper fixture, serving as a heatsink. We assessed the performance of the prototype circuit using both continuous-wave (CW) and modulated signals. During the measurement, the gate and drain bias voltage

of the main amplifier was set at −3 V and 28 V, respectively, with a quiescent drain current of 45 mA.

The measurement results are presented in Figure 2.15(a) and 2.15(b), showing the drain efficiency and gain versus the output power. Note that the prototype effectively exhibits the anticipated back-off efficiency enhancement behavior within the designated frequency range. In Fig. 2.15(c), we observe the measured drain efficiency at both peak and back-off output power levels, the delivered peak output power, and the gain across the operational frequency range. The maximum output power consistently falls within the range of 43.3 dBm to 44.3 dBm over a 1-GHz bandwidth, demonstrating its wideband capabilities. Additionally, the PA achieves an excellent drain efficiency, ranging from 51% to 63% at the peak output power levels and from 41% to 53% at the back-off output power levels across the entire operational frequency spectrum.

2.4 Chapter Summary

In this chapter, the operational principles of two-way Doherty PAs have been presented. The theoretical performance of the Doherty combiner networks, derived using the black combiner synthesis method, was demonstrated and compared over an expansive bandwidth.

A Tee-line-based Doherty combiner network was then introduced and its validity was confirmed through experimentation. The theoretical analysis of the proposed topology was performed, emphasizing its potential for broadband applications. To facilitate a more efficient design process, equations were formulated that assist in the synthesis of this combiner network, which also considers the effects of output parasitics and the packaged elements originating from packaged transistors.

Chapter 3

Three-Stage Doherty Power Amplifiers

In the previous chapter, we observed a significant efficiency drop in both the asymmetrical two-way Doherty PA and N-way Doherty PA when attempting to enhance efficiency at deeper back-off power levels. Addressing this challenge, F. Raab proposed the three-stage Doherty PA concept in 1987 [70]. This innovative architecture was designed to boost efficiency at two specific output power back-off levels, denoted as $\gamma_{\mathbf{B1}}$ and $\gamma_{\mathbf{B2}}$. A comparison of efficiency versus output power for standard two-way, asymmetrical two-way (N-way), and three-stage Doherty PAs is presented in Figure 3.1. Essentially, the literature highlights two primary types of three-stage Doherty PA architectures, with one being the conventional three-stage Doherty PA [71–75]. The other is referred to as the modified three-stage Doherty PA [76–80].

In this chapter, we begin by reviewing the operational principles of both the conventional and modified three-stage Doherty PAs. Building on the black-box combiner synthesis approach adopted for the two-way Doherty PA in the preceding chapter, we generalize the operation and analysis of these three-stage Doherty PAs using the reciprocal and lossy three-port output combiners, with the load embedded.

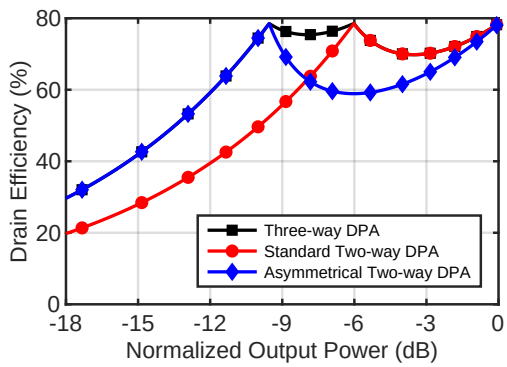


Figure 3.1: Drain efficiency versus normalized output power of different Doherty PA architectures: Standard two-way, asymmetrical two-way (N-way), and three-stage.

Subsequently, we introduce a load-pull-based three-port combiner synthesis method. This method paves the way for the design of an ultra-compact, low-loss combiner network tailored for the three-stage Doherty PA. Finally, we present the design and characterization of a three-stage Doherty PA demonstrator circuit, realized using the proposed design methodology as a proof-of-concept.

3.1 Conventional Three-Stage Doherty PAs

The operational principle of the conventional three-stage Doherty PA can be described as follows: Initially, its Main amplifier is load-modulated by the first auxiliary amplifier (Aux1) in the low-power region (when $\beta_{\mathrm{B1}} < \beta \leq \beta_{\mathrm{B2}}$). Subsequently, the second auxiliary amplifier (Aux2) is activated to modulate the common load of the two-way Doherty PA, which now consists of the Main and Aux1 amplifiers. It is important to note that the current of the class-B biased Main amplifier first increases linearly and then saturates after reaching the second back-off level. In contrast, the class-C biased Aux1 and Aux2 amplifiers turn on sequentially at the first and second back-off levels, respectively.

The amplifiers Main, Aux1, and Aux2 are characterized by current sources with fundamental output currents of I_{m}, I_{a1} and I_{a2}, respectively. These currents are dependent on the input voltage as

$$I_{\mathrm{m}} = \begin{cases} (\beta/\beta_{\mathrm{B2}})\, i_{\mathrm{m,M}}, & 0 \leq \beta \leq \beta_{\mathrm{B2}} \\ i_{\mathrm{m,M}}, & \beta_{\mathrm{B2}} \leq \beta \leq 1 \end{cases} \tag{3.1}$$

$$I_{\mathrm{a1}} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{\mathrm{B1}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B1}}}{1 - \beta_{\mathrm{B1}}}\right) i_{\mathrm{a1,M}} \cdot e^{-j\theta_1}, & \beta_{\mathrm{B1}} \leq \beta \leq 1 \end{cases} \tag{3.2}$$

$$I_{\mathrm{a2}} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{\mathrm{B2}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B2}}}{1 - \beta_{\mathrm{B2}}}\right) i_{\mathrm{a2,M}} \cdot e^{-j\theta_2}, & \beta_{\mathrm{B2}} \leq \beta \leq 1 \end{cases} \tag{3.3}$$

where $i_{\mathrm{m,M}}$, $i_{\mathrm{a1,M}}$ and $i_{\mathrm{a2,M}}$ represent the maximum fundamental current magnitudes for the Main, Aux1, and Aux2 amplifiers, respectively.

Note that it is crucial to maintain the output voltage amplitude from the Main amplifier at the drain-source bias voltage, V_{ds} within the high power range ($\beta_{\mathrm{B1}} < \beta \leq 1$). This ensures the amplifier's full voltage swing capability, leading to high-efficiency operation. To comprehensively define the operation of the conventional three-stage Doherty PA, the relationship between the maximum currents of the Aux1 and Main amplifiers must be established. This is described by the following relationship

$$\alpha_{1,\mathrm{M}} = \frac{i_{\mathrm{a1,M}}}{i_{\mathrm{m,M}}} = \frac{1}{\beta_{\mathrm{B1}}} - 1. \tag{3.4}$$

Similarly, the relationship between the maximum currents of the Aux2 and Main amplifiers is given by

$$\alpha_{2,\mathrm{M}} = \frac{i_{\mathrm{a2,M}}}{i_{\mathrm{m,M}}} = \frac{1}{\beta_{\mathrm{B1}}} \left(\frac{1}{\beta_{\mathrm{B2}}} - 1\right). \tag{3.5}$$

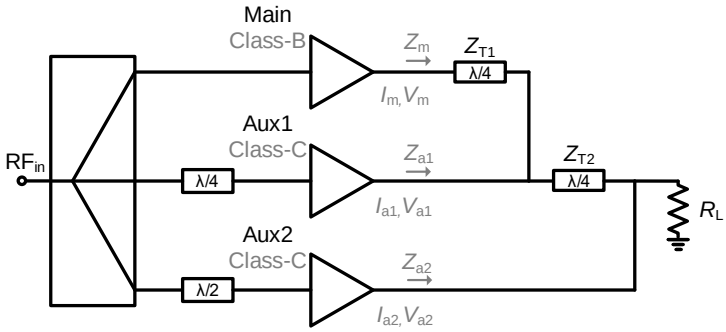
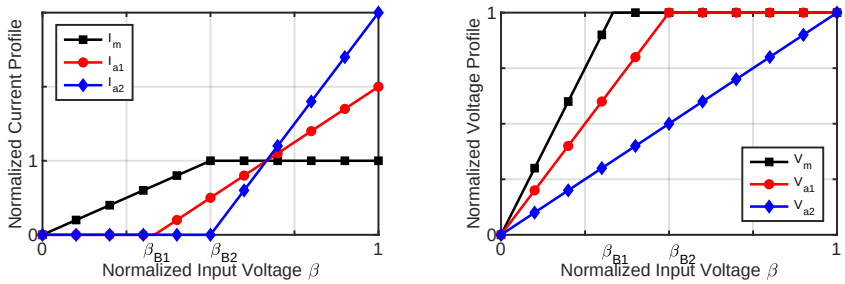
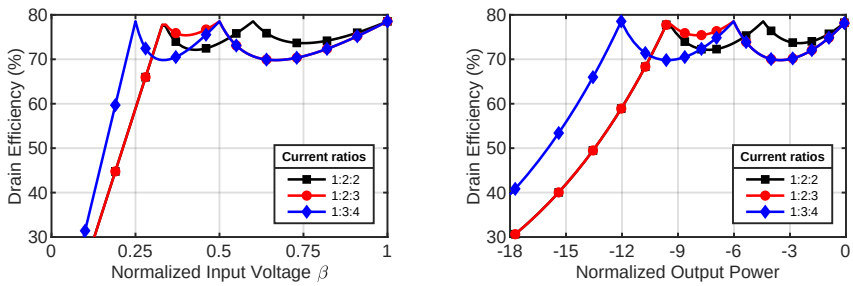


Figure 3.2: The conventional three-stage Doherty PA.



(a) **(b)**

Figure 3.3: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the conventional three-stage Doherty PA versus normalized input drive voltage.



(a) **(b)**

Figure 3.4: Drain efficiency of the conventional three-stage Doherty PA versus (a) normalized input drive voltage, and (b) normalized output power, for varying current ratios.

When the previously mentioned current ratios are satisfied, the resulting conventional three-stage Doherty PA, depicted in Figure 3.2, follows the commonly adopted configuration. The Main and Aux1 amplifiers are combined using a $\lambda/4$ transmission line impedance inverter with a characteristic impedance Z_{T1} at the output of the Main amplifier. The output of the Aux2 amplifier is connected to the common output node of the Main and Aux1 amplifiers via another $\lambda/4$ transmission line with a characteristic impedance Z_{T2}. The values

of Z_{T1} and Z_{T2} can be determined as follows [71]

$$Z_{\mathrm{T1}} = \frac{R_{\mathrm{L}}}{\beta_{\mathrm{B1}}\beta_{\mathrm{B2}}} \tag{3.6}$$

$$Z_{\mathrm{T2}} = \frac{R_{\mathrm{L}}}{\beta_{\mathrm{B2}}}. \tag{3.7}$$

Note that the input configuration comprises a three-way power splitter, accompanied by a $\lambda/4$ transmission line and a $\lambda/2$ transmission line. This setup ensures the same phase delay across all three amplifier paths.

The drive profiles and theoretical efficiency performance of the conventional three-stage Doherty PA are depicted in Figures 3.3 and 3.4, respectively. These figures illustrate that the conventional three-stage Doherty PA relies on sub-amplifiers with different fundamental current components, leading to variations in device peripheries to achieve back-off efficiency reconfigurability. Additionally, it is evident from the figures that the Main amplifier saturates after the Aux2 amplifier is turned on. Consequently, this PA architecture suffers from the saturation of the Main amplifier and increased complexity due to the varying device peripheries of the three amplifiers.

3.2 Modified Three-Stage Doherty PAs

In the previous section, we conducted a thorough analysis and examination of the conventional three-stage Doherty PA. Now, we shift our focus to the modified three-stage Doherty PA, which was initially introduced in [76]. This alternative architecture employs a modified output combiner featuring identical amplifier cells to improve efficiency at two specific fixed output power back-off levels: 6 dB and 9.54 dB. Furthermore, we will demonstrate that its output power back-off efficiency can also be reconfigured by varying the device peripheries of the sub-amplifiers.

To analyze the operational principle of the modified three-stage Doherty PA, we adopt a similar approach as with previous analyses. The fundamental output currents of the Main, Aux1, and Aux2 amplifiers, namely I_{m}, I_{a1}, and I_{a2}, are expressed in terms of the input voltage as follows

$$I_{\mathrm{m}} = \beta i_{\mathrm{m,M}}, 0 \leq \beta \leq 1 \tag{3.8}$$

$$I_{\mathrm{a1}} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{\mathrm{B1}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B1}}}{1 - \beta_{\mathrm{B1}}}\right) i_{\mathrm{a1,M}} \cdot e^{-j\theta_1}, & \beta_{\mathrm{B1}} \leq \beta \leq 1 \end{cases} \tag{3.9}$$

$$I_{\mathrm{a2}} = \begin{cases} 0, & 0 \leq \beta \leq \beta_{\mathrm{B2}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B2}}}{1 - \beta_{\mathrm{B2}}}\right) i_{\mathrm{a2,M}} \cdot e^{-j\theta_2}, & \beta_{\mathrm{B2}} \leq \beta \leq 1 \end{cases} \tag{3.10}$$

where $i_{\mathrm{m,M}}$, $i_{\mathrm{a1,M}}$ and $i_{\mathrm{a2,M}}$ are the maximum current from the Main, Aux1 and Aux2 amplifiers, respectively.

In the modified three-stage Doherty PA, the output voltage amplitude of the Main amplifier must consistently equal the drain-source bias voltage, V_{ds} throughout the higher power region to maximize its efficiency. Furthermore, to

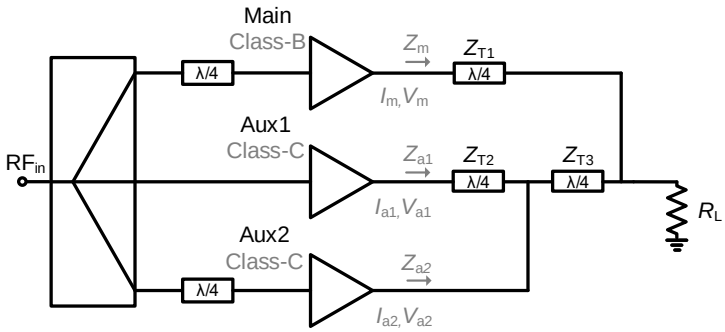
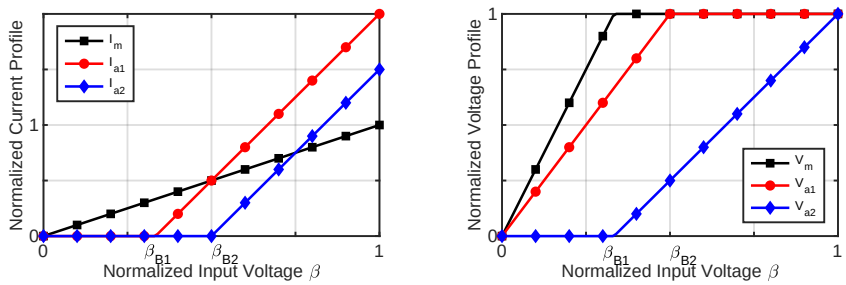
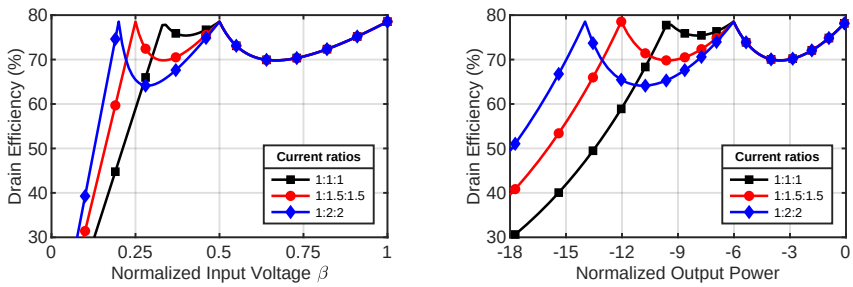


Figure 3.5: The modified three-stage Doherty PA.



(a) **(b)**

Figure 3.6: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the modified three-stage Doherty PA versus normalized input drive voltage.



(a) **(b)**

Figure 3.7: Drain efficiency of the modified three-stage Doherty PA versus (a) normalized input drive voltage, and (b) normalized output power, for varying current ratios.

fully establish its operation characteristics, the ratio of the maximum current from the Aux1 amplifier to that of the Main amplifier should be related by

$$\alpha_{1,\mathrm{M}} = \beta_{\mathrm{B2}} \left(\frac{1}{\beta_{\mathrm{B1}}} - 1 \right). \tag{3.11}$$

The ratio of the maximum current from the Aux2 amplifier to that of the Main

amplifier can be expressed as

$$\alpha_{2,\mathrm{M}} = (1 - \beta_{\mathrm{B2}}) \left(\frac{1}{\beta_{\mathrm{B1}}} - 1 \right). \tag{3.12}$$

The modified three-stage Doherty PA, configured to meet the specified current ratios, is represented by the schematic, as shown in Figure 3.5. The Aux1 and Aux2 amplifiers are connected through a $\lambda/4$ transmission line impedance inverter with a characteristic impedance of Z_{T2} at the output of the Aux1 amplifier. Additionally, the output of the Main amplifier is linked to the common output node of the Aux1 and Aux2 amplifiers, using two $\lambda/4$ transmission lines with characteristic impedances Z_{T1} and Z_{T3}. The expressions for Z_{T1}, Z_{T2}, and Z_{T3} are given by [77]

$$Z_{\mathrm{T1}} = \sqrt{\frac{R_{\mathrm{L}} R_{\mathrm{opt}}}{\beta_{\mathrm{B1}}}} \tag{3.13}$$

$$Z_{\mathrm{T2}} = \frac{\beta_{\mathrm{B1}} \left(\beta_{\mathrm{B2}} - 1\right) R_{\mathrm{opt}}}{\beta_{\mathrm{B2}}^2 \left(\beta_{\mathrm{B1}} - 1\right)} \tag{3.14}$$

$$Z_{\mathrm{T3}} = \frac{\beta_{\mathrm{B1}} \left(\beta_{\mathrm{B2}} - 1\right)^2}{\left(\beta_{\mathrm{B1}} - 1\right) \left(3\beta_{\mathrm{B2}}^2 - 3\beta_{\mathrm{B2}} + 1\right)} \sqrt{\frac{R_{\mathrm{L}} R_{\mathrm{opt}}}{\beta_{\mathrm{B1}}}}. \tag{3.15}$$

.

The drive profiles for the modified three-stage Doherty PA are depicted in Figure 3.6. Correspondingly, the theoretical simulated results are illustrated in Figure 3.7, demonstrating the drain efficiency in relation to both normalized input voltage and normalized output power. It should be noted that the modified three-stage Doherty PA exhibits distinct advantages over its conventional counterpart in two main aspects. Firstly, its Main amplifier operates linearly throughout the entire power range. Secondly, it theoretically allows for an enhancement in back-off efficiency using identical fundamental current components for all three amplifiers at peak output power.

3.3 Generic Three-Port Combiner Synthesis

As discussed in the previous chapter, when using equally-sized transistors, the Aux amplifiers, which operate in class C mode, have a reduced fundamental current component compared to class-B-biased Main amplifiers. This demands increased input power for the Aux amplifiers. As a result, in the context of the three-stage Doherty PA, both gain and PAE see a notable decline due to the Aux amplifiers being biased in deep class C mode to ensure efficiency at substantial power back-off levels. Therefore, even with the modified three-stage Doherty PA, its PAE performance is severely affected by the two auxiliary amplifiers. At microwave frequencies, the inherent parasitics and nonlinear behavior of real transistors become pronounced, causing considerable deviation from the behavior of ideal current sources. As a solution, a design approach based on the transistor load-pull data is desired.

In this section, we propose a generic load-pull-based design methodology for three-stage Doherty PAs [Paper C]. The theory is applied to maintain

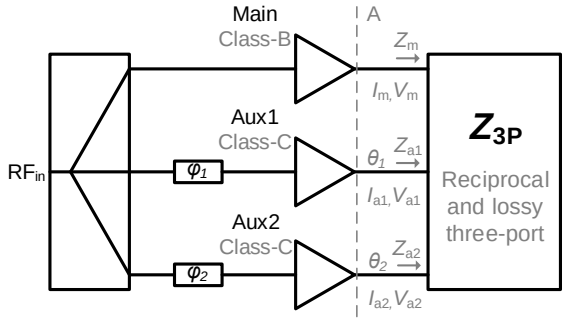


Figure 3.8: Generalized reciprocal and lossy three-port combiner used for the analysis of the three-stage Doherty PA. The load is terminated inside. $Z_{\mathbf{m}}$, $Z_{\mathbf{a1}}$ and $Z_{\mathbf{a2}}$ denote, the impedances seen by the Main, Aux1 and Aux2 amplifiers, respectively. Plane A represents the output plane of the amplifiers. The input and output current phase delays are denoted as $\varphi_{1,2}$ and $\theta_{1,2}$, respectively.

high efficiency at two reconfigurable output power back-off levels. The design approach solves the network parameters of the output combiner and the output current phase delays in terms of predefined boundary conditions, which comprise transistor loading conditions for high efficiency from large-signal load-pull characterizations [81]. The design methodology opens up a new design space, which enables a high power utilization factor and thus enhanced efficiency in three-stage Doherty PAs.

Figure 3.8 depicts a generalized analysis of the three-stage Doherty PA, which comprises two input phase shifters, a Main amplifier operating in class B mode, two auxiliary amplifiers operating in class C mode, and a reciprocal lossy three-port output combiner with an integrated load. Subsequent sections will discuss the transition from this lossy three-port combiner to a lossless four-port combiner that terminates with a resistive load, provided specific boundary conditions are satisfied. The voltages and currents shown in Figure 3.8 are related through $\mathbf{Z}_{3\mathrm{P}}$ as

$$\begin{bmatrix} V_{\mathrm{m}} \\ V_{\mathrm{a1}} \\ V_{\mathrm{a2}} \end{bmatrix} = \mathbf{Z_{3P}} \begin{bmatrix} I_{\mathrm{m}} \\ I_{\mathrm{a1}} \\ I_{\mathrm{a2}} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{12} & Z_{22} & Z_{23} \\ Z_{13} & Z_{23} & Z_{33} \end{bmatrix} \begin{bmatrix} I_{\mathrm{m}} \\ I_{\mathrm{a1}} \\ I_{\mathrm{a2}} \end{bmatrix}. \tag{3.16}$$

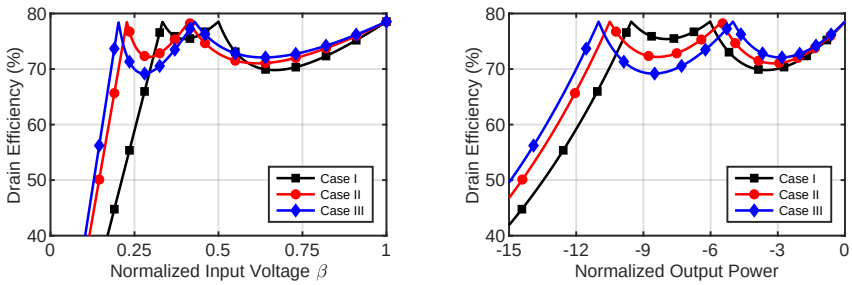
3.3.1 Symmetrical Three-Stage Doherty PAs

The symmetrical three-stage Doherty PA is essentially a modified three-stage Doherty PA with current ratios below unity. This configuration more accurately mirrors the fundamental current from realistic class-C biased Aux transistors, especially when these transistors are of the same size as the Main transistors.

Based on equation (3.16), it is feasible to determine the impedance parameters of the reciprocal and lossy three-port combiner, based on the values of $|\alpha_{1,\,\mathrm{M}}|$, $|\alpha_{1,\,\mathrm{B2}}|$, $|\alpha_{2,\,\mathrm{M}}|$, and the two output current phase delays θ_1 and θ_2. It is important to note that these parameters should meet certain conditions to allow the transformation of the derived lossy three-port combiner into a lossless four-port combiner, with one of its ports terminated by a resistive load. To

Table 3.1: Different three-stage Doherty PA design cases

	Case I Modified	Case II Symmetrical	Case III
γ_{B1} (dB)	9.54	10.5	11
γ_{B2} (dB)	6	5.5	5
$\lvert\alpha_{1,M}\rvert$	1	0.85	0.85
$\lvert\alpha_{2,M}\rvert$	1	0.7	0.7
$\lvert\alpha_{1,B2}\rvert$	0.25	0.31	0.38
θ_1 (deg)	-90	-76.56	-67.61
θ_2 (deg)	0	25.86	31.42



(a) **(b)**

Figure 3.9: Drain efficiency of the symmetrical three-stage Doherty PA versus (a) normalized input drive voltage, and (b) normalized output power, for Cases I, II and III in Table 3.1

facilitate this conversion, the following conditions should be satisfied

$$\Re\{Z_{12}\}^2 = \Re\{Z_{11}\}\Re\{Z_{22}\} \tag{3.17}$$

$$\Re\{Z_{13}\}^2 = \Re\{Z_{11}\}\Re\{Z_{33}\} \tag{3.18}$$

$$\Re\{Z_{23}\}^2 = \Re\{Z_{22}\}\Re\{Z_{33}\}. \tag{3.19}$$

Given the three boundary conditions, our system of five unknown parameters is under-determined, leaving two parameters that can be freely chosen. To illustrate the reconfigurable output power back-off efficiency of the symmetrical three-stage Doherty PA, three different cases were examined. The derived parameters for each case are summarized in Table 3.1, while their corresponding efficiency profiles are depicted in Figure 3.9. These results validate our proposition: With different current ratios ($|\alpha_{1,\,M}|$ and $|\alpha_{2,\,M}|$), by solving for output current phase delays (θ_1 and θ_2), one can design three-stage Doherty PAs that exhibit high efficiency at two back-off power levels (γ_{B1} and γ_{B2}).

3.3.2 Combiner Network Synthesis

While the previous section focuses on the ideal analysis of both generic and symmetrical three-stage Doherty PAs, it is crucial to note that real-world microwave transistors have pronounced nonlinear behaviors and the presence of parasitic components. Consequently, our subsequent direction focuses on

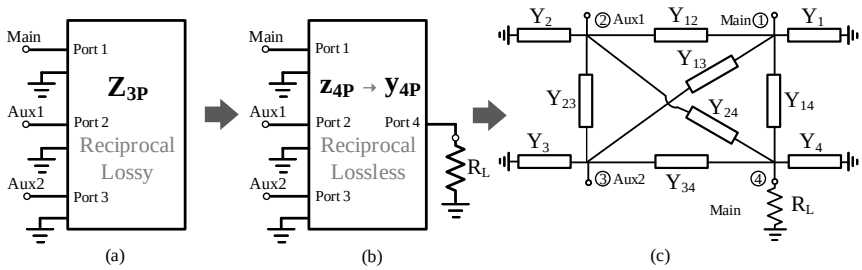


Figure 3.10: Step-by-step conversion of the generalized output combiner into a realizable network. First, the lossy and reciprocal three-port output combiner in (a) is converted to a lossless and reciprocal four-port output combiner terminated with a purely resistive load R_{L} in (b). The obtained four-port impedance parameters are then converted to the admittance parameters, which can be converted into an equivalent network topology in (c).

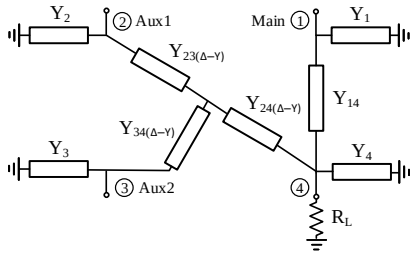


Figure 3.11: Simplified combiner network after tuning of z_{44} and $\Delta - \mathrm{Y}$ transformation.

developing a load-pull-based combiner synthesis method tailored for the three-stage Doherty PA, which enables the highest possible efficiency and output power performance with real transistors. The method is referred to as the three-port black-box combiner synthesis approach. Similar to the two-port black-box combiner approach described previously, we first obtain the optimal output impedance and power of the Main and Aux transistors. These crucial parameters are acquired through load-pull simulation or experiments at the peak, first, and second power back-off levels, together with the off-state output impedance from the two Aux transistors. A reciprocal and lossy three-port combiner, with impedance matrix $\mathbf{Z}_{3\mathrm{P}}$, as presented in Figure 3.10, is then determined from the load-pull data to satisfy the optimal loading conditions. The lossy three-port combiner is, thereafter, converted to a lossless four-port combiner terminated with an external resistor when the three boundary conditions (3.17)-(3.19) are satisfied. Using these conditions, the phase delays between the Main and two Aux amplifiers are determined. Finally, it is possible to realize the actual lumped-element combiner network from the four-port admittance parameters ($\mathbf{y}_{4\mathrm{P}}$), as illustrated in Figure 3.11. The value of each element in the combiner network can thus be expressed as

$$Y_k = y_{kk} + \sum_{j=1, j\neq k}^{n} y_{kj} \tag{3.20}$$

$$Y_{kj} = -y_{kj}. \tag{3.21}$$

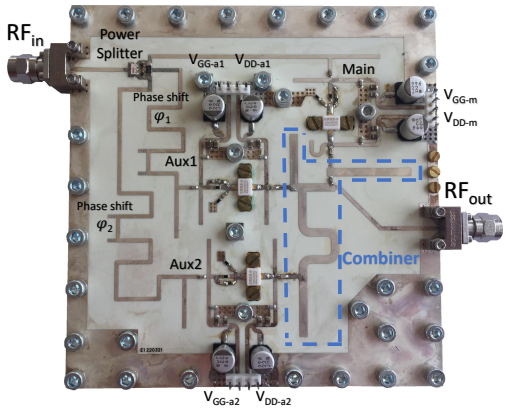


Figure 3.12: Photo of the fabricated three-stage Doherty PA prototype in [Paper C].

Note that there are two extra degrees of freedom when converting from the lossy three-port to lossless four-port combiner, i.e., z_{44} and R_{L}. These two parameters can thereby be tuned to further simplify the actual combiner, for instance, to avoid the cross elements Y_{12} and Y_{13} and to let the combiner directly interface the 50 Ω load termination. Furthermore, the layout of the combiner network can be even more compact and easier to fabricate, if $\Delta - \mathrm{Y}$ circuit transformation is applied, as shown in Figure 3.11.

3.3.3 Circuit Realization and Results

To validate the proposed theoretical framework and design methodology, a three-stage Doherty PA demonstrator circuit was designed and evaluated, as illustrated in [Paper C] and shown in Figure 3.12. This design aims to achieve optimal efficiency at two output power back-off levels, centered around a frequency of 2.14 GHz. The circuit incorporated three amplifiers of identical size. The input transmission lines were designed to ensure the necessary phase delays for the two Aux paths. Using the combiner synthesis method described earlier, a compact output combiner network was developed. Both simulation and measurement results confirmed that this combiner network facilitated high-efficiency performance at the targeted 2.14 GHz frequency. Comprehensive results, including evaluations with CW and digitally modulated signals, will be presented subsequently.

The measured and simulated drain efficiency, PAE, and power gain at 2.14 GHz are plotted versus output power in Figure 3.13. The measured drain efficiency at 6-dB and 10-dB output power back-offs are 68% and 56%, respectively. The measured PAE at the same back-off levels is 56% and 45%, respectively. The agreement between measured and simulated results is in general very good, although the measured PAE and power gain show a small degradation compared to simulations in the lower output power region.

The demonstrator circuit was characterized at 2.14 GHz using Long Term Evolution (LTE)-like signals with varying PAPR and bandwidth to further examine its performance. Besides, DPD with a generalized memory polynomial model was used to evaluate the performance and the linearizability of the proto-

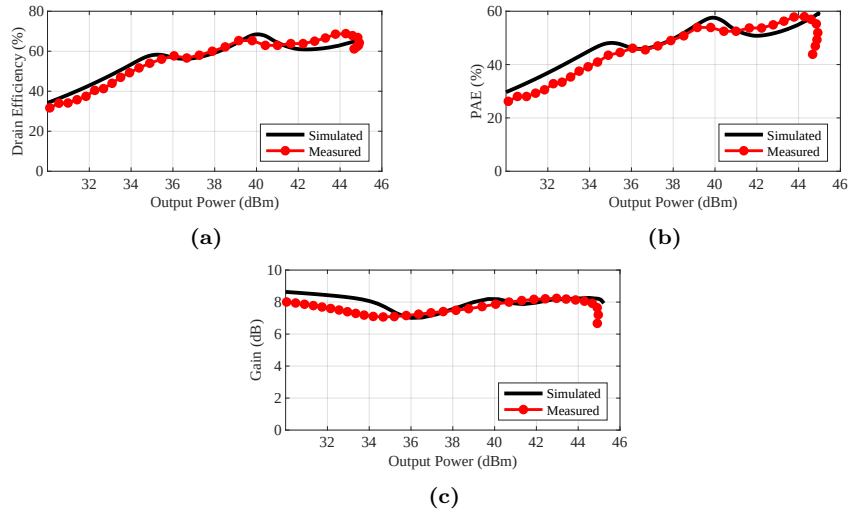


Figure 3.13: CW measurement results of the three-stage Doherty PA prototype circuit at 2.14 GHz. (a) Drain efficiency versus output power, (b) PAE versus output power, and (c) gain versus output power.

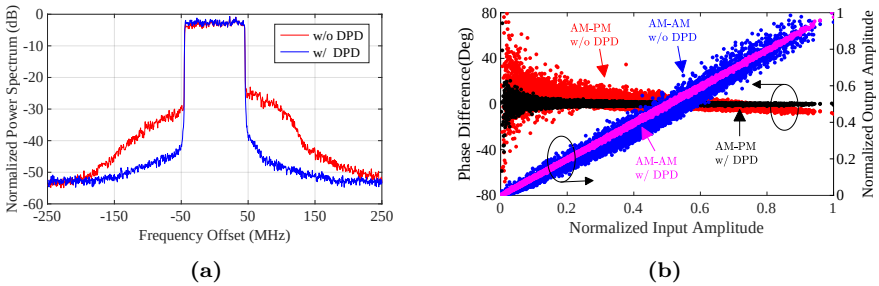


Figure 3.14: Modulated-signal measurement results of the three-stage Doherty PA prototype at 2.14 GHz. (a) Measured spectrum with and without DPD, (b) measured AM-AM and AM-PM characteristics with and without DPD, when using a 100-MHz 8.5-dB PAPR communication signal.

type circuit. The measured output spectrum with and without applying DPD is presented in Figure 3.14(a). Without any linearization, the demonstrator circuit provided an average drain efficiency of 54.5% and an adjacent channel leakage ratio (ACLR) of below −26.3 dBc at an average output power of 36.2 dBm. After applying DPD, the ACLR of the prototype was improved to −45.7 dBc at an average output power of 36.2 dBm. Additionally, the corresponding AM/AM and AM/PM characteristics are presented in Figure 3.14(b).

3.4 Chapter Summary

This chapter demonstrated the operating principles of both the conventional and modified three-stage Doherty PA. Each mode of operation mandated a specific interrelation between its full current ratios and back-off levels. We then illustrated how the black-box method could expand the design space by unlocking these constraints. This flexibility becomes particularly useful when designing practical three-stage Doherty PAs where the class-C biased Aux amplifiers have a smaller fundamental current compared to their class-B biased Main counterparts.

A load-pull-based combiner synthesis approach for three-stage Doherty PAs, together with the realization and simplification of the actual combiner network, has been proposed and described. The resulting combiner network has, in many cases, much lower insertion loss and a very compact size. A demonstrator circuit has been presented to verify the proposed technique. The measurement results show that the circuit provides excellent performance in terms of efficiency at deep output power back-off levels.

Chapter 4

Circulator Load Modulated Amplifiers

In the preceding chapter, we explored the principle of operation and practical implementations of both two-way and three-stage Doherty PA. As wireless communication systems evolve, there is a growing need for new PA architectures that not only enhance deep back-off efficiency but also have the potential to operate over a wide bandwidth.

This chapter begins with a review of recently published wideband PA architectures that focus on back-off efficiency enhancement. Following this, we introduce a novel efficient PA architecture with a non-reciprocal output combiner. The operational principles and theoretical performance of the introduced architecture are subsequently illustrated. To validate the concept, we will present the design, implementation, and characterization of the proposed architecture, as illustrated in [Paper D & E].

4.1 Overview

In 2016, a high-efficiency, wide-bandwidth architecture known as the LMBA was introduced by Shepphard [25]. Essentially, the LMBA comprises a balanced amplifier acting as the Main amplifier. Additionally, an Aux amplifier is incorporated to inject a control signal into the isolated port of the quadrature coupler, effectively modulating the impedance seen by the balanced amplifiers.

Initially, the LMBA employed a dual-input configuration, enabling dynamic modulation of the load impedance of its Main amplifier by concurrently adjusting both the phase and magnitude of the input drive signal. This approach evolved, with the first RF-input LMBA configuration illustrated in [82, 83]. Shortly thereafter, the RF-input LMBA having a Doherty-like drive operation was proposed, as seen in [84,85]. This topology employs an input power splitter with a fixed phase delay between the Main balanced amplifiers biased in class B mode and the Aux amplifier operating in class C mode, as illustrated in Figure 4.1. To further enhance bandwidth capabilities, an RF-input LMBA with CM operation was introduced in [86]. Compared to the Doherty PA, the Doherty-like LMBA architecture offers a notable advantage in bandwidth.

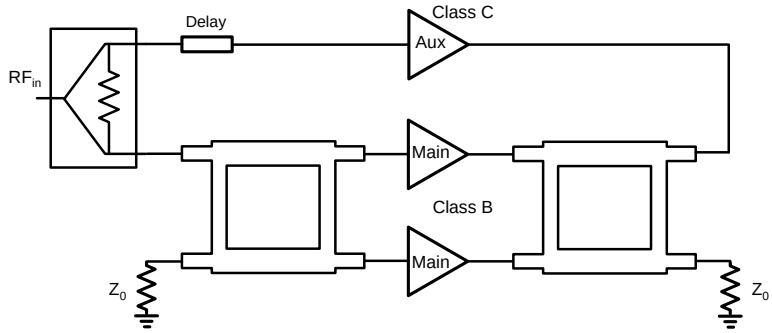


Figure 4.1: Block diagram of the load modulated balanced amplifier (LMBA).

This advantage comes from the inherent broader bandwidth of the quadrature coupler, compared to the $\lambda/4$-line-based output combiner of a standard Doherty PA. However, this enhancement comes at a cost. The LMBA architecture is more complex, and the incorporation of input and output quadrature couplers contributes to increased circuit losses and an overall larger footprint. The addition of an extra transistor also adds to the manufacturing cost.

A novel active load modulation PA architecture, known as the CLMA was proposed in our recent work [Paper D & b]. This innovative design incorporates two active devices and leverages a non-reciprocal circulator-based combiner. The CLMA stands out for its remarkable ability to maintain high efficiency over a large output power dynamic range. Moreover, the availability of wideband and low-loss circulators makes this architecture promising for wideband applications. Therefore, the CLMA represents a promising alternative to other load modulated PA architectures.

4.2 Principle of Operation

The CLMA comprises a class-B biased Main amplifier, a class-C biased Aux amplifier, and a circulator-based output combiner network as illustrated in Figure 4.2. The fundamental concept of the CLMA architecture can be described as follows: An Aux amplifier injects power into the output of the Main amplifier through the circulator to modulate its load impedance and thereby maintain high efficiency at both peak power and back-off power level. Due to the inherent non-reciprocal property of the circulator, the powers injected by the Main and Aux amplifiers are both fully delivered to the load. Moreover, the impedance seen by the Aux amplifier is maintained constant due to the high isolation from the Main to the Aux port in the circulator [87–90].

To further study the operation principle of the CLMA, it is important to analyze the microwave circulator. Typically, an ideal circulator directs a signal from one port to the next in a cyclic manner, while ensuring minimal signal leakage to other ports. It is worth noting that the scattering parameters of an

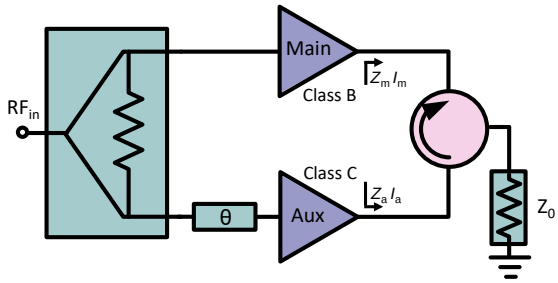


Figure 4.2: Block diagram of the circulator load modulated amplifier (CLMA).

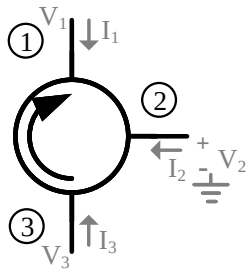


Figure 4.3: Block diagram of an ideal circulator for the analysis of the CLMA architecture.

ideal circulator, as depicted in Figure 4.3, can be expressed as

$$\mathrm{S_{circ}} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}. \tag{4.1}$$

Note that transitioning from the scattering parameters ($\mathrm{S_{circ}}$) to admittance parameters simplifies the analysis. Once the three-port scattering parameters are converted to their corresponding admittance parameters, the operational mechanism of the CLMA can be analyzed using the three-port admittance parameter matrix representative of an ideal circulator. It should be stressed that this formulation assumes that the port currents, I_n, flow into the corresponding port of the circulator, and the voltages V_n are referenced to the common ground connection. The port currents and voltages are therefore related by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = Y_0 \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{4.2}$$

where $Y_0 = 1/Z_0$ is the characteristic admittance of the circulator.

The Main (connected at port 1) and Aux (connected at port 3) amplifiers can be represented as current sources in the analysis, having magnitudes I_m and I_a, respectively. Thus, $I_1 = I_\mathrm{m}$, $I_3 = I_\mathrm{a} e^{j\theta}$, where θ is the output current phase delay between the Main and Aux amplifier branches. In addition, the output port (port 2) is terminated with a resistive load matched to the characteristic impedance of the circulator Z_0, so $V_2 = -Z_0 I_\mathrm{L}$.

Substituting the above equations into the three-port admittance matrix from (4.2), the resulting three equations can be resolved. This yields the desired

expression representing the impedance seen at the output of the Main amplifier, represented by Z_{m}, as follows

$$Z_{\mathrm{m}} = Z_0 \left(1 - 2\frac{I_{\mathrm{a}} e^{j\theta}}{I_{\mathrm{m}}}\right). \tag{4.3}$$

The above equation reveals that the impedance seen by the Main amplifier can be dynamically modulated by the magnitude and phase delay of the Aux current. Additionally, the relationship between the currents is given by

$$I_{\mathrm{L}} = I_{\mathrm{m}} - I_{\mathrm{a}} e^{j\theta}. \tag{4.4}$$

The power delivered to the output load is therefore given by

$$\begin{aligned} P_{\mathrm{L}} &= \frac{1}{2} Z_0 \Re\left\{|I_{\mathrm{L}}|^2\right\} \\ &= \frac{1}{2} Z_0 \left(I_{\mathrm{m}}^2 - 2 I_{\mathrm{m}} I_{\mathrm{a}} \cos(\theta) + I_{\mathrm{a}}^2\right) \end{aligned} \tag{4.5}$$

The power generated by the Main and Aux amplifiers can be expressed as

$$\begin{aligned} P_{\mathrm{m}} &= \frac{1}{2} I_{\mathrm{m}}^2 Z_0 \Re\left\{1 - 2\frac{I_{\mathrm{a}} e^{j\theta}}{I_{\mathrm{m}}}\right\} \\ &= \frac{1}{2} Z_0 \left(I_{\mathrm{m}}^2 - 2 I_{\mathrm{m}} I_{\mathrm{a}} \cos(\theta)\right) \end{aligned} \tag{4.6}$$

$$P_{\mathrm{a}} = \frac{1}{2} Z_0 \Re\left\{|I_{\mathrm{a}}|^2\right\} = \frac{1}{2} Z_0 I_{\mathrm{a}}^2 \tag{4.7}$$

It can be noticed that $P_{\mathrm{L}} = P_{\mathrm{m}} + P_{\mathrm{a}}$, which indicates that the power generated by the Main and Aux amplifiers is fully delivered to the output load.

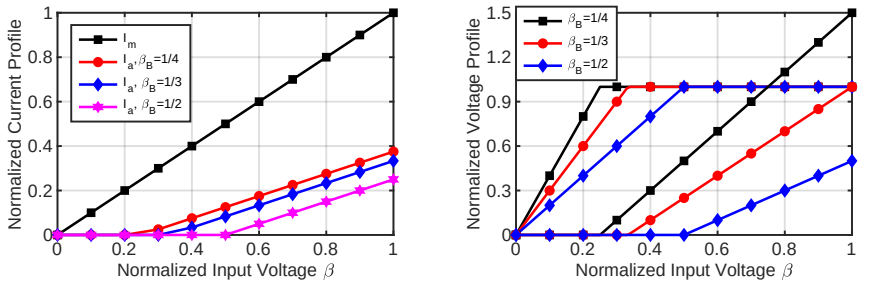
4.3 Theoretical Performance

In the previous section, it was shown that the impedance seen by the Main amplifier of the CLMA is load modulated by the active current injection from the Aux amplifier. Furthermore, the power generated by both Main and Aux amplifiers can be fully recovered at the CLMA output port, and thus delivered to the load. To further investigate its theoretical performance, the Main and Aux amplifier are represented by current sources having fundamental output currents I_{m} and I_{a} that depend on the input voltage as

$$I_{\mathrm{m}} = \beta i_{\mathrm{m,M}} \tag{4.8}$$

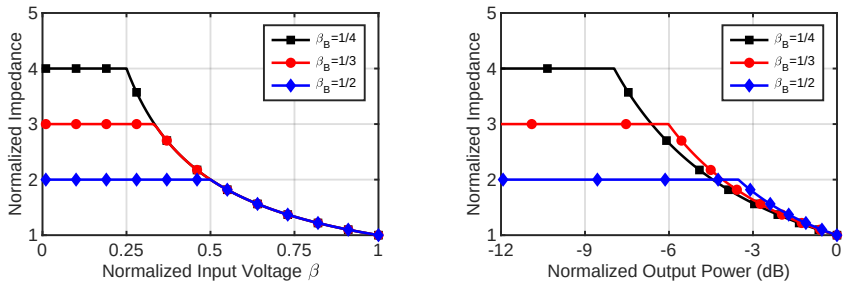
$$I_{\mathrm{a}} = \begin{cases} 0, & 0 \le \beta \le \beta_{\mathrm{B}} \\ \left(\dfrac{\beta - \beta_{\mathrm{B}}}{1 - \beta_{\mathrm{B}}}\right) i_{\mathrm{a,M}} \cdot e^{-j\theta}, & \beta_{\mathrm{B}} \le \beta \le 1 \end{cases}. \tag{4.9}$$

For the Main amplifier, it is important to maintain the amplitude of the output voltage consistently at the drain-source bias voltage V_{ds} throughout the high power region (when $\beta_{\mathrm{B}} < \beta \le 1$) to guarantee its full voltage swing capability, and thereby high-efficiency operation. To fully determine the operation



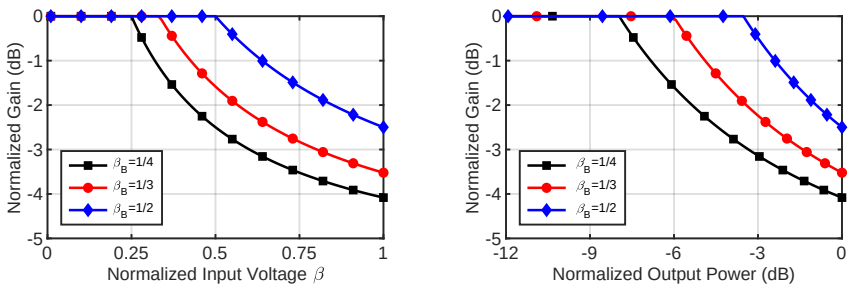
(a) **(b)**

Figure 4.4: (a) Normalized amplitude of the output currents and (b) output voltage profiles of the CLMA versus normalized input drive voltage, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) **(b)**

Figure 4.5: Normalized optimal load impedance of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.



(a) **(b)**

Figure 4.6: Normalized gain of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, $1/3$, and $1/2$.

of the CLMA, the current ratio (α) between the maximum current of the Aux and Main amplifiers should be related by

$$\alpha = \frac{i_{\text{a, M}}}{i_{\text{m, M}}} = \frac{1 - \beta_{\text{B}}}{2}. \tag{4.10}$$

In Figure 4.4, the current and voltage profiles of the CLMA are plotted versus the normalized input voltage (β). Notably, the peak fundamental

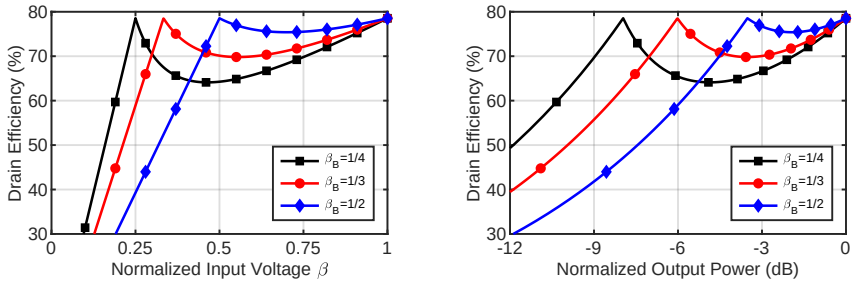


Figure 4.7: Drain efficiency of the CLMA versus (a) normalized input drive voltage, and (b) normalized output power, for $\beta_B = 1/4$, 1/3, and 1/2.

current required from the Aux amplifier is markedly lower than that of the Main amplifier. Similar to the behavior of the conventional two-way Doherty PA, the current ratio (α) of the CLMA should be increased to extend its high-efficiency back-off power level. Furthermore, the maximum voltage swing required for the Aux amplifier varies with different back-off levels.

The ideal simulation results are shown in Figures 4.5-4.7, where the normalized load modulation, normalized gain, and drain efficiency are plotted versus normalized input voltage and normalized output power, respectively. The theoretical analysis and performance presented in this section illustrate how a simple combination of the Main and Aux amplifiers, together with correct driving conditions and the non-reciprocal circulator-based combiner, results in enhanced efficiency performance at deep output back-off power levels.

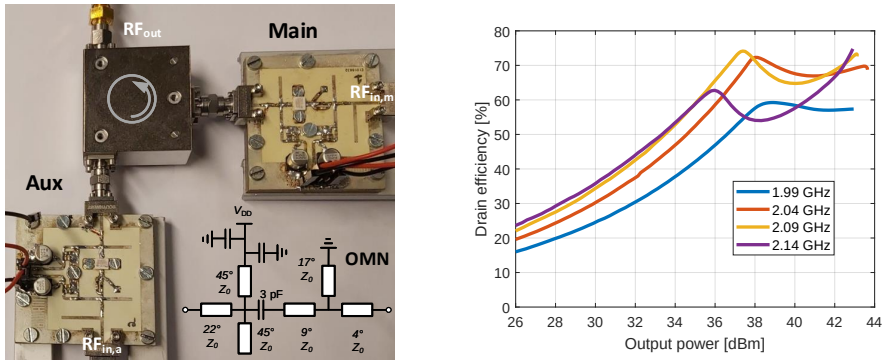
4.4 Demonstrator Circuits

To validate the theory and to demonstrate the utility of the CLMA architecture, [Paper D, E, & b] present the design and measurement results of the three demonstrator circuits. This section reviews the reported measurement results and compares them with the theoretical predictions.

4.4.1 Dual-Input Prototype

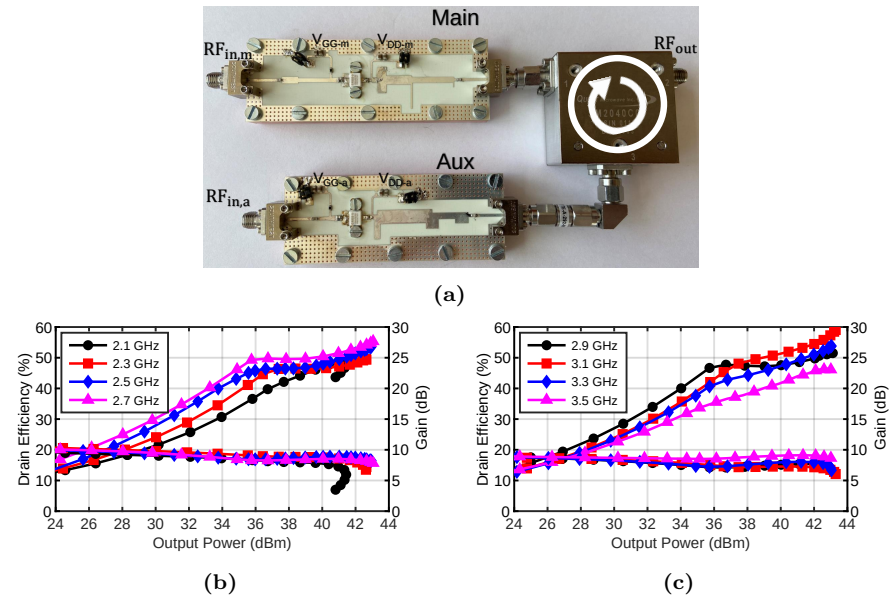
The proposed CLMA architecture was first experimentally verified with a prototype circuit as discussed in [Paper b]. As depicted in Figure 4.8(a), the circuit was constructed at a center frequency of 2.1 GHz. It employed two PA test boards with commercial 10-W GaN devices (specifically, the CGH40010F from Wolfspeed) for its Main and Aux amplifiers. The non-reciprocal combiner was realized by a circulator (the SM2040C09 from Quest Microwave), which was selected for its low insertion loss, sufficient isolation, and wide bandwidth.

The CLMA prototype circuit demonstrated in [Paper b] was characterized by static CW measurements. The drain bias of the Main and Aux amplifiers was set to 28 V and 34 V, respectively. The gate bias of the Main and Aux amplifiers was set to -3 V and -6 V, respectively. Figure 4.8(b) shows the measured drain efficiency versus output power for frequencies between 1.99 and



(a) (b)

Figure 4.8: (a) Photo of the CLMA prototype circuit. (b) Measured drain efficiency of the CLMA prototype circuit versus the output power. [Paper b]



(a) (b) (c)

Figure 4.9: (a) Photo of the CLMA prototype circuit. (b) Measured drain efficiency of the CLMA prototype circuit versus the output power from (b) 2.1 to 2.7 GHz and (c) 2.9 to 3.5 GHz. [Paper D]

2.14 GHz. The results highlight a distinct efficiency enhancement at the power back-off level across these frequencies. Particularly noteworthy is the measured performance at 2.09 GHz, where the drain efficiency is 73% at 6 dB output power back-off level and 72% at the peak power. It is essential to highlight that this validation of the CLMA concept was realized through a prototype designed for narrowband operation, mainly due to the bandwidth limitations inherent to the utilized PA boards.

The second CLMA prototype was introduced in [Paper D]. This version was geared towards broader bandwidth operation. To realize this, wideband Main and Aux amplifiers with CM output-matching networks were incorporated.

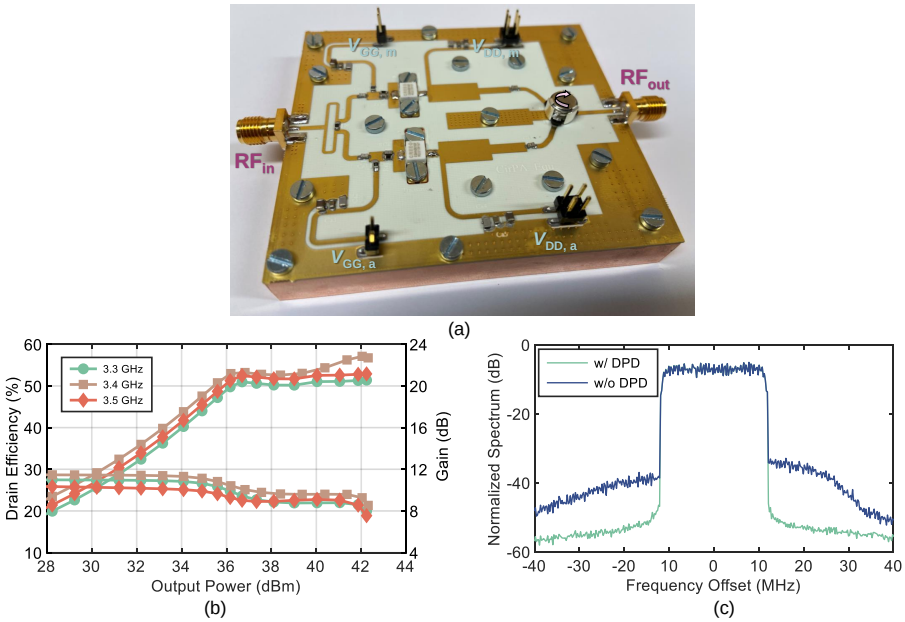


Figure 4.10: (a) Photo of the CLMA prototype circuit. (b) Measured drain efficiency of the CLMA prototype circuit versus the output power from 3.3 to 3.5 GHz and (c) Normalized spectrum of the prototype circuit when applying a 20-MHz 7-dB PAPR OFDM signal at 3.4 GHz, before and after applying DPD. [Paper E]

The active devices selected for both the Main and Aux amplifiers were the CGH40010F GaN-packaged transistors from Wolfspeed. Additionally, the SM2040C09 microwave circulator was selected to act as the output combiner. A photograph of the fabricated CLMA prototype is shown in Figure. 4.9(a). During testing, this CLMA prototype was stimulated by a single-tone CW signal spanning from 2.1 to 3.5 GHz. The measured results, as illustrated in Figure. 4.9(b) and (c), include the measured drain efficiency and gain performance versus the output power. Notably, the prototype exhibited back-off efficiency enhancement behavior over a considerable 1.4 GHz bandwidth.

4.4.2 Single RF-input prototype circuit

A third CLMA prototype circuit was presented in [Paper E], featuring a single RF-input configuration. This design aimed to eliminate the need for external control signals with phase tuning, simplifying the architecture and making it more attractive for practical applications.

In the construction of the RF-input CLMA prototype, we selected the surface mount (SMT) single-junction circulator from Skyworks (SKYFR-001822) to act as the combiner. Additionally, the CGH40010F GaN transistors from Wolfspeed were selected to serve as both Main and Aux amplifiers. A photograph of the fabricated RF-input CLMA prototype is shown in Figure 4.10(a).

To provide a comprehensive characterization of this prototype, we conducted measurements utilizing both CW and modulated signal approaches.

Specifically, the gate bias for the Main and Aux amplifiers was set at −2.7 V and −6.5 V, respectively. Figure 4.10(b) presents the CW measurement results obtained from the prototype circuit. Notably, the maximum measured output power reached 42.3 dBm, with measured drain efficiency values of 57% at the peak power level and 53% at the 6-dB back-off power level at 3.4 GHz. In Figure 4.10(c), we demonstrate the measured output spectrum before and after applying DPD. The measured average drain efficiency was 51%, with an average output power of 35.6 dBm. The ACLR exhibits substantial improvement, transitioning from −30.8 dBc to −51.6 dBc after applying DPD.

4.5 Chapter summary

This chapter has proposed and illustrated the CLMA architecture, emphasizing its capability to enhance efficiency across a substantial output power range. The intricate operational principles and the theoretical prospects of the CLMA architecture have been comprehensively presented and discussed.

Three CLMA demonstrator circuits have been developed to verify the theoretical findings. Large-signal characterization results show that the prototype circuit provides promising performance in terms of efficiency enhancement at the back-off power level. The empirical findings underscore the viability of the CLMA, positioning it as a potential alternative for PA architectures aiming at back-off efficiency enhancement.

Chapter 5

Sequential Circulator Load Modulated Amplifiers

As established in earlier chapters, active load modulated PA architectures, such as the Doherty PA, LMBA, CLMA, etc., have been recognized for their efficiency enhancement capabilities. It should be noted that the bandwidth potential of these architectures highly depends on the frequency response of their output combiner networks.

This chapter begins by addressing the inherent bandwidth constraints of the active load modulated PA architectures, with a particular focus on deep power back-off scenarios. We also review the evolution of PA architectures designed to enhance back-off efficiency without resorting to load modulation. Drawing from the foundational concepts and the previously introduced CLMA architecture, we introduce a novel SCLMA architecture. The theoretical performance of this proposed architecture is illustrated. To substantiate the concept, we present the design, implementation, and characterization of the SCLMA prototype circuits, as illustrated in [Paper F & G].

5.1 Overview

Load-modulated PA architectures have been widely employed to enhance the back-off efficiency of PAs. The Doherty PA, LMBA, and CLMA architectures, which were previously discussed, are exemplary representatives of this classification. Although they are able to improve PA efficiency at deep back-off power levels, these methods face a large load impedance at the back-off level. The drawback of it can be explained by the Bode-Fano criterion [91]

$$\Delta\omega \leq \frac{\pi}{RC \ln \frac{1}{|\Gamma|}}. \tag{5.1}$$

This criterion clearly indicates that the bandwidth achieving a satisfactory match is inherently limited by the parallel resistor and capacitor network. In the context of active devices, R and C typically denote the optimal load resistance and parasitic capacitance. Consequently, load modulated PA architectures often

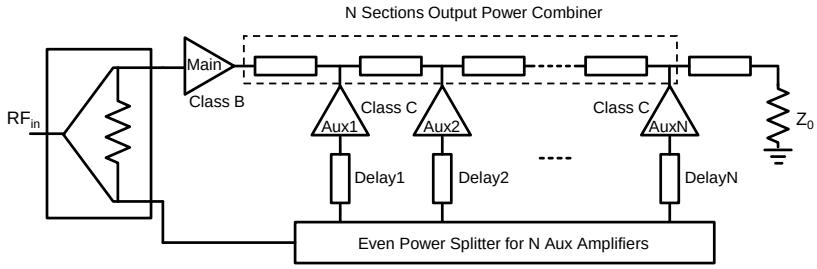


Figure 5.1: Block diagram of the distributed balanced power amplifier (DEPA).

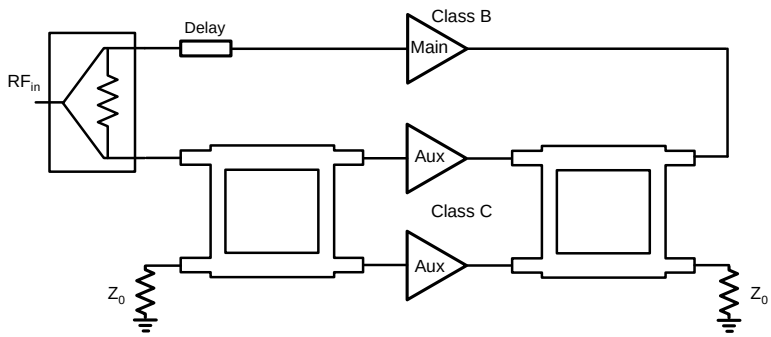


Figure 5.2: Block diagram of the sequential load modulated balanced amplifier (SLMBA).

exhibit narrow-band characteristics at back-off power levels due to the increased load impedance. Moreover, large load modulation may lead to degradation in back-off efficiency, attributed to the potential shunt loss in active devices as explored in [92, 93].

Hence, there is a growing need for a PA design that negates the compromise between the high-efficiency back-off level and the load modulation ratio. The sequential PA, which was first proposed in [94], presents a solution to this demand. In principle, it enhances back-off efficiency without the need for load modulation. Nevertheless, it has an inherent trade-off between back-off and peak efficiency. This compromise predominantly stems from the inherent losses of its power combiner, as elaborated upon in [95, 96].

The DEPA has recently been proposed in [24]. This innovative architecture improves back-off efficiency by avoiding load modulation and instead leveraging multiple Aux sub-amplifiers distributed within a broadband multisection impedance transformer, as demonstrated in Figure 5.1. However, the incorporation of several Aux sub-amplifiers augments both the complexity of the DEPA circuit and its combiner losses. Meanwhile, the SLMBA, as introduced in [26, 27, 97–100], has emerged as a widely adopted architecture that draws great attention in the field. Originating from the fundamental LMBA concept [25], the SLMBA, as shown in Figure 5.2, not only retains comparable functionalities but also exhibits a less complicated circuitry in comparison to the DEPA.

Expanding upon this foundation, we introduce the sequential CLMA (SCLMA) architecture. This progression from the original CLMA concept [Paper D & b] merges non-load modulation with improved back-off efficiency,

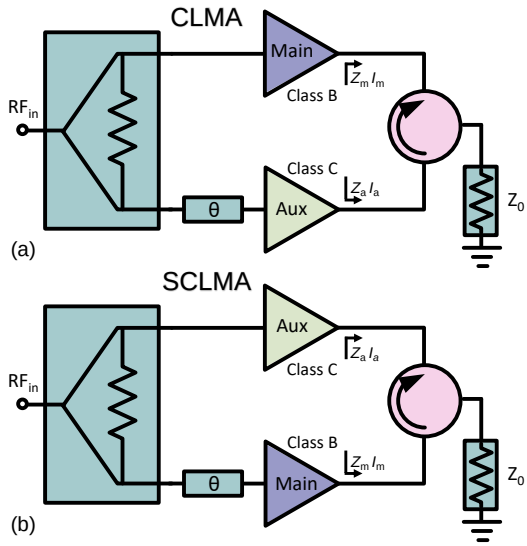


Figure 5.3: Block diagram of the (a) circulator load modulated amplifier (CLMA) and (b) sequential circulator load modulated amplifier (SCLMA).

showing promising potentials for broadband and high-efficiency applications.

5.2 Theoretical Performance

In Figure 5.3, we present ideal block diagrams for both the CLMA and SCLMA architectures. The SCLMA, similar to its CLMA counterpart, comprises a three-port non-reciprocal circulator combiner, a class-B biased Main amplifier, and a class-C biased Aux amplifier. A key distinction, however, lies in the positioning of the Main and Aux amplifiers; their placements are interchanged between the two architectures. Additionally, the driving conditions for both amplifier branches diverge notably. While the main amplifier of the CLMA functions in a continuous linear mode, the SCLMA relies on its main amplifier's saturation to boost back-off efficiency [101].

As described in [Paper G], the load impedance encountered by both the Main and Aux amplifiers within the SCLMA architecture is determined by exploiting the relations between voltage and current at the ports of the circulator. Therefore, for the SCLMA architecture, the load impedance of its Main amplifier remains constant across all driving power levels, equivalent to that of the Aux amplifier from the CLMA architecture.

The current drive profiles of the SCLMA are depicted in Figure 5.4(a). When the input voltage goes beyond the back-off level (β_{B}), the Main amplifier is notably over-driven. To present this in a more straightforward manner, we utilize a piece-wise current source model, reflecting the Main amplifier's saturation behavior. In contrast, the Aux amplifier, operating under a class C bias, becomes active only when the input voltage exceeds the back-off level. The voltage profiles and the theoretical efficiency performance of the SCLMA are illustrated in Figure 5.4(b) and (c). These plots highlight the capabil-

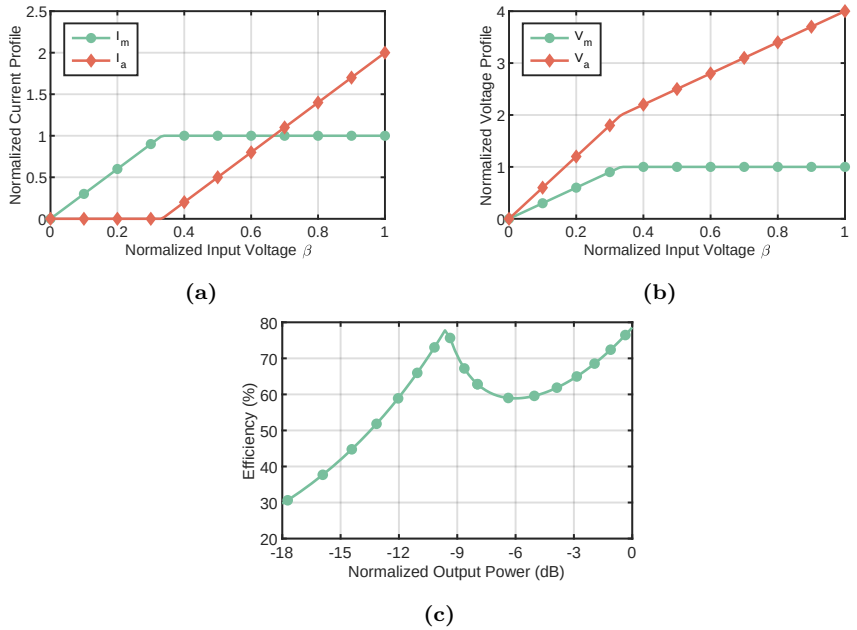


Figure 5.4: Normalized amplitude of the fundamental (a) currents and (b) voltage from the SCLMA versus normalized input drive voltage. (C) Drain efficiency of the SCLMA versus normalized output power.

ity of the SCLMA architecture to enhance deep back-off efficiency without load modulation. Furthermore, an important observation is that the optimal performance of the SCLMA requires a higher drain bias voltage for the Aux amplifier. To address the discrepancy in bias voltages between the Main and Aux amplifiers, it is advisable to select a DC supply voltage for the Main amplifiers that under-utilizes the transistor. It is worth noting that the SLMBA architecture demonstrates a similar behavior, as discussed in [26, 27, 97–99].

The operation of the SCLMA can thereby be generalized as follows: In the low-power region, prior to achieving the high-efficiency output power back-off level, the class-B biased Main amplifier governs both the output power and efficiency attributes of the SCLMA. During this phase, the class-C biased Aux amplifier remains inactive rendering its load impedance to be infinite. The Main amplifier is designed to reach saturation and peak efficiency when the overall output power reaches the back-off level. Conversely, in the high-power region after the high-efficiency back-off level, the Aux amplifier is turned on and starts to inject current into the combiner. Meanwhile, the load impedance of the Main amplifier remains constant, thereby maintaining its high efficiency. Moreover, with careful adjustment of the magnitude and phase delay of the currents, the high efficiency of the Aux amplifier can be achieved. As a result, the SCLMA architecture achieves overall high-efficiency performance consistently, from the back-off power level to the peak power.

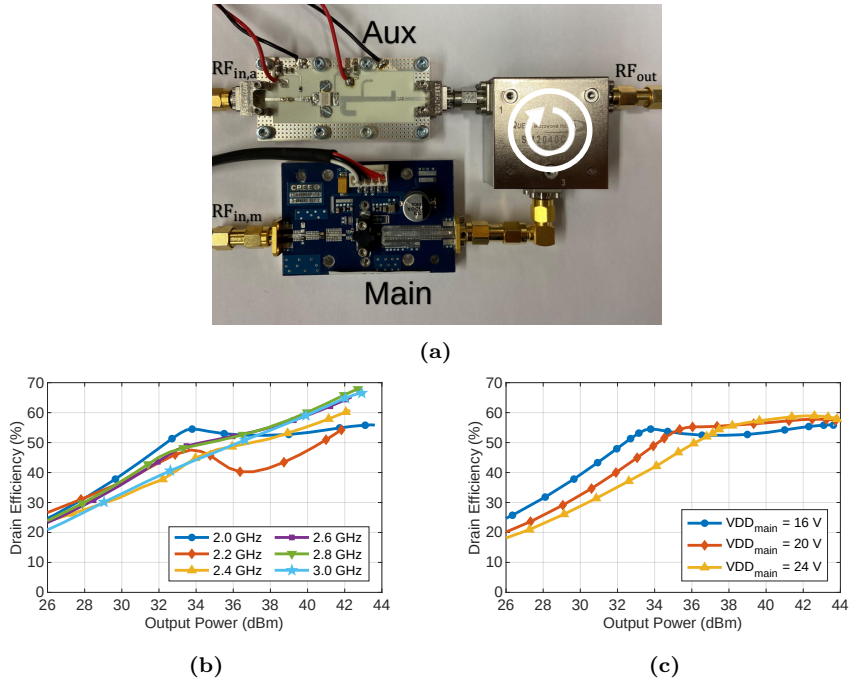


Figure 5.5: (a) Photograph of the dual-input SCLMA prototype circuit, (b) Measured drain efficiency versus output power across $2.0-3.0$ GHz, and (C) Measured drain efficiency at 2 GHz for different drain bias voltages of the Main amplifier.

5.3 Demonstrator Circuits

To validate the theory and underscore the practical viability of the SCLMA architecture, two demonstrator circuits are illustrated in [Paper F & G]. This section conducts a review of the measurement findings presented in these papers and draws comparisons between the results and the theoretical expectations.

5.3.1 Dual-Input Prototype

Figure 5.5(a) shows the fabricated dual-input SCLMA prototype circuit. The Aux amplifier circuit utilized a 25-W GaN HEMT CG2H40025F transistor from Wolfspeed as the active device. Meanwhile, the 6-W CHG4006P GaN test board also from Wolfspeed was chosen for the Main amplifier due to its high efficiency over a considerable bandwidth. Moreover, a Quest Microwave SM2040C09 circulator was served as the non-reciprocal output combiner.

The measured drain efficiency of the prototype is plotted in Figure 5.5(b) versus the measured output power across $2.0-3.0$ GHz. The results demonstrate a peak output power ranging from 42.0 to 43.4 dBm, over the entire frequency band. Meanwhile, the corresponding peak drain efficiency is measured within the range of $55-68\%$, while the efficiency at an 8-dB back-off power level varies between $46-53\%$. It is important to note that the back-off efficiency of the SCLMA can be conveniently adjusted by modifying the drain bias of its Main amplifier, as illustrated in Figure5.5(c). It is evident that a lower drain bias

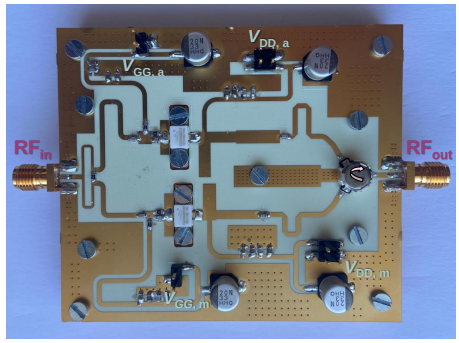
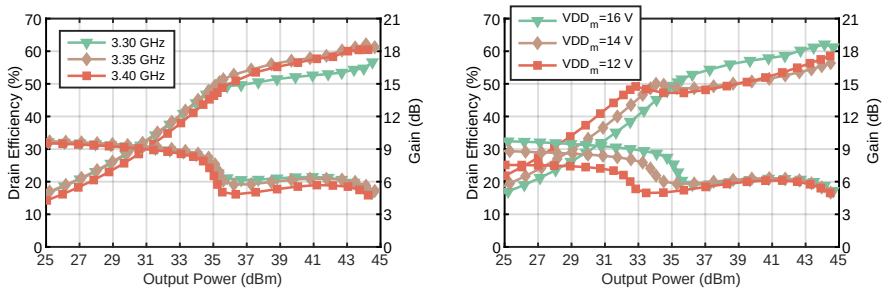


Figure 5.6: Photograph of the single RF-input SCLMA prototype circuit.



(a) **(b)**

Figure 5.7: Measured drain efficiency of the RF-input SCLMA versus output power (a) at $3.3 - 3.4$ GHz, and (b) at 3.35 GHz for varying drain bias voltage of the Main amplifier.

setting leads to efficiency enhancement in deeper power back-off levels. Note that a similar behavior is exhibited by the SLMBA architecture [26, 27, 97–99].

5.3.2 Single RF-Input Prototype

The fabricated single RF-input SCLMA prototype is demonstrated in Figure 5.6. The CW test results of the prototype circuit are shown in Figure 5.7(a). The measured peak output delivered power was 44.9 dBm at 3.35 GHz. Additionally, the measured peak drain efficiency was 62%, while at a back-off power level of 9.5 dB, the measured drain efficiency reaches 52%. Furthermore, as illustrated in Figure 5.7(b) , when $\mathrm{VDD_m}$ was set to 12 V, a drain efficiency of 49% was achieved at a 12-dB back-off power level.

5.4 Discussion

Despite the unique characteristic of the SCLMA, which includes a non-reciprocal output combiner, it is insightful to notice commonalities of the operational principles shared among the sequential PA, DEPA, SLMBA, and SCLMA. Specifically, these architectures utilize the sequential activation of Main and Aux amplifiers as the output power increases, for enhanced efficiency at deep power back-off. Furthermore, they all employ directional combining of the Aux

power to minimize or eliminate its load modulation effect on the Main device.

While the sequential mode of operation provides significant potential for broadband capabilities and enhanced efficiency at deep power back-off levels, its drawbacks must be acknowledged. Specifically, the deep saturation of the Main amplifier can lead to compromised linearity performance and potential reliability issues with the transistor.

5.5 Chapter Summary

In this chapter, the trade-offs of the active load modulated PA architectures were explored. It was observed that a higher load modulation ratio is associated with a deeper back-off power efficiency enhancement and a narrower bandwidth. Then we discussed the PA architectures that are not constrained by the need to balance between the back-off efficiency enhancement and load modulation ratio, namely the sequential PA, the DEPA, and the SLMBA.

Furthermore, the SCLMA architecture, built upon our previous findings, was proposed. Deep efficiency enhancement can be achieved by the SCLMA without load modulation. Two demonstrator circuits were introduced to validate the theoretical findings. It was observed from measurements that both prototypes demonstrated remarkable performance in achieving deep efficiency enhancement.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

With the increasing demand for data traffic, wireless communication systems require more spectrally efficient modulation schemes and frequency agility. As highlighted in the introduction chapter, it presents new challenges and requirements in enhancing the PA's energy efficiency and frequency adaptability. This thesis has introduced innovative operational modes, circuit topologies, and design methodologies, particularly targeting the transmission of modern communication signals with a large PAPR.

In this thesis, the intrinsic bandwidth constraints of the two-way Doherty PA were extensively explored. We presented the frequency responses for a variety of Doherty combiner networks. Furthermore, a novel Doherty combiner network was introduced with inherent broadband frequency and the capability to absorb output parasitics and packaged elements. Through the integration of the proposed combiner network and the introduced design methodology, a wideband Doherty PA was developed, demonstrating excellent performance.

To enhance efficiency at larger output power back-off levels, we focused on the realm of three-stage Doherty PA architectures. A load-pull-based three-port combiner synthesis approach for these three-stage Doherty PAs was subsequently proposed. Through experimental validation, this methodology was shown to unveil a new design space, effectively increasing the power utilization factor of the transistors. Consequently, the design and realization of highly efficient three-stage Doherty PAs with identical transistors and compact output combiners became possible, leading to potential enhancements in efficiency and cost reductions.

A novel PA architecture known as CLMA was introduced, featuring two active devices and utilizing a non-reciprocal circulator-based combiner. The operational principles of this architecture were comprehensively explained, leading to the design of a wideband demonstrator circuit with dual inputs and CM matching. Furthermore, a single RF-input Doherty-like CLMA was successfully fabricated and characterized, exhibiting promising performance.

Building upon the CLMA architecture and the sequential PA operation modes, the SCLMA architecture was proposed. This innovative architecture achieves enhanced back-off efficiency without resorting to load modulation, paving the way for superior deep back-off efficiency and broader bandwidth capabilities.

In summary, this thesis has introduced novel PA operational modes, circuit topologies, and design strategies, with a special emphasis on handling modern communication signals exhibiting a high PAPR. The findings will therefore contribute to the development of the next generation of energy-efficient, frequency-agile, and highly integrated wireless transmitters.

6.2 Future Work

There are several research directions arising from the work presented in this thesis which is in need of continued research, the author believes the following topics to be interesting directions for future research:

- **Mm-wave three-way high-efficiency silicon PAs.** In Chapter 3, the presented theory paves the way for examining combiner networks with diverse drive profiles. Exploring the multi-port coupled-line-based balun, especially in conjunction with series/parallel combining of multi-way high-efficiency PAs, proves particularly beneficial for silicon designs.
- **Wideband GaN MMIC Doherty PAs.** Chapter 2 introduces a combiner network that is well-suited for GaN MMIC implementation, given its flexibility. When paired with asymmetrical biasing, this approach holds promise for achieving a wideband MMIC Doherty design.
- **Improved linearity of GaN MMIC Doherty PAs.** The Doherty PA design that employs push-pull PAs utilizes distributed baluns with capacitive neutralization networks. This configuration, together with the series power combining, could potentially lead to improved AM-AM and AM-PM characteristics.
- **Reconfigurable SCLMA.** The SCLMA's reconfigurability offers potential advantages, such as adaptive back-off efficiency enhancement and addressing loading insensitivity issues.

Chapter 7

Summary of Appended Papers

Paper A

Doherty Power Amplifier Combiner Network for Improved Bandwidth and Efficiency

In this article, we propose and demonstrate a wideband Doherty combiner network. The proposed topology undergoes a thorough theoretical analysis, exploring its capabilities in terms of broadband frequency coverage and compactness. Furthermore, analytical expressions are derived to facilitate the synthesis of the proposed combiner network while accounting for the influence of output parasitics arising from the transistors. To validate the feasibility of the concept, a wideband prototype Doherty PA is designed and experimentally evaluated, covering $1.6 - 2.7$ GHz, utilizing GaN HEMT transistors.
My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper B

Design of a Compact GaN Power Amplifier with High Efficiency and Beyond Decade Bandwidth

This paper presents a PA design and network synthesis approach to achieve wideband and efficient performance with a compact circuit size. A design method is presented in detail to convert a canonical filter-based high-order matching network to the proposed matching configuration with transistor parasitic and packaged elements absorption, and a compact passive network footprint. As proof of concept, a prototype GaN HEMT PA is implemented. The measured results show that the fabricated prototype circuit achieves an output power of 41.9–44.3 dBm and a 55%–74% drain efficiency, over a record-high decade bandwidth.

My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper C

A Generic Theory for Design of Efficient Three-Stage Doherty Power Amplifiers

This paper proposed a load-pull-based design methodology for three-stage Doherty PAs. A compact output combiner network, together with the input phase delays, is derived directly from transistor load-pull data and the design requirements. The method is designed to enable high transistor power utilization by maintaining full voltage and current swings of the main and auxiliary amplifier cells. To demonstrate its feasibility, a 2.14-GHz 30-W three-stage Doherty PA with identical GaN HEMT transistors is designed, fabricated, and characterized with excellent performance.
My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper D

A Wideband and Highly Efficient Circulator Load Modulated Power Amplifier Architecture

This paper presents an innovative PA architecture named the CLMA. This architecture comprises a class-B biased Main amplifier, a class-C biased Aux amplifier, and a microwave circulator employed as the output combiner. The CLMA is able to achieve high efficiency at output power back-off levels. The paper provides a comprehensive analysis by presenting the complete theory and demonstrating a proof-of-concept wideband CLMA prototype circuit.
My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper E

RF-input Sequential Circulator Load Modulated Amplifier with Extended Efficiency Range

This paper introduces the design and analysis of an RF-input CLMA, with Doherty-like operation and efficiency enhancement. Through a theoretical study, the performance of the proposed architecture under varying isolation levels and losses is elucidated. To demonstrate the viability of the concept, a prototype RF-input CLMA employing GaN HEMT transistors and an SMT circulator is constructed with promising measurement performance.

My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper F

RF-input Sequential Circulator Load Modulated Amplifier with Extended Efficiency Range

This paper presents the analysis and design of an RF-input SCLMA that operates similarly to a sequential PA. The sequential arrangement achieves an extended back-off efficiency range without load modulation. The paper provides a theoretical examination, showing the performance of the proposed architecture under varied isolation levels and losses. Experiment results from the fabricated RF-input SCLMA exhibit excellent deep efficiency enhancement performance.
My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Paper G

Wideband Sequential Circulator Load Modulated Amplifier with Back-Off Efficiency Enhancement

This paper proposes the first SCLMA architecture with a dual-input topology. The sequential configuration resulted in excellent bandwidth and extended back-off efficiency enhancements. A wideband prototype PA based on GaN HEMT transistors, and a commercial circulator were employed to validate the SCLMA concept.
My contributions: *Development of concept and theory, design and implementation of the prototype circuit, performing the measurements, and writing of the manuscript, all with technical support or inputs from the co-authors.*

Acknowledgments

I would like to express my gratitude to the people who have supported me and made this work possible.

Thank you Prof. Herbert Zirath for being my examiner of both my MSc. and Ph.D. studies, and for giving me the opportunity to work and conduct research in an outstanding research group. My utmost appreciation is reserved for my main supervisor, Prof. Christian Fager. Your unwavering guidance, expertise, and patience have been instrumental in shaping my trajectory as an independent researcher. I am also grateful to Prof. Hua Wang for hosting my research visit at the IDEAS group at ETH Zurich. Collaborating with you and the IDEAS team members was genuinely enriching. Prof. Koen Buisman, your introduction to the world of microwave circuits was enlightening, and I value our constructive discussions. Thank you Dr. Jose-Ramon Perez-Cisneros for all the brainstorming, lab work, and coffee breaks during these challenging times. And Dr. Lena Peterson, thank you for the fruitful discussions.

Special mention to Edward for excellent collaborations in 45nm CMOS SOI, and Victor and Lars for fruitful discussions and for your great work handling the 22nm CMOS FD-SOI tape-outs. My sincere thanks also go to Haojie, for great collaborations in circuit design, manufacturing, and characterization. I would like to thank Yu and Aniello, for our SiGe BiCMOS circuit design collaborations, which have been inspirational and highly rewarding. Thank you, both Vessen and Gregor, for your work handling the 150nm GaN MMIC tape-outs. I express gratitude to my colleagues in MEL and TML for fostering an excellent work environment. To my peer doctoral students, Junjie, Husileng, Kai-Hsin, Martin, Frida, Dingyuan, Roger, and many others, I cherish the camaraderie we shared.

I am immensely thankful to my circle of friends, Alvaro, Ahmed, Sining, Han, Weijie, Kaiteng, Juling, Bowen, Jose, Isa, and others. Thank you for being there with me through thick and thin, and for sticking together all along.

I would like to express my deepest gratitude to my parents Jianfeng and Shuqiong, for their unconditional support and love throughout my life. My deepest appreciation goes to my wife Lei, your love and unwavering support have been my guiding light throughout this journey. I am sure that we are ready for the next chapter in our life.

This research was supported by:

The Efficient and Linear Millimeter Wave Transmitters (ELEMENT) project in the GigaHertz Centre, financed by the Swedish Government Agency for Innovation Systems (VINNOVA), Chalmers University of Technology, Ericsson, Gotmic, Infineon Technologies Austria, Qamcom, RISE, and SAAB.

The Wideband and Efficient DSP-assisted Transceivers (WINTER) project, financed by Chalmers, Ericsson, Gotmic, Infineon, Kongsberg, Saab, and UniqueSec.

My research visit to ETH Zurich, Switzerland was supported by grants from the Ericsson Research Foundation.

Bibliography

[1] "Cisco global networking trends report," Cisco, Tech. Reb., 2023.

[2] "Cisco visual networking index: Global mobile data traffic forecast update, 2018–2023 white paper," Cisco, Tech. Reb., Mar. 2020.

[3] "Ericsson mobility report," Ericsson AB, Tech. Reb., Nov. 2023.

[4] U. Gustavsson, P. Frenger, C. Fager, T. Eriksson, H. Zirath, F. Dielacher, C. Studer, A. Pärssinen, R. Correia, J. N. Matos, D. Belo, and N. B. Carvalho, "Implementation challenges and opportunities in beyond-5G and 6G communication," *IEEE J. Microw.*, vol. 1, no. 1, pp. 86–100, 2021.

[5] C. Fager, T. Eriksson, F. Barradas, K. Hausmair, T. Cunha, and J. C. Pedro, "Linearity and efficiency in 5G transmitters: New techniques for analyzing efficiency, linearity, and linearization in a 5G active antenna transmitter context," *IEEE Microwave Mag.*, vol. 20, no. 5, pp. 35–49, 2019.

[6] H. Wang, P. M. Asbeck, and C. Fager, "Millimeter-wave power amplifier integrated circuits for high dynamic range signals," *IEEE J. Microw.*, vol. 1, no. 1, pp. 299–316, 2021.

[7] Z. Zhang, K. Long, A. V. Vasilakos, and L. Hanzo, "Full-Duplex wireless communications: Challenges, solutions, and future research directions," *Proc. IEEE*, vol. 104, no. 7, pp. 1369–1409, 2016.

[8] H. Zhou, "Design of mm-wave front-end for multiantenna communication systems," Chalmers University of Technology, Gothenburg, Sweden, 2018.

[9] G. Auer, O. Blume, and V. Giannini, "Energy efficiency analysis of the reference systems, areas of improvements and target breakdown," EARTH project deliverable D2.3, Tech. Rep., Jan. 2010.

[10] "Improving energy performance in 5G networks and beyond," Ericsson AB, Tech. Reb., Aug. 2022.

[11] S. K. A. Landou and A. N. Barreto, "Use of comp in 4G cellular networks for increased network energy efficiency," in *Proc. Int. Workshop Telecommun. (IWT)*, 2015, pp. 1–6.

[12] H. Zhou, "Theory and design of efficient active load modulation power amplifiers," Chalmers University of Technology, Gothenburg, Sweden, 2021.

[13] L. Guan and A. Zhu, "Green communications: Digital predistortion for wideband RF power amplifiers," *IEEE Microwave Mag.*, vol. 15, no. 7, pp. 84–99, 2014.

[14] V. Åberg, H. Zhou, C. Fager, and L. Svensson, "Rf pa predistortion using non-linear rf-dacs," in *Proc. IEEE Nordic Circuits Syst. Conf. (NorCAS)*, 2022, pp. 1–6.

[15] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. of the IRE*, vol. 40, no. 7, pp. 803–806, 1952.

[16] A. Saleh and D. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying-envelope signals," *IEEE Trans. Microw. Theory Techn.*, vol. 31, no. 1, pp. 51–56, 1983.

[17] F. Raab, "High-efficiency linear amplification by dynamic load modulation," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, vol. 3, 2003, pp. 1717–1720 vol.3.

[18] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos, and H. Zirath, "Design of varactor-based tunable matching networks for dynamic load modulation of high power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1110–1118, 2009.

[19] H. Chireix, "High power outphasing modulation," *Proc. Inst. Radio Eng*, vol. 23, no. 11, pp. 1370–1392, 1935.

[20] W. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng*, vol. 24, no. 9, pp. 1163–1182, 1936.

[21] R. Pengelly, C. Fager, and M. Ozen, "Doherty's legacy: A history of the Doherty power amplifier from 1936 to the present day," *IEEE Microwave Mag.*, vol. 17, no. 2, pp. 41–58, 2016.

[22] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho, and B. Kim, "The Doherty power amplifier: Review of recent solutions and trends," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 559–571, 2015.

[23] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband Doherty power amplifier design for 5G," *IEEE Microwave Mag.*, vol. 21, no. 4, pp. 57–75, 2020.

[24] P. Saad, R. Hou, R. Hellberg, and B. Berglund, "A 1.8–3.8-GHz power amplifier with 40% efficiency at 8-dB power back-off," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 11, pp. 4870–4882, 2018.

[25] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, 2016.

[26] Y. Cao and K. Chen, "Pseudo-Doherty load-modulated balanced amplifier with wide bandwidth and extended power back-off range," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3172–3183, 2020.

[27] J. Pang, Y. Li, M. Li, Y. Zhang, X. Y. Zhou, Z. Dai, and A. Zhu, "Analysis and design of highly efficient wideband RF-input sequential load modulated balanced power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 5, pp. 1741–1753, 2020.

[28] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. Inst. Radio Eng.*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[29] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *IEEE Microwave Mag.*, vol. 7, no. 5, pp. 42–50, Nov. 2006.

[30] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.

[31] J. Pang, S. He, C. Huang, Z. Dai, J. Peng, and F. You, "A post-matching Doherty power amplifier employing low-order impedance inverters for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4061–4071, 2015.

[32] J. Xia, M. Yang, Y. Guo, and A. Zhu, "A broadband high-efficiency Doherty power amplifier with integrated compensating reactance," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2014–2024, Jul. 2016.

[33] W. Chen, S. A. Bassam, X. Li, Y. Liu, K. Rawat, M. Helaoui, F. M. Ghannouchi, and Z. Feng, "Design and linearization of concurrent dual-band Doherty power amplifier with frequency-dependent power ranges," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 10, pp. 2537–2546, 2011.

[34] H. Lyu, Y. Cao, and K. Chen, "Highly efficient and linearity-enhanced quasi-balanced Doherty power amplifier at 3.5 GHz: Linear quasi-balanced Doherty power amplifier design methodology," *IEEE Microw. Mag.*, vol. 24, no. 3, pp. 52–58, 2023.

[35] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, 2019.

[36] E. Kaymaksut, D. Zhao, and P. Reynaert, "Transformer-based Doherty power amplifiers for mm-wave applications in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 4, pp. 1186–1192, 2015.

[37] M. Iwamoto, A. Williams, Pin-Fan Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2472–2479, Dec. 2001.

[38] J. Kim, B. Fehri, S. Boumaiza, and J. Wood, "Power efficiency and linearity enhancement using optimized asymmetrical Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 2, pp. 425–434, Feb. 2011.

[39] H. Jang, P. Roblin, C. Quindroit, Y. Lin, and R. D. Pond, "Asymmetric Doherty power amplifier designed using model-based nonlinear embedding," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3436–3451, Dec. 2014.

[40] Youngoo Yang, Jeonghyeon Cha, Bumjae Shin, and Bumman Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 986–993, Apr. 2003.

[41] M. Özen, K. Andersson, and C. Fager, "Symmetrical Doherty power amplifier with extended efficiency range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1273–1284, Apr. 2016.

[42] W. Hallberg, M. Özen, D. Gustafsson, K. Buisman, and C. Fager, "A Doherty power amplifier design method for improved efficiency and linearity," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4491–4504, 2016.

[43] O. A. Iupikov, W. Hallberg, R. Maaskant, C. Fager, R. Rehammar, K. Buisman, and M. V. Ivashina, "A dual-fed PIFA antenna element with nonsymmetric impedance matrix for high-efficiency Doherty transmitters: Integrated design and OTA-characterization," *IEEE Trans. Antennas Propag.*, vol. 68, no. 1, pp. 21–32, 2020.

[44] O. A. Iupikov, J.-R. Perez-Cisneros, P. Meyer, D. Åkesson, R. Maaskant, K. Buisman, R. Rehammar, C. Fager, and M. V. Ivashina, "A cavity-backed patch antenna with distributed multi-port feeding, enabling efficient integration with Doherty power amplifier and band-pass filter," *IEEE Trans. Antennas Propag.*, vol. 69, no. 8, pp. 4412–4422, 2021.

[45] M. Özen, N. Rostomyan, K. Aufinger, and C. Fager, "Efficient millimeter wave Doherty PA design based on a low-loss combiner synthesis technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 12, pp. 1143–1145, 2017.

[46] N. Rostomyan, M. Özen, and P. Asbeck, "28 GHz Doherty power amplifier in CMOS SOI with 28% back-off PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 446–448, 2018.

[47] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet, and J. A. Jayamon, "Power amplifiers for mm-wave 5G applications: Technology comparisons and CMOS-SOI demonstration circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3099–3109, 2019.

[48] A. Grebennikov, *Radio Frequency and Microwave Power Amplifiers, Volume 2 - Efficiency and Linearity Enhancement Techniques.* Institution of Engineering and Technology, 2019, ch. 5.

[49] P. Colantonio, F. Giannini, R. Giofre, and L. Piazzon, "Theory and experimental results of a class f ab-c doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 8, pp. 1936–1947, 2009.

[50] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband Doherty power amplifier design for 5G," *IEEE Microw. Mag.*, vol. 21, no. 4, pp. 57–75, 2020.

[51] J. H. Qureshi, L. Nan, E. Neo, F. V. Rijs, I. Blednov, and L. de Vreede, "A wide-band 20W LDMOS Doherty power amplifier," in *IEEE MTT-S Int.Microw. Symp. Dig,*, 2010, pp. 1–1.

[52] J. M. Rubio, J. Fang, V. Camarchia, R. Quaglia, M. Pirola, and G. Ghione, "3–3.6-GHz wideband GaN Doherty power amplifier exploiting output compensation stages," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 8, pp. 2543–2548, 2012.

[53] K. Bathich, A. Z. Markos, and G. Boeck, "Frequency response analysis and bandwidth extension of the Doherty amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 934–944, 2011.

[54] D. Gustafsson, C. M. Andersson, and C. Fager, "A modified Doherty power amplifier with extended bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 533–542, Jan. 2013.

[55] D. Y.-T. Wu and S. Boumaiza, "A modified Doherty configuration for broadband amplification using symmetrical devices," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3201–3213, 2012.

[56] X. A. Nghiem, J. Guan, and R. Negra, "Broadband sequential power amplifier with Doherty-type active load modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2821–2832, 2015.

[57] X.-H. Fang, H.-Y. Liu, K.-K. M. Cheng, and S. Boumaiza, "Modified Doherty amplifier with extended bandwidth and back-off power range using optimized peak combining current ratio," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5347–5357, 2018.

[58] M. Akbarpour, M. Helaoui, and F. M. Ghannouchi, "A transformer-less load-modulated (TLLM) architecture for efficient wideband power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 9, pp. 2863–2874, 2012.

[59] X. Chen, W. Chen, F. M. Ghannouchi, Z. Feng, and Y. Liu, "A broadband Doherty power amplifier based on continuous-mode technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4505–4517, 2016.

[60] A. Grebennikov and J. Wong, "A dual-band parallel Doherty power amplifier for wireless applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 10, pp. 3214–3222, 2012.

[61] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "A closed-form design technique for ultra-wideband Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3414–3424, 2014.

[62] A. Barakat, M. Thian, V. Fusco, S. Bulja, and L. Guan, "Toward a more generalized Doherty power amplifier design for broadband operation," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 3, pp. 846–859, 2017.

[63] H. Zhou, H. Chang, and C. Fager, "Symmetrical Doherty power amplifier with high efficiency and extended bandwidth," in *Proc. Int. Workshop Integr. Nonlinear Microw. MillimetreWave Circuits (INMMiC)*, 2023, pp. 1–3.

[64] J. Haider, H. Zhou, P. Saad, R. Hou, and C. Fager, "Design and validation of a concurrent dual-band 1.84/2.65 GHz GaN Doherty power amplifier," in *Proc. Int. Workshop Integr. Nonlinear Microw. MillimetreWave Circuits (INMMiC)*, 2023, pp. 1–4.

[65] H. Zhou, J.-R. Perez-Cisneros, B. Langborn, T. Eriksson, and C. Fager, "Design of a compact GaN power amplifier with high efficiency and beyond decade bandwidth," *IEEE Microw. Wireless Compon. Lett.*, pp. 1–4, 2022.

[66] G. Matthaei, "Tables of Chebyshev impedance–transforming networks of low-pass filter form," *Proceedings of the IEEE*, vol. 52, no. 8, pp. 939–963, 1964.

[67] K. Chen and D. Peroulis, "Design of highly efficient broadband class-E power amplifier using synthesized low-pass matching networks," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3162–3173, 2011.

[68] ——, "Design of adaptive highly efficient GaN power amplifier for octave-bandwidth application and dynamic load modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1829–1839, 2012.

[69] ——, "Design of broadband highly efficient harmonic-tuned power amplifier using in-band continuous class-F^{-1}/F mode transferring," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 4107–4116, 2012.

[70] F. H. Raab, "Efficiency of Doherty RF power-amplifier systems," *IEEE Trans. Broadcast.*, vol. BC-33, no. 3, pp. 77–83, Sep. 1987.

[71] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 3, pp. 852–860, Mar. 2005.

[72] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 866–879, May. 2007.

[73] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.

[74] A. Barthwal, K. Rawat, and S. K. Koul, "A design strategy for bandwidth enhancement in three-stage Doherty power amplifier with extended dynamic range," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 1024–1033, Feb. 2018.

[75] ——, "Dual input digitally controlled broadband three-stage Doherty power amplifier with back-off reconfigurability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 4, pp. 1421–1431, Mar. 2021.

[76] W. Neo, M. Pelk, L. de Vreede, Y. Zhao, and R. Gajadharsing, "3-way Doherty amplifier with minimum output network," 2009, NXP B.V. - Eindhoven; WO 2009/081341; H03F.

[77] I. Kim, J. Moon, S. Jee, and B. Kim, "Optimized design of a highly efficient three-stage Doherty PA using gate adaptation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2562–2574, Aug. 2010.

[78] H. Golestaneh, F. A. Malekzadeh, and S. Boumaiza, "An extended-bandwidth three-way Doherty power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 9, pp. 3318–3328, Aug. 2013.

[79] A. Barthwal, K. Rawat, and S. Koul, "Bandwidth enhancement of three-stage Doherty power amplifier using symmetric devices," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2399–2410, Aug. 2015.

[80] J. Xia, W. Chen, F. Meng, C. Yu, and X. Zhu, "Improved three-stage Doherty amplifier design with impedance compensation in load combiner for broadband applications," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 2, pp. 778–786, Feb. 2019.

[81] H. Zhou, J.-R. Perez-Cisneros, S. Hesami, K. Buisman, and C. Fager, "A generic theory for design of efficient three-stage Doherty power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1242–1253, 2022.

[82] P. H. Pednekar and T. W. Barton, "RF-input load modulated balanced amplifier," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2017, pp. 1730–1733.

[83] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-input load modulated balanced amplifier with octave bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5181–5191, 2017.

[84] P. H. Pednekar, W. Hallberg, C. Fager, and T. W. Barton, "Analysis and design of a Doherty-like RF-input load modulated balanced amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5322–5335, 2018.

[85] R. Quaglia and S. Cripps, "A load modulated balanced amplifier for telecom applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1328–1338, 2018.

[86] J. Pang, C. Chu, Y. Li, and A. Zhu, "Broadband RF-input continuous-mode load-modulated balanced power amplifier with input phase adjustment," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 10, pp. 4466–4478, 2020.

[87] H. Zhou, J.-R. Perez-Cisneros, and C. Fager, "Circulator load modulated amplifier: A non-reciprocal wideband and efficient PA architecture," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2021, pp. 603–605.

[88] H. Zhou, J.-R. Perez-Cisneros, B. Langborn, T. Eriksson, and C. Fager, "A wideband and highly efficient circulator load modulated power amplifier architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 8, pp. 3117–3129, 2023.

[89] J.-R. Perez-Cisneros, H. Zhou, C. Fager, and K. Buisman, "Emulation of non-reciprocity applied in load-modulated power amplifier architectures using single amplifier load-pull measurements," in *Proc. 51st Eur. Microw. Conf. (EuMC)*, 2022, pp. 647–650.

[90] P. Saad, H. Zhou, J.-R. Perez-Cisneros, R. Hou, and B.-B. Fager, Christian, "Doherty load modulation based on non-reciprocity," in *Proc. 51st Eur. Microw. Conf. (EuMC)*, 2022, pp. 938–941.

[91] H. Carlin and P. Crepeau, "Theoretical limitations on the broad-band matching of arbitrary impedances," *IRE Trans. Circuit Theory*, vol. 8, no. 2, pp. 165–165, 1961.

[92] J. C. Pedro and L. C. Nunes, "Efficiency dependence on the load-pull ratio of a Doherty pa," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2014, pp. 1–4.

[93] S. J. C. H. Theeuwen and J. H. Qureshi, "LDMOS technology for RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1755–1763, 2012.

[94] S. Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition*, Artech, 2006.

[95] T. Lehmann and R. Knoechel, "Design and performance of sequential power amplifiers," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2008, pp. 767–770.

[96] G. R. Nikandish, R. B. Staszewski, and A. Zhu, "Unbalanced power amplifier: An architecture for broadband back-off efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 367–381, 2021.

[97] Y. Cao, H. Lyu, and K. Chen, "Asymmetrical load modulated balanced amplifier with continuum of modulation ratio and dual-octave bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 682–696, 2021.

[98] ——, "Continuous-mode hybrid asymmetrical load-modulated balanced amplifier with three-way modulation and multi-band reconfigurability," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 3, pp. 1077–1090, 2022.

[99] Y. Cao and K. Chen, "Hybrid asymmetrical load modulated balanced amplifier with wide bandwidth and three-way-Doherty efficiency enhancement," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 721–724, 2021.

[100] ——, "Dual-octave-bandwidth RF-input pseudo-Doherty load modulated balanced amplifier with ≥ 10-dB power back-off range," in *Proc. IEEE MTT-S Int. Microw. Symp. Dig*, 2020, pp. 703–706.

[101] H. Zhou, J.-R. Perez-Cisneros, and C. Fager, "Wideband sequential circulator load modulated amplifier with back-off efficiency enhancement," in *Proc. 52nd Eur. Microw. Conf. (EuMC)*, 2022, pp. 214–217.