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Energy Reports 9 (2023) 337–342

Contents lists available at ScienceDirect

Energy Reports

journal homepage: www.elsevier.com/locate/egyr

# Evaluation of antiparallel SiC Schottky diode in SiC MOSFET phase-leg configuration of synchronous rectifier☆

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ARTICLE INFO

*Keywords:*
SiC MOSFET
Synchronous rectification
Anti-parallel
Phase-leg configuration

ABSTRACT

The MOSFET synchronous rectification (SR) is widely used to reduce the conduction loss during the freewheeling period. Due to the wide band gap of silicon carbide (SiC), the intrinsic body diode of SiC MOSFET exhibits a high voltage drop. Therefore, SiC Schottky diodes (SBD) and SiC MOSFETs are usually used in reverse parallel to reduce power loss. However, the increase of equivalent junction capacitance due to the addition of an external SiC SBD could bring larger turn-on current on opposite power transistor of the phase-leg. Furthermore, as the parasitic inductance associated with layout hinders the prompt transfer of current between SiC SBD and body diode, the external SiC SBD cannot be fully utilized, and it may deteriorate the overall performance, especially at heavy load. We comprehensively compare power losses when SiC SBD are antiparallel or not, at different working conditions, including different layout compactness, load current and dead time. It's hard to get the effect of loss reduction loss when add antiparallel SiC SBD due to the parasitic inductance induced by the layout. The results can provide a guidance to properly select SiC SBD in a phase-leg configuration under SR mode for freewheeling during the dead time.

## 1. Introduction

One of the enabling technologies for electric drive systems is to develop power electronic converters with higher reliability and efficiency, including AC-DC, DC-DC and DC-AC converters (Wang et al., 2018; Yamaguchi et al., 2020). Synchronous rectification (SR) is widely used to replace the traditional diode rectifier and reduce the conduction loss in various power converters because the channel of MOSFETs can conduct in both directions with a positive gate bias. During the freewheeling period, MOSFETs provide a current path that has a smaller voltage drop across both ends than traditional diodes. The freewheeling current only flows through the body diode, during the dead time. The presence of wide bandgap material silicon carbide (SiC) allows the MOSFET to compete with Si CoolMOS and IGBT in the range of 600 V and above, and SiC MOSFET is regarded as an attractive alternative for applications in MEA system. Due to the wide band gap of SiC material, the body diode of SiC MOSFET exhibits a higher voltage drop than that of Si MOSFET (Qin et al., 2021; Zhou et al., 2015). It leads to a high conduction loss when operating as a rectifier. Hence, an antiparallel SiC Schottky diode is normally employed as a freewheeling diode (FWD), which is also recommended by the device supplier (Jahdi et al., 2015; Yamaguchi et al., 2020). In addition, the method of antiparallel SBD is widely used in commercial off the shelf all-SiC power modules (Yamaguchi et al., 2020; Tiwari et al., 2018).

The body diode of SiC MOSFET shows an excellent reverse recovery performance due to the much shorter lifetime of minority carriers, and an antiparallel SiC SBD will increase the equivalent junction capacitance of the body diode, the charging and discharging process of the equivalent junction capacitance will increase turn-on transient current of the opposite SiC MOSFET when compared to the conditions without the external SiC SBD (Qin et al., 2021; Sun et al., 2020). As a consequence, it becomes unnecessary to use an additional FWD to improve the dynamic performance of body diode (Sun et al., 2020; Yamaguchi et al., 2020; Tiwari et al., 2018). Some previous works have investigated the advantages of SiC power converters without the external FWD (Yamaguchi et al., 2020). In (Jahdi et al., 2015; Yamaguchi and Katsura, 2015), the temperature instability of the phase-leg configuration led to the reverse recovery loss of the bulk diode being greater than the reverse SiC SBD, but there was a lack of analysis of the total loss of the phase leg configuration. (Kadavelugu et al., 2019; Yamaguchi and Katsura, 2015)

☆ 2023 8th International Conference on Sustainable and Renewable Energy Engineering (ICSREE 2023) 11–13 May, Nice, France

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https://doi.org/10.1016/j.egyr.2023.09.126
Received 31 August 2023; Accepted 21 September 2023
Available online 10 October 2023

proposed a detailed experiment comparison between conditions with antiparallel SBD and without it in a SiC voltage source inverter using SR, and the results showed that the external SiC SBD would lower the efficiency when the switching frequency and load current is increased. The results give a guidance on how to use a SiC SBD in a SiC MOSFET inverter. Although these works have proven the high efficiency advantage of SR without the use of an external SiC SBD from the detailed experiments, the real reason that an anti-parallel SiC SBD can bring much more losses than only using SR without an external SBD is unclear, and the detailed analysis considering non-ideal characteristics associated with power devices and real circuit layout is still needed. In some special cases, adding antiparallel SBD can reduce reverse recovery loss and freewheeling loss, but it can worsen the power density of the SR converter. Therefore, it is necessary to specify when it is necessary to add antiparallel SBD and the parameter changes after adding antiparallel SBD to the SR converter (Yin et al., 2018; Zhang et al., 2017).

This article analyzes the parameter changes brought about by antiparallel SiC SBD, and analyzes the influence of parasitic parameters on the commutation process under different load currents and dead time. Thus, the total power losses when using an external SiC SBD or not are thoroughly compared at different conditions. The rest of this paper is organized as follows. In Section II, we present an improved analytical model and loss analysis for a SiC MOSFET phase-leg configuration, considering the parasitic inductance and commutation time in freewheeling loop (the branch composed of anti-parallel diode and power transistor). In Section III, the simulations of a phase-leg configuration using SR are conducted to reveal the impact of different factors on commutation time, and corresponding power losses. In Section IV, a double pulse experimental platform is established, and total losses comparison of phase-leg with antiparallel SiC SBD and without it are conducted. Finally, some conclusions are summarized in section V.

## 2. Theoretical analysis and power loss analysis

### 2.1. Operating principle of a phase-leg configuration during a switching period

Fig. 1(a) shows the models of a phase-leg configuration under real situation. LP is the parasitic inductance in the branch composed of SiC SBD and load inductance. QH and QL stand for the upper transistor and the lower one respectively, L represents as load inductance, DH represents as anti-parallel SiC SBD and Vbus as bus voltage. For the ideal phase-leg configuration, the freewheeling current only flows through SiC SBD during the dead time. But for the real situation, the freewheeling current cannot be transferred to SiC SBD instantly due to the existence of LP, and it will firstly flow through body diode and SiC SBD simultaneously, and then all flow through SiC SBD.

As shown in Fig. 1(b) to (f) and Fig. 2, the operating modes of the half bridge circuit using SR are given in detail, and the upper transistor participates in freewheeling. Since the channel on-resistance of SiC MOSFET is at the milliohm level and its voltage drop is much smaller than that of the freewheeling diode, the freewheeling current only flows through the channel of SiC MOSFET under the SR mode, but during the dead time, the diode participates in freewheeling. The operating modes of the half bridge circuit under SR mode can be divided into five stages.

Stage1[0-t1]: The transistor QL is in the on state, and its gate-source voltage is VGS. The load current flows from the load inductor to QL, and the drain-source voltage of QL remains at zero.

Stage2[t1-t2]: During the dead time(t1-t3) prior to turn-on of QH, also called turn-on dead time(td-on), QL is slowly turned off and SiC SBD starts freewheeling stage and the freewheeling current in the load inductor would instantly commutate to the channel under the ideal situation(the waveforms representing ideal situation is described by green wire) at t1, but the freewheeling current gradually commutates to SiC SBD due to the parasitic inductance LP and the delay of the gate driver of QL. The commutation time is named turn-on commutation time ts-on.

Stage3[t2-t3]: The freewheeling current completely commutates to

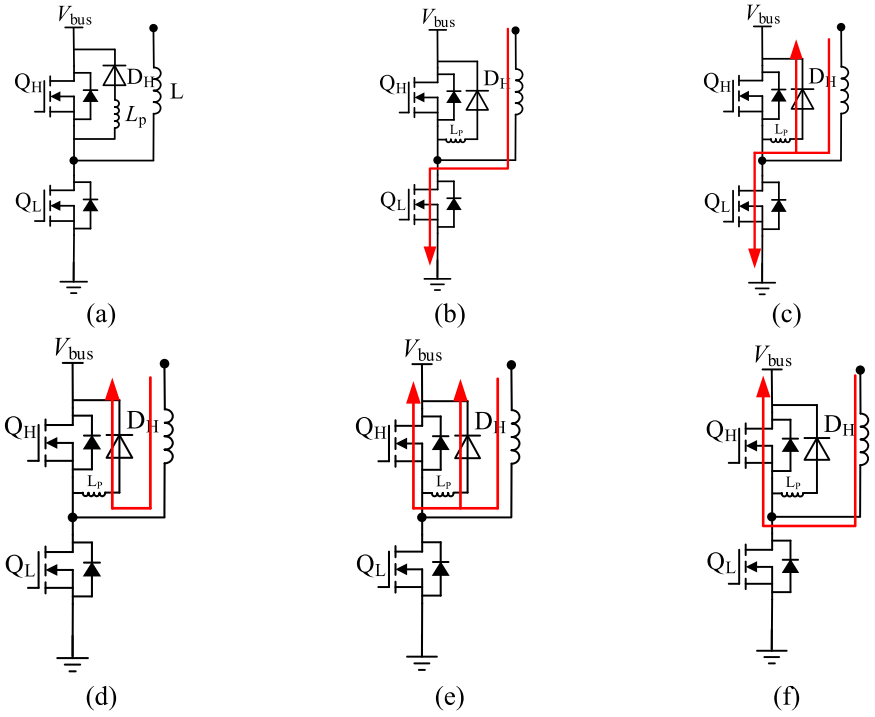


**Fig. 1.** Operating modes of the half bridge circuit using SR. (a) Real situation; (b) Mode 1 (0-$t_1$); (c) Model 2 ($t_1$-$t_2$); (d) Model 3 ($t_2$-$t_3$); (e) Model 4 ($t_3$-$t_4$); (f) Model 5 ($t_4$-$t_5$).

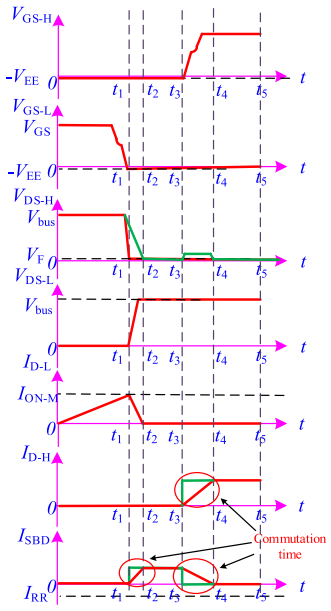


**Fig. 2.** Waveforms of the half bridge circuit using SR.

SiC SBD from QL.

Stage4[t3-t4]: The transistor QH is turned on when the gate-source voltage rises to VGS at t3, and the freewheeling current in the load inductor would instantly commutate to the channel under the ideal situation (the waveforms representing ideal situation is described by green wire), but the real current slowly commutates from SiC SBD to the channel of the transistor QH due to the parasitic inductance LP and the delay of the gate driver of QH. Both the channel and SiC SBD work in the freewheeling stage. This period is called SR commutation time ts-SR.

Stage5[t4-t5]: The freewheeling current completely commutates to the channel of QH from SiC SBD.

The stage that $Q_L$ begins to be turned on and SiC SBD finishes freewheeling stage is called turn-off dead time($t_{D\text{-}off}$), and during this stage, there will occur a commutation stage between SiC SBD and body diode, which has a similar modal analysis to the stage between the channel and SBD. In order to get a unified expression to facilitate analysis, we define $t_{s\text{-}on}$, $t_{s\text{-}off}$ and $t_{s\text{-}SR}$ as commutation time $t_s$, and the relationship between commutation time and parasitic inductance is given by (1):

$$L_p = \frac{V_F \cdot t_s}{i} \tag{1}$$

Where i represents load current, and VF represents equivalent conduction voltage drop composed of the power transistor's channel, the body diode, and SiC SBD.

The changing situations can be deduced from the analysis that different freewheeling ways have different VF and ts as shown in Fig. 3, and their working characteristics will be changed as shown in Fig. 3. From theoretical analysis, it can be seen that compared to the ideal situation, the practical phase-leg configuration during dead time will experience a stage that SiC SBD and body diode simultaneously provide freewheeling paths, and SiC SBD undergoes a slow commutation process.

### 2.2. Loss analysis

Through the previous analysis of operating principle, it can be concluded that the overall loss related with freewheeling ways of a phase-leg configuration $P_{tot}$ is composed of switching loss $P_{on\_L}$ and $P_{off\_L}$ of $Q_L$, the reverse recovery loss of the freewheeling diode (including SBD and body diode) $P_{rr}$, the freewheeling loss during dead time of the freewheeling diode $P_{FW\text{-}D}$, and the channel conduction loss of $Q_H$ $P_{FW\text{-}channel}$.

$$P_{tot} = P_{on\_L} + P_{off\_L} + P_{rr} + P_{FW-D} + P_{FW-channel} \tag{2}$$

Among them, it is obvious that the $P_{on\_L}$, $P_{off\_L}$ and $P_{rr}$ are affected by the increase of junction capacitance brought by SBD, while the freewheeling loss is affected by the layout is the focus of this study.

### 2.3. Freewheeling loss analysis

Channel conduction loss exists in power transistor during on-state. Due to the parasitic inductance $L_P$ brought by SiC SBD, there will exist a period of time called $t_{s\text{-}SR}$ when both the channel and SiC SBD provide freewheeling paths in the SR stage. Otherwise, there will be no commutation time when there is no parallelled diode. Therefore, the circuit will have relatively larger conduction voltage drop $V_F$' during $t_{s\text{-}SR}$, which produce more freewheeling loss than non-SBD condition. The channel conduction loss and freewheeling loss in SR stage is given by (3):

$$\begin{aligned} P_{FW-channel} &= 2f_s \int_0^{t_{on\_state}} V_F \cdot I_{channel} \\ &= 2f_s \left( \int_0^{t_{s-SR}} V_F' \cdot I_{channel} + \int_{t_{s-SR}}^{t_{on\_state}} V_F \cdot I_{channel} \right) \end{aligned} \tag{3}$$

Where $t_{SR}$ is SR time, $t_{on\_state}$ is ON time, $I_{channel}$ is the current in the channel of $Q_H$, $T$ is switching period.

During the turn-off dead time, the commutation stage also occurs, which similar to the turn on dead time. The freewheeling loss during dead time is given by (4):

$$P_{loss} = \begin{cases} 2f_s \int_0^{t_d} U_F \cdot I \cdot dt L_P = 0 \\ 2f_s \left( \int_0^{t_s} V_F' \cdot I \cdot dt + \int_{t_s}^{t_d} V_F \cdot I \cdot dt \right) 0 < L_P < L_{Limit} \\ 2f_s \int_0^{t_d} V_F' \cdot I \cdot dt L_P > L_{Limit} \end{cases} \tag{4}$$

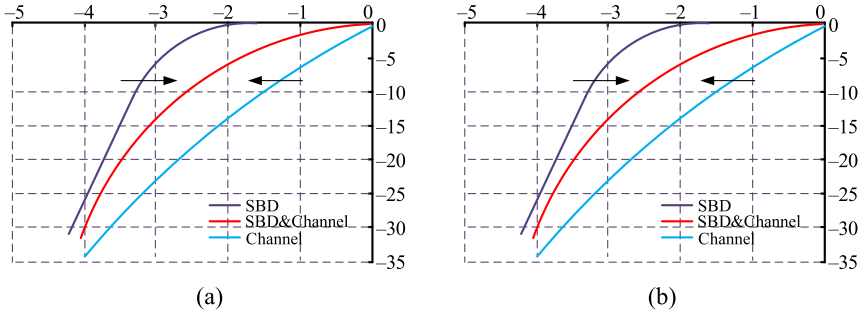


**Fig. 3.** The change of operating characteristics during commutation time. (a) the characteristic curve in third quadrant during $t_{s\text{-}on}$; (b) the characteristic curve in third quadrant during $t_{s\text{-}off}$.

It can be seen that the parasitic inductance connected to the SiC SBD will increase commutation time during dead time, and thus increase power loss, which will deteriorate the advantage of conduction loss reduction brought by parallelling SiC SBD. Therefore, whether or not to parallel SiC SBD with SiC MOSFET in a typical phase-leg configuration using SR needs to comprehensively evaluate the overall loss of the phase-leg configuration $P_{tot}$ at different conditions, such as load current level, layout compactness (the parasitic inductance in the freewheeling loop), and dead time.

## 3. Simulation verifications

### 3.1. Simulation results

A simulation model of a phase-leg configuration with SR control consisting of SiC MOSFET (SCT3060AL) and SiC SBD (SCS240AE) was established. Table 1 lists main parameters of the body diode of SCT3060AL with a rating of 650 V/40 A and SCS240AE2 with a rating of 650 V/39 A at some specific temperature.

Compared with the body diode of SiC MOSFET, the reverse recovery charge of SiC SBD is around 56% that of the former under the same test conditions, the reverse recovery time of SiC SBD is around half of the body diode, and the conduction voltage drop of SiC SBD is 42.2% of the body diode. the Fig. 4 shows the drain-source voltage waveforms of $Q_H$ and $Q_L$, and freewheeling current waveforms through $Q_H$ and SBD during $t_{d\_on}$ and $t_{d\_off}$, and simulation conditions are set as $V_{bus}$= 400 V, $L$= 475μH, $i_L$= 5 A and $t_d$= 200 ns. When the $L_P$ in the freewheeling loop becomes larger, the $t_s$ will become longer. When $L_P$ increases from 10nH to 60nH, $t_{s\text{-}SR}$ increases from 192 ns to 519 ns, $t_{s\text{-}on}$ increases from 175 ns to 200 ns, and $t_{s\text{-}off}$ increases from 94 ns to 200 ns. Meanwhile, when the $L_P$ is greater than 40nH, the phase-leg configuration cannot complete commutation during $t_{d\_off}$. And when the $L_P$ is greater than 20nH, the phase-leg configuration also cannot finish commutation during $t_{d\_on}$, and $t_{s\text{-}SR}$ continues increasing. The relationship curve between $L_P$ and $t_s$ are shown in Fig. 4(c).

### 3.2. Scalability analysis

According to (1), $t_s$ is limited by load current $i$ and $L_P$ at the condition of same voltage drop. Besides $i$ and $L_P$, $t_s$ is also limited by $t_d$ because commutation stage happens within dead time. According to simulation and (1), we can deduce the relationships between $i$, $t_d$ and $L_P$, as shown in Fig. 5(a). If the commutation stage couldn't be finished completely during $t_d$, the use of SiC SBD for the phase-leg configuration is meaningless as there will exist less current in the SBD than the channel or body diode and brings more losses. According to the simulation results, complete commutation during $t_{D\text{-}off}$ has higher requirements on the layout compactness related with freewheeling loop, so if commutation can't be finished completely during $t_{d\_off}$, so does $t_{d\_on}$. As shown in Fig. 5 (b), the critical parasitic inductance value shows negative linear relationship with $i$ and $t_d$, and when $i > 5$ A, and $t_d <$ 200 ns, the critical parasitic inductance value is mostly less than 20nH. It can be seen that if greater freewheeling current flows through the freewheeling loop, the longer $t_d$ needs to be set in the phase-leg configuration, and the layout needs higher compactness degree, because the parasitic inductance will block freewheeling current.

Since the minimal critical inductance value of the experimental platform is limited by LP= 20nH and is hard to be reduced further due to real layout, the simulation can be operated at the condition of a smaller parasitic inductance to find the best situation for the use of SiC SBD in a phase-leg configuration under broader conditions. To find the relationships between load current, parasitic inductance and total losses of a phase-leg configuration, taking td= 200 ns as an example, under different load current and parasitic inductance, the total losses of the phase-leg configuration during a switching period under simulation are shown in Fig. 5(b). Only when i = 5 A, and LP≤ 20nH, the use of SBD could bring about 1.5% loss reduction for the total losses, and as the load current and parasitic inductance increase, the total losses of the phase-leg configuration will begin to deteriorate due to the use of SBD.

To find the relationships between dead time, parasitic inductance and total losses of a phase-leg configuration, we also take i = 5 A as an example, and conduct the SR double pulse simulation in the phase-leg configuration during a switching period under different dead time and the results are shown in Fig. 5(c). Only when td= 200 ns, and LP≤ 20nH, the use of SBD could bring about 1.5% loss reduction for the total losses. And when the dead time becomes shorter, the use of SBD could make total losses of the phase-leg configuration increase at the conditions of LP= 20nH. Even if parasitic inductance value could be reduced to 10nH or less, the loss reduction effect is hardly obtained.

Therefore, according to the simulation results and analysis, it can be concluded that the greater the load current through freewheeling loop and the shorter the dead time is set in this configuration, the higher layout compactness (the smaller LP) needs. In order to achieve complete commutation between SiC SBD and the body diode or the channel, a smaller LP is required for freewheeling loop. When i > 10 A, and td< 200 ns, the total losses of the phase-leg configuration begin to deteriorate due to the use of SBD, so the use of SBD is only meaningful at very special conditions of light load(i < 5 A) and relatively long dead time(td≥200 ns), under the premise of a typical and feasible layout (LP=20nH).

**Table 1**
Parameters of body diode of SCT3060AL and SCS240AE2.

| Parameters | $U_{DS}$/V | $I_{DS}$/A | $U_F$/V | $Q_{rr}$/nc |
|---|---|---|---|---|
| Body diode of SCT3060AL | 650 | 39 | 3.2($I_D$=13 A, $U_{GS}$=0 V, $T_a$=25 ℃), 1.35($I_F$=20 A, $T_j$ =25 ℃) | 55 ($U_R$=300 V) |
| SCS240AE2 (SiC SBD) | 650 | 40 | 1.55($I_F$=20 A, $T_j$ =150 ℃), 1.63($I_F$=20 A, $T_j$ =175 ℃) | 31 ($U_R$=400 V) |

## 4. Experimental results and discussion

In order to verify the above theoretical analysis and simulation results, we established a double pulse test platform to explore the influence of LP to the operation of a phase-leg configuration with parallelled SiC SBD under SR mode. The picture of the prototype is shown in Fig. 6 (a). The experimental parameters are set as same as simulation research.

Fig. 6(a) and (b) show the experimental waveforms of SR double pulse test in a phase-leg configuration composed of SiC MOSFET and SiC SBD at the conditions of i = 5 A and td= 200 ns, where UDS-L is the drain-source voltage of QL, UDS-H is the drain-source voltage of the QH, and iSBD is the current in SiC SBD. It can be seen that as the parasitic inductance LP of the freewheeling loop is increased from 20nH to 60nH, commutation time ts becomes longer. As for ts, ts-SR increases from 516 ns to 662 ns, ts-on increases from 136 ns to 178 ns, and ts-off increases from 100 ns to 200 ns. Regarding to turn-off dead time, the commutation can't be finished completely at the condition of LP≥ 40nH, which is basically consistent with the simulation results. The observed maximum current flowing through the anti-parallel SBD is less than 5 A, which means the average value of the current flowing through SiC SBD is less than that flowing through the body diode, so it cannot achieve the purpose of loss reduction by using an anti-parallel SiC SBD for freewheeling.

The experimental data at the condition of $I_L$= 5 A is shown in Table 2. $I_{D\text{-}L}$ is the peak value of the turn-on current of $Q_L$, $E_{on\text{-}L}$ is the turn-on loss of $Q_L$, $I_{RRM}$ is the peak value of the diode reverse recovery current, $E_{RR}$ is the diode reverse recovery loss, $E_{D\text{-}FW\text{-}on}$ and $E_{D\text{-}FW\text{-}off}$ are freewheeling loss in diodes during different dead times, $E_{H\text{-}FW}$ is $Q_H$'s SR freewheeling loss, $E_{L\text{-}DS(ON)}$ is $Q_L$'s conduction loss, $E_{tot}$ is the total loss in a phase-leg configuration during a switching period. At last, the degree

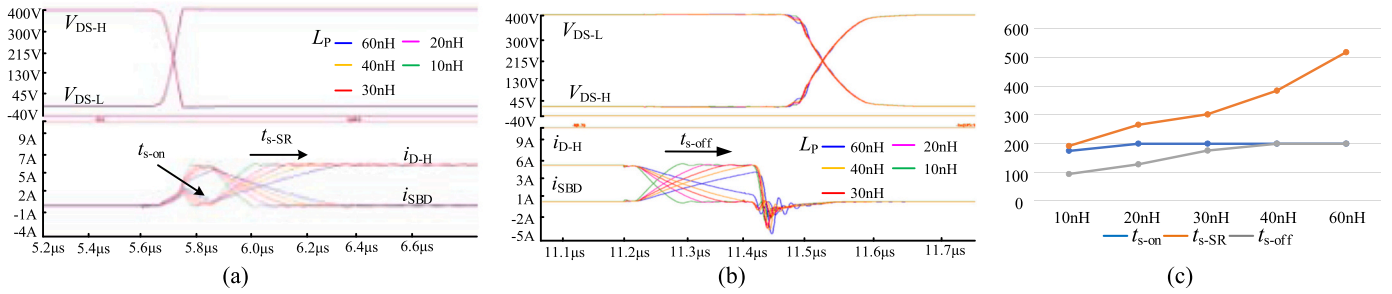


**Fig. 4.** Simulation waveforms under different $L_P$. (a) simulation waveforms during $t_{D-on}$; (b) simulation waveforms during $t_{D-off}$; (c) simulation results under different $L_P$.

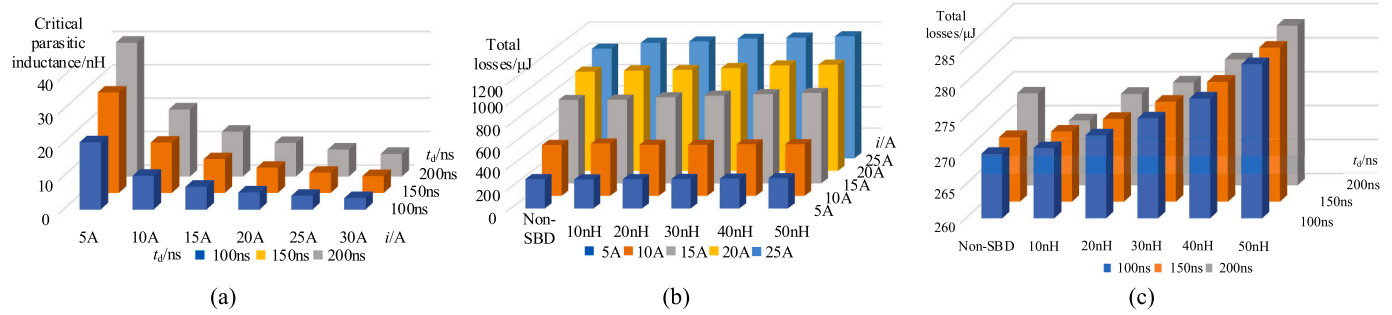


**Fig. 5.** Simulation waveforms under different parasitic inductance $L_P$. (a) critical parasitic inductance value under different $t_d$ and $i$; (b) total losses under different values of parasitic inductance and load current; (c) total losses under different parasitic inductance and $t_d$.

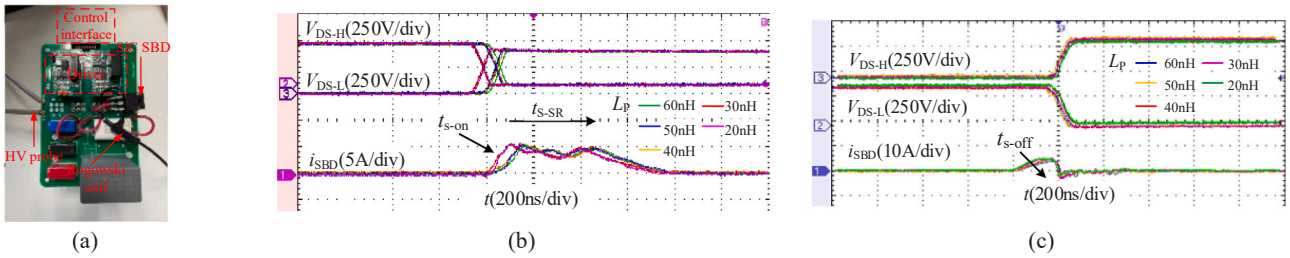


**Fig. 6.** Experimental waveforms under different $L_P$. (a) top view of the platform; (b) experimental waveforms during $t_{d\_on}$; (c) experimental waveforms during $t_{d\_off}$.

**Table 2**
Experimental data at the conditions of $I_L$= 5 A.

| Parameters | LP= 20 | $L_P$ = 30 | $L_P$ = 40 | $L_P$ = 50 | LP= 60 | Non-SBD |
|---|---|---|---|---|---|---|
| $I_{D-L}$/A | 10.5 | 13 | 13.2 | 13.4 | 15.2 | 11.8 |
| $E_{on-L}$/μJ | 57.82 | 57.49 | 66.3 | 63.06 | 66.98 | 47.24 |
| $I_{RRM}$/A | 3 | 3 | 2.4 | 2.6 | 3.2 | 6.8 |
| $E_{RR}$/μJ | 1.908 | 4.79 | 5.5 | 6.4 | 5.757 | 13.52 |
| $E_{D-FW-off}$/μJ | 0.3994 | 1.156 | 1.394 | 1.599 | 2.356 | 2.536 |
| $E_{D-FW-on}$/μJ | 12.12 | 13.71 | 14.08 | 19.37 | 21.88 | 23.15 |
| $E_{H-FW}$/μJ | 25.01 | 32.76 | 34.56 | 35.81 | 37.31 | 20.68 |
| $E_{L-DS(ON)}$/μJ | 49.79 | 49.65 | 49.61 | 49.6 | 49.63 | 49.63 |
| $E_{tot}$/μJ | 178.2546 | 190.784 | 202.777 | 207.413 | 215.59 | 186.472 |
| Optimization degree/% | 4.4 | − 2.3 | − 8.7 | − 11.2 | − 15.6 | 0 |

of loss reduction under different parasitic inductances is listed.

According to the experimental data in Table 2, when LP≥ 30nH, the antiparallel SiC SBD has brought the deterioration to the total losses of the phase-leg configuration compared to non-SBD condition, which is mainly manifested in the increase of the freewheeling loss and turn-on loss, caused by the increase of the commutation time and junction capacitance, deteriorating the advantages of reverse recovery loss reduction and freewheeling loss reduction brought by SiC SBD. When LP= 60nH, the total loss of the phase-leg configuration with SiC SBD is 15.6% worse than non-SBD condition, and when LP= 20nH, the loss reduction degree of the total losses is only 4.4%. When LP= 20nH, i = 10 A and td= 200 ns, the total loss of the phase-leg configuration with SiC SBD is 3.6% worse than that of non-SBD condition, so when parasitic inductance is about 20nH or greater, the use of SBD is not recommended at the condition of i ≥ 10 A. For SiC MOSFET based phase-leg configuration, dead time is more likely to be less than 200 ns, so in order to get loss reduction effect, the layout needs to be extremely tight, and the parasitic inductance should be kept to be less than 10nH.

As the parasitic inductance of the freewheeling loop increases, the commutation time between the SiC SBD and the body diode or the channel also increases, which conforms to Eq. (1). Therefore, it can be deduced that if the degree of layout compactness cannot be increased further, the phase-leg configuration cannot completely finish commutation during the dead time, so that antiparallel SiC SBD will increase the total losses in the phase-leg configuration due to the increase of freewheeling loss, and even if the phase-leg configuration could finish commutation, the total losses with SBD may become worse than non-SBD condition due to the increase of turn-on loss of QL. So antiparallel an external SiC SBD with SiC MOSFET in a typical phase-leg configuration only can get minor loss reduction in very low load current range, and it's hard to get remarkable loss reduction effect at most load current ranges. On the contrary, antiparallel SiC SBD will increase total power loss at higher load current.

## 5. Conclusion

This paper compares the total power loss under different combinations of influencing factors with the total loss under the condition of no anti parallel SBD through simulation and experimental results. Based on the analysis and experimental research in this article, there are conclusions from (1) to (4). (1) Due to physical limit, antiparallel SiC SBD will introduce parasitic inductance in freewheeling loop, resulting in additional commutation time, which makes the average value of the freewheeling current in SBD is smaller than the body diode, and will increase the total loss. (2) As load current increases and dead time is shortened, the layout compactness should be made tighter, i.e. the critical parasitic inductance value should be as low as possible. In the fabricated test platform, when the load current is 5 A and the parasitic inductance $L_P$ is less than 30nH, antiparallel SiC SBD will bring a very minor loss re-duction for the phase-leg configuration, and even when the parasitic inductance $L_P$ is reduced to 20nH, the loss reduction of the phase-leg configuration is only 4.4%. At larger load current, it's hard to get the effect of loss reduction due to the parasitic inductance induced by the layout. (3) The cost of the SiC SBD and SiC MOSFET used in the experiment is almost the same, which causes the cost of power stage increase dramatically compared to non-SiC SBD condition. Therefore, weighing the loss reduction degree and the proportion of cost increase in the SiC MOSFET based phase-leg configuration using SR, it is not recommended to use an external SiC SBD. (4) For the integrated SiC MOSFET combining SiC MOSFET and SiC SBD in a co-package, due to the still existing wire-bond connection, it will inevitably produce parasitic inductance of about 5–10nH or more. Thus, through the use of integrated SiC MOSFET, the load range that can realize loss reduction is slightly broadened, but the effect of loss reduction is incomparable with the increased cost and complexity.

## Declaration of Competing Interest

The authors declare no conflict of interest.

## Data availability

The authors are unable or have chosen not to specify which data has been used.

## Acknowledgments

This paper is supported financially in part by State Key Laboratory of Wide-Bandgap Semiconductor Power Electronic Devices, China, under Grant Number 2019KF001 and in part by National Natural Science Foundation of China under grant Number 51677089.

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