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Sub-mW Cryogenic InP HEMT LNA for Qubit Readout

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***Abstract*— The cryogenic indium phosphide (InP) high-electron-mobility transistor (HEMT) low-noise amplifier (LNA) is used for the readout amplification of qubits at 4 K where cooling capabilities are limited implying that the dc power of the active circuits is an essential design constraint. In this article, the RF and noise performance of the InP HEMT under ultralow-power (ULP) operation at 4 K has been characterized. The small-signal and noise parameter model of the InP HEMT was extracted down to 1 μW. The tradeoff between noise performance and dc power consumption was analyzed in terms of the drain current and drain voltage. A 4–6 GHz hybrid cryogenic HEMT LNA designed for qubit readout and optimized for lowest noise below 1 mW dc power consumption was fabricated. The measured performance of the LNA at 4 K attained 23.1 dB average gain and 2.0 K average noise temperature at 200 μW dc power.**

***Index Terms*— Cryogenic, indium phosphide high-electron-mobility transistor (InP HEMT), low power, low-noise amplifier (LNA), qubit.**

I. Introduction

QUANTUM computers are developed rapidly, integrating more and more qubits in the system. Superconducting quantum computing using 53 qubits already demonstrated higher performance than classical computing for a selected problem [1]. Many more qubits are needed to realize the demands on error correction in future quantum computing [2]. However, the massive scale-up in qubits implies a surge in dc power consumption for the readout electronics which challenges the maximum cooling capacity of the dilution refrigerator in the quantum system.

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One of the most power-hungry devices in qubit readout is the cryogenic indium phosphide (InP) high-electron-mobility transistor (HEMT) low-noise amplifier (LNA) at the 4 K cooling stage [3]. Today, a typical LNA for qubit readout consumes several milliwatts [3], [4]. The noise temperature is typically 1.5–2 K. Previous works for InP HEMTs and silicon–germanium (SiGe) hetero-junction bipolar transistors (HBTs) have shown the potential to reduce the dc power consumption for the cryogenic LNA to 1 mW or below [5], [6], [7], [8], [9]. However, for the InP HEMT cryogenic LNA, this comes with a penalty in gain and noise with a typical average noise temperature above 3 K [7], [8]. The quest is if cryogenic LNAs for qubit readout can be engineered for ultralow-power (ULP) consumption much less than 1 mW, and still achieve an average noise temperature of 2 K or below. Such a design would be highly desirable for the anticipated future up-scaling of qubit readout circuits involving many LNAs [4].

For RF circuit design under ULP, an accurate small-signal and noise model is crucial. In quantum applications, the operation of the LNA implies that the model must be based on experiment data measured at 4 K. Such transistor models are normally not available. Small-signal and noise modeling for SiGe HBT has been reported for ULP cryogenic LNA operation [5]. The LNA rapidly degraded in noise performance when the SiGe HBT reached a collector–emitter voltage below 0.125 V. Scalable small-signal and noise models down to 5 mW/mm at cryogenic temperature have been investigated in the InP HEMT community [10], [11]. The absence of a cryogenic small-signal and noise model at ULP for the InP HEMT motivates a study that allows us to fully utilize its RF and noise performance in sub-mW cryogenic LNA design [8], [12], [13], [14], [15].

In this article, we report a cryogenic model for the InP HEMT describing RF and noise performance down to 1 μW dc power. A 4–6 GHz hybrid cryogenic HEMT LNA optimized for sub-mW qubit readout is presented. The measured LNA demonstrated 23.1 dB average gain and 2.0 K average noise temperature at 200 μW dc power under 4 K ambient temperature.

II. DC Characterization of InP HEMTs for Cryogenic LNA

The transistor used for the model extraction and circuit design was a 100 nm gate-length InP HEMT. The epitaxial

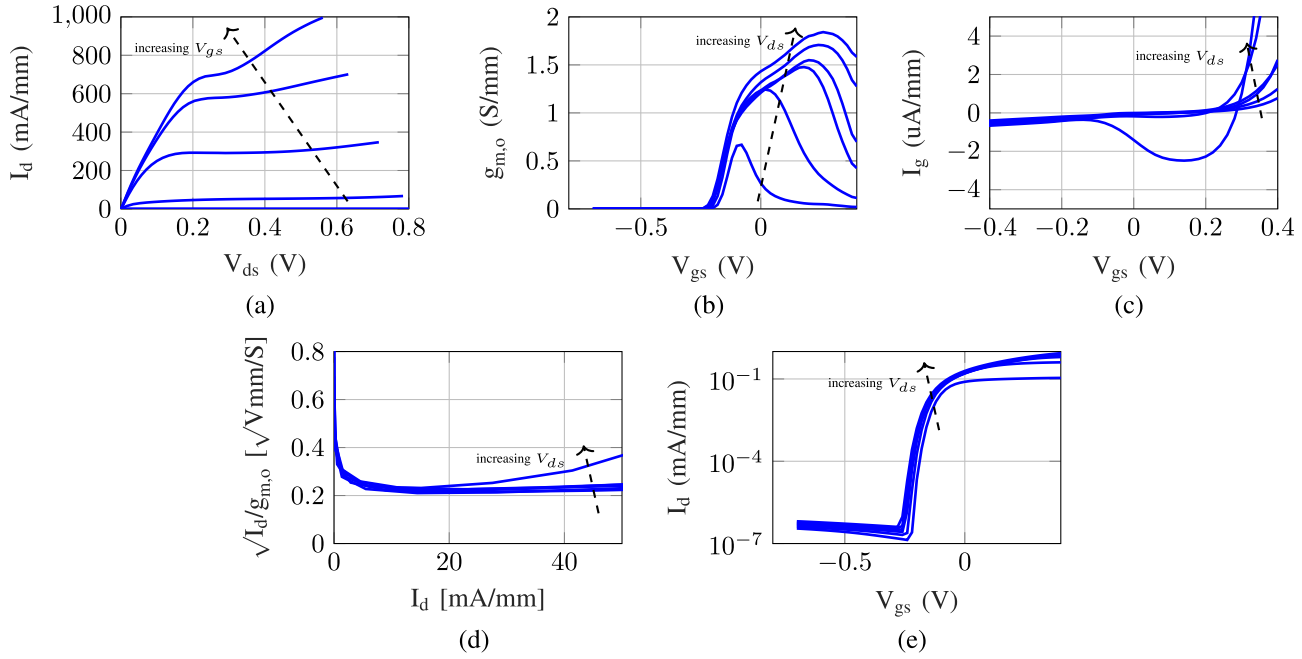

Fig. 1. DC characterization of 4 × 50 μm gate width and 100 nm gate-length InP HEMT at 4 K used in circuit design. (a) Output current where V_{gs} is from −0.5 to 0.5 V in steps of 0.2 V. V_{ds} is from 0.05 to 0.8 V in steps of 0.15 V for (b) $g_{m,o}$, (c) I_g, (d) $\sqrt{I_d}/g_{m,o}$ versus drain current I_d, and (e) SS where I_d versus V_{gs} plot in log scale.

layer structure from top to bottom was 20 nm InGaAs cap followed by 3 nm InP etch stop, 8 nm InAlAs barrier, silicon δ-doping (5×10^{12} cm^{-2}), 3 nm InAlAs spacer, 15 nm InGaAs channel with 65% indium content and 500 nm InAlAs buffer layer. From room-temperature Hall measurements, the electron mobility and sheet carrier concentration were determined to be 12 000 cm^2/V·s and 3.6×10^{12} cm^{-2}, respectively. For further details on the HEMT fabrication see [12].

The dc characterization was performed at a 4 K environment in a Lakeshore model CRX-4K cryogenic probe station for a 4 × 50 μm gate width device under test (DUT). In Fig. 1(a), the drain current I_d versus drain–source voltage V_{ds} curve shows a peak drain current of 900 mA/mm at $V_{ds} = 0.5$ V with an ON-resistance (R_{ON}) of 0.33 Ω·mm. The extrinsic transconductance $g_{m,o}$ of the InP HEMT is shown in Fig. 1(b). The threshold voltage V_{th} for the device is −0.25 V and the maximum $g_{m,o}$ reaches 1.8 S/mm at $V_{ds} = 0.7$ V. The gate current I_g shown in Fig. 1(c) is in the order of 0.1 μA/mm for V_{ds} up to 0.7 V indicating a satisfactory level of gate leakage. This is essential for the final HEMT LNA noise performance at the frequency band used in qubit readout [12], [14].

The minimum noise temperature T_{min} for the HEMT is well-known to appear at the bias for minimum $\sqrt{I_d}/g_{m,o}$ [14]. A smaller value of the ratio of I_d and $g_{m,o}$ means that the transistor provides higher transconductance at a lower drain current. Thus, a lower $\sqrt{I_d}/g_{m,o}$ value leads potentially to improved noise at low dc power as discussed in [8]. In Fig. 1(d), a minimum $\sqrt{I_d}/g_m$ value of 0.22 $(\text{V} \cdot \text{mm/S})^{1/2}$ is observed at $I_d = 16$ mA/mm for the DUT at 4 K. Moreover, the lower the subthreshold swing (SS), the higher $g_{m,o}/I_d$ for the HEMT. Hence the SS is also indicative of the potential low-noise performance at low dc power [16]. In Fig. 1(e), we observe a very small SS of only 18 mV/dec at 4 K. The data in Fig. 1(d) and (e) suggests a potential of the InP HEMT technology used here for the design of a cryogenic LNA at low dc power.

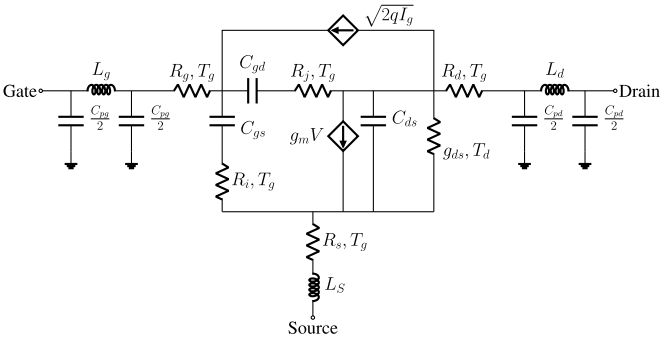

Fig. 2. Equivalent small-signal noise model of the InP HEMT.

III. Cryogenic InP HEMT Small-Signal Noise Model Under ULP

To enable the targeted LNA design at ULP, an adequate small-signal noise model for the InP HEMT is needed. In this study, Pospieszalski's noise model [17] was employed for the InP HEMT described in Section II. The model topology is shown in Fig. 2 [18]. The RF and noise performance at 4 K was modeled for a device size 4 × 50 μm. Different levels of V_{ds} and I_d were tested to measure the InP HEMT at various dc power ranging from 600 to 1 μW. By adjustment of the gate–source voltage V_{gs}, V_{ds} was swept from 0.3 to 0.01 V while keeping the I_d at a fixed value in the range 0.1–2 mA. Since the magnitude of the I_g was only a few tens of nanoampere, the contribution of the gate current to the total dc power consumption was considered negligible.

According to the Pospieszalski's noise model [17], $T_{\min}$ is expressed by

$$T_{\min} \approx 2\frac{f}{f_T}\sqrt{R_t T_g g_{ds} T_d} \tag{1}$$

where R_t is the sum of the gate resistance R_g, the intrinsic gate–source resistance R_i and the source resistance R_s. The T_d and T_g are the equivalent drain and gate temperatures, respectively. T_d is bias-dependent whereas T_g usually is considered equal or close to the ambient temperature. The g_{ds} is the intrinsic output conductance of the applied drain voltage. The intrinsic cut-off frequency f_T can be described by [19]

$$f_T = \frac{g_m}{2\pi\left(C_{gs}+C_{gd}\right)\cdot\left(1+\frac{R_s+R_d}{R_{ds}}\right)+g_m C_{gd}(R_s+R_d)} \tag{2}$$

where C_{gs} and C_{gd} are the intrinsic gate–source and gate–drain capacitance, respectively, R_d is the drain resistance, and R_{ds} is the inverse of g_{ds}. g_m is the intrinsic transconductance. f_T is proportional to g_m and inversely proportional to the sum of the intrinsic capacitances. Similar to the small-signal noise model parameters, $T_{\min}$ is dependent upon bias.

The behavior of the small-signal noise model parameters at low V_{ds} can be understood from the 2-D electron gas (2DEG) in the HEMT channel [20]. When sweeping V_{ds} from saturation to the triode region (0.3–0.01 V) under a fix I_d, g_m is initially expected to remain unchanged as the increased V_{gs} offsets the diminishing influence of reduced V_{ds}. However, at low V_{ds}, there will be an insufficient number of channel carriers for V_{gs} modulation, resulting in a decrease in g_m.

When V_{ds} is low, C_{gd} is expected to increase due to the reduction of the depletion region of the 2DEG at the drain side. The behavior of C_{gs} is sensitive to variations in both V_{gs} and V_{ds}. When lowering V_{ds} in saturation, the increased V_{gs} required to sustain I_d acts to enhance carrier concentration in the channel, leading to a slight increase in C_{gs}. However, as V_{ds} decreases further, the carrier distribution in the 2DEG is anticipated to become more uniform, resulting in decreased carrier density at the source side and a consequent decrease in C_{gs}. The opposing influences of increased V_{gs} and decreased V_{ds} at constant I_d for C_{gs} are expected to overlap. Under high current bias (and high V_{gs}), channel carrier concentration reaches saturation and the impact from low V_{ds} is expected to dominate, leading to a decrease in C_{gs}. In contrast, at a low drain current where V_{gs} is low and the channel is not fully open, it is anticipated that the increase in V_{gs} at lower V_{ds} will overcome the decrease in V_{ds}, resulting in an increase in C_{gs}.

At low V_{ds} in the triode region, the HEMT channel behaves like a voltage-controlled resistor. Small fluctuations in V_{ds} will induce significant current variations, resulting in an increase in g_{ds}.

The noise model parameter T_d assigned to g_{ds} is known to be linearly dependent on the drain current and reflects the fluctuations in the electron flow of the channel [15], [21]. As the V_{ds} decreases, there will be a corresponding decrease in T_d since the carriers in the channel become less hot.

Based on the interpretation of the small-signal model parameters at varying bias, it is expected that f_T will decrease as V_{ds} is reduced, as indicated by (2). A decrease in f_T will negatively impact $T_{\min}$ whereas a lower T_d will mean the opposite; see (1). In Section III-A and III-B, the small-signal noise model parameters will be experimentally quantified and confirmed for the InP HEMT under ULP.

A. Small-Signal Model Under ULP

Small-signal model parameters at low dc power bias for the DUT at 4 K were determined by direct extraction methods [18]. S parameters were measured on-wafer at 4 K in the cryogenic probe station used for dc characterization (Section II) equipped with a Rohde Schwarz ZVA67 vector network analyzer up to 67 GHz. An on-wafer through-reflect-match calibration was used to de-embed the influence from the probes, cables, and bias tees.

In Fig. 3, measured and simulated S parameters for the 4×50 μm InP HEMT at 4 K are presented up to 40 GHz for 600, 40, and 1 μW dc bias power. The simulated data are based on the extracted small-signal model parameters listed in Table I. The agreement between measured and simulated S parameters is excellent for all dc power levels. This validates the effectiveness of the extracted small-signal model for dc bias power below 1 mW. It is worth noticing that the lateral isolation S_{12} degrades with lower bias power as shown in Fig. 3(e). The degraded isolation suggests a higher g_{ds} at lower bias power, when entering the triode region of the HEMT [20].

Fig. 4 presents extracted g_m, C_{gs}, C_{gd}, and g_{ds} versus V_{ds} for different I_d at 6 GHz. The device was the 4×50 μm gate-width and 100 nm gate-length InP HEMT at 4 K ambient temperature. In Fig. 4(a), it is seen that the g_m is strongly dependent on I_d. The g_m shows a roll-off around 0.05 V. This roll-off starts earlier and is stronger for higher drain current levels. This is due to the higher V_{gs} leading to higher V_{ds} for the HEMT to enter the triode region. The mean g_m value in Fig. 4(a) before roll-off are 50, 75, 160, 330, and 530 mS/mm for I_d of 0.1, 0.15, 0.4, 1, and 2 mA, respectively. g_m exhibits an approximate linear dependence on I_d.

The C_{gs} and C_{gd} are shown in Fig. 4(b) and (c). The C_{gs} behavior is similar to the g_m for I_d of 1 mA or higher, sustaining a stable value. For I_d of 0.4 mA or lower, the C_{gs} exhibits a slight increase with reduced V_{ds}. On the other hand, the C_{gd} is independent of I_d for V_{ds} above 0.1 V. Below this bias, C_{gd} increases two to six times (depending on I_d) faster compared to $V_{ds} > 0.1$ V. The extracted g_{ds} exhibits higher values for higher I_d, see Fig. 4(d). Depending on I_d, g_{ds} increases rapidly when V_{ds} is lower than 0.03–0.07 V.

The extracted small-signal model parameters all show a clear trend when biased for ULP operation. All parameters respond relatively weakly to a decrease in V_{ds} until reaching a value around 0.05 V for the DUT. This suggests that the cryogenic InP HEMT can maintain its microwave performance even at bias power below 1 mW. Slightly below $V_{ds} = 0.05$ V, g_m decreases rapidly accompanied by an increase in g_{ds} and the total intrinsic capacitance. According to (1) and (2), a fast degradation is then anticipated in f_T and $T_{\min}$. The consequences of noise modeling under ULP will be analyzed in Section III-B.

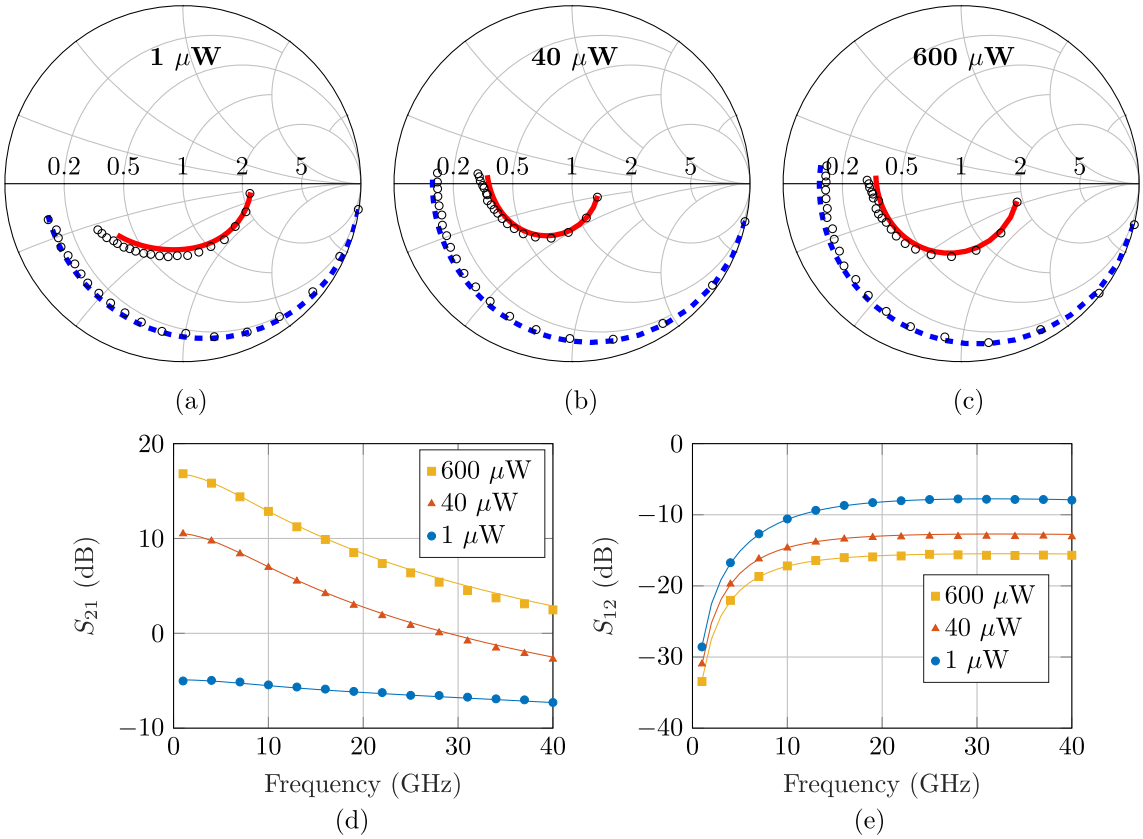

Fig. 3. Comparison of measured (circles) and simulated (lines) S parameters from 0.01 to 40 GHz of a 4 × 50 μm gate width and 100 nm gate-length InP HEMT at 4 K for different ULP levels. S_{11} (red solid line) and S_{22} (blue dashed line) plotted in Smith chart with bias power at (a) 1 μW ($V_{\text{ds}} = 0.01$ V, $I_{\text{d}} = 0.1$ mA), (b) 40 μW ($V_{\text{ds}} = 0.04$ V, $I_{\text{d}} = 1$ mA), and (c) 600 μW ($V_{\text{ds}} = 0.3$ V, $I_{\text{d}} = 2$ mA). (d) S_{21} and (e) S_{12} for 600, 40, and 1 μW.

TABLE I
EXTRACTED SMALL-SIGNAL MODEL PARAMETERS OF THE 4 × 50 μM INP HEMT AT 1, 40, AND 600 μW BIAS POWER AT 4 K. UNITS ARE V, mA, mS, Ω, fF, pH, AND K

		1 μW	40 μW	600 μW
Bias	V_{ds}	0.01	0.04	0.3
	I_d	0.1	1	2
	V_{gs}	-0.15	-0.13	-0.14
	I_g	-4.1×10^{-5}	-3.8×10^{-5}	-6.1×10^{-5}
Intrinsic	C_{gs}	97	107	116
	C_{gd}	87	75	51
	C_{ds}	46	47	47
	g_m	8.4	62.7	115.2
	R_i	0.2	0.1	1.3
	R_j	2.7	4.0	4.5
	g_{ds}	9.1	15.7	11.2
Extrinsic	C_{pg}, C_{pd}	23.4	23.4	23.4
	L_g	61	61	61
	L_s	3	3	3
	L_d	57	57	57
	R_g	0.2	0.2	0.2
	R_d	0.8	0.8	0.8
	R_s	0.7	0.7	0.7

B. Noise Model Under ULP

The ULP bias analysis is carried out with respect to the fitting parameter T_{d}, noise parameters, and associated gain. We start with a description of the experiment procedure for measuring and extracting T_{d} of the transistor under a certain dc bias.

On-wafer noise measurements of InP HEMTs at cryogenic temperature suffer from poor accuracy [13], [18]. Therefore, an indirect method using extraction of noise parameters from an LNA measurement at 4 K was applied here. 4 × 50 μm gate-width and 100 nm gate-length InP HEMTs were mounted in a three-stage hybrid 4–8 GHz LNA [22]. A dual-bias dc circuit was implemented in the LNA to provide individual V_{gs} and V_{ds} biases for the first stage, and the second and third stages, respectively, as shown in Fig. 5. The noise temperature and gain of the LNA were characterized at 4 K using an Agilent N8975B noise figure analyzer (NFA) with a cold attenuator setup [23].

The noise parameters in the Pospieszalski model are based on the fitting parameters T_{d} and T_{g} defined in the small-signal model; see Fig. 2 [18]. Equivalent circuit models of the LNA with extracted bias-dependent parameters for the InP HEMTs were implemented in the AWR Microwave Office to determine T_{d}. This value was fit to match the simulated noise with the measured data for the LNA. To account for potential self-heating in the device [7], [14], [21], [24], the T_{g} was set to 10 K. The noise contribution from I_{g} was modeled as a shot noise source, see Fig. 2, with noise current $(2 \cdot q \cdot I_{\text{g}})^{1/2}$. The I_{g} values were recorded during the S parameter measurements for each bias point.

The dual-biased LNA was utilized for device noise characterization at ULP. The first stage InP HEMT was biased at the same conditions as used in the S parameter measurement.

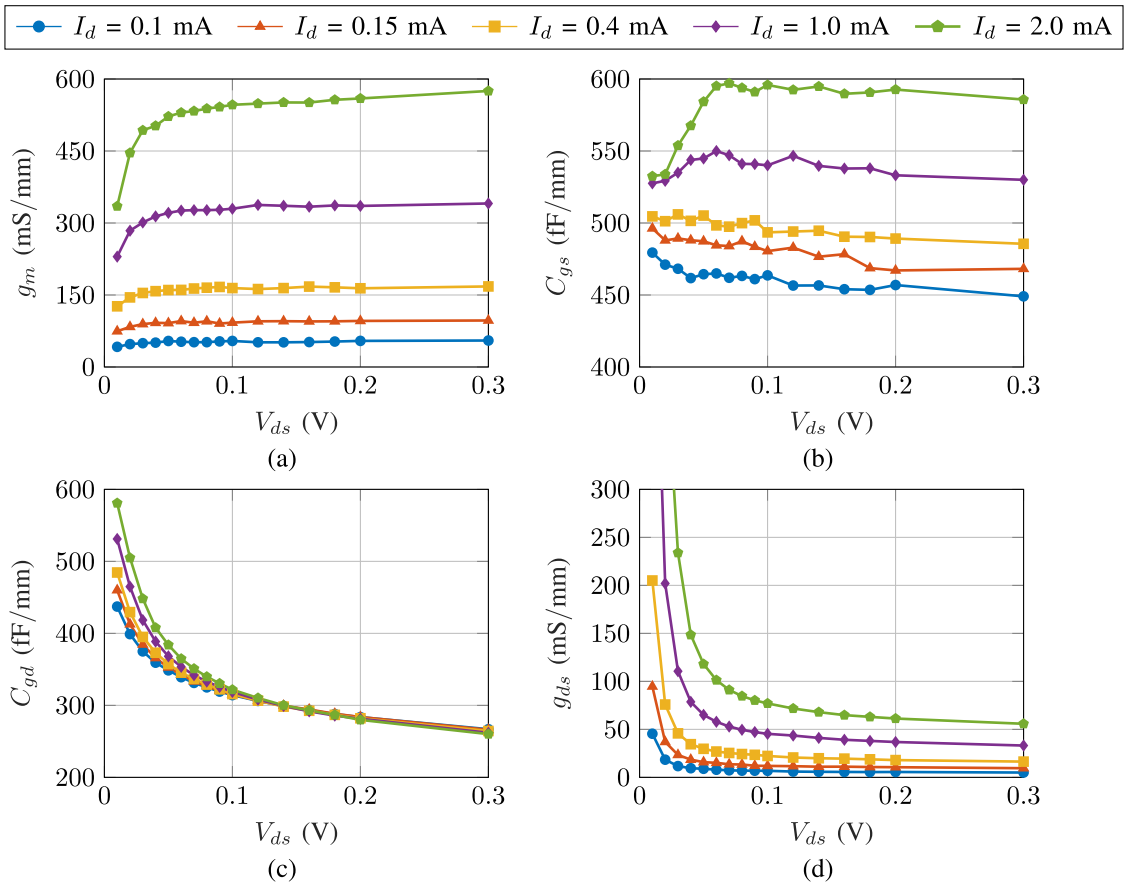

Fig. 4. Extracted (a) intrinsic g_m, (b) C_{gs}, (c) C_{gd}, and (d) g_{ds} as a function of V_{ds} at 6 GHz of a 4 × 50 μm gate width and 100 nm gate-length InP HEMT at 4 K with I_d bias from 2 mA down to 0.1 mA.

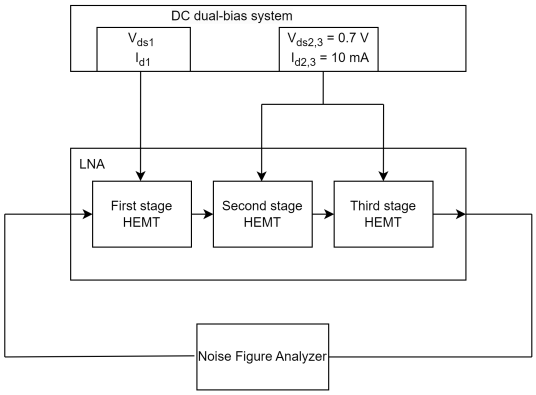

Fig. 5. Schematic of the 4–8 GHz LNA for T_d extraction with dual-bias dc system. The V_{ds} on the second and third-stage HEMTs is 0.475 V after the series resistance voltage drop in the bias line.

The second and third InP HEMTs were biased at V_{ds} = 0.475 V and I_d = 5 mA, which was the bias point for low noise and high gain with known small-signal model parameters and T_d values. The T_d for the first stage InP HEMT was extracted by de-embedding the subsequent two stages under fixed bias. As a result, all bias-dependent noise parameters could be acquired by applying the Pospieszalski model [17] for the extracted small-signal model parameters and recorded I_g values. The T_d was extracted for the first stage HEMT from 1 to 600 μW dc power. Fig. 6 shows the measured and simulated noise and gain of the reference LNA from 4 to 8 GHz when the first stage HEMT was biased at 1, 40, and 600 μW, respectively. Even when the first stage is biased at 1 μW, the second and third HEMT stages enable the LNA to reach more than 20 dB gain hence providing a signal-to-noise ratio needed for the NFA to work properly; see Fig. 6(b). However, as power drops, the first stage gain drops and the mismatch increases which leads to a degradation in T_d extraction accuracy. This error has not been studied in detail for dc power below 16 μW (V_{ds} = 0.04 V, I_d = 0.4 mA) used for second and third stage HEMTs in the 100 μW LNA design described in Section V.

In Fig. 7, the extracted noise-related parameters versus V_{ds} for different I_d of the InP HEMT at 6 GHz at 4 K are presented. The T_d is shown in Fig. 7(a). T_d is reduced with lower I_d and V_{ds}. The lower I_d due to lower V_{gs} leads to fewer carriers in the channel which results in a decreased T_d. As mentioned in Section III, the 2DEG electrons are less hot and predominantly move with velocities in response to the local electric field intensity, explaining the decrease of T_d and its less dependence on the drain current.

T_{min} is shown in Fig. 7(b). T_{min} was simulated in AWR Microwave Office using the extracted T_d and small-signal model parameters. The T_{min} improves with higher I_d and saturates beyond 1 mA. Before reaching V_{ds} = 0.05 V where noise rapidly degrades, T_{min} remains constant and even slightly decreases with reduced V_{ds}. The latter is due to the decrease

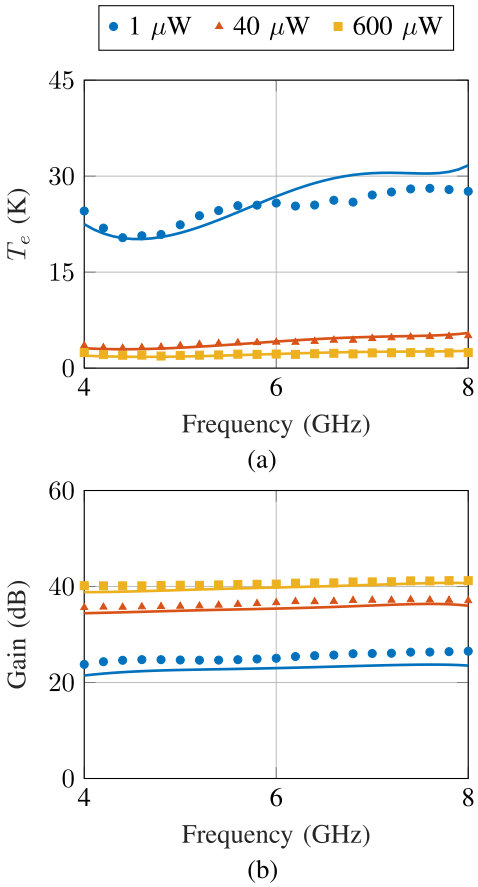

Fig. 6. Comparison of measured (symbols) and modeled (solid lines) (a) noise and (b) gain of the 4–8 GHz reference LNA used for T_d extraction at 4 K for the first stage HEMT biased at 1 μW ($V_{ds1} = 0.01$ V, $I_{d1} = 0.1$ mA), 40 μW ($V_{ds1} = 0.04$ V, $I_{d1} = 1$ mA), and 600 μW ($V_{ds1} = 0.3$ V, $I_{d1} = 2$ mA). The second and third HEMT stages were biased with $V_{ds2,3} = 0.7$ V, $I_{d2,3} = 10$ mA (see Fig. 5).

in T_d which dominates over the degradation in small-signal model parameters. Similar behavior of T_{min} versus collector–emitter voltage V_{CE} at a fixed forward collector-current density has been observed for SiGe HBTs at cryogenic operation, with V_{CE} between 0.1 and 0.2 V [5]. In Fig. 7(b), it is also noted that T_{min} for I_d at 1 mA or above degrades faster below 0.05 V than T_{min} with I_d below 1 mA. According to (1) and (2), the increase in T_{min} below $V_{ds} = 0.05$ V is mostly related to the small-signal model parameters since T_d is a monotonically decreasing function for I_d below 2.0 mA. The behavior of the small-signal parameters in Fig. 4 serves as a good indicator for the T_{min} performance at ULP.

Fig. 8 is a contour plot of T_{min} based on Fig. 7(b), from which the bias point for the lowest T_{min} with the lowest dc bias power can be found for the InP HEMT at 4 K. In a single-stage analysis of the HEMT LNA design, the overall noise performance must consider noise parameters in terms of impedance matching

$$T_e = T_{min} + T_0 \frac{R_n}{\Re\{Z_{opt}\}} |Z_s - Z_{opt}|^2 \tag{3}$$

where T_e is the LNA equivalent noise temperature, T_0 is the reference temperature (290 K), R_n is the noise resistance, Z_s is the source impedance, and Z_{opt} is the optimum impedance for the noise matching. To obtain a low T_e across the full bandwidth of the cryogenic LNA, the influence of R_n and Z_{opt} is significant.

The N parameter is introduced as the invariant to account for the combined effect of R_n and $\Re\{Z_{opt}\}$ and is defined as [25]

$$N = \frac{R_n}{\Re\{Z_{opt}\}}. \tag{4}$$

See plot in Fig. 7(c). At low frequency, N is proportional to T_{min} [17]. Hence Fig. 7(c) shows a similar trend as Fig. 7(b). Below $V_{ds} = 0.05$ V, N rapidly surges for all I_d, leading to an InP HEMT more sensitive to the noise mismatch. The $4NT_0/T_{min}$ was checked for all bias points in Fig. 7 and the values were between 1.8 and 1.9 irrespective of bias [26]. This suggests that the low-frequency approximation of (1) holds for all extracted noise models [17]. The close to two values of $4NT_0/T_{min}$ implies that the gate noise source and drain noise source of the HEMT have similar contributions to total noise at the Z_{opt} input impedance [27].

In a multistage HEMT LNA, the associated gain G_{assoc} for each stage has to be considered [28]. The G_{assoc} at 6 GHz deteriorates for lower I_d as shown in Fig. 7(d). Similar to the other noise parameters, G_{assoc} declines smoothly with reduced V_{ds} and rolls off rapidly when reaching $V_{ds} = 0.05$ V. The fast decrease of G_{assoc} is caused by the decrease of g_m and increase of g_{ds}, shown in Fig. 4 (a) and (d) [17]. Note that at a dc power of only 40 μW ($V_{ds} = 0.04$ V; $I_d = 1$ mA), the InP HEMT still sustains $G_{assoc} = 10$ dB at 6 GHz. To take the influence of G_{assoc} into account for the cascade noise analysis, a modified noise measure is introduced [29]

$$M_{opt} = \frac{T_{min}}{T_0} \frac{1}{1 - \frac{1}{G_{assoc}}}. \tag{5}$$

The total noise temperature T_{total} of infinite cascade stages is

$$T_{total} = T_0 \cdot M_{opt}. \tag{6}$$

T_{total} is plotted in the insert of Fig. 7(d), revealing a pattern similar to T_{min} with a slight shift in V_{ds} toward 0.07 V where noise starts to degrade. This is due to the rapid decrease of G_{assoc} with V_{ds} as compared to T_{min}.

The projected Z_{opt} in the Smith chart in Fig. 9 shows that the lower the bias power, the further away Z_{opt} is from the origin of the Smith chart, highlighting the difficulty in impedance matching between noise and bandwidth at ULP.

In summary, the noise parameters and G_{assoc} depend significantly on the I_d under ULP bias. The influence of the V_{ds} on the noise parameters for the DUT in this study is relatively insignificant above $V_{ds} = 0.05$ V. Below this voltage, noise performance and G_{assoc} degrade rapidly. This puts a minimum V_{ds} for low power optimization in the cryogenic HEMT LNA design.

IV. Cryogenic HEMT LNA Design for Qubit Readout

In this study, the design of the sub-mW cryogenic InP HEMT LNA was specifically optimized for qubit readout in

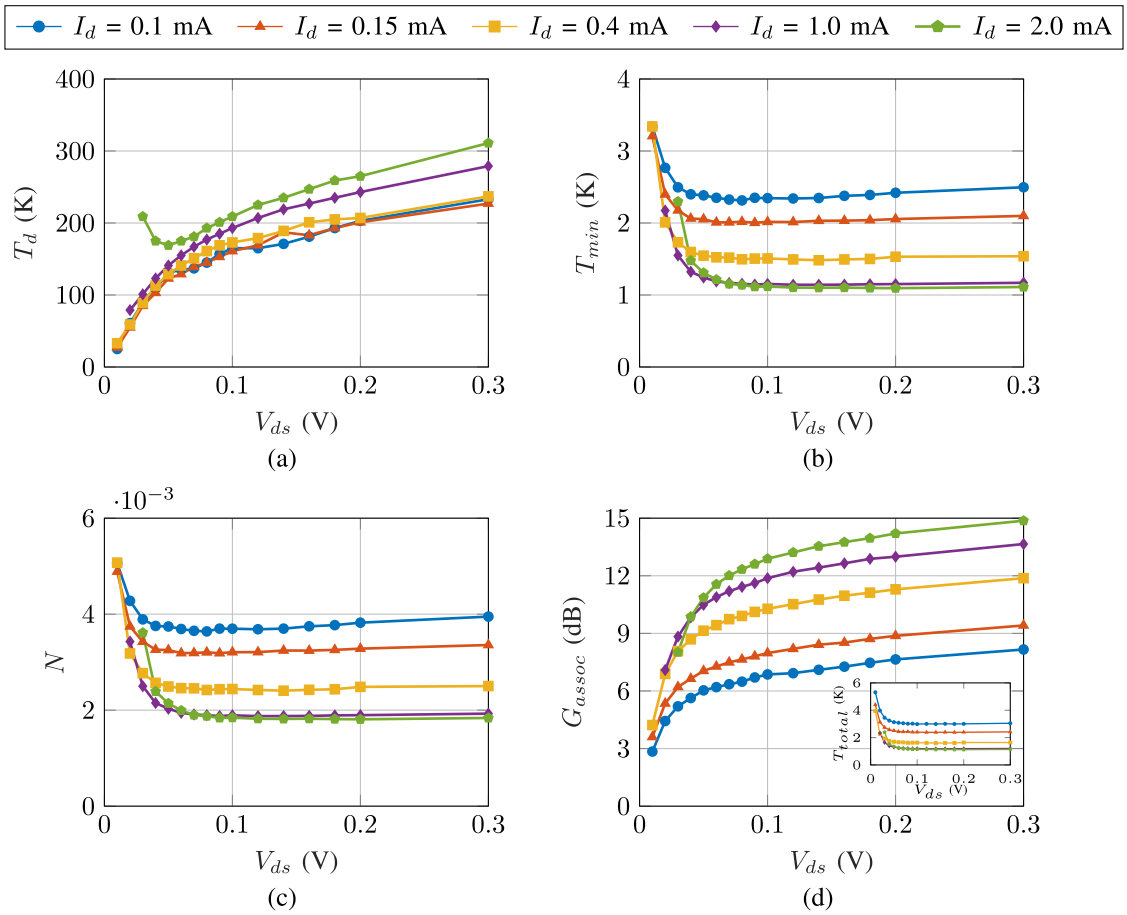

Fig. 7. Extracted (a) $T_{\rm d}$, (b) $T_{\rm min}$, (c) N, and (d) $G_{\rm assoc}$ as a function of Vds at 6 GHz for a 4 × 50 μm gate width and 100 nm gate-length InP HEMTs at 4 K with $I_{\rm d}$ biased from 2 mA down to 0.1 mA. The insert in (d) is $T_{\rm total}$ versus $V_{\rm ds}$.

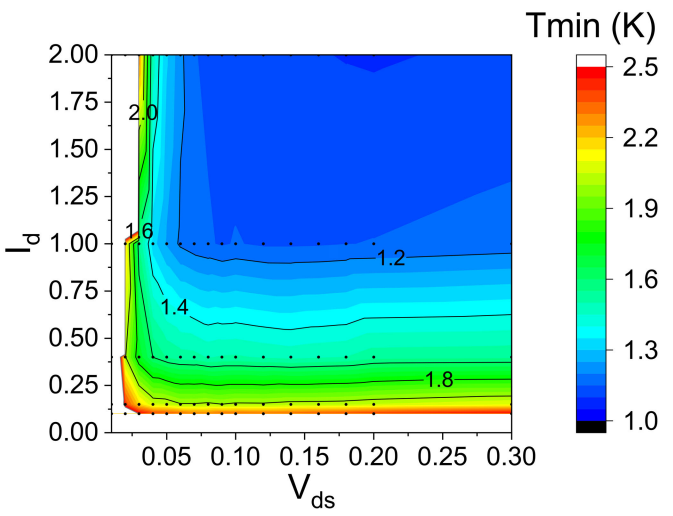

Fig. 8. Contour plot of extracted $T_{\rm min}$ versus bias at 6 GHz for a 4 × 50 μm gate width and 100 nm gate-length InP HEMTs at 4 K. The dots denote the extracted bias points.

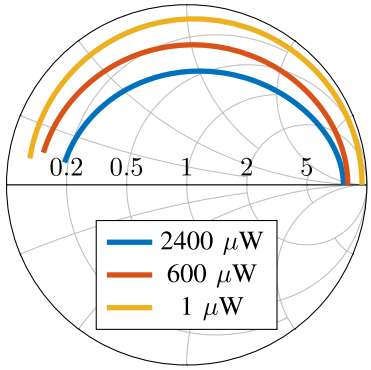

Fig. 9. Extracted $Z_{\rm opt}$ at 4 K of a 4 × 50 μm gate width and 100 nm gate-length InP HEMT with bias power of 2.4 mW ($V_{\rm ds}$ = 0.475 V, $I_{\rm d}$ = 5 mA), 600 μW ($V_{\rm ds}$ = 0.3 V, $I_{\rm d}$ = 2 mA), and 1 μW ($V_{\rm ds}$ = 0.01 V, $I_{\rm d}$ = 0.1 mA) at 4 K in the Smith chart. The data are plotted up to 40 GHz.

a quantum computer. To find out realistic design goals for best noise performance, the application requirements were taken into consideration which led to a design tradeoff based on the cryogenic InP HEMT small-signal noise model under ULP.

A. Design Analysis for Qubit Readout

In a typical superconducting qubit readout system, the HEMT LNA is often employed as the second stage amplifier at the 4 K stage with 1 to 1.5 W maximum cooling capability in the refrigerator [3]. The HEMT LNA follows the first stage parametric amplifier at the milli Kelvin stage including several isolators to prevent noise emitted from the HEMT LNA's input to reach the parametric amplifier [30].

In the majority of qubit readout systems, the HEMT LNA is optimized for the lowest noise, typically T_e is between 1.5 and 2 K [31]. The HEMT LNA bandwidth is 4–8 GHz and the dc power consumption is in the order of several milliwatts [4]. In addition, amplifier linearity can be critical in large-scale quantum systems, since each LNA is responsible for simultaneous qubit readout. The linewidth and frequency distancing between each resonator readout envelope can be designed below 11 and 160 MHz, respectively [3]. Ideally, the available frequency band should be fully utilized for qubit readout signal distancing with minimum feasible frequency separation. If we only consider the limitation of HEMT LNA performance, assuming each qubit occupies 2 MHz bandwidth, the upper limit workload for a 4–8 GHz cryogenic LNA is 2000 qubits. The full utilization of a 4 GHz bandwidth LNA for qubit readout increases the requirement for input linearity with +33 dB compared with an LNA used for a single qubit readout. Assuming the previous stage parametric amplifier reaches output 1 dB compression point P1dB around −90 dBm [32], input P1dB for the HEMT LNA should be at least higher than −57 dBm for the ideal case.

The qubit resonator readout frequency ω_r is dependent on the qubit frequency ω_q and frequency detuning Δ from the qubit to the resonator as

$$\omega_r = \omega_q \pm \Delta \tag{7}$$

where $\omega_r/2\pi$ and $\Delta/2\pi$ are in the range of 4–8 GHz [4] and 0.5–1.5 GHz [33], respectively. The frequency range of ω_r is a flexible design parameter eventually determined in the fabrication implying that the HEMT LNA bandwidth of 4–8 GHz is negotiable. This amplifier property can therefore be traded off for lower dc power consumption as long as the feasible number of qubit readouts is increased under limited cooling capability.

The analysis of the extracted small-signal noise model of the InP HEMT in Section III highlights the tradeoff parameters between dc power and bandwidth under ULP. When the bias is reduced, the degradation of Z_{opt} and G_{assoc} is more significant compared to T_{min} and N, leading to a reduction in bandwidth for a given gain and noise. The design priorities for the ULP LNA design here can then be summarized as: 1) reduce the power consumption of the cryogenic LNA much less than 1 mW [4]; 2) maintain sufficient noise performance ($\leq$2 K) for the qubit readout operation; and 3) have good enough linearity ($\geq$−60 dBm) for the LNA in order to support large-scale qubit readout capability.

B. Design and Implementation of LNA for Qubit Readout

The LNA realized in this work was a three-stage cascade in common source topology based on 4 × 50 μm gate-width 100 nm gate-length InP HEMTs [34]. The designed bandwidth was 4–6 GHz to enable a good tradeoff between the noise temperature and dc power consumption. The targeted total dc power consumption for the HEMT LNA was either 100 or 200 μW with more than 20 dB gain and a noise temperature as low as possible at 4 K ambient temperature. A simplified schematic of the HEMT LNA is shown in Fig. 10.

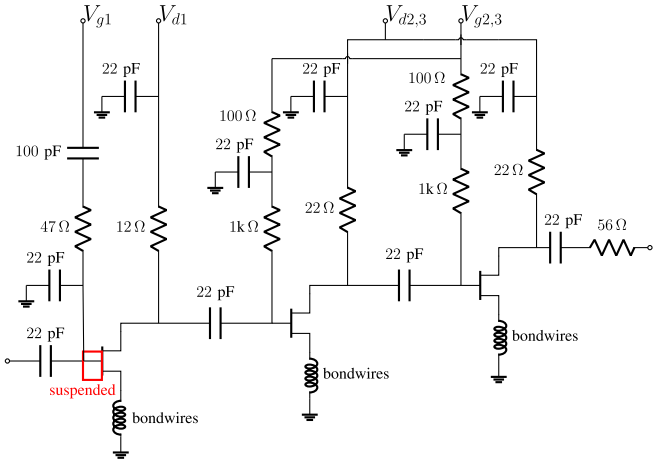

Fig. 10. Circuit schematic of the designed 4–6 GHz cryogenic HEMT LNA. The red frame represents the suspended transmission line [34].

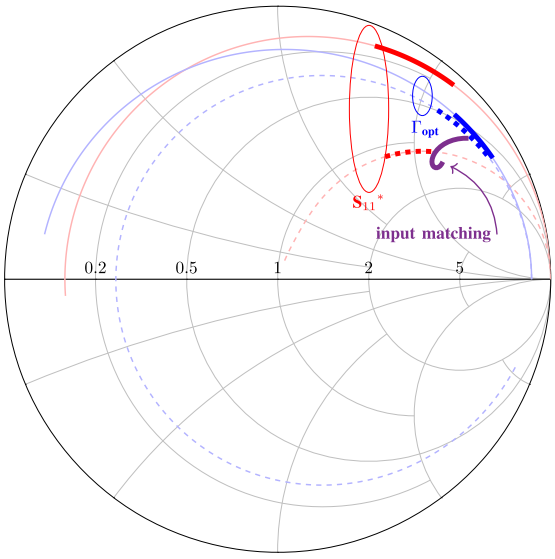

Fig. 11. Simulated Γ_{opt} and conjugate S_{11} at 4 K of a 4 × 50 μm gate-length and 100 nm gate-width InP HEMT biased at V_{ds} = 0.05 V and I_d = 1 mA up to 40 GHz. The dashed lines represent Γ_{opt} and S_{11} for the HEMT with two 1.6 mm long bond wires connected at the source using the inductance degeneration technique. The S_{22} of the input matching circuit was plotted at the purple solid line. The targeted frequency band from 4 to 6 GHz is marked in bold line.

The LNA was integrated with the dual-bias dc system described in Section III.

According to the cascade noise equation, the first stage HEMT is expected to contribute to most of the noise. Therefore, the first stage HEMT was matched for the lowest noise performance and sufficient gain to mitigate the noise contribution from the following stages. Considering the rapid degradation of G_{assoc} [Fig. 7(d)] and Z_{opt} (Fig. 9) at reduced dc power, it was reasonable to bias the first stage with a higher dc power to sustain G_{assoc} above 10 dB for a wider frequency band response. In addition, bond wires were implemented to act as an inductive source degeneration. Not only did the bond wires greatly improve the impedance matching by adjusting the conjugate S_{11} closer to the middle of the Smith chart but also slightly altering Γ_{opt} as shown in Fig. 11. This alleviated the simultaneous match of the noise and gain for

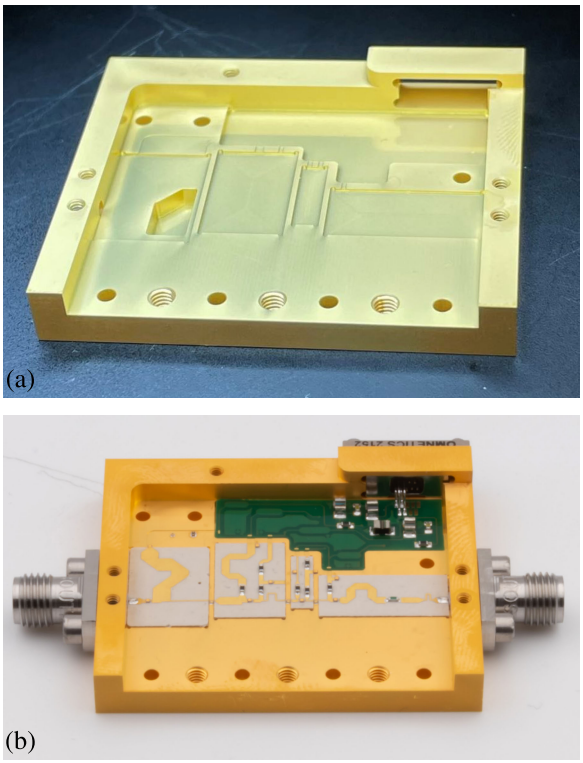

Fig. 12. Photographs of the fabricated hybrid 4–6 GHz cryogenic HEMT LNA. (a) Open chassis showing the chamber for the suspended transmission line in the input matching network. (b) Gold-plated open module with mounted RF and dc PCBs. The size of the full module is 34.9 × 42.5 × 3 mm [34].

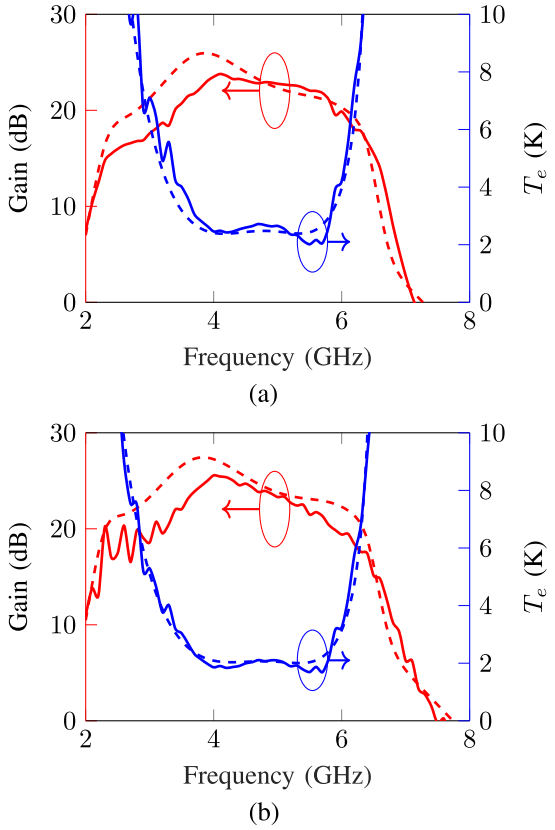

Fig. 13. Simulated and measured gain and noise under cryogenic environment (4 K) for the designed InP HEMT LNA at (a) 100 μW bias (V_{d1} = 0.06 V and I_{d1} = 1 mA, and $V_{d2,3}$ = 0.05 V and $I_{d2,3}$ = 0.8 mA) and (b) 200 μW bias (V_{d1} = 0.08 V and I_{d1} = 1.5 mA, and $V_{d2,3}$ = 0.08 V and $I_{d2,3}$ = 1 mA). The red solid line is measured gain performance and the red dashed line is simulated gain performance. The blue solid line is the measured noise temperature and the blue dashed line is the simulated noise temperature.

the InP HEMT, however, with a penalty on the available gain. This design tradeoff was made with the help of numerical optimization in the simulation.

The S_{22} of the input matching network (purple solid line in Fig. 11) was implemented by a high impedance suspended transmission line. This was realized by a 2-mm deep air chamber beneath the substrate in the circuit package visible in the photograph of the amplifier chassis in Fig. 12(a). The suspended transmission line provided 277 Ω impedance at 5.5 GHz.

The fabricated RF circuit PCBs and dc bias PCBs were packaged in a gold-plated aluminum chassis with SMA coaxial RF connectors and connected with bond wires. The photograph in Fig. 12(b) shows the open module of the fabricated three-stage hybrid HEMT LNA intended for cryogenic ULP operation.

V. Cryogenic LNA Measurement and Results

The measurement of the noise and gain of the LNA module was conducted by an Agilent N8975B NFA using the Y-factor method with an in-house 20 dB cold attenuator at 4 K [35]. A 4–8 GHz LNA connected at the output helped to sustain a high signal-to-noise ratio for sufficient measurement accuracy. We estimated a noise measurement uncertainty of ±0.3 K and a measurement repeatability of ±0.1 K.

Fig. 13 shows the simulated and measured gain and noise of the fabricated cryogenic LNA at 4 K biased at 100 and 200 μW total dc power. The measured results of the cryogenic LNA agree well with the simulations, which confirms the validity of the extracted small-signal noise model parameters under ULP. For the LNA biased at 100 μW, the measured average noise temperature $T_{e,avg}$ from 4 to 6 GHz is 2.6 K with a minimum value of 2.0 K at 5.7 GHz. The average gain is 22.5 dB for the designed frequency band. The LNA at 200 μW dc power reaches 23.1 dB average gain and 2.0 K $T_{e,avg}$ with a minimum value of 1.7 K at 5.7 GHz. At higher dc power for the first stage, the T_e is closer to the T_{min} meaning a relaxed tradeoff situation for noise and bandwidth as predicted by the extracted noise model parameters in Figs. 7 and 9. For qubit readout applications, an LNA gain higher than 20 dB is sometimes desirable to compensate for signal losses from the 4 K stage (where the HEMT LNA is located) to the 300 K stage. The gain can be increased by an additional stage in the HEMT LNA design or by adding another LNA at the 77 K stage.

The S parameters and P1dB at 4 K were measured by a Keysight N52478 PNA-X network analyzer. Fig. 14 shows the simulated and measured S_{11} and S_{22} of the designed LNA biased at 100 and 200 μW dc power. The average measured S_{11} of 4–6 GHz is −4.8 dB (lowest −9.6 dB) for 100 μW and −8.9 dB (lowest −13.5 dB) for 200 μW. The deviation between the measured S_{11} and the simulated S_{11}

TABLE II
COMPARISON WITH STATE-OF-THE-ART CRYOGENIC LNAS

Ref.	Amplifier type	Transistor	Freq. (GHz)	T_{eavg} (K)	Average Gain (dB)	P_{dc} (μW)	FOM (10^{-2}mW^{-1})
[7]	Hybrid	InP HEMT	4-8	1.2	42	7800	5.7
[8]	Hybrid	InP HEMT	4-8	2.8	27	300	68.6
[8]	Hybrid	InP HEMT	4-8	4.1	20	112	125.5
[13]	Hybrid	InP HEMT	4-8	1.6	44	4200	8.57
[9]	MMIC	SiGe HBT	3-6	4.3	36	1800	5.58
[36]	MMIC	SiGe HBT	0.1-3	4.6	30.5	1000	48.5
[6]	MMIC	SiGe HBT	4-8	3.2	27.5	1000	18.0
This work	Hybrid	InP HEMT	4-6	2.6	22.5	100	138.5
This work	Hybrid	InP HEMT	4-6	2.0	23.1	200	90.0

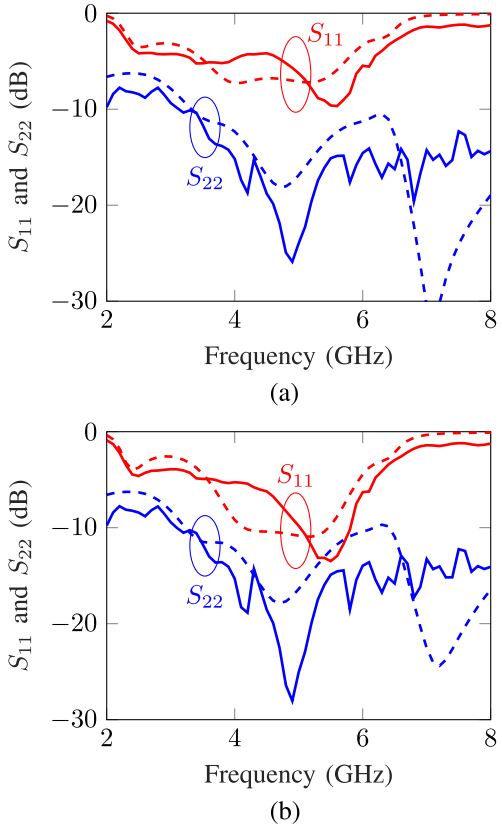

Fig. 14. Simulated and measured S_{11} and S_{22} in dB under cryogenic environment (4 K) for the designed InP HEMT LNA at (a) 100 μW bias (V_{d1} = 0.06 V and I_{d1} = 1 mA, and $V_{d2,3}$ = 0.05 V and $I_{d2,3}$ = 0.8 mA) and (b) 200 μW bias (V_{d1} = 0.08 V and I_{d1} = 1.5 mA, and $V_{d2,3}$ = 0.08 V and $I_{d2,3}$ = 1 mA). The red lines are measured (solid) and simulated (dashed) S_{11} and the blue lines are measured (solid) and simulated (dashed) S_{22}.

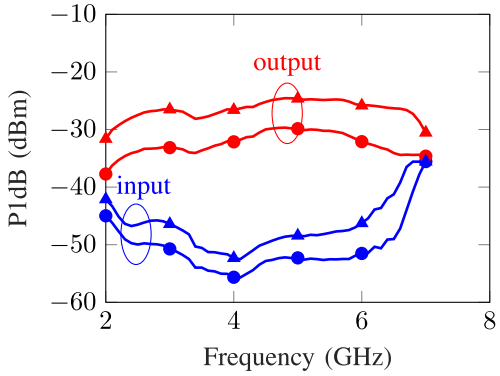

Fig. 15. Measured input and output P1dB of the fabricated LNA circuit at 4 K for various dc power. The blue lines are input P1dB and the red lines are output P1dB. Circle and triangle lines represent bias power of 100 and 200 μW, respectively.

can be attributed to assembly imperfections, VNA calibration errors, and variations in the HEMTs used for model extraction and LNA fabrication. Nonetheless, S_{11} is less critical for the qubit readout system due to the 60 dB isolation provided by the isolators between the parametric amplifier and the HEMT LNA [3]. The average S_{22} for the designed frequency band is −16.3 and −18.7 dB for 100 and 200 μW dc power, respectively.

The input and output P1dB of the fabricated amplifier are presented in Fig. 15. The average output P1dB for 100 and 200 μW is −30.6 and −23.2 dBm, respectively. The difference between the input P1dB from the output P1dB is the gain. Hence the corresponding average input P1dB is −53.0 and −49.0 dBm. The output P1dB increases with higher bias power.

The circuit performance was compared with other reported low-power cryogenic LNAs operating at similar frequency bands; see Table II. A figure of merit (FOM) which accounts for the tradeoff between bandwidth, noise, and power consumption is [36]

$$\text{FOM} = \frac{f_h}{f_l} \times \frac{hf_0}{kT_{\text{e,avg}}} \times \frac{1}{P_{\text{dc}}} \tag{8}$$

where P_{dc} is the dc power of the LNA, and f_h, f_l, and f_0 are the upper-band, lower-band, and central frequency, respectively. As seen from Table II, the performance of the LNA in this work biased at 100 μW exhibits the highest FOM. Moreover, to the best of our knowledge, this is the first time an LNA dissipating 200 μW provides a $T_{\text{e,avg}}$ of 2.0 K as required for several qubit readout systems [4], [31].

VI. CONCLUSION

We investigated the small-signal and noise model parameters for a cryogenic InP HEMT at ULP down to 1 μW. The extracted model showed that the InP HEMT for a fixed drain current sustained its noise performance until reaching a drain voltage of 0.05 V. After analysis of the LNA bandwidth requirement for superconducting qubit readout at 4 K, a 4–6 GHz hybrid cryogenic LNA was designed based on the extracted small-signal noise model at ULP. The fabricated

cryogenic HEMT LNA reached $T_{\mathrm{e,avg}} = 2.6$ and 2.0 K at $P_{\mathrm{dc}} = 100$ and 200 μW, respectively. To date, 200 μW represents the lowest dc power for a cryogenic HEMT LNA to attain 2.0 K average noise temperature for qubit readout frequencies. The input-referred P1dB for all biases was higher than -55 dBm. The large reduction in dc power consumption demonstrated for the cryogenic HEMT LNA designed for qubit readout [1], [4] makes the reported circuit interesting for future large-scale quantum systems.

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