VNA-Based Large-Signal Drain-Modulated Power Amplifier Measurement Setup With Digital Pre-Distortion

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***Abstract*—In this work a Vector Network Analyzer (VNA)-based large-signal drain-modulated measurement setup with simultaneous input and output signal extraction and Digitial Pre-Distortion (DPD) for Power Amplifier (PA) characterization is discussed. The proposed architecture is capable of handling coherent wideband modulated signaling with a calibrated reference plane down to the tip of the wafer probes, making it resilient to component changes outside the VNA directional couplers like signal generators and pre-amplifiers. Furthermore, a laboratory-grade drain modulator circuit with current sensing is proposed, being re-configurable for both Gallium Nitride (GaN) and Gallium Arsenide (GaAs) voltage ranges. Modulated measurements with a 500 MHz bandwidth have been performed on a two-way power-combined Doherty PA designed in 22 nm FD-SOI, resulting in an improvement of the Adjacent Channel Power Ratio (ACPR) of 10.7 dB and an improvement of the RMS Error Vector Magnitude (EVM) of 8.5% after DPD.**

***Index Terms*—Digital pre-distortion (DPD), microwave measurements, modulation, receivers, supply modulation, vector network analyzer.**

I. Introduction

Wideband characterization of Power Amplifiers (PAs) with real-time modulated communication signals has become more crucial over the years since higher frequencies allow for larger modulation bandwidths. These modulated signals have a relatively high Peak-to-Average Power Ratio (PAPR), which can result in spectral regrowth and out-of-band emissions. Aforementioned linearity issues can be resolved with Digital Pre-Distortion (DPD). This is an important characterization step of the PA under real operating conditions in modern communication systems. Simple, but powerful DPD can be implemented using the Indirect Learning Architecture (ILA), which is based on training a model [1], or the Iterative Learning Control (ILC) algorithm, which revolves around error minimization of the input signal [2]. DPD can be performed since the setup supports coherent signaling and simultaneous input and output signal extraction [3]–[5].

Another effective method of enhancing the average efficiency and potentially the linearity of a PA is drain modulation. Continuous drain modulation is limited by bandwidth, but it is still a versatile tool to improve the efficiency of the PA. Another implementation is Envelope Tracking (ET), where the time-varying envelope of the input signal is used to keep the PA near compression for highest efficiency, but it has implications on linearity [6].

This paper presents a Vector Network Analyzer (VNA)-based large-signal drain-modulated PA measurement setup where the input and output signal can be simultaneously extracted to allow for accurate DPD. The main benefit of this setup is that the reference calibration plane is not affected by any externally added active or passive devices by rerouting the internal receivers of the VNA [3], [7]. Furthermore, the setup is extended with drain modulation capabilities that are time-synchronized with the input signal waveform. Lastly, the design and characterization of a re-configurable drain modulator board are discussed in more detail.

II. Measurement Setup

A block diagram of the measurement setup is depicted in Fig. 1, where all highlighted items in blue show the internal hardware of the VNA, namely the Keysight PNA-X N5247A. An Arbitrary Waveform Generator (AWG) generates modulated signals for PA characterization under real-time communication scenarios. Furthermore, the AWG will drive a drain modulator board, which is used to investigate the effects of drain modulation on PAs in terms of efficiency and linearity. The main contribution of this setup is the possibility to simultaneously modulate and extract the drain voltage and current, respectively, for efficiency calculation of supply modulated PAs. These features are acquired by clever rerouting of the internal hardware of the VNA by removing some front panel jumpers to ensure that the receivers A, R1, B, and R2 (shown in red) are present before and after the PA. It is a crucial step to link the receivers to each other, while also being able to accurately determine the incident and reflected waves for highly linear operation after calibration. Hence, any external components added before receiver R1 will not alter the calibrated reference plane. Care should be taken that the receivers are not saturated when performing the measurements, having a 0.1 dB compression point of -4 dBm, so both internal and external attenuation is used to alleviate this issue.

On top of that, it is important to ensure coherent signaling between the VNA, AWG, and oscilloscope [8]. The reference clock of 10 MHz is taken from the VNA and connected to the AWG and oscilloscope. To correctly capture the generated signal of the AWG on the VNA it is crucial to set the correct tone spacing, Δf_{Tone}, when configuring the multitone measurement settings in the Spectrum Analyzer (SA) mode of the VNA. The tone spacing is calculated as

$$\Delta f_{\text{Tone}} = \frac{f_{\text{s,VNA}}}{N}, \tag{1}$$

where $f_{\text{s,VNA}}$ is the sampling frequency of the VNA, and N is the number of AWG samples. Moreover, vector averaging

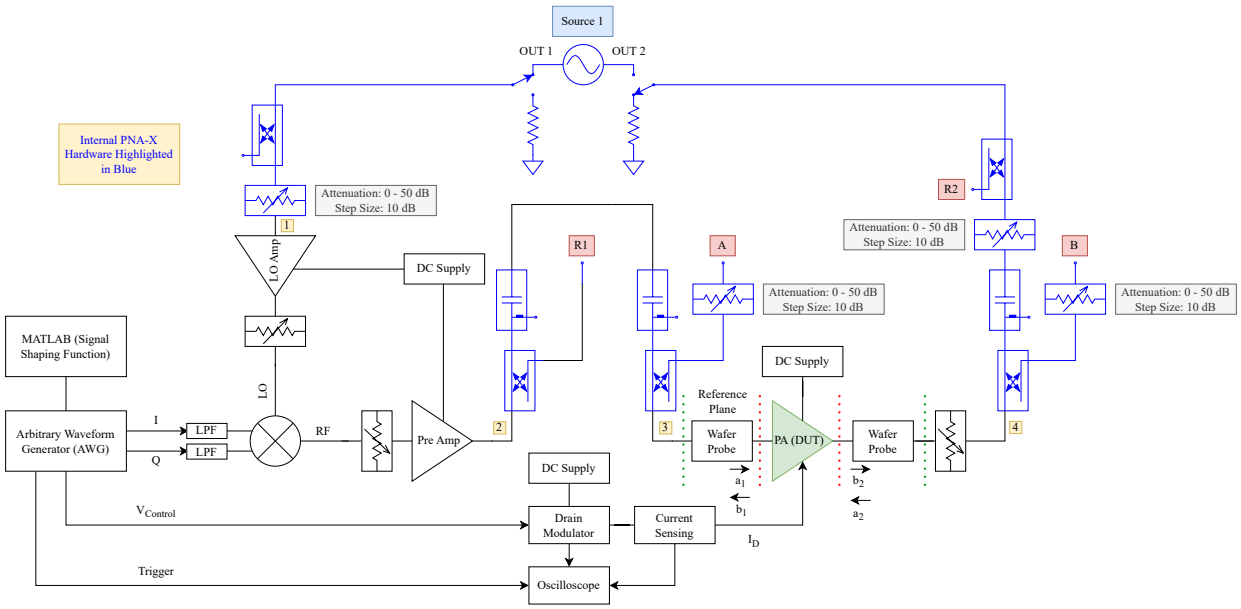

Fig. 1: On-wafer measurement setup employing drain modulation, simultaneous signal extraction, and digital pre-distortion. All internal connections and components of the VNA are highlighted in blue and the cable and wafer probe calibration reference planes are highlighted in green and red, respectively. The 10 MHz reference clock of the VNA is connected to the AWG and oscilloscope.

can be applied to enhance the Dynamic Range (DR) of the VNA, yielding more accurate measurement results at the cost of increased measurement times.

III. Calibration Procedure

It is of utmost importance to properly calibrate the measurement setup, which is done in three simple steps. Calibration is performed by connecting node 1 directly to node 2 in Fig. 1, not considering all components in between. Any coherence and vector averaging options in the SA mode have been disabled in the process.

First of all, a power calibration is performed, after which the loss of the cables is accounted for with a Short-Open-Load-Through (SOLT) calibration using an ECal module. This calibration file is then saved as Tier 1 calibration, highlighted in green in Fig. 1. Secondly, a SOLT calibration using a wafer impedance calibration substrate is performed, which is saved as Tier 2 calibration. Lastly, fixture de-embedding is performed, where the Tier 1 and Tier 2 calibration files are merged and the reference plane is correctly placed at the tip of the wafer probes, highlighted in red in Fig. 1. After calibration any external components may be added between node 1 and node 2, while the plane between node 3 and node 4 should not be altered anymore.

The current sensing circuitry is frequency dependent and also has to be calibrated. This is done by connecting it to a known resistive load, after which the differential voltage over the load is measured and its respective current is calculated. An equalization function for the AC current is then computed from the measured and ideal currents [9].

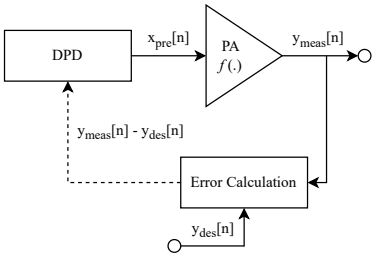

Fig. 2: Adaptive digital pre-distortion with iterative learning control implementation.

IV. Digital Pre-Distortion

The capabilities of the setup are extended with DPD, since it is possible to simultaneously extract the input and output signals. It is implemented according to the ILC scheme, as published in [2]. One of the main benefits of this algorithm is that it does not rely on training a model, but it focuses on optimizing the input signal directly via error minimization. Hence, this method has less complexity and will in turn speed up the measurement process. Fig. 2 shows the block diagram, where the input signal vector is updated as

$$\mathbf{x_{pre,n+1}} = \mathbf{x_{pre,n}} - \gamma \frac{\mathbf{y_{meas,n}} - \mathbf{y_{des}}}{G_{PA}}, \tag{2}$$

where $\mathbf{x_{pre,n+1}}$ is the new input signal vector, $\mathbf{x_{pre,n}}$ is the previous input signal vector, γ is a convergence scaling factor (typically 0.5), $\mathbf{y_{meas,n}}$ is the measured output signal vector, $\mathbf{y_{des}}$, is the desired linear output signal vector, and G_{PA} is the PA gain.

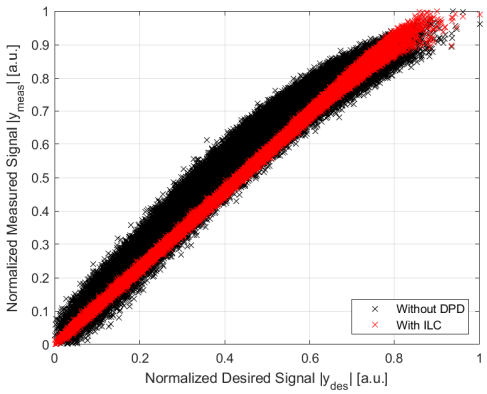

Fig. 3: Linearized measured output signal as function of the desired linear signal using iterative learning control digital pre-distortion.

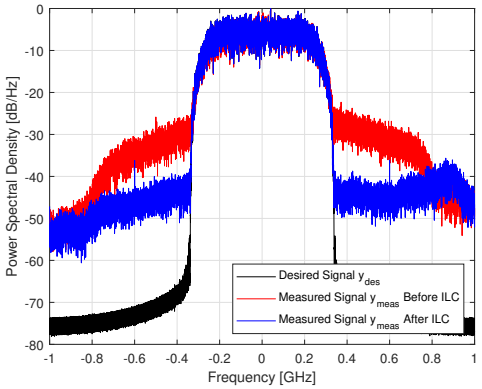

Fig. 4: Normalized desired and measured power spectral density before and after using iterative learning control digital pre-distortion.

V. Measurement Results

Measurements have been performed on a 28 GHz two-way power-combined Doherty PA designed in 22 nm FD-SOI. To improve heat dissipation, the PAs have been mounted on a suitable carrier. In the measurements, a 64-QAM constellation is considered, together with a 500 MHz modulation bandwidth. The tone spacing, calculated through (1), is 24.44 kHz.

Fig. 3 depicts the desired linear output signal compared to the measured output signal before and after applying the ILC algorithm. It can easily be seen that the PA is not driven into full saturation due to the lack of drive power available from the pre-amplifier, but slight compression is still visible due to back-off operation caused by the high PAPR of a real-time communication signal. The effect of this slight compression is tackled by applying DPD, which shows a nicely linear curve with significant reduction in memory effects afterwards.

The desired and measured Power Spectral Density (PSD) before and after applying DPD is shown in Fig. 4, where it should be noted that the enhanced linearity yields a significant improvement in the Adjacent Channel Power Ratio (ACPR) from -26.4 dBc to -37.1 dBc. Next to that, the RMS Error Vector Magnitude (EVM) has improved from 10.1% to 1.6%.

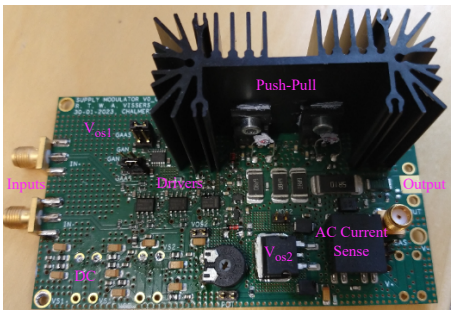

Fig. 5: PCB of the drain modulator, where the differential inputs are shown to the left, and the single-ended output is shown to the right.

VI. Drain Modulator

Fig. 5 presents the drain modulator PCB, whereas Fig 6 shows a simplified schematic of the design. An adaptive design has been made, which can be used for drain modulation of both Gallium Nitride (GaN) and Gallium Arsenide (GaAs) PAs, having respective voltage swings between 6 - 28 V (GaN) and 0 - 4 V (GaAs). Moreover, the desired small-signal design bandwidth should exceed 200 MHz.

The design consists of three current-feedback operational amplifiers, where the first one yields differential-to-single-ended conversion and most of the gain, while the second one provides a DC offset, V_{os1}, and some gain. The third operational amplifier forms a feedback loop over the driver and output push-pull stages to keep the output impedance of the drain modulator as low as possible. Furthermore, another DC offset, V_{os2}, is added in the inverting configuration to allow for the desired voltage swings. At the emitters of the transistors RC-networks have been added to avoid thermal leakage from the top to the bottom device. Moreover, between the push-pull stages an RC-network is added for stability. At the output of the PCB AC current sensing circuitry is added, as published in [9]. This is used to accurately compute the dynamic efficiency over time, since current measurements can be performed with a differential probe connected to the 0.2 Ω resistor at the output and accurate average current sensing is done at the decoupled lower output, $\overline{V_i}$.

The GaAs configuration of the drain modulator has been characterized, where the simulated output impedance and simulated/measured large-signal response are shown in Fig. 7. It can immediately be seen that the output impedance is below 1 Ω up to a frequency of 100 MHz, while staying below 6.5 Ω up to a frequency of 1 GHz. Furthermore, the simulated and measured large-signal responses correspond nicely to each other, but the simulations show less peaking due to limited parasitics being modeled. Large-signal characterization is performed with a 0.15 $V_{\text{pk-pk}}$ single-ended input signal, as this is the minimum amplitude setting of the AWG, which yields a 3.8 V voltage swing at the output of the drain modulator. The resulting half-power (3-dB) bandwidth of the measured large-signal response is more than 130 MHz, being comparable to the 160 MHz bandwidth obtained from simulations. The bandwidth is mainly limited by the third operational amplifier being slowed down with larger feedback resistors to ensure

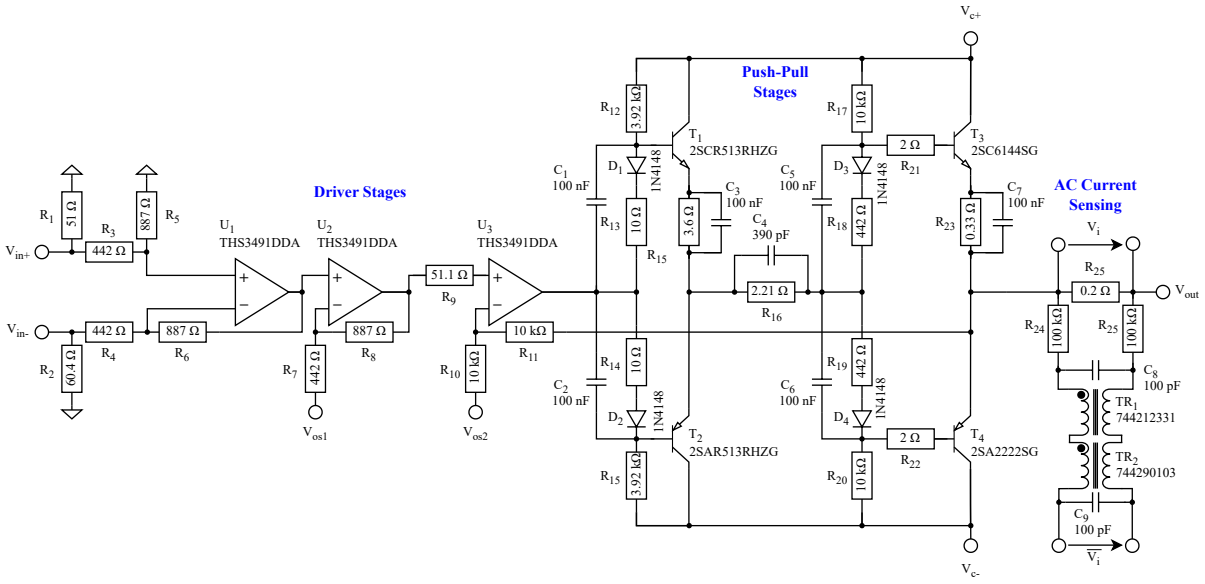

Fig. 6: Simplified circuit diagram of the drain modulator highlighting the driver stages, push-pull stages, and drain current sensing circuitry.

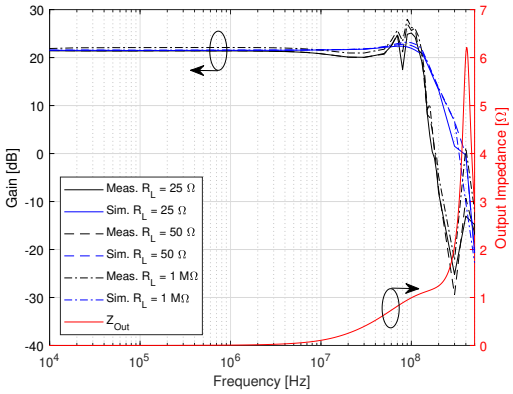

Fig. 7: Simulated and measured large-signal response of the drain modulator for different loads and the simulated output impedance.

stable operation. All stages in the GaAs configuration are biased with ±7.5 V.

VII. Conclusion

This work has presented a VNA-based large-signal drain-modulated wideband PA measurement setup. The front-plane jumpers of the VNA have been rerouted to isolate the calibrated reference plane to the wafer probe tips to enable simultaneous input and output signal extraction, which is then used to implement DPD. Moreover, the previously mentioned setup has been tested with 64-QAM measurements having 500 MHz bandwidth, where the implementation of DPD clearly shows a significant linearity improvement, decreasing the ACPR by 10.7 dB and the RMS EVM by 8.5%. Lastly, a re-configurable drain modulator design has been presented, which has a bandwidth larger than 130 MHz for GaAs operation. The combined setup forms a powerful tool for accurate and wideband characterization of supply modulated PAs.

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