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APL Materials

RESEARCH ARTICLE | NOVEMBER 21 2023

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APL Mater. 11, 111121 (2023)
https://doi.org/10.1063/5.0160287

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Cite as: APL Mater. 11, 111121 (2023); doi: 10.1063/5.0160287
Submitted: 31 May 2023 • Accepted: 2 November 2023 •
Published Online: 21 November 2023

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ABSTRACT

Very fast interface traps have recently been suggested to be the main cause behind poor channel-carrier mobility in SiC metal–oxide–semiconductor field effect transistors. It has been hypothesized that the NI traps are defects located inside the SiO_2 dielectric with energy levels close to the SiC conduction band edge and the observed conductance spectroscopy signal is a result of electron tunneling to and from these defects. Using aluminum nitride and aluminum oxide as gate dielectrics instead of SiO_2, we detect NI traps at these SiC/dielectric interfaces as well. A detailed investigation of the NI trap density and behavior as a function of temperature is presented and discussed. Advanced scanning transmission electron microscopy in combination with electron energy loss spectroscopy reveals no SiO_2 at the interfaces. This strongly suggests that the NI traps are related to the surface region of the SiC rather than being a property of the gate dielectric.

I. INTRODUCTION

Silicon carbide (SiC) power metal–oxide–semiconductor field effect transistors (MOSFETs) with a blocking voltage ≥650 V have become commercially available in recent years. However, devices for lower voltage applications (<650 V) are still not viable, mainly due to the rather poor channel-carrier mobility of the SiC MOSFETs. The low channel-carrier mobility has been attributed to interface defects or traps that are created during the oxidation process when thermally growing or depositing the silicon dioxide (SiO_2) to form the gate dielectric. These traps can be categorized into interface traps located at the SiC/SiO_2 interface and near-interface traps (NITs) located close to the interface inside the oxide. The origin of these traps is not well established, but some traps have been attributed to various carbon-related defects and dangling bonds that form during the oxidation process.[1,2] Traps that have a relatively slow response time (1 us–1 s at room temperature), labeled OX traps, give rise to a clear frequency dispersion in high–low frequency capacitance–voltage (high–low CV) analysis of MOS capacitors at room temperature.[3–5] These traps are both interface traps and

near-interface traps. Traps with a relatively fast response time (shorter than 1 us), labeled NI, are traps that are not detected at room temperature by high–low CV measurements. However, at cryogenic temperatures, these NI traps are observed as a frequency dispersion in high–low CV analysis and as a peak in conductance spectroscopy.[4–6] Currently, the most effective way of passivating the OX traps is to anneal dry thermal oxide in pure NO ambient at high temperatures (1150–1350 °C). Commercial SiC MOSFETs are based on such nitridation of the interface. However, even with an order of magnitude reduction in OX interface-trap density, the channel-carrier mobility is only about 30–40 cm^2/Vs in lightly doped p-type epilayers.[7–9]

Recent studies show that NO annealing results in an increased density of NI traps that are present in dry thermal oxides.[4] Since the NI traps have about two orders of magnitude higher density than OX traps in NO annealed oxides, it has been suggested that the NI traps are the main factor limiting the channel-carrier mobility in commercial SiC MOSFETs.[3] The origin of the NI traps is yet unclear, but they have been modeled as near-interface traps located within the SiO_2 gate dielectric.[6] MOSFETs using sodium enhanced gate oxides exhibit high field effect mobilities (up to 150 cm^2/Vs).[10] A recent study showed the absence of NI traps in such oxides.[11] Alternative gate dielectrics, such as aluminum oxide (Al_2O_3) and aluminum nitride (AlN), are of interest because they are high-κ dielectrics and possibly free of NI traps. Studies on Al_2O_3 as a gate dielectric have shown some promising results with reported peak channel-carrier mobility of 50–150 cm^2/Vs.[12,13] Few studies have been published on AlN as a gate dielectric, although a low density of interface traps (D_{it}) in AlN/SiC structures has been reported.[14,15] AlN is of special interest since the 2H–AlN crystal structure has a very close lattice match to the 4H–SiC crystal with about 1.2% mismatch between the values of the lattice parameter *a*.[16–18] Unfortunately, both Al_2O_3 and AlN suffer from severe charge injection and gate leakage. Thus, to reduce leakage, AlN and Al_2O_3 dielectrics are often implemented using a dielectric stack, where SiO_2 is used as a secondary dielectric forming the Al/SiO_2/AlN/SiC or Al/SiO_2/Al_2O_3/SiC stack.[14] However, that does not fix the charge injection problem.

In this work, we investigate the interface quality and density of interface traps using metal–insulator–semiconductor (MIS) capacitors and four different dielectrics: (1) NO annealed oxide, (2) sodium enhanced oxide (SEO), (3) AlN, and (4) Al_2O_3. The MIS capacitors are investigated using high–low CV and conductance spectroscopy analysis at cryogenic temperatures. Scanning transmission electron microscopy (STEM) was performed on the AlN and Al_2O_3 samples to investigate the SiC/dielectric interface. Our observations show that the NI traps are only absent in the SEO oxide and are present in large densities in both AlN and Al_2O_3 samples. This suggests that the NI traps are native to the SiC surface rather than the SiO_2 dielectric.

II. EXPERIMENTAL DETAILS

Samples were fabricated on 4° off-axis, n-type, epitaxial 4H–SiC wafers with doping concentrations in the range from 3.3×10^{15} to 2.7×10^{16} cm^{-3}. The NO sample was made by dry oxidation at 1250 °C for 60 min and post-annealed in pure NO for 60 min, resulting in a 41 nm thick oxide. The sodium enhanced oxide (SEO) was grown for 40 min in O_2 atmosphere at 1200 °C in alumina carrier boats that are sodium contaminated, resulting in a 52 nm thick oxide.[10] The SEO sample is used here as a reference sample where the NI trap is absent. The single crystalline AlN layer of the AlN sample was grown in a horizontal hot-wall MOCVD reactor at 1100 °C.[19] Ammonia and $Al_2(CH_3)_6$ were used as precursors for nitrogen and aluminum, respectively. Prior to growth, the SiC surface was exposed to H_2 ambient at 1320 °C in order to obtain an oxide-free surface. The details of the SiC surface cleaning and AlN growth are given in Ref. 19. The thickness of the crystalline 2H–AlN is 30 nm. The Al_2O_3 sample was made by depositing 1–2 nm of Al by electron beam evaporation of Al in a vacuum chamber at a rate of 0.05 nm/s, and then, the sample was immediately baked on a hot plate in air at a temperature of 200 °C for 5 min to form an Al_2O_3 layer.[20] This process of deposition and subsequent oxidation was repeated twelve times to get a target thickness of 15 nm with an overall time span of about 4 h. In our case, this method produced Al_2O_3 amorphous films that have a lower density of interface traps, are more resistant to charge injection, and exhibit lower leakage as compared to our ALD grown Al_2O_3 samples.[20]

Scanning transmission electron microscopy in combination with electron energy loss spectroscopy (EELS) was performed on the AlN and Al_2O_3 samples to investigate the SiC/AlN and SiC/Al_2O_3 interfaces. The two samples were prepared using mechanical cutting, mechanical polishing, and Ar-ion thinning (Gatan PIPS Model 691) at a 5° angle. The imaging and spectroscopy were performed at 300 keV on the Linköping double-corrected FEI Titan^3 60–300. Images were acquired in high-angle annular dark-field (HAADF) mode with collection semi-angles between ~60 and 200 mrad. A series of images were reconstructed using *SmartAlign*[21] for *Digital Micrograph* (Gatan Inc.). The EELS was performed using a GIF Quantum ERS detector (Gatan Inc.), with a convergence semi-angle of 22.0 mrad and a collection semi-angle of 56.5 mrad. It was operated in dual-EELS mode with dispersions of 0.05 in the ranges of −10.0–92.4 and 50.0–152.4 eV, for Al and Si $L_{2,3}$-edges, or 490.0–592.4 eV, for C and O K-edges. In addition, 0.25 eV/channel was used in the ranges of −50.0–462.0 and 50.0–562.0 eV for all the edges mentioned above as well as the N K-edge. The scans were acquired as spectrum images of sites neighboring the sites where high-resolution images were acquired. Subsequently, these were integrated along the interface to form linescans with a spectrum in each pixel. The intensity of each element as a function of position was calculated by removing the background according to a power law, and the signal intensity was integrated from the onset energy and ~50 eV above. To distinguish Si from Al, which are overlapping, the Al intensity was subtracted from the measured Si intensity: $I_{Si} = I^*_{Si} - I_{Al}$, where I_{Si} denotes the real Si-intensity, I^*_{Si} denotes the measured intensity at Si onset energy, and I_{Al} denotes the measured intensity at Al onset energy.

All electrical measurements were performed in a closed loop helium cryostat controlled and monitored using a Lakeshore 311 temperature controller. High-frequency capacitance–voltage and conductance spectroscopy measurements were performed using the Agilent 4980A LCR meter and quasi-static capacitance–voltage measurements using a Keithley 6517B electrometer.

High frequency measurements were performed by sweeping a DC voltage with a 10 mV AC test signal at different frequencies (1 kHz–1 MHz) from depletion to accumulation at fixed temperatures between 75 and 300 K. Samples are cooled down to the measurement temperatures without bias applied to the capacitors.

Between measurements at cryogenic temperatures, the samples were heated to 300 K without bias to enable electrons that got trapped at the interface during the measurements at cryogenic temperatures to be thermally emitted from the interface. Quasi-static capacitance is performed by sweeping DC voltage from depletion to accumulation at a constant sweep rate while the charge is measured. Then, the capacitance was calculated as $C = dQ/dV$. Conductance spectroscopy measurements were performed by cooling the samples down to 50 K without bias applied. At 50 K, a fixed DC bias coupled with an AC test signal with 10 mV amplitude at different frequencies (1 kHz–1 MHz) was applied to the MIS capacitor. The samples were then heated with a fixed ramp of 5 K/min to 300 K while the conductance and temperatures were monitored. This was repeated with different DC voltage biases applied to the MIS capacitors, ranging from weak depletion to weak accumulation. The exact gate voltage range depends on the flatband voltage of each sample.

III. RESULTS

Figure 1 shows the conductance spectra of the MIS samples, (a) NO annealed, (b) sodium enhanced oxide, (c) aluminum nitride, and (d) aluminum oxide, at a frequency of 100 kHz for different applied bias voltages. The applied bias range for each sample is chosen such that the surface potential is within a similar range for all samples, corresponding to weak depletion. In this bias range, charge injection and leakage in the AlN and Al_2O_3 samples are negligible. The peak at about 75 K, noted as N(c), visible in all samples is a signal from nitrogen dopant ions in the SiC epilayer located at cubic sites, and the rising signal at 50 K is attributed to nitrogen dopant ions located at hexagonal sites.[4] A small peak appears in the SEO sample [Fig. 1(b)] at about 140 K at low applied voltages corresponding to depletion conditions. This signal is attributed to titanium (Ti) impurities within the SiC epilayer located at cubic sites with activation energies between 150 and 170 meV, in agreement with the literature.[22] This signal disappears at higher voltages when the sample enters weak accumulation, which agrees with the assumption that the signal is due to point defects within the SiC epilayer and not related to interface traps.

The increasing signal at 250 K and above is from slow traps labeled OX.[4,5] These traps are located at the SiC/dielectric interface within the SiC bandgap and give rise to frequency dispersion in CV measurements at room temperature.[5] Compared to the NO sample, this signal is suppressed in the SEO, AlN, and Al_2O_3 samples.

The peak labeled NI is observed in the NO annealed, AlN, and Al_2O_3 samples but is absent in the SEO sample. The peak is observed at a surface potential of about −100 mV within the same temperature range in all samples where it appears. This is an agreement with previous observations of NI in NO annealed samples.[6] This signal is due to very fast interface traps and has in previous studies been attributed to electrons tunneling to and from near-interface traps located inside the SiO_2 dielectric with energy levels very close to the SiC conduction band edge.[6] However, the presence of the NI signal in the AlN and Al_2O_3 samples suggests that the NI trap is not a native trap within the SiO_2 dielectric. Previous studies used the SiC/SiO_2

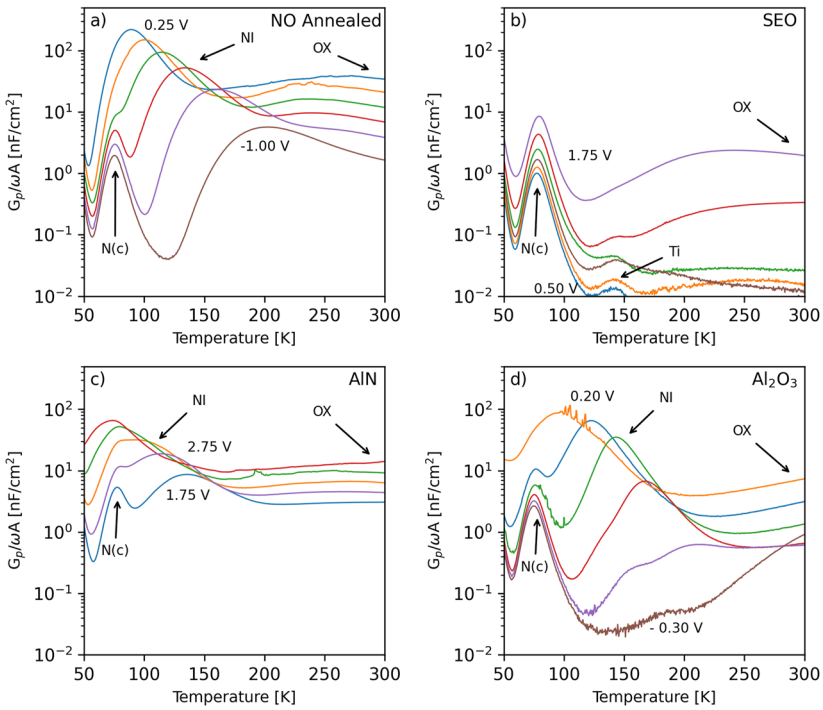

FIG. 1. Conductance spectra of all samples with different voltages applied at a test signal frequency of 100 kHz. Voltage steps are chosen to correspond to weak depletion for each sample. (a) NO annealed, (b) sodium enhanced oxide, (c) aluminum nitride, and (d) aluminum oxide.

conduction band offset as an energy barrier to model the NI signal. The conduction-band offsets of AlN and Al_2O_3 with respect to SiC are 1.3 and 1.9 eV, respectively,[23,24] which are much smaller values in comparison to SiO_2. However, the NI signal is observed in all three dielectrics under almost identical bias conditions, corresponding to weak depletion. This suggests that the physical location of the defect responsible for the NI signal is in the surface region of SiC rather than being a property of the gate dielectric.

It is possible to analyze the OX traps and the NI traps using CV analysis, even though the NI trap is not as well resolved as in the conductance spectroscopy analysis. Figure 2 shows the capacitance–voltage curves for all the samples at 300 and 75 K. The samples are cooled down to a fixed temperature without applying bias. At each temperature, the capacitance is recorded, while the MIS capacitor is biased from depletion to accumulation. Between measurements at cryogenic temperatures, the samples are heated to 300 K to emit all the electrons that get trapped at the interface.

We first focus on the CV data at 300 K. The CV of the NO annealed sample at 300 K is shown in Fig. 2(a). A small frequency dispersion between the high frequency curves is observed. The main contribution to such a dispersion at room temperature is due to OX traps, whose density is much higher in dry oxides than in NO oxides.[5] The NO annealing of a dry oxide reduces the density of OX traps by an order of magnitude (not shown). A significant dispersion is still observed between the 1 kHz and quasi-static curves in weak depletion. This is due to slow OX traps that are still present and are too slow to respond to the 1 kHz test signal by emitting the captured electrons, but can follow the quasi-static CV. The SEO sample [Fig. 2(b)] shows similarly a small frequency dispersion between the high frequencies but a significant dispersion between the 1 kHz and the quasi-static curve at 300 K. The AlN and Al_2O_3 samples are sensitive to charge injection and leakage. Therefore, CV measurements are not performed in high accumulation to minimize charge injection and the risk of leakage in these samples. The conventional high–low method extracts D_{it} from weak depletion to the weak accumulation region of the CV curve, so it is not necessary to probe for high accumulation. The AlN sample [Fig. 2(c)] shows very small frequency dispersion at higher frequencies and a much smaller dispersion between the 1 kHz and quasi-static curve in weak depletion as compared to the NO annealed and SEO samples. The Al_2O_3 [Fig. 2(d)] shows almost no frequency dispersion at high frequencies but a small dispersion between the quasi-static and 1 kHz curves. The quasi-static curve for the Al_2O_3 sample is questionable and shows a poor fit to the high frequency curves in depletion. This is due to the sensitivity of the Al_2O_3 layer to electron injection.[20]

We now discuss the 75 K CV curves that include information regarding the NI trap.[5] When the NO annealed sample is cooled down to 75 K, a large frequency dispersion between the higher frequencies is observed. This is in part caused by the freezing of slow traps and is mainly due to the frequency response of NI traps, which is accompanied by a knee in the curves that becomes more pronounced with increasing frequency,[5] as noted in Fig. 2(e). This knee is observed in weak depletion, close to the flatband voltage of the sample at this temperature, at the onset of the dispersion. The voltage where the knee is observed corresponds to the surface potential where the NI trap signal is observed in the conductance spectroscopy at this temperature. This knee and the frequency dispersion are thus attributed to the very fast interface trap NI. The

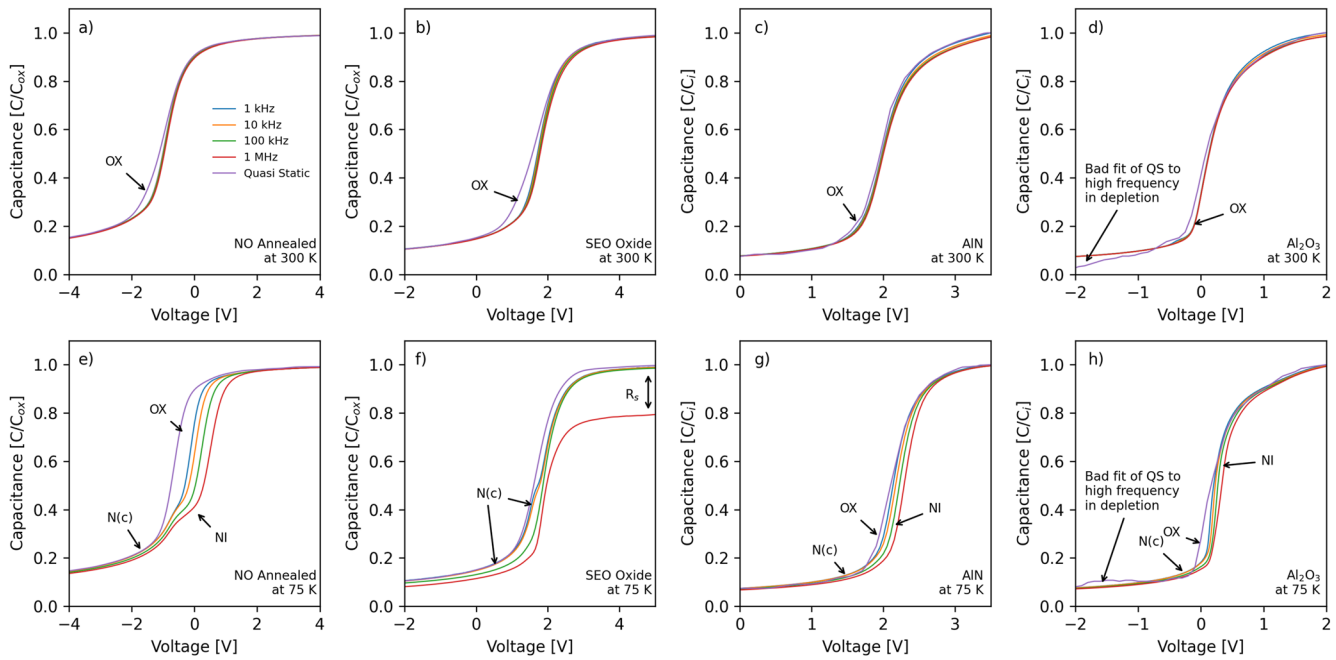

FIG. 2. Capacitance–voltage spectra of all samples at 300 and 75 K for NO annealed (a) and (e), sodium enhanced oxide (b) and (f), aluminum nitride (c) and (g), and aluminum oxide (d) and (h). The frequencies used are quasi-static, 1, 10, 100 kHz, and 1 MHz.

SEO sample [Fig. 2(f)] shows dispersion in depletion between the higher frequencies; however, this dispersion is different from the dispersion we observe in the NO annealed sample. This dispersion appears close to the flat-band voltage and continues to deplete. This corresponds to the nitrogen doping ions at cubic sites in the SiC epilayer that form a peak in the conductance spectra at this temperature and is, therefore, noted as N(c) in Figs. 2(e)–2(h). All the samples have this dispersion in depletion due to the partial freeze out of the nitrogen ions.[5] The SEO sample shows evidence of series resistance in accumulation, as the 1 MHz curve does not reach accumulation. The AlN sample [Fig. 2(g)] shows frequency dispersion, although much smaller than what we observe in the NO sample. This frequency dispersion can again be attributed to the NI traps since this dispersion appears at the same surface potential as the NI peak in the conductance spectroscopy at this temperature. The Al_2O_3 sample also shows frequency dispersion at 75 K. Again, as for the AlN sample, this dispersion appears at the same surface potential as when the NI peak is observed in the conductance spectroscopy measurements. Figure 3 shows the density of interface traps as a function of energy below the conduction band edge, extracted from both CV and conductance spectroscopy. The extracted values from CV and conductance spectroscopy show the same trend as a function of energy. However, the absolute values from the two techniques are not directly comparable. The D_{it} from the conductance spectroscopy is only extracted from the NI peak, whereas the D_{it} from the high–low CV is the accumulative density of all traps that contribute to the frequency dispersion. These traps are OX traps as well as NI traps. At room temperature (0.3–0.5 eV), the D_{it} is dominated by the density of OX traps, whereas at 75 K (0.07–0.12 eV), most of the signal is due to NI, with some contribution from OX traps.

The extracted values from the CV curves are calculated using the high–low method, where we use the 1 MHz and quasi-static curves for the calculations at all tested temperatures (75, 125, 200, and 300 K), and the results are shown by solid lines in Fig. 3. The extracted D_{it} from CV analysis at room temperature suggests that the Al_2O_3 sample has the highest density of OX traps. However, the poor fit of the quasi-static curve to the high frequency curves of the sample results in an overestimate of the D_{it}. The D_{it} of the Al_2O_3 sample increases as we probe closer to the SiC conduction band edge, due to response from the NI trap, but is significantly lower than the D_{it} in the NO sample. The NO and SEO show a similar D_{it} at room temperature that corresponds to OX traps. Near the SiC conduction band edge, the NO shows the highest D_{it}, but the SEO shows the lowest D_{it} due to the absence of the NI trap and is about 10 factors lower than the NO sample. The AlN sample shows the lowest D_{it} at room temperature, but increases closer to the SiC conduction band edge and has about two times higher D_{it} than the SEO.

The symbols in Fig. 3 show D_{it} obtained from conductance spectroscopy and extracted from the NI peak using Arrhenius analysis. The conventional Arrhenius analysis, assuming thermal emission of electrons, does not correctly describe the behavior of the NI signal since it is largely due to direct tunneling.[6] However, a comparison between the densities of NI in differently prepared dielectrics can still be made using this approach. An accurate estimate of the total concentration of NI traps is not possible, but one can compare the density of electrons trapped in NI in different types of gate dielectrics using CV or conductance analysis.

The STEM analysis of the Al_2O_3 and AlN samples reveals the sharp interface with atomic resolution, where the 4H–SiC is contrasted to the amorphous Al_2O_3 (Fig. 4) and the 2H–AlN (Fig. 5). Spectroscopically, the Si, N, O, Al, and C signals are presented as linescans next to their corresponding high-resolution images (Figs. 4 and 5). The transitions from SiC to the dielectric are clearly observed, with Al and O replacing Si and C (Fig. 4), and Al and N replacing the same (Fig. 5). The Si signal appears a bit noisier due to the spectroscopic overlap with Al, as described in the experimental

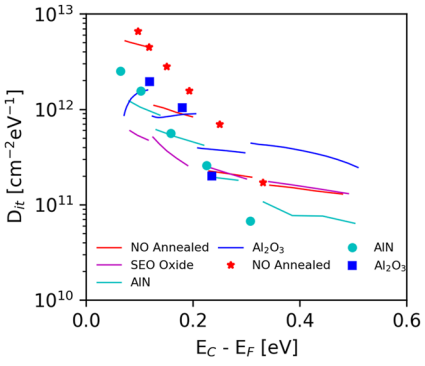

FIG. 3. Density of interface traps extracted from high–low capacitance–voltage measurements (solid lines) and the peak value of the NI peak from conductance spectroscopy (symbols).

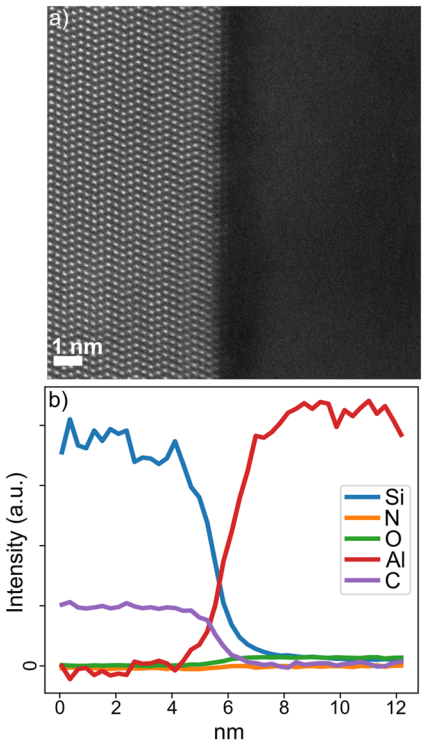

FIG. 4. (a) STEM image of the SiC/Al_2O_3 interface. (b) EELS plot showing the intensity of the Si, N, O, Al, and C signals.

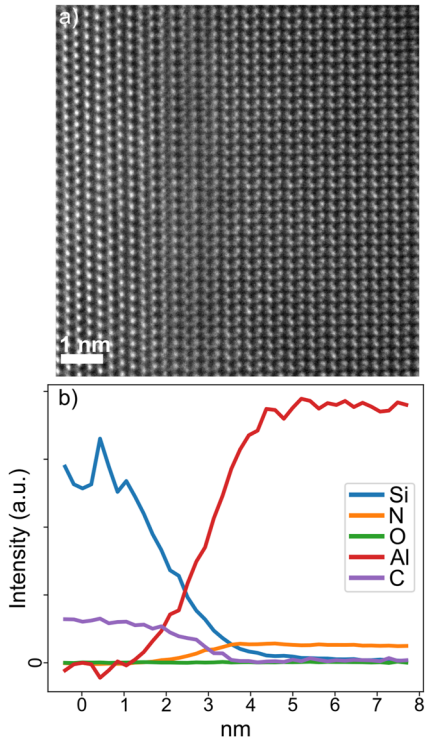

FIG. 5. (a) STEM image of the SiC/AlN interface. (b) EELS plot showing the intensity of the Si, N, O, Al, and C signals.

details. For the Al_2O_3 sample, the O is seen to be introduced after the interface, not detected in the SiC. For the AlN sample, the O signal is extremely low, just about detectable, and only in the AlN but not in the SiC. In addition, the fine structures of C, N, and O, indicative of local chemistry, were all qualitatively analyzed and are shown in the supplementary material. The structures from the interface region were compared to the same further from the interface, with no detectable differences.

IV. DISCUSSION

The NI trap detected at the SiC/SiO_2 interface is also present at the SiC/AlN and SiC/Al_2O_3 interfaces. Previously, it was reported that the peak position in temperature of the NI conductance signal depends strongly on the surface potential. For a given frequency, the NI peak appears at a certain surface electron density.[6] The same behavior is observed here for the NI signal in the AlN and Al_2O_3 samples. Furthermore, this is reflected in Fig. 3, where the D_{it} based on the NI signal increases rapidly toward the conduction band edge for all three samples. It is evident that the gate dielectric has no significant effect on the signature of the NI trap since the NI signal appears at approximately the same temperature for each sample for a given bias corresponding to weak depletion.

Since the NI signal is observed in the AlN and Al_2O_3 dielectric samples, we performed STEM-EELS on these samples to ensure that there is no native SiO_2 or traces of SiO_2 islands left at the SiC/dielectric interface. This is to make sure that there is no SiO_2 near the interface that might produce the NI signal. Such a presence of SiO_2 was neither observed in the STEM images nor in the EELS linescans. The linescans across the interface for both samples revealed relatively sharp interfaces, with O-presence only in the Al_2O_3 dielectric, where Si was not observed. In addition, the fine-structure comparison indicates that the structures do not suffer from inclusions of native oxidation or islands at the interface. This can be compared to the study by Serin *et al.*,[25] where O inclusion in AlN would affect the fine-structure of N, which was not observed in our case. Hence, this further strengthens the conclusion that no SiO_2 inclusions are observed at the interface. Based on these findings, we suggest that the NI traps are native to the surface region of the SiC epilayer rather than the SiO_2 dielectric. It is clear that the type of gate dielectric used has little impact on the NI trap. This suggests that the trap is located at the SiC surface, located at atomic-bond distances from the free electrons in SiC. This is supported by recent simulation and modeling of conductance data of the NI trap, which concluded that the majority of the NI traps are at distances between 0.2 and 0.3 nm from the SiC surface, which corresponds to the length of inter-atomic bonds.[26] The exact chemical nature of NI remains unknown. The STEM and EELS studies exclude the possibility of thin SiO_2 layers or SiO_2 islands being the source of the NI trap. However, EELS cannot detect any accumulation of chemical elements such as nitrogen or carbon at the interface. It is, therefore, not possible to exclude the possible role of these chemical elements in forming the NI trap. It is clear that the density of NI traps increases upon nitridation, and a pile up of nitrogen is detected at the SiO_2/SiC interface.[27] Therefore, nitrogen is one possible ingredient in the defect giving rise to the NI signal. Since no difference in the fine structure between the interface and regions away from the interface was detected by STEM-EELS, no difference in bonding at the interface could be concluded.

V. CONCLUSIONS

In this work, we have demonstrated the presence of very fast NI traps in AlN and Al_2O_3 dielectrics at the SiC/dielectric interface using capacitance–voltage and conductance spectroscopy at cryogenic temperatures. Furthermore, we have shown that there is no native SiO_2 at the SiC/dielectric interface using STEM-EELS analysis. Therefore, the results strongly suggest that the very fast NI traps are not a property of the gate dielectric but are related to inter-atomic bonds at the SiC surface.

SUPPLEMENTARY MATERIAL

The figures in the supplementary material show a comparison of the EELS edge structures for C, N, and O going across the interface from SiC to the AlN and the Al_2O_3 dielectrics.

ACKNOWLEDGMENTS

A. M. Vidarsson and E. Ö. Sveinbjörnsson were supported by the Icelandic Centre for Research (Rannís) under Grant No. 185412-052 and the University of Iceland Research Fund. Parts of this work were performed at the Queensland node of the Australian National Fabrication Facility (ANFF), a company established

under the National Collaboration Research Infrastructure Strategy to provide nanofabrication and microfabrication facilities to Australia's researchers. This work was in part performed in the competence center for III-nitride technology, C3Nit–Janzén, supported by the Swedish Governmental Agency for Innovation Systems (VINNOVA) under the Competence Center Program Grant No. 2022-03139 and by the Swedish Foundation for Strategic Research under Grant No. EM16-0024.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Arnar M. Vidarsson: Data curation (lead); Formal analysis (lead); Writing – original draft (lead); Writing – review & editing (lead). **Axel R. Persson**: Writing – review & editing (equal). **Jr.-Tai Chen**: Writing – review & editing (supporting). **Daniel Haasmann**: Writing – review & editing (supporting). **Jawad Ul Hassan**: Writing – review & editing (supporting). **Sima Dimitrijev**: Writing – review & editing (supporting). **Niklas Rorsman**: Writing – review & editing (supporting). **Vanya Darakchieva**: Writing – review & editing (supporting). **Einar Ö. Sveinbjörnsson**: Writing – review & editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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