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Integrated 10-GHz Graphene FET Amplifier

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(Regular Paper)

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ABSTRACT Graphene has unique electrical and mechanical properties which can pave the way for new types of devices for microwave applications. However, emerging technologies often have problems with yield and still considerable variation in device parameters cause great challenges for circuit design. In this paper, we present the design and development of an integrated graphene FET amplifier addressing this challenge. A representative graphene FET was selected from a set of devices and then the input and output matching circuits were designed using the negative-image technique. The two-finger GFET with a gate length of 0.5 μ m exhibit a typical f_T and f_{max} of 35 GHz and 37 GHz, respectively. The integrated graphene FET amplifier was fabricated on a high-resistivity silicon substrate together with thin film capacitors, airbridges, and spiral inductors. A record high gain of 4.2 dB at 10.6 GHz was measured for a single transistor amplifier stage and agrees well with simulations. These results indicate significant progress towards active microwave circuits based on emerging 2D materials.

INDEX TERMS Amplifiers, field-effect transistors, graphene, integrated circuits, microwave electronics, negative-image techniques.

I. INTRODUCTION

Since the first top-gated graphene field-effect transistors (GFETs) demonstrated by Lemme et al. in 2007 [1], the microwave performance of GFETs has improved significantly in recent years [2]. The high carrier velocity and mobility in graphene as well as the possibility for heterogeneous integration open up interesting opportunities in future microwave applications. Until today, several graphene RF/microwave circuits have been reported. This includes frequency converters [3], phase shifters [4], power detectors [5]–[7], multiplier [8], rectifier [9], as well as microwave amplifiers [10]–[13]. Still, the power gain in such amplifiers is limited due to inherent challenges associated with the zero bandgap in graphene that results in poor current saturation. In addition, high parasitic resistances due to contamination and imperfections during fabrication degrades the maximum frequency of oscillation even further. However, recent progress in GFET technology shows a figure-of-merit of $f_{max}L =$ 23 GHz μ m [14] and with a promising scaling behaviour.

The first graphene-based amplifier providing voltage gain was reported in [15]. In 2012, the first matched small-signal

graphene FET amplifier with a power gain of 10 dB at 1 GHz was reported by Anderson *et al.* [10]. Noise properties of graphene FETs was analysed in 2014 [11] and a gain of 1.5 dB at 0.2 GHz was presented in 2015 [12]. A GFET amplifier with integrated microstrip lines was published in 2016 [13] with a gain of 3.4 dB at 14.3 GHz. Recently, a C-band graphene low-noise amplifier with a maximum gain of 8.3 dB at 5.5 GHz was reported [16]. However, graphene transistor technology is still in its infancy and faces several manufacturing difficulties resulting in poor yield and large variation in device parameters [17]. Hence, there is a strong need to improve graphene technology as well as to develop methods for robust design in order to reduce sensitivity to variations in transistor parameters.

In this paper, an integrated microwave GFET amplifier has been designed, fabricated, and characterized with respect to small-signal gain. To overcome the wide variations of GFET parameters as well as the poor unilateral figure-of-merit, U, the negative-image equivalent circuit technique was applied. A set of several GFET devices was analysed in order to define a representative performance as well as estimate the spread in



FIGURE 1. S-parameters measured between 1 GHz and 20 GHz at optimum gate bias and $V_D = 1.2$ V for a set of thirteen different GFETs (*1 – 13) fabricated on the same chip. The total width of the GFET is 30 μ m.

gain and return loss of the final amplifier design. The results show good prospects for future microwave- and millimeterwave amplifiers based on graphene technology.

II. DESIGN OF MICROWAVE GFET AMPLIFIER

In Fig. 1, *S*-parameters of thirteen devices, from a previous batch, show a wide variation. The *S*-parameters were measured at optimum gate bias with respect to power gain. The on-wafer *S*-parameter measurements were calibrated using short, open, load, and through structures (SOLT) and in a coplanar waveguide (CPW) environment.

The extracted maximum available gain (MAG) at 10.5 GHz is calculated and shown in Fig. 2. A variation of the extracted MAG is up to 4 dB across all thirteen GFETs and the average MAG is approximately 7.7 dB. GFET #1 and #8 exhibit poor MAG compared to other devices. The spread in transistor performance is mainly associated with variations in source and drain resistances [17]. The average value of the series resistance ($R_S + R_D$) of the GFET is around 15 Ω with a corresponding standard deviation of 5 Ω .

The measured S-parameters show that the fabricated GFETs are not unilateral, *i.e.*, $U \approx 0.1$. The integrated GFET amplifier design is based on the negative-image technique



FIGURE 2. Calculated maximum available gain (MAG) at 10.5 GHz for a set of thirteen different GFETs ($^{#}1 - 13$) fabricated on the same chip.

presented by Medley *et al.* [18] since a unilateral assumption as in standard design processes, is not valid. Based on the statistical study, device GFET #7 exhibits the highest MAG







FIGURE 3. Schematic of the GFET amplifier topology.

TABLE 1. Amplifier Impedance Matching Circuit Elements

Component	Value	Q
C_1 (pF)	3.6	5
L_1 (nH)	1.5	10
L_2 (nH)	0.5	8
L_3 (nH)	0.5	8
L_P (nH)	0.1	46

and a representative characteristic with respect to the average *S*-parameters and was therefore selected as a reference device for the further amplifier design process.

The amplifier topology is illustrated in Fig. 3. The negativeimage network was derived from transistor S-parameters (GFET#7) and then an iterative design methodology was carried out to obtain a compromise between impedance matching, gain, and stability. Whereas the matching network consists of a series inductor L_1 , a shunt connected series LCcircuit, L_2 and C_1 , the output matching network consists only of a series inductance, L_3 . The parasitic inductance, L_P , models the nonperfect ground interconnection. Additional parasitic capacitances, $C_{P1} = C_{P2} = C_{P3} = 6$ fF, were introduced to accommodate for the backside ground plane.

The whole amplifier circuit and passive matching components were designed and optimised using Keysight ADS with the 2.5D EM simulator, ADS Momentum. The final component values and their corresponding quality factors (Q) after optimisation are summarised in Table I. The complete layout of the amplifier including probe pads, air bridges as well as the ground connection have been EM simulated. The physical size of the final integrated circuit is 1.44 mm × 0.99 mm.

III. GFET TECHNOLOGY

The complete circuit consists of a two-finger GFET that is integrated with passive components including thin-film capacitors, inductors, microstrip transmission lines, and air bridges fabricated on a 275- μ m thick high resistivity silicon substrate, as shown in Fig. 4. The gate length of the two-finger GFET is 0.5 μ m and the total width is 30 μ m. The integrated circuit process is based on the GFET fabrication process developed at the Nanofabrication



FIGURE 4. Scanning electron microscope image of the integrated GFET amplifier circuit. Important circuit elements are indicated.



FIGURE 5. Photograph of the measurement setup.

Laboratory at Chalmers and is described in [17]. First, a monolayer chemical vapor deposited (CVD) graphene was transferred on a high resistivity silicon substrates covered by 1- μ m-thick thermally grown SiO₂ layer. The graphene channel was then covered with an initial 5-nm-thick Al₂O₃ gate dielectric layer, deposited by electron-beam evaporation of Al followed by thermal oxidation. After mesa formation, source/drain contacts (Ti/Pd/Au (1 nm/15 nm/285 nm) were formed using electron beam evaporation and lift-off process. The gate dielectric stack was completed by an additional layer of 5-nm-thick Al₂O₃, thermally oxidized Al, followed with a final atomic layer deposition (ALD) of a 12-nm-thick Al₂O₃ dielectric layer. The second Al₂O₃ layer serves simultaneously as a dielectric layer for the thin-film capacitors. For electrical contact and access to the bottom ground plane, via holes were wet etched and metallized. The gate fingers, top contacts of capacitors, inductors, transmission lines, the source, and drain contact pads were realized in the next step by deposition and patterning Ti/Au (100 nm/300 nm) layers. Finally, gold air bridges were formed using a two-layer photo resist and lift-off process. The in-house GFET process is currently limited to 10 mm \times 10 mm large graphene sheets. Therefore, only twelve integrated circuits of three different designs were included on the chip.



FIGURE 6. I-V characterisation of the integrated GFET circuit. (a) Drain resistance versus gate voltage. Solid line represents the drain resistance model [19] fitted to experimental data (symbols). (b) Drain current versus drain voltage at different gate voltages. The total width of the GFET is 30 μ m and dc-measurements were performed at room temperature.



FIGURE 7. Integrated GFET amplifier performance at room temperature. Measured and simulated S-parameters of the complete circuit. Grey lines indicate simulations with other GFETs as shown in Fig. 1. The transistor was biased at $V_{CS} = 0.5$ V and $V_{DS} = -1.3$ V.

IV. RESULTS

The yield of the GFET process was determined from optical inspection and initial I-V measurements to be circa 75%. The *S*-parameters of the integrated GFET amplifier were measured using an Agilent N5230 A vector network analyzer (VNA) with a source power of -10 dBm and using on-wafer probes, see Fig. 5. The transistor was biased using a dual channel Keithley source-meter through an external bias-tee. Standard two-port SOLT calibration was performed using a calibration substrate. A series resistance (R_S+R_D) of 11 Ω , which is the sum of metal-graphene junction resistance and the access area resistances, was estimated from I-V measurements using Kim's drain-resistance model [19],

as shown in Fig. 6(a). Moreover, the Dirac point is around $V_{\rm GS} = 1$ V, which indicates that the graphene channel is p-doped. A channel mobility of $1700 \,{\rm cm^2/Vs}$ was extracted. Hence, the integrated GFET exhibits lower parasitic resistances compared to the data used for the design. Fig. 6(b) shows the $I_{\rm D}$ versus $V_{\rm DS}$ output characteristics of the same GFET measured at different $V_{\rm GS}$. The maximum drain current density is $0.7 \,{\rm mA}/\mu{\rm m}$ at $V_{\rm DS} = -1.1$ V and $V_{\rm GS} = -2$ V.

The measured gain and return loss of the fabricated GFET amplifier are shown in Fig. 7 together with simulated Sparameters. A maximum gain of 4.2 dB at 10.6 GHz was obtained at $V_{\text{GS}} = 0.5$ V and $V_{\text{DS}} = -1.3$ V. Measured input and output return loss of 14.6 dB and 19.7 dB are achieved, respectively. The simulated peak gain based on GFET#7 is 3.3 dB at 10.9 GHz. The difference in amplifier gain compared to the maximum available gain of 8.4 dB (GFET#7) is mainly due to the insertion losses of the input and output matching networks as well as the uncertainly of the actual implemented GFET transistor in the design. The 3-dB bandwidth of insertion gain is around 33%. Moreover, the measured return loss is better than predicted which is likely due to additional inductor losses. The stability factor obtained from the measured S-parameter is above 1 from 9 GHz to 20 GHz indicating the amplifier is unconditionally stable in this frequency range.

To illustrate the robustness of the amplifier design, we have included simulations of the performance for all GFETs as shown in Fig. 7. The simulated overall gain has a mean of 0.9 dB with a ± 2.2 dB variation at the frequency of 10.9 GHz. The insertion gain and the return loss at the output port of the integrated amplifier show large variation due to the large spread in S_{21} and S_{22} of the various GFETs. The performance of the fabricated amplifier are summarised in Table II with other graphene FET amplifiers.





TABLE 2. Performance Summary and Comparison of the State-of-The-Art Single-Stage GFET Amplifiers

Dof	Freq.	Gain	3 dB Gain	FBW	Integrated matching
KCI.	(GHz)	(dB)	(GHz)	(%)	networks (y/n)
[10]	1	10	0.8-1.1	32	n
[12]	2.4	4.8	2.3-2.4	2	n
[16]	5.5	8.3	4.5-6.1	5	У
This work	10.6	4.2	9.2 - 12.8	33	у
[13]	14.3	3.4	12.6-15.6	21	У

V. CONCLUSION

An integrated single-stage GFET amplifier has been demonstrated showing state-of-the art microwave performance. Table II shows a comparison with other graphene FET amplifiers. The negative-image technique was found to be an efficient method to synthesise the input and output GFET matching networks. Good agreement between simulated and measured amplifier was achieved. In our case, the fabricated demonstrator showed better performance than envisaged thanks to a successful batch with lower GFET parasitic series resistances. To summarize, substantial improvements remain to be achieved in the development of GFET technology, including improving integration and manufacturing techniques. The technical potential and cost-effective solutions that graphene technology motivates further research and technical development on GFETs for use in active micro- and millimetre-wave electronics.

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