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Integrated 10-GHz Graphene FET Amplifier

AHMED HAMED [1], MUHAMMAD ASAD [2], MUH-DEY WEI [1], ANDREI VOROBIEV [2] (Senior Member, IEEE), JAN STAKE [2] (Senior Member, IEEE), AND RENATO NEGRA [1]

(Regular Paper)

[1]Chair of High Frequency Electronics, RWTH Aachen University, 52074 Aachen, Germany
[2]THz and Millimetre Wave Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, SE-412 96 Gothenburg, Sweden

CORRESPONDING AUTHOR: M.-D. Wei (e-mail: muh-dey.wei@hfe.rwth-aachen.de).

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ABSTRACT Graphene has unique electrical and mechanical properties which can pave the way for new types of devices for microwave applications. However, emerging technologies often have problems with yield and still considerable variation in device parameters cause great challenges for circuit design. In this paper, we present the design and development of an integrated graphene FET amplifier addressing this challenge. A representative graphene FET was selected from a set of devices and then the input and output matching circuits were designed using the negative-image technique. The two-finger GFET with a gate length of 0.5 μm exhibit a typical f_T and f_{max} of 35 GHz and 37 GHz, respectively. The integrated graphene FET amplifier was fabricated on a high-resistivity silicon substrate together with thin film capacitors, airbridges, and spiral inductors. A record high gain of 4.2 dB at 10.6 GHz was measured for a single transistor amplifier stage and agrees well with simulations. These results indicate significant progress towards active microwave circuits based on emerging 2D materials.

INDEX TERMS Amplifiers, field-effect transistors, graphene, integrated circuits, microwave electronics, negative-image techniques.

I. INTRODUCTION

Since the first top-gated graphene field-effect transistors (GFETs) demonstrated by Lemme *et al.* in 2007 [1], the microwave performance of GFETs has improved significantly in recent years [2]. The high carrier velocity and mobility in graphene as well as the possibility for heterogeneous integration open up interesting opportunities in future microwave applications. Until today, several graphene RF/microwave circuits have been reported. This includes frequency converters [3], phase shifters [4], power detectors [5]–[7], multiplier [8], rectifier [9], as well as microwave amplifiers [10]–[13]. Still, the power gain in such amplifiers is limited due to inherent challenges associated with the zero bandgap in graphene that results in poor current saturation. In addition, high parasitic resistances due to contamination and imperfections during fabrication degrades the maximum frequency of oscillation even further. However, recent progress in GFET technology shows a figure-of-merit of $f_{max}\,L = 23$ GHz μm [14] and with a promising scaling behaviour.

The first graphene-based amplifier providing voltage gain was reported in [15]. In 2012, the first matched small-signal graphene FET amplifier with a power gain of 10 dB at 1 GHz was reported by Anderson *et al.* [10]. Noise properties of graphene FETs was analysed in 2014 [11] and a gain of 1.5 dB at 0.2 GHz was presented in 2015 [12]. A GFET amplifier with integrated microstrip lines was published in 2016 [13] with a gain of 3.4 dB at 14.3 GHz. Recently, a C-band graphene low-noise amplifier with a maximum gain of 8.3 dB at 5.5 GHz was reported [16]. However, graphene transistor technology is still in its infancy and faces several manufacturing difficulties resulting in poor yield and large variation in device parameters [17]. Hence, there is a strong need to improve graphene technology as well as to develop methods for robust design in order to reduce sensitivity to variations in transistor parameters.

In this paper, an integrated microwave GFET amplifier has been designed, fabricated, and characterized with respect to small-signal gain. To overcome the wide variations of GFET parameters as well as the poor unilateral figure-of-merit, U, the negative-image equivalent circuit technique was applied. A set of several GFET devices was analysed in order to define a representative performance as well as estimate the spread in

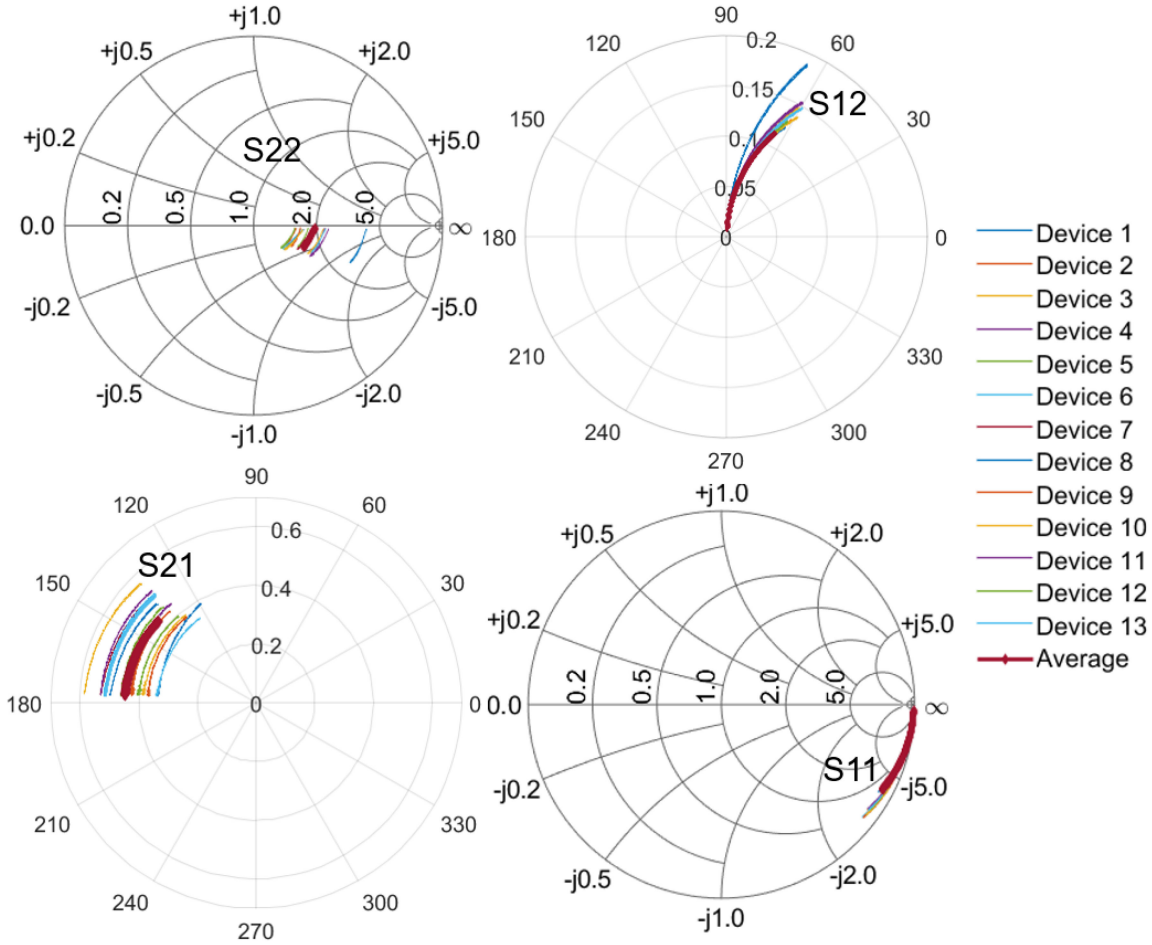

FIGURE 1. S-parameters measured between 1 GHz and 20 GHz at optimum gate bias and $V_D = 1.2$ V for a set of thirteen different GFETs ($^{\#}1 - 13$) fabricated on the same chip. The total width of the GFET is 30 μm.

gain and return loss of the final amplifier design. The results show good prospects for future microwave- and millimeter-wave amplifiers based on graphene technology.

II. DESIGN OF MICROWAVE GFET AMPLIFIER

In Fig. 1, *S*-parameters of thirteen devices, from a previous batch, show a wide variation. The *S*-parameters were measured at optimum gate bias with respect to power gain. The on-wafer *S*-parameter measurements were calibrated using short, open, load, and through structures (SOLT) and in a coplanar waveguide (CPW) environment.

The extracted maximum available gain (MAG) at 10.5 GHz is calculated and shown in Fig. 2. A variation of the extracted MAG is up to 4 dB across all thirteen GFETs and the average MAG is approximately 7.7 dB. GFET $^{\#}1$ and $^{\#}8$ exhibit poor MAG compared to other devices. The spread in transistor performance is mainly associated with variations in source and drain resistances [17]. The average value of the series resistance ($R_S + R_D$) of the GFET is around 15 Ω with a corresponding standard deviation of 5 Ω.

The measured *S*-parameters show that the fabricated GFETs are not unilateral, *i.e.*, $U \approx 0.1$. The integrated GFET amplifier design is based on the negative-image technique

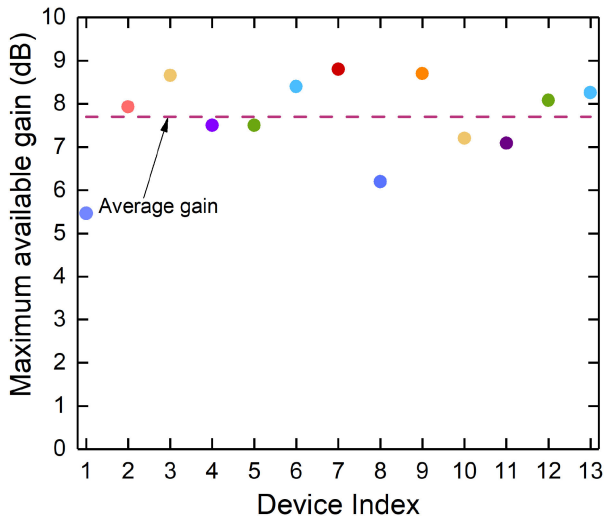

FIGURE 2. Calculated maximum available gain (MAG) at 10.5 GHz for a set of thirteen different GFETs ($^{\#}1 - 13$) fabricated on the same chip.

presented by Medley *et al.* [18] since a unilateral assumption as in standard design processes, is not valid. Based on the statistical study, device GFET #7 exhibits the highest MAG

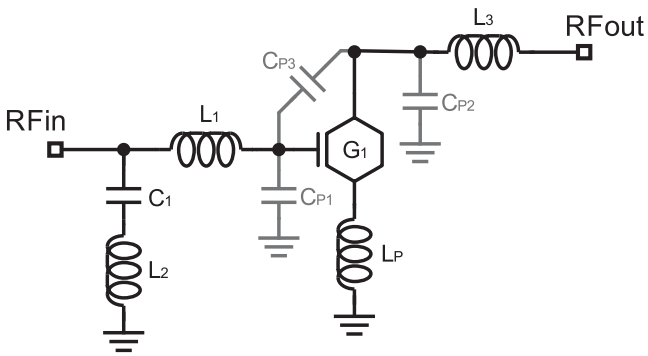

FIGURE 3. Schematic of the GFET amplifier topology.

TABLE 1. Amplifier Impedance Matching Circuit Elements

Component	Value	Q
C_1 (pF)	3.6	5
L_1 (nH)	1.5	10
L_2 (nH)	0.5	8
L_3 (nH)	0.5	8
L_P (nH)	0.1	46

and a representative characteristic with respect to the average S-parameters and was therefore selected as a reference device for the further amplifier design process.

The amplifier topology is illustrated in Fig. 3. The negative-image network was derived from transistor S-parameters (GFET#7) and then an iterative design methodology was carried out to obtain a compromise between impedance matching, gain, and stability. Whereas the matching network consists of a series inductor L_1, a shunt connected series LC-circuit, L_2 and C_1, the output matching network consists only of a series inductance, L_3. The parasitic inductance, L_P, models the nonperfect ground interconnection. Additional parasitic capacitances, $C_{P1} = C_{P2} = C_{P3} = 6$ fF, were introduced to accommodate for the backside ground plane.

The whole amplifier circuit and passive matching components were designed and optimised using Keysight ADS with the 2.5D EM simulator, ADS Momentum. The final component values and their corresponding quality factors (Q) after optimisation are summarised in Table I. The complete layout of the amplifier including probe pads, air bridges as well as the ground connection have been EM simulated. The physical size of the final integrated circuit is 1.44 mm $\times$ 0.99 mm.

III. GFET TECHNOLOGY

The complete circuit consists of a two-finger GFET that is integrated with passive components including thin-film capacitors, inductors, microstrip transmission lines, and air bridges fabricated on a 275-μm thick high resistivity silicon substrate, as shown in Fig. 4. The gate length of the two-finger GFET is 0.5 μm and the total width is 30 μm. The integrated circuit process is based on the GFET fabrication process developed at the Nanofabrication

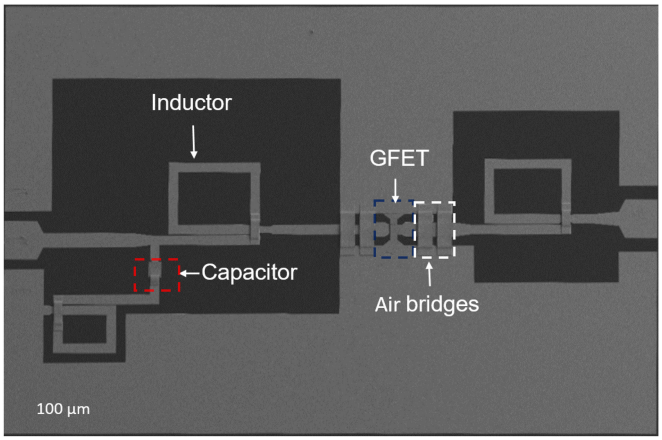

FIGURE 4. Scanning electron microscope image of the integrated GFET amplifier circuit. Important circuit elements are indicated.

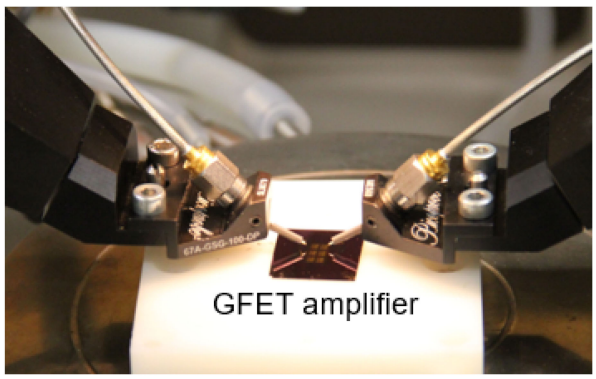

FIGURE 5. Photograph of the measurement setup.

Laboratory at Chalmers and is described in [17]. First, a monolayer chemical vapor deposited (CVD) graphene was transferred on a high resistivity silicon substrates covered by 1-μm-thick thermally grown SiO_2 layer. The graphene channel was then covered with an initial 5-nm-thick Al_2O_3 gate dielectric layer, deposited by electron-beam evaporation of Al followed by thermal oxidation. After mesa formation, source/drain contacts (Ti/Pd/Au (1 nm/15 nm/285 nm) were formed using electron beam evaporation and lift-off process. The gate dielectric stack was completed by an additional layer of 5-nm-thick Al_2O_3, thermally oxidized Al, followed with a final atomic layer deposition (ALD) of a 12-nm-thick Al_2O_3 dielectric layer. The second Al_2O_3 layer serves simultaneously as a dielectric layer for the thin-film capacitors. For electrical contact and access to the bottom ground plane, via holes were wet etched and metallized. The gate fingers, top contacts of capacitors, inductors, transmission lines, the source, and drain contact pads were realized in the next step by deposition and patterning Ti/Au (100 nm/300 nm) layers. Finally, gold air bridges were formed using a two-layer photo resist and lift-off process. The in-house GFET process is currently limited to 10 mm $\times$ 10 mm large graphene sheets. Therefore, only twelve integrated circuits of three different designs were included on the chip.

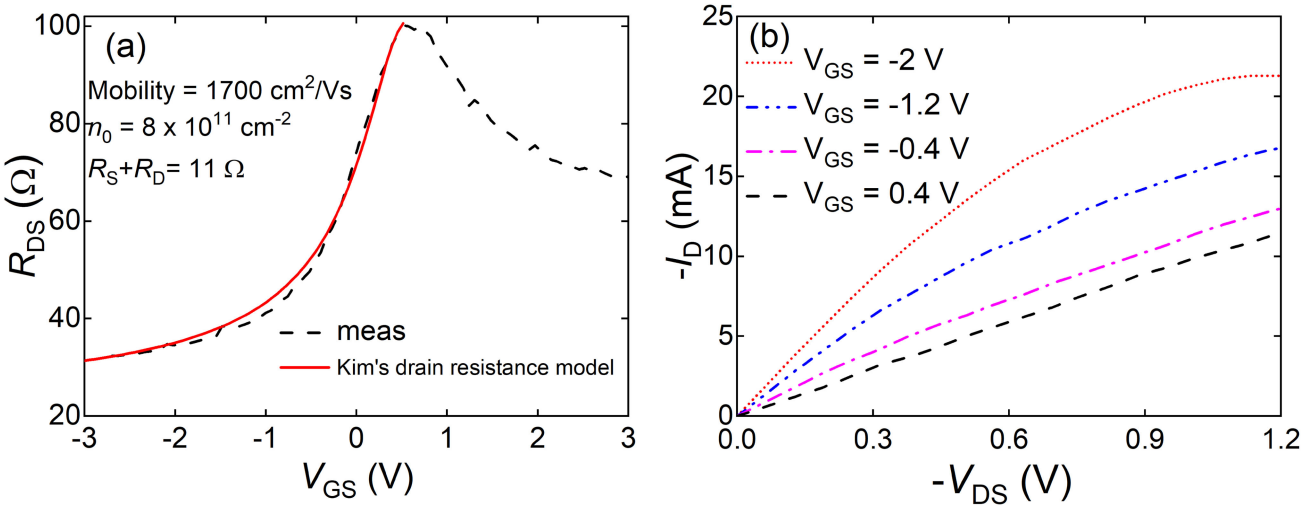

FIGURE 6. I-V characterisation of the integrated GFET circuit. (a) Drain resistance versus gate voltage. Solid line represents the drain resistance model [19] fitted to experimental data (symbols). (b) Drain current versus drain voltage at different gate voltages. The total width of the GFET is 30 μm and dc-measurements were performed at room temperature.

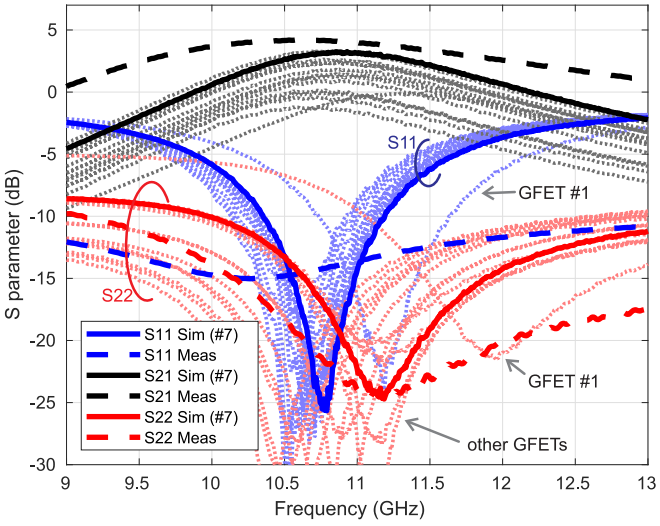

FIGURE 7. Integrated GFET amplifier performance at room temperature. Measured and simulated *S*-parameters of the complete circuit. Grey lines indicate simulations with other GFETs as shown in Fig. 1. The transistor was biased at $V_{GS} = 0.5$ V and $V_{DS} = -1.3$ V.

IV. RESULTS

The yield of the GFET process was determined from optical inspection and initial I-V measurements to be circa 75%. The *S*-parameters of the integrated GFET amplifier were measured using an Agilent N5230 A vector network analyzer (VNA) with a source power of −10 dBm and using on-wafer probes, see Fig. 5. The transistor was biased using a dual channel Keithley source-meter through an external bias-tee. Standard two-port SOLT calibration was performed using a calibration substrate. A series resistance (R_S+R_D) of 11 Ω, which is the sum of metal-graphene junction resistance and the access area resistances, was estimated from I-V measurements using Kim's drain-resistance model [19], as shown in Fig. 6(a). Moreover, the Dirac point is around $V_{GS} = 1$ V, which indicates that the graphene channel is p-doped. A channel mobility of 1700 cm^2/Vs was extracted. Hence, the integrated GFET exhibits lower parasitic resistances compared to the data used for the design. Fig. 6(b) shows the I_D versus V_{DS} output characteristics of the same GFET measured at different V_{GS}. The maximum drain current density is 0.7 mA/μm at $V_{DS} = -1.1$ V and $V_{GS} = -2$ V.

The measured gain and return loss of the fabricated GFET amplifier are shown in Fig. 7 together with simulated *S*-parameters. A maximum gain of 4.2 dB at 10.6 GHz was obtained at $V_{GS} = 0.5$ V and $V_{DS} = -1.3$ V. Measured input and output return loss of 14.6 dB and 19.7 dB are achieved, respectively. The simulated peak gain based on GFET#7 is 3.3 dB at 10.9 GHz. The difference in amplifier gain compared to the maximum available gain of 8.4 dB (GFET#7) is mainly due to the insertion losses of the input and output matching networks as well as the uncertainly of the actual implemented GFET transistor in the design. The 3-dB bandwidth of insertion gain is around 33%. Moreover, the measured return loss is better than predicted which is likely due to additional inductor losses. The stability factor obtained from the measured *S*-parameter is above 1 from 9 GHz to 20 GHz indicating the amplifier is unconditionally stable in this frequency range.

To illustrate the robustness of the amplifier design, we have included simulations of the performance for all GFETs as shown in Fig. 7. The simulated overall gain has a mean of 0.9 dB with a ±2.2 dB variation at the frequency of 10.9 GHz. The insertion gain and the return loss at the output port of the integrated amplifier show large variation due to the large spread in S_{21} and S_{22} of the various GFETs. The performance of the fabricated amplifier are summarised in Table II with other graphene FET amplifiers.

TABLE 2. Performance Summary and Comparison of the State-of-The-Art Single-Stage GFET Amplifiers

Ref.	Freq. (GHz)	Gain (dB)	3 dB Gain (GHz)	FBW (%)	Integrated matching networks (y/n)
[10]	1	10	0.8−1.1	32	n
[12]	2.4	4.8	2.3−2.4	2	n
[16]	5.5	8.3	4.5−6.1	5	y
This work	**10.6**	**4.2**	**9.2 − 12.8**	**33**	**y**
[13]	14.3	3.4	12.6−15.6	21	y

V. CONCLUSION

An integrated single-stage GFET amplifier has been demonstrated showing state-of-the art microwave performance. Table II shows a comparison with other graphene FET amplifiers. The negative-image technique was found to be an efficient method to synthesise the input and output GFET matching networks. Good agreement between simulated and measured amplifier was achieved. In our case, the fabricated demonstrator showed better performance than envisaged thanks to a successful batch with lower GFET parasitic series resistances. To summarize, substantial improvements remain to be achieved in the development of GFET technology, including improving integration and manufacturing techniques. The technical potential and cost-effective solutions that graphene technology motivates further research and technical development on GFETs for use in active micro- and millimetre-wave electronics.

REFERENCES

[1] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007.

[2] M. Bonmann *et al.*, "Graphene field-effect transistors with high extrinsic f_t and f_{max}," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 131–134, Jan. 2019.

[3] M. A. Andersson, Y. Zhang, and J. Stake, "A 185215-GHz subharmonic resistive graphene FET integrated mixer on silicon," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 1, pp. 165–172, Jan. 2017.

[4] A. Medina-Rull *et al.*, "A graphene field-effect transistor based analogue phase shifter for high-frequency applications," *IEEE Access*, vol. 8, pp. 209 055–209 063, Dec. 2020.

[5] M. Shaygan *et al.*, "High performance metalinsulatorgraphene diodes for radio frequency power detection application," *Nanoscale*, vol. 9, no. 33, pp. 11 944–11 950, Jul. 2017

[6] A. A. Generalov, M. A. Andersson, X. Yang, A. Vorobiev, and J. Stake, "A 400-GHz graphene FET detector," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 5, pp. 614–616, Sep. 2017.

[7] X. Yang, A. Vorobiev, J. Yang, K. Jeppson, and J. Stake, "A linear-array of 300-GHz antenna integrated GFET detectors on a flexible substrate," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 5, pp. 554–557, Sep. 2020.

[8] M. E. Ramón *et al.*, "Three-gigahertz graphene frequency doubler on quartz operating beyond the transit frequency," *IEEE Trans. Nanotechnol.*, vol. 11, no. 5, pp. 877–883, Sep. 2012.

[9] C.-Y. Fan, M.-D. Wei, B. Uzlu, Z. Wang, D. Neumaier, and R. Negra, "Fully integrated 2.4-GHz flexible rectifier using chemical-vapor-deposition graphene MMIC process," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1326–1333, Mar. 2021.

[10] M. Andersson, O. Habibpour, J. Vukusic, and J. Stake, "10 dB small-signal graphene FET amplifier," *Electron. Lett.*, vol. 48, no. 14, p. 861–863, Jul. 2012.

[11] M. Tanzid, M. Andersson, J. Sun, and J. Stake, "Microwave noise characterization of graphene field effect transistors," *Appl. Phys. Lett.*, vol. 104, no. 1, 2014, Art. no. 013502.

[12] J. Aguirre-Morales *et al.*, "Towards amplifier design with a SiC graphene field-effect transistor," in *Proc. Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integration Silicon (EUROSOI-ULIS)*, 2015, pp. 93–96.

[13] C. Yu *et al.*, "Graphene amplifier MMIC on SiC substrate," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 684–687, May 2016.

[14] M. Asad, K. O. Jeppson, A. Vorobiev, M. Bonmann, and J. Stake, "Enhanced high-frequency performance of top-gated graphene FETs due to substrate- induced improvements in charge carrier saturation velocity," *IEEE Trans. Electron Devices*, vol. 68, no. 2, pp. 899–902, Feb. 2021.

[15] S.-J. Han *et al.*, "High-frequency graphene voltage amplifier," *Nano Lett.*, vol. 11, no. 9, pp. 3690–3693, 2011.

[16] C. Yu *et al.*, "Field effect transistors and low noise amplifier MMICs of monolayer graphene," *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 268–271, Feb. 2021.

[17] M. Asad *et al.*, "The dependence of the high-frequency performance of graphene field-effect transistors on channel transport properties," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 457–464, 2020.

[18] M. Medley and J. Allen, "Broad-band GaAs FET amplifier design using negative-image device models," *IEEE Trans. Microw. Theory Techn.*, vol. 27, no. 9, pp. 784–788, Sep. 1979.

[19] S. Kim *et al.*, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, Feb. 2009, Art. no. 062107.

AHMED HAMED received the B.Sc. and M.Sc. degrees in electrical engineering from Ain Shams University, Cairo, Egypt, in 2004 and 2012, respectively, and the Ph.D. degree in electrical engineering from RWTH Aachen University, Aachen, Germany, in 2019.

From 2004 to 2011, he was an RF Design Engineer with SySDSoft Inc., Cairo, Egypt, and SiWare Systems Inc., Cairo, Egypt, where he was involved in the design of RF circuits for Bluetooth and WIMAX transceivers, and highly stable *LC* reference oscillators. In 2011, he joined Hittite Microwave Corporation (currently Analog Devices Inc.), Cairo, Egypt, where he focused on the design of microwave mixers, switches, and power detectors for E-band communication systems using GaAs and SiGe technologies. He is currently a Postdoctoral Researcher with the Chair of High Frequency Electronics, RWTH Aachen University. His research focuses on the development of microwave and millimeter-wave devices, circuits, and systems based on 2D materials and the design of high-efficiency microwave power amplifiers for 5G communication systems using CMOS, GaAs, and GaN technologies.

MUHAMMAD ASAD (Student Member, IEEE) was born Bahawalnagar, Pakistan, in 1986. He received the M.Sc. degree in experimental physics from Ulm University, Ulm, Germany, in 2014 and the Ph.D. degree in engineering from Chalmers University of Technology, Gothenburg, Sweden, in 2021. His research interests include technology developments in the areas of emerging 2D materials and III-nitride semiconductors and their applications in high-frequency and high-power electronics.

MUH-DEY WEI received the M.Sc. and Ph.D. degree in electrical engineering from the National Chung Cheng University, Chiayi, Taiwan, in 2006 and 2011, respectively. During the Ph.D., he spent 18 months with Mixed Signal CMOS Circuits and Chair for Integrated Analog Circuits and RF Systems with RWTH Aachen University, Aachen, Germany. He is currently a Chief Engineer with the Chair of High Frequency Electronics, RWTH Aachen University, Aachen, Germany. His current research interests include 2D material, advanced transceivers, microwave frequency sources, power amplifiers, and rectifiers.

Dr. Wei was the recipient of a Deutscher Akademischer Austauschdienst Scholarship.

ANDREI VOROBIEV (Senior Member, IEEE) was born in Gorky, Russia, in 1963. He received the M.Sc. degree in physics of semiconductors and dielectrics from Gorky State University, Gorky, Russia, in 1986 and Ph.D. degree in physics and mathematics from the Institute for Physics of Microstructures, Russian Academy of Sciences, Nizhny Novgorod, Russia, in 2000. From 1986 to 1991, he was with the Design Office of Measuring Instruments, Nizhny Novgorod, Russia, first as a Leading Engineer and then, as the Head of the Microelectronics laboratory. From 1991 to 2001, he was with the Institute for Physics of Microstructures, Russian Academy of Sciences, as a Senior Research Associate. Since 2001, he has been with the Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg, Sweden, first as a Postdoctoral Fellow and currently, as a Senior Researcher. He has authored and coauthored more than 180 papers and conference presentations, three books and book chapters, and four patents. His research interests include the development and application of emerging materials and phenomena in microwave and terahertz components and devices, including those based on graphene, ferroelectrics, and multiferroics, focusing on development of materials, microtechnology processing steps, and experimental and theoretical investigations. He reviewed more than 60 manuscripts in peer-reviewed journals. In 2008, he received title of Docent in physical electronics, broadly equivalent to Associate Professor.

JAN STAKE (Senior Member, IEEE) was born in Uddevalla, Sweden, in 1971. He received the M.Sc. degree in electrical engineering and the Ph.D. degree in microwave electronics from Chalmers University of Technology, Gothenburg, Sweden, in 1994 and 1999, respectively. In 1997, he was a Research Assistant with the University of Virginia, Charlottesville, VA, USA. From 1999 to 2001, he was a Research Fellow with the Millimetre Wave Group, Rutherford Appleton Laboratory, Didcot, U.K. He then joined Saab Combitech Systems AB, Linköping, Sweden, as a Senior RF/microwave Engineer, until 2003. From 2000 to 2006, he held different academic positions with the Chalmers University of Technology and from 2003 to 2006, he was also the Head of the Nanofabrication Laboratory, Department of Microtechnology and Nanoscience. In 2007, he was a Visiting Professor with the Sub-millimetre Wave Advanced Technology Group, Caltech/JPL, Pasadena, CA, USA. In 2020, he was a Visiting Professor with TU Delft, Delft, The Netherlands. He is currently a Professor and the Head of the Terahertz and Millimetre Wave Laboratory, Chalmers University of Technology. He is also the Co-founder of Wasa Millimeter Wave AB, Gothenburg, Sweden. His research interests include graphene electronics, high frequency semiconductor devices, THz electronics, sub-millimetre wave measurement techniques (THz metrology), and THz in biology and medicine. Between 2016 and 2018, was the Editor-in-Chief of IEEE TRANSACTIONS ON TERAHERTZ SCIENCE AND TECHNOLOGY and between 2012 and 2015, the Topical Editor.

RENATO NEGRA received the M.Sc. degree in telematics from the Graz University of Technology, Graz, Austria and the Ph.D. degree in electrical engineering from ETH Zurich, Zurich, Switzerland. During the M.Sc. studies, he spend one year as an exchange student with the Norwegian University of Science and Technology, Trondheim, Norway.

From 1998 to 2000, he was with Alcatel Space Norway AS (currently NorSpace AS), Horten, Norway, where he was involved in the design and characterisation of space-qualified RF equipment. In 2000, he joined the Laboratory for Electromagnetic Fields and Microwave Electronics, ETH Zurich. There, his Ph.D. research was focused on power-efficient linear amplification of wireless communication signals. From 2006 to 2008, he was a Postdoctoral Fellow with iRadio Lab, University of Calgary, Calgary, AB, Canada, working on switching-mode power amplifiers and advanced wireless transmitters. Within the Ultra high speed Mobile Information and Communication Research Centre, RWTH Aachen University, Aachen, Germany, he was appointed as an Assistant Professor for Mixed-Signal CMOS Circuits from June 2008 to December 2013. Since December 2013, he has been the Chair of High Frequency Electronics at the same university. His research interests include high frequency circuits and systems in silicon, III-V and 2D-material technologies, power amplifiers, and transmitter architectures.