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A Push-Pull 6–12GHz GaN Dual-Stage MMIC PA with Capacitive Cross-Coupling Neutralization for Increased Gain

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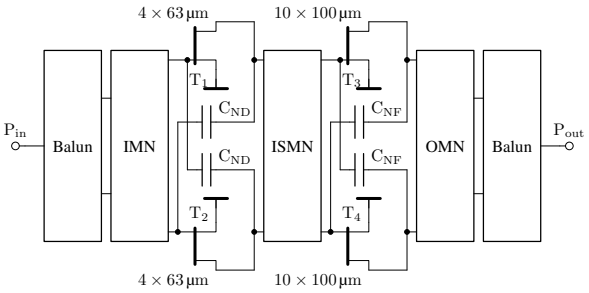
***Abstract* — This paper presents a 6–12 GHz GaN on SiC two-stage MMIC push-pull PA using Marchand baluns. The differential topology is used to implement capacitive cross-coupling neutralization to increase the amplifier gain. A methodology to create an accurate model of the neutralized transistor including the parasitics of the neutralization network is discussed. An octave bandwidth balun with amplitude and phase imbalances below 0.2 dB and 2.5° is described. The MMIC PA is fully characterized and 26 dB of small signal gain and a peak output power of 37.2 dBm with a PAE of 30.5% is measured at 7 GHz.**

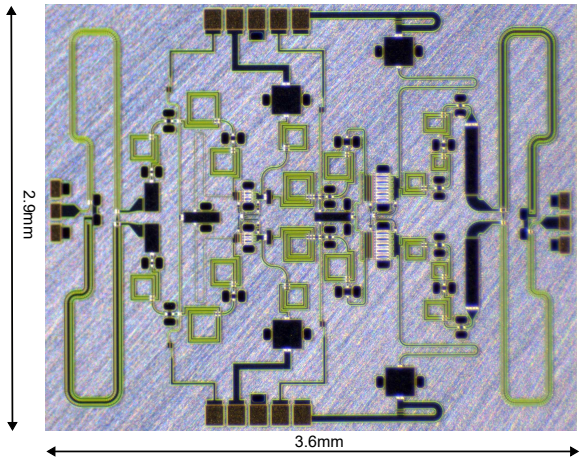
***Keywords* — GaN, MMIC, Power Amplifier, Neutralization, Push-Pull, Gain-Boosting, Differential Amplifier**

I. Introduction

The push-pull configuration for power amplifiers (PAs) is known to suppress even order harmonics, which is especially helpful for PAs with a bandwith of an octave or beyond [1]. However, the drawback of the push-pull design is the requirement for transformers, 180°-hybrids, or baluns to create the differential signals and combine them at the output of the PA, which demands real estate on chip and introduces extra losses. While these losses are unavoidable, the differential signaling enables simple transistor neutralization with cross-coupled capacitors, as shown in Fig. 1a. The technique of neutralization, i.e. the addition of passive networks to cancel the internal undesireable feedback of an amplifying device [2], has been used since the 1940s for vacuum tubes [3] and later bipolar transistors [4]. For CMOS technology, this neutralization method is now very matured and sometimes called gain boosting [5], used to operate at the frequency limits of the employed technology [6], and can also be found in tunable variants [7]. In compound semiconductors neutralization is rarely used, notable exceptions are two GaAs designs [8], [9] and a two-stage GaN MMIC amplifier at 17.7 GHz where neutralization is employed for AM/PM distortion compensation [10]. In this paper cross-coupling neutralization is used in both stages of the 6 to 12 GHz GaN MMIC PA shown in Fig. 1 to boost gain. The next sections will discuss the design and simulation of neutralization networks, baluns and chip layout, and present a complete characterization of the measured PA implemented in a 150 nm GaN on SiC process from WIN Semiconductors (NP15-00).



(a)



(b)

Fig. 1. Block diagram of neutralized, two-stage, push-pull MMIC PA. IMN, ISMN, and OMN abbreviate Input –, InterStage – and Output Matching Network, respectively; dc bias lines are omitted (a). Chip photograph of the MMIC PA with circuit dimensions (b).

II. Circuit Design and Layout

A. Neutralization

For this design we were aiming for a peak output power of 36 dBm so two $10 \times 100\,\mu\text{m}$ devices biased in class AB (125 mA / device) were chosen for the final stage. In an initial step the best neutralization capacitor size C_{NF} was chosen by tuning its value for minimum feedback $|S_{12}|$ of the neutralized transistor across the desired 6–12 GHz band, which yielded $C_{\text{NF}} = 39\,\text{fF}$. Comparing the original PDK transistor with this neutralized transistor an improvement of

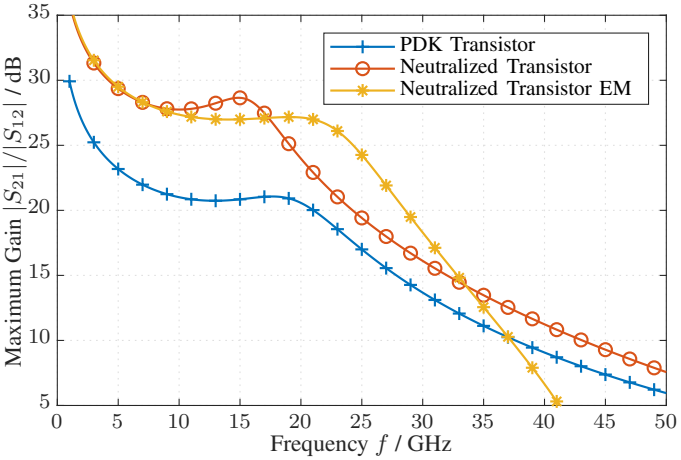


Fig. 2. Maximum gain of the $10 \times 100\,\mu\text{m}$ transistor of the final stage, comparing the regular PDK device with a neutralized transistor pair with ideal neutralization capacitors, and a pair with EM simulated capacitors and crossover lines as shown in Fig. 3.

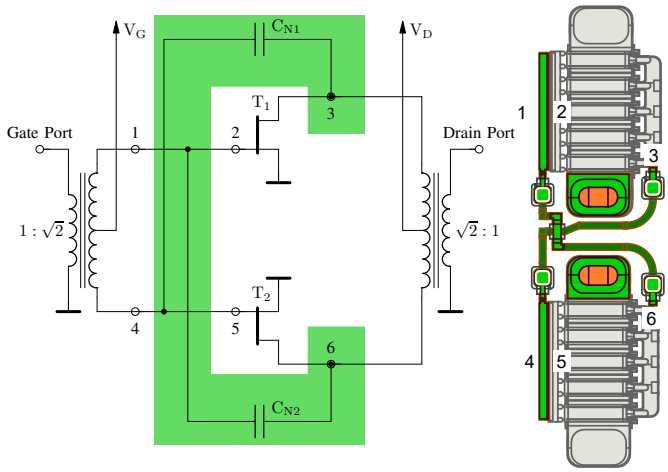


Fig. 3. Simulation technique for neutralized transistors: Schematic diagram for equivalent single neutralized transistor with neutralization network shown in green (a), EM simulation setup for neutralization network for final stage in color, with the transistors drawn in grey for reference (b).

6.7 dB in maximum gain is observed at 10 GHz, see Fig. 2. For simulation of the neutralized transistor the circuit in Fig. 3a is used. The two ideal transformers with a $1 : \sqrt{2}$ transformation ratio at the input and output convert the single port to two ports of identical impedance (to ground) but opposite phase with the added benefit that the transformer center tap makes a bias-T superfluous. This circuit behaves like a single neutralized device in all small-signal aspects. The layout of the implemented neutralization network is shown in Fig. 3b, with the transistor geometry plotted in grey for reference. Since the required small capacitance of 39 fF cannot be implemented directly as metal insulator metal (MIM) capacitor in this process, it is realized by two $20 \times 20\,\mu\text{m}$ capacitors (nominal capacitance 92 fF) in series. Note that the required series transmission lines to connect these capacitors add series inductance and shunt capacitance to ground, effectively altering the neutralization capacitance. To capture this and the effect of coupling to the nearby source vias of the transistors, an electromagnetic (EM) simulation including these vias is conducted. For these EM simulations six ports are defined as shown in Fig. 3b, and the 6-port results are used to replace the ideal neutralization network highlighted in green in Fig. 3a according to the port numbers. The result in terms of maximum gain of the EM simulated neutralized transistor is shown in Fig. 2. We note that the interconnect parasitics improve the maximum gain flatness beyond the operating band, but ultimately lead to a faster drop off crossing the performance of the regular device at 37 GHz.

The same approach was followed for the $4 \times 63\,\mu\text{m}$ driver neutralization capacitors. Here a capacitance of 21.5 fF yielded the lowest $|S_{12}|$ result, which was implemented as three $17 \times 17\,\mu\text{m}$ capacitors in series, each with a nominal capacitance of 67 fF. The layout of this network can be seen in Fig. 6.

B. Balun

After the design of the neutralization networks for driver and final stages, the Marchand baluns for the PA are designed. They are implemented as coupled microstrip traces, using a similar folded shape as in [1]. A series of initial simulations confirmed that a large deviation from a $50\,\Omega$ single ended to $100\,\Omega$ differential balun ($2{\times}50\,\Omega$ to ground) impedance ratio was not possible on the $100\,\mu\text{m}$ SiC substrate, so this ratio was chosen. In contrast to [1], the A and B sections of the balun use different transmission line widths and gaps, see Fig. 4 and Table 1. Within the 6 to 12 GHz range these extra degrees of freedom allowed for a simulated amplitude and phase imbalance below 0.2 dB and 2.5°, respectively, see Fig. 5. The return loss of the balun input (port 1) is above 11 dB, while the return loss of the output ports 2 and 3 is low, reaching only 5.3 dB at 6 GHz. This is not surprising for this type of Marchand balun, since a perfect match on all ports requires an extra line and resistors [11] that are omitted here for space and loss reasons. However, the poor return loss needs to be taken into account when analyzing the PA stability, as will be discussed in the next section.

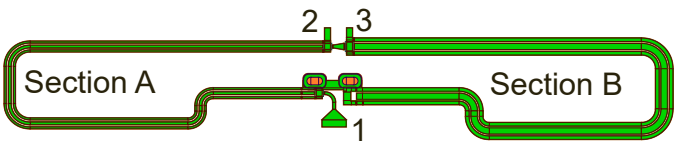


Fig. 4. Balun layout with port numbering.

Table 1. Geomerty of Balun

Section	Inner line width	Gap	Total width
Section A	13.3 µm	6.1 µm	45.5 µm
Section B	27.1 µm	5 µm	69.7 µm

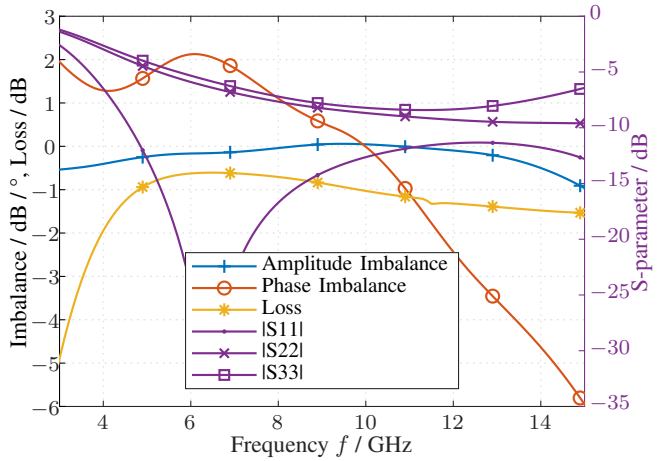


Fig. 5. Simulated data of balun with port numbering as shown in Fig. 4.

C. Matching Networks and Layout

Since the balun design had shown that adequate impedance matching could not be obtained by the balun itself, the same $50\,\Omega$ single ended to $100\,\Omega$ differential baluns are used at the input and output of the amplifier. The design started with the output matching network, after the efficiency optimum load impedance for the final stage devices was obtained from loadpull simulations. For these simulations the circuit of Fig. 3a is used again. The results do not require any impedance scaling for the single transistor, except that the power levels are shifted by a factor of 2. The symmetric output matching network uses a ladder network with three series inductors and three shunt capacitors. The inductors are implemented as square planar inductors, which ease parametric EM simulation. The drain bias line also acts as a shunt inductor, cancelling some of the device's output capacitance.

The symmetric interstage network follows the same design ideas as the output matching network. The gate bias lines again act as shunts but this time meet at the symmetry axis of the PA utilizing the virtual short provided due to the push-pull operation. A bypass capacitor is still provided at this center location for out-of-band stability where the balun imbalance will be severe. The IMN uses a three section ladder network and the inductance of the gate bias line, which again connects to a virtual short in a central capacitor.

The stability of the circuit was tested extensively using gamma probes at all gates and drains, evaluating loop gain. Series resistors of $11\,\Omega$ and $2.7\,\Omega$ were placed at the gates of the driver and final stage, respectively, to ensure stability for various dc bias bondwire inductances which were swept from 0 to $10\,\mathrm{nH}$. To avoid low frequency instabilities at the final stage the drain bias line contains a parallel LR network between the dc pad and the bypass capacitor. The gate bias lines each contain $6.4\,\Omega$ series resistors for the same reason.

III. Measurement Results

The PA chips were mounted on gold plated copper slabs using conductive epoxy together with $100\,\mathrm{pF}$ and $10\,\mathrm{nF}$ single

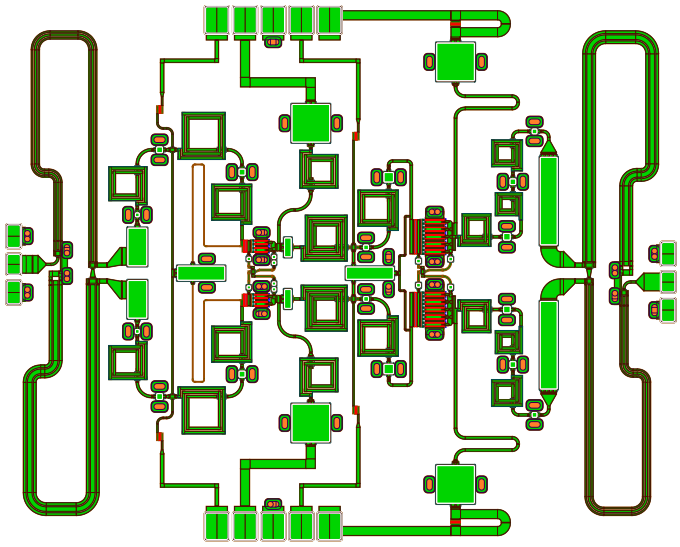


Fig. 6. Exported Layout of the PA with the RF input pads to the left and output to the right, dc biasing pads for SSGSS probes shown at top and bottom.

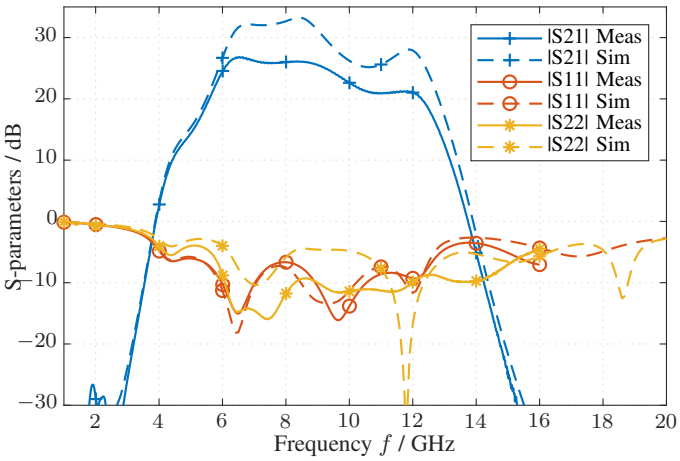


Fig. 7. Small signal characterization comparing measurement and simulation.

layer capacitors. The PA dc pads were each bonded to a pair of these capacitors, and the whole assembly was mounted on a probe station. The PA is measured using a vector network analyzer configured with an external test-set and driver amplifier. The calibration reference plane is de-embedded down to the GSG pads for power and scattering parameters.

The small signal characterization and comparison with simulation is shown in Fig. 7 for the PA biased at its design parameters of $20\,\mathrm{V}$ and $58\,\mathrm{mA}$ for the driver and $250\,\mathrm{mA}$ for the final stage. We observe very good agreement of the input return loss with simulations, however the output return loss deviates significantly where the measured return loss in the 6 to $11\,\mathrm{GHz}$ range exceeds $8.6\,\mathrm{dB}$. The measured small signal gain falls behind the simulated results but still exceeds $21\,\mathrm{dB}$ across the band and is above $25\,\mathrm{dB}$ from 6 to $9.2\,\mathrm{GHz}$, which is very high for a two-stage design.

Measured powersweeps for $6.75\,\mathrm{GHz}$ and $11\,\mathrm{GHz}$ are plotted in Fig. 8 to demonstrate that the amplifier compresses

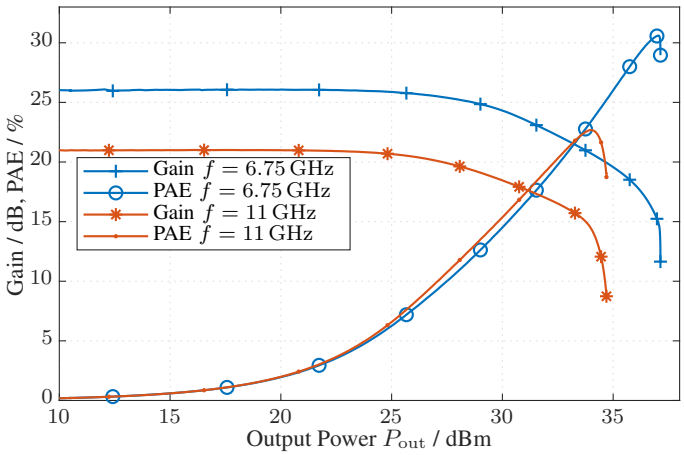
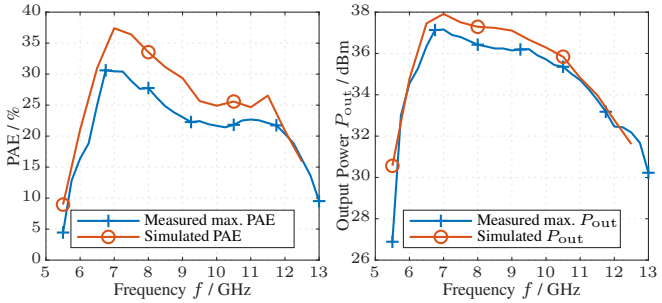


Fig. 8. Measured large signal gain and PAE of PA at 6.75 GHz and 11 GHz.



(a) (b)

Fig. 9. Comparing measured maximum PAE (a) and output power P_{out} (b) to simulations at an input power $P_{\text{in}} = 19$ dBm.

gently without parametric oscillations. The maximum power added efficiencies (PAE) for these two frequencies are 30.6% at 37 dBm and 22.7% at 34 dBm, respectively. The maximum measured PAE and output power values are compared to simulations in Fig. 9, showing a discrepancy of up to 6% points in PAE. It is believed that the rood cause for these deviations and the discrepancy in measured $|S_{22}|$ lays in a suboptimal realized neutralization due to process variation in the small MIM neutralization capacitors.

IV. Conclusion

This work presents a two-stage, push-pull GaN MMIC PA that delivers 32.5 to 37.2 dBm of power in the 6–12 GHz band. Compared to the state-of-the-art of GaN MMIC PAs this work uses a push pull configuration and cross-coupling capacitive neutralization in both the driver and final stages to boost gain to 25–33 dB in simulations. The measured small signal gain exceeds 25 dB from 6 to 9.2 GHz, which beats the demonstrated gain for octave bandwidth, two-stage GaN PAs (Table 2) but falls behind simulation. It is believed that the discrepancy in gain and efficiency is caused by process variations affecting the small MIM neutralization capacitors, leading to suboptimal neutralization. For future designs the use of planar interdigitated neutralization capacitors will be explored.

Table 2. State of the art wideband GaN MMIC PAs in 6-12 GHz band.

Frequency (GHz)	PAE (%)	Pout (dBm)	SS. Gain (dB)	# Stages	Gate Length (µm)	Ref.
6 – 12	17 – 33	32.3 – 34.3	28 – 33	3 B	0.25	[1]
8 – 12	35 – 37	46.8 – 47.9	22 – 27	3	0.25	[12]
8 – 12	33 – 38	42	28 – 36	3	0.25	[13]
8 – 12.5	50 – 62*	41.5 – 42.3	21 – 23	2	0.15	[14]
6.3 – 12.6	25 – 38.4	38.1 – 40.1	18 – 21	2	0.15	[15]
6 – 12	16.4 – 30.5	32.5 – 37.2	21 – 27	2 B&N	0.15	TW

* Pulsed Measurements, B: Balanced, N: Neutralized, TW: This work

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