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# Symmetrical Doherty Power Amplifier with High Efficiency and Extended Bandwidth

# Symmetrical Doherty Power Amplifier with High Efficiency and Extended Bandwidth

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***Abstract* — This paper introduces a load modulation network for the Doherty power amplifier (PA). The proposed combiner network demonstrates inherent wideband characteristics and effectively addresses the impact of output parasitics resulting from the transistors, thereby achieving exceptional bandwidth performance. To validate the concept, a wideband prototype Doherty PA is designed and measured, employing GaN HEMT transistors. The experimental results exhibit a drain efficiency of 51-63 % at the peak output power and 41-53 % at 6-dB output power back-off across 1.6-2.7 GHz. Furthermore, the measured peak output power of 43.8±0.5 dBm within the same frequency range confirms the theoretical framework and demonstrates the promising potential of the proposed wideband Doherty PA for future applications in wireless transmitters.**

***Keywords* — Doherty, energy efficiency, gallium nitride (GaN), power amplifiers, wideband amplifier.**

## I. Introduction

The requirement for higher data transmission capacity has led modern communication systems to utilize complex modulation schemes. Nonetheless, these schemes give rise to modulated signals with a large peak-to-average power ratio (PAPR). Power amplifiers (PA) are notorious for high power consumption and play a crucial role in determining the performance of communication systems. Consequently, it is vital to improve the PA efficiency, especially at a significantly back-off output power level.

Active load-modulated PA architectures have gained significant recognition as viable solutions for enhancing PA back-off efficiency. In recent years, researchers have proposed several innovative architectures to further advance load-modulated PA designs, each with unique features and advantages. Noteworthy examples include the load-modulated balanced amplifier (LMBA) [1], the distributed efficient power amplifier (DEPA) [2], and the circulator load-modulated amplifier (CLMA) [3], [4]. These new architectures have shown promise in enhancing the efficiency and bandwidth performance of load-modulated PAs. However, their complex circuitry poses a challenge for widespread adoption. In contrast, the Doherty PA offers a relatively simple circuit topology that can be easily implemented across different frequencies and semiconductor processes.

The Doherty output combiner network is essential as it controls the interaction between the main and auxiliary amplifier paths, thereby determining the PA operation. These networks also play a crucial role in extending the efficiency range and enabling broader carrier bandwidth. In previous works [5], [6], a systematic combiner synthesis approach was proposed for two-way and three-way Doherty combiner networks, respectively. This approach, known as the black-box combiner synthesis method, offers the advantage of lower insertion loss and more compact size compared to other designs, as it integrates matching, load-modulation, and impedance transformation functionalities in a systematic process. However, the black-box approach for Doherty PAs has predominantly been adopted in narrow-band applications.

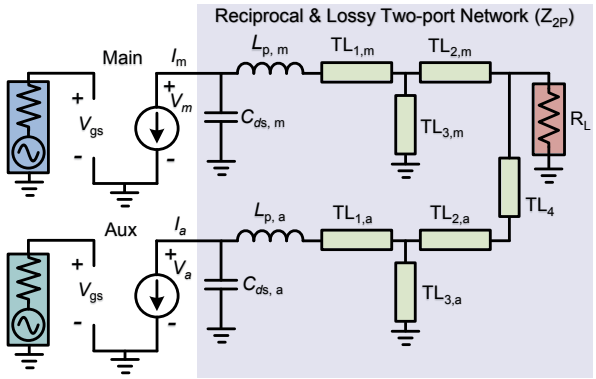


Fig. 1. The load modulation network for wideband Doherty power amplifiers.

In this paper, we present a novel load modulation network for the Doherty PA that can be analyzed using the black-box combiner method, as shown in Fig. 1. The proposed approach effectively addresses the two main factors limiting the bandwidth of Doherty PAs, namely the transistor parasitics and the frequency response of the Doherty combiner. The theoretical and experimental analysis will be conducted to provide evidence of the substantial improvement in bandwidth achievable with the proposed Doherty PA topology.

## II. Theory

The key innovation of the proposed Doherty PA is its distinctive load modulation network, which consists of two Tee-line-based networks and an extra transmission line, as shown in Fig. 1. Through mathematical analysis, the T-network structure serves as an effective representation of a series quarter-wavelength transmission line with certain characteristic impedance [7], thereby supporting the wideband capabilities of this topology. Notably, the packaged GaN HEMT transistor output can be modeled as an ideal current source in parallel with an output capacitor ($C_{\mathrm{ds}}$) and a series inductor ($L_{\mathrm{p}}$) [8]. By appropriately configuring the Tee-line-based network, it becomes possible to effectively compensate for transistor

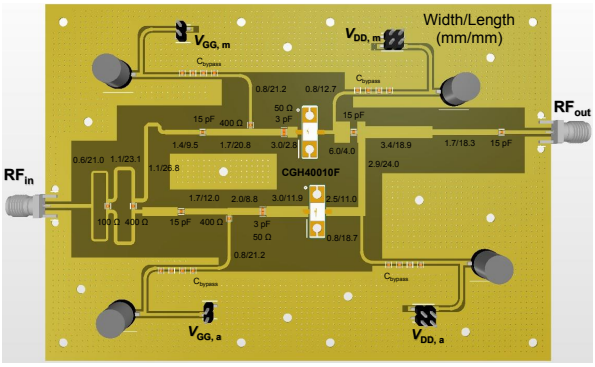


Fig. 2. Circuit schematic of the proposed wideband Doherty PA.

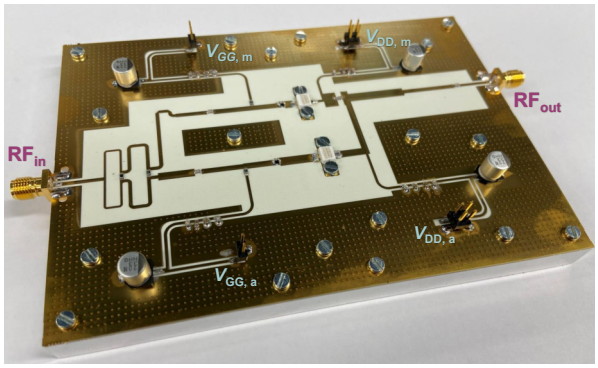


Fig. 3. Photograph of the fabricated wideband Doherty PA prototype circuit.

parasitics, including $C_{\rm ds}$ and $L_{\rm p}$. Additionally, the shunt transmission lines to the ground serve the purpose of biasing both active devices, contributing to the compactness of the Tee-line-based network.

To analyze the load modulation network, the black-box approach is employed. The complete Doherty output combiner can assumed to be a lossy 2×2 cascade matrix with the load integrated, denoted as $A_{\rm 2P}$, for easier analysis. It is worth noting that the product of the cascade matrices corresponding to each element in Fig. 1, evaluated at the center frequency $\omega_0$, must be equivalent to the cascade matrix of the lossy two-port network. This gives

$$\mathbf{A_{2P}} = \mathbf{A_{par,m}}\mathbf{A_{T,m}}\mathbf{A_{RL}}\mathbf{A_{TL4}}\mathbf{A_{T,a}}\mathbf{A_{par,a}} \tag{1}$$

where

$$\mathbf{A_{par,m}} = \begin{bmatrix} 1 & 0 \\ j\omega_0 C_{\rm ds,\,m} & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega_0 L_{\rm p,\,m} \\ 0 & 1 \end{bmatrix} \tag{2}$$

$$\mathbf{A_{par,a}} = \begin{bmatrix} 1 & j\omega_0 L_{\rm p,\,a} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega_0 C_{\rm ds,\,a} & 1 \end{bmatrix}. \tag{3}$$

Subsequently, it becomes straightforward to transform the two-port cascaded matrix $A_{\rm 2P}$ into an impedance matrix, $Z_{\rm 2P}$. The Tee-line-based load modulation networks can thereby be analyzed with respect to the frequency, under the conditions of varying characteristic impedance and electrical length of each line. Note that the system equations governing the load modulation networks are under-determined. As a result, the values for the transmission line characteristic impedance and electrical length can be chosen in a manner that effectively compensates for the transistor parasitics and packaged elements.

## III. Prototype Circuit Design

To validate the theoretical concepts, an RF-input wideband Doherty PA prototype circuit was designed and implemented, utilizing 10-W Wolfspeed GaN HEMT transistors (CGH40010F) for both the main and auxiliary amplifiers, with a center frequency of 2.15 GHz. The complete schematic of the prototype circuit can be seen in Fig. 2. The implementation was carried out on a 20-mil Rogers 4350B substrate. The Doherty load modulation network was realized based on the proposed method. The equivalent output parasitic and packaged model of the CGH40010F transistor, as shown in Fig. 1, were obtained through the de-embedding of small-signal and load-pull simulations. The optimum load resistance ($R_{\rm opt}$) was then calculated from the transistor's $I$-$V$ curves. The Tee-line-based load modulation networks were derived to achieve a wideband response resembling that of a series transmission-line-based network. These networks were further synthesized using the black-box approach to determine the characteristic impedance and electrical length of each line, while effectively compensating for the transistor's output parasitic and packaged effects. To match the common load impedance ($R_{\rm L}$) to 50 Ω, a low-order filter-based matching network was employed. Additionally, a series RC network at the input, along with a resistor in the gate bias path, was utilized for both the main and auxiliary amplifiers to maintain stability across the entire operating frequency bands. A photo of the implemented prototype circuit is shown in Fig. 3.

## IV. Measurement Results

The implemented prototype circuit was characterized through static continuous-wave (CW) measurements. Both the main and auxiliary amplifiers were biased with a drain bias voltage of 28 V. The main amplifier operated in class-B mode with a quiescent current of 50 mA, while the auxiliary amplifier was biased in class-C.

The prototype was tested under the excitation of a single-tone CW signal spanning from 1.6 to 2.7 GHz. The measurement results, as depicted in Fig. 4 and Fig. 5, demonstrate a distinct enhancement in back-off efficiency within the designed frequency band. The fabricated prototype exhibits excellent broadband performance, as illustrated in Fig. 6, with a peak output power ranging from 43.3 dBm to 44.3 dBm over a 1.1-GHz bandwidth, confirming its wideband large-signal capability. Furthermore, the PA achieves a drain efficiency of 51%–63% at the peak power level and 41%-53% at the 6-dB back-off power level across the entire operating frequency band. The proposed Doherty PA exhibits decent efficiency improvements over a broad range of frequencies when compared to other advanced high-efficiency PAs outlined in Table I. Additionally, its compact size and the systematic design procedure further contribute to the value of this work.

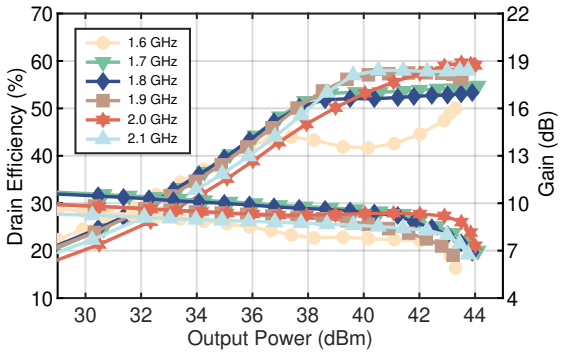


Fig. 4. Measured drain efficiency and gain versus output power of the wideband Doherty PA prototype from 1.6 to 2.1 GHz.

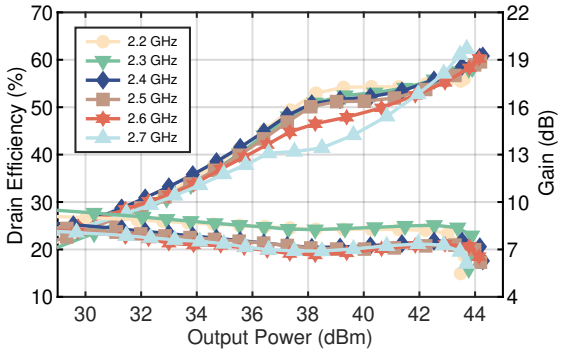


Fig. 5. Measured drain efficiency and gain versus output power of the wideband Doherty PA prototype from 2.2 to 2.7 GHz.

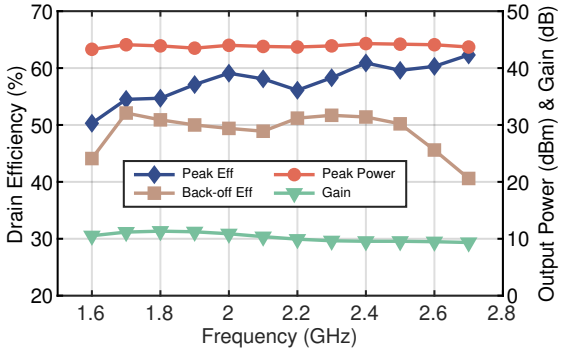


Fig. 6. Measured drain efficiency at peak and 6-dB back-off power level, peak output power, and gain versus frequencies across 1.6 to 2.7 GHz.

## V. Conclusion

This paper presents a combiner network for the Doherty PA that is based on the Tee-line networks. The proposed network exhibits inherent wideband characteristics and effectively addresses the impact of output parasitics caused by the transistors, resulting in excellent bandwidth performance. To validate the proposed topology, a wideband Doherty PA prototype operating in the frequency range of 1.6 GHz to 2.7 GHz is experimentally demonstrated. The prototype achieves a drain efficiency of 51%–63% at the peak power level and 41%-53% at the 6-dB back-off power level. Additionally, the prototype achieves a peak output power ranging from 43.3 dBm to 44.3 dBm over a 1.1 GHz bandwidth, further confirming the effectiveness of the proposed approach.

Table 1. Comparison with state-of-the-art load modulated PAs.

| Ref. Year | Arch. | Freq (GHz) | FBW (%) | $P_{\text{peak}}$ (dBm) | $\eta_{\text{peak}}$ (%) | $\eta_{\text{OBO}}$ (%) |
|---|---|---|---|---|---|---|
| [9] 2020 | LMBA | 1.5-2.5 | 51 | 45.6-46.7 | 67-77 | 51-64 |
| [10] 2023 | SLMBA | 1.3-2.1 | 47 | 50.3-53.0 | 28-62 | 42-53 |
| [2] 2019 | DEPA | 2.5-3.8 | 41 | 48.8-49.8 | 54-67 | 47-60 |
| [4] 2023 | CLMA | 2.1-3.5 | 50 | 41.4-43.1 | 47-58 | 36-51 |
| [11] 2022 | SCLMA | 2.0-3.0 | 40 | 42.0-43.5 | 55-68 | 46-53 |
| [12] 2022 | DPA | 2.5-3.3 | 28 | 42.5-44.2 | 61-66 | 45-52 |
| [13] 2023 | DPA | 3.3-3.9 | 17 | 45.6-47.6 | 48-53 | 35-45 |
| **This work** | **DPA** | **1.6-2.7** | **51** | **43.3-44.3** | **51-63** | **41-53** |

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