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Tunable Dual-Frequency Interference Suppression Circuit with GaN MMIC Delay Lines

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***Abstract*— This paper presents a broadband interference suppression circuit covering the 2–4 GHz octave. The circuit is capable of placing simultaneously two notches within the band with tunable center frequencies. A hybrid four-branch interferometer topology with gain incorporates GaN MMIC loaded tunable transmission-line delays. The circuit reduces the power of interfering signals by at least 10 dB, while amplifying the desired signal by as much as 18 dB. The overall circuit had a NF of 5–8.5 dB across the band. This technique lends itself to produce sharp notches without the requirement of high-Q resonators, so implementations on low complexity PCBs is feasible.**

I. Introduction

Interference suppression is required when either an in-band or out-of-band interfering signal saturates the mixer and analog-to-digital converter in the receiver of a RF front end. Self-interference methods are detailed in [1], mainly for narrowband receivers. In wideband receivers, out-of-band interference is equally important, and a possible solution are electronically-tunable passive filters, e.g. [2] which are not amenable to monolithic integration and can be lossy and/or bulky. An overview of interference suppression circuits for reconfigurable front ends is given in [3]. Analog finite-impulse response (FIR) filters have been implemented in CMOS as switched capacitor or delay line N-path topologies, e.g. [4], [5] and are limited in input power handling. Digital cancellation can provide a large degree of suppression provided linear receiver operation [6]. Therefore, analog suppression at the front end is useful for providing the initial coarse suppression.

Hybrid varactor-based tunable dual-notch filters covering approximately an octave in the 700 MHz – 1.5 GHz range are demonstrated in [7], [8] with the goal of suppressing two interferers in two separate parts of the band, with an insertion loss on the order of 1 dB and no reported linearity metric. Additionally, a CMOS active N-path tunable bandpass filter with sideband suppression is reported in [9] in the 0.2–1.2 GHz tuning range with about 20 dB of gain, a noise figure of 4.5 –6.2 dB. Here we present an active circuit that can place two frequency notches within the 2 –4 GHz octave to simultaneously suppress two interfering signals while providing gain to the desired signal. The circuit is based on Gallium Nitride (GaN) MMIC delay lines with a GaAs low-noise pre-amplifier. The block diagram of the approach is shown in Fig. 1, where a four-branch interferometer includes a gain stage in each branch followed by a tunable delay line.

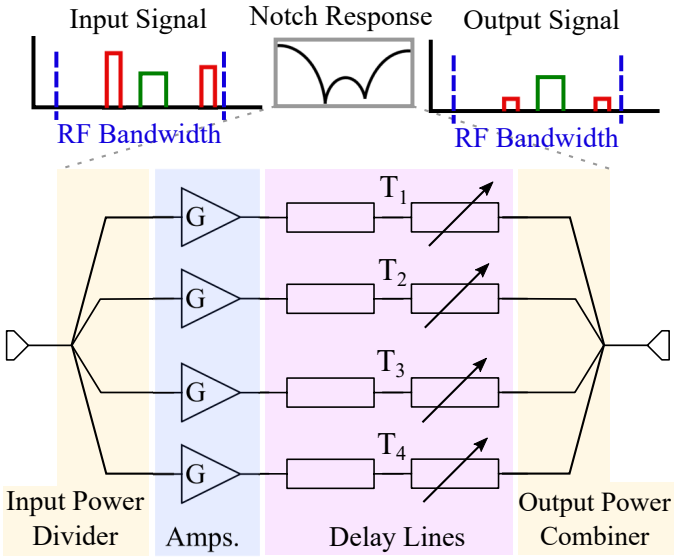

Fig. 1. Diagram of the tunable dual frequency interference suppression circuit with gain depicting the interference suppression of two unwated signals either side of the desired signal within the RF bandwidth.

The delays are adjusted to provide subtraction of signals at the output at two distinct frequencies.

II. Interformeter Analysis

The four-branch interferometer from Fig. 1 can be viewed as two parallel dual-branch circuits with a relative delay. Referring to Fig. 2, each subcircuit consists of two branches with gain G, fixed delay lines D_1 and variable delay lines $\Delta\tau_1$. In the four-branch full circuit, there is an additional delay $\Delta\tau_2$ between the two subcircuits. The variable lines create delays T_i in each of the four branches given by:

$$T_2 = \Delta\tau_1 + T_1, \quad T_3 = \Delta\tau_2 + T_1, \quad T_4 = \Delta\tau_1 + T_3,$$

where $T_1 = D_1$ is the delay in Line 1. The key principle is that the difference in delay between the lines inside both interferometer subsections, $\Delta\tau_1$, creates a notch at frequency f_1, while $\Delta\tau_2$ creates a notch at a second frequency f_2. The interformeter creates a null through the vector addition of signals in the two branches at the output power combiner. The null is a result of destructive interference when the phases in the two paths at a given frequency are $(2n+1)\pi$ apart. The

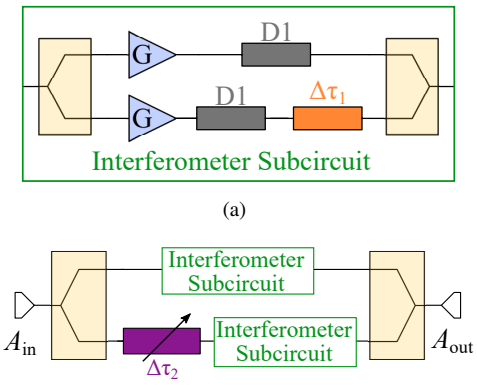

Fig. 2. Ideal dual frequency suppression circuit topology used to analyse the topology and determine parameters for the board design. (a) Block diagram of a two-branch interferometer that creates the first notch. (b) Block diagram of combined interferometer subcircuits with additional delay to create the second notch.

phase in each branch is determined by the fixed and variable delay, expressed as $\phi_i = -2\pi f(T_{\text{fixed},i} + T_{\text{variable},i})$. The frequency of the notch is set by the phase difference of the two paths. For example, for branches 1 and 2, assuming equal gain blocks and balanced power dividers and combiners, the phase difference is given by:

$$\phi_2 - \phi_1 = -2\pi f \Delta\tau_1, \tag{1}$$

The resulting relationship between frequency of the null and the difference in delays is:

$$f_1 = \frac{(2n+1)\pi}{2\pi\Delta\tau_1} = \frac{2n+1}{2}\frac{1}{\Delta\tau_1}, \quad \forall n \in \mathbf{Z}. \tag{2}$$

For the desired octave bandwidth of tuning the $n = 0$ null is used, resulting in $f_1 = 1/(2\Delta\tau_1)$. A similar expression can be obtained for the second null center frequency $f_2 = 1/(2\Delta\tau_2)$. In order to have comparable loss in all four branches, a variable delay line is used in each branch. In a physical implementation, there is an additional equal fixed delay, C, in each path which ensures a positive delay in all paths. The delay differences $\Delta\tau_1$ and $\Delta\tau_2$ are split between all branches making the shortest and longest delays equal to:

$$T_{1,4} = C \mp \frac{1}{4f_1} \mp \frac{1}{4f_2}, \tag{3}$$

and the other two delays equal to

$$T_{2,3} = C \pm \frac{1}{4f_1} \mp \frac{1}{4f_2}. \tag{4}$$

The required tuning range is found by iterating through all four combinations of maximum and minimum frequency settings for the notches in the 2 – 4 GHz octave. The range for the delays is calculated to be:

$$\begin{aligned} T_1 &= C - (187.5 \pm 62.5)\,\text{ps} \\ T_2 &= C + (62.5 \pm 62.5)\,\text{ps} \\ T_3 &= C - (62.5 \pm 62.5)\,\text{ps} \\ T_4 &= C + (187.5 \pm 62.5)\,\text{ps} \end{aligned} \tag{5}$$

In the expression for $T_{1,4}$ the $+$ sign corresponds to delays for both notches at 2 GHz, while the $-$ sign corresponds to both notches set at the upper 4 GHz frequency. Whereas, in the expressions of $T_{2,3}$ the $+$ sign corresponds to the largest notch separation (2 GHz), and the $-$ sign corresponds to the case when the notches overlap. For the actual physical implementation shown in next section, the shortest line is obtained for $C > 250$ ps, to ensure T_1 is positive. Assuming ideal lossless and amplitude-balanced 4-to-1 divider and combiner, and equal gain G in each path, the transmission gain amplitude ($A_{\text{out}}/A_{\text{in}}$ in Fig. 2) over frequency is given by:

$$\frac{A_{\text{out}}}{A_{\text{in}}} = \frac{G}{4}e^{-2\pi f T_1} + \frac{G}{4}e^{-2\pi f T_2} + \frac{G}{4}e^{-2\pi f T_3} + \frac{G}{4}e^{-2\pi f T_4} \tag{6}$$

and substituting $(T_2 - T_1) = (T_4 - T_3) = \Delta\tau_1$ and $(T_3 - T_1) = \Delta\tau_2$, the transmission gain can then expressed as:

$$\frac{A_{\text{out}}}{A_{\text{in}}} = \frac{G}{4}[e^{-2\pi f T_1}(1 + e^{-2\pi f \Delta\tau_2})(1 + e^{-2\pi f \Delta\tau_1})]. \tag{7}$$

An example is shown in Fig. 3 for two pairs of notch frequencies, showing how the separation between notches affects the gain of any desired signal at frequencies around the notches. The delays in each path are calculated for two example notch settings, f_1 and f_2, shown in Fig.4. Using these delays along with $C = 477.5$ ps and an amplifier gain of 20 dB, equation (6) is used to calculate the theoretical frequency response compared to simulation and measurement in the next section.

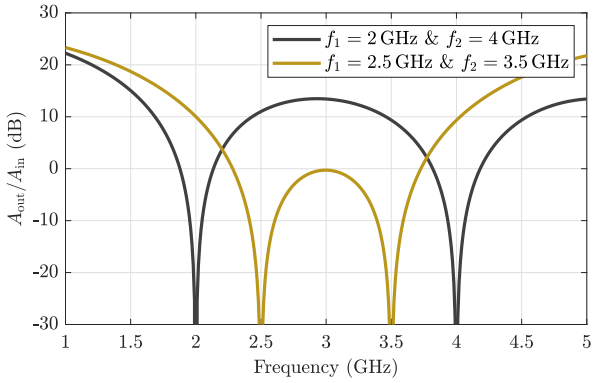

Fig. 3. Theoretical signal transmission through the interference suppression circuit over frequency for two pairs of notch frequency settings.

III. Design and Implementation

The circuit is designed on a 0.508-mm thick Rogers 4350B substrate with gain provided by MiniCircuits PMA3-83MP+ amplifiers that cover 0.4 to 8 GHz, with a drop in gain from 20 dB at 2 GHz to 18.8 dB at 4 GHz. The 1-to-4 power dividers/combiners are implemented with three microstrip Wilkinson dividers. Fixed microstrip delay lines are meandered symmetrically around the variable delay lines, which are

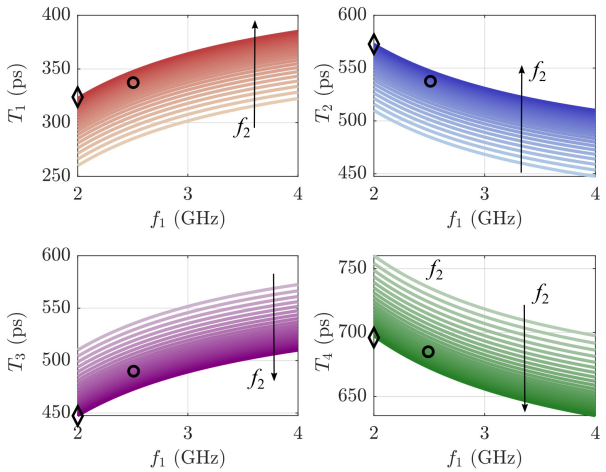

Fig. 4. Plot of the time delays according to (3), (4) required for different notch frequency combinations f_1 and f_2 when $C = 477.5$ ps. Black diamonds indicate 2 and 4 GHz setting delay values used in Fig. 3, while black circles are the values used for the 2.5 and 3.5 GHz setting.

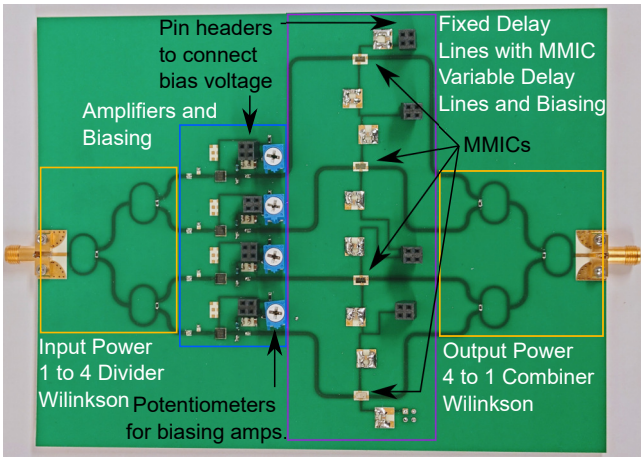

Fig. 5. Photograph of the tunable dual notch fabricated board sized 17.5 cm by 13.5 cm. The microstrip circuit is on a 20 mil Rogers 4350b substrate with 4 QFN amplifiers and 4 GaN MMICs mounted onto the PCB.

hybridly integrated MMICs mounted on the same circuit board, Fig. 5.

Using GaN MMIC delay lines described in [10], the delay tuning of ± 62.5 ps can be achieved over the desired 2–4 GHz tuning bandwidth. Briefly, these MMICs, implemented in the WIN Semiconductors NP15 GaN on SiC process, are artificial transmission line $L - C$ networks with 7 sections and with varactor-connected HEMTs in shunt. Four MMICs are mounted with silver epoxy in the circuit and bonded to the 50-Ω microstrip lines. The notch frequencies depend on the voltage bias applied to each line to create the specified time delays. This can be calculated from measurements of the variable delay lines. For the overall delay in each path, equations (3) and (4) are used to solve for the variable delay based on the notch frequency setting with $C = 477.5$ ps. The simulated delay in each line as a function of the notch frequencies is shown in Fig. 4, where each colored line corresponds to a fixed f_2.

Subtracting the fixed delay, implemented through a fixed-length microstrip line, the variable delay is used to calculate voltage settings for the MMICs in each path. The relationship between the voltage and notch frequency is not intuitive and the voltage is inversely related to the delay given by equations (3) and (4).

IV. Measured Circuit Performance

Small-signal characterization of the hybrid circuit from Fig. 5 is performed with a 3.5-mm SOLT calibration and compared to two kinds of simulations in Fig. 6. The ideal case is based on the theory from the previous section, with the gain of the amplifiers taken from the manufacturer's datasheet. The circuit simulations are performed with measured MMIC delay line S-parameters, and including 0.1 nH bond-wire inductances at inputs and outputs. Manufacturer-provided S-parameters for the resistors and amplifiers are used. The measured and simulated results directly apply the voltage settings found from the delays in Fig. 4 without any further optimization. The match remains below 9 dB over the measured 1 to 5 GHz range. It is limited by the input match of the chosen broadband amplifier and barely changes with the notch setting. The depth of the notch is less than in the ideal case as expected, and is predicted well by simulations. The measured notch is below -10 dB for all notch settings. There is distortion in both the simulated and measured notches around 4 GHz due to the variation in insertion loss of the delay lines over voltage at this and higher frequencies. For desired signals, the delays in each path can be set to create a passband at the signal frequency. For the two edge cases this is shown in Fig. 7, though the response can be tuned for signals in the center of the band maintaining gain above 10 dB.

Noise figure (NF) measurements are done in comparison with the amplifier alone to see the impact of the tunable dual notch topology on the noise figure. The amplifier is chosen as a compromise between noise figure (around 4 dB across the 2–4 GHz band) and high $P_{1\mathrm{dB}} = 26$ dBm and OIP3 measured above = 35 dBm. The dual notch circuit creates loss after the amplifier and the noise figure should increase based on this loss. For this reason the noise figure was measured when the hybrid board was set to the maximum gain at the desired frequency. The measured minimum NF varies from 6–8.5 dB from the center to the edges of the band. The difference from the stand alone amplifier noise figure is limited by the MMIC delay lines used that have a transmission coefficient $|S_{21}|$ ranging from -1.8 to -2.5 dB over tuning voltage. There is an additional 0.6 dB of loss from the Wilkinson dividers and combiners.The IIP3 was found to be greater than 20 dBm across the band for most notch settings with passband IIP3 degradation down to 10 dBm at the edge of the delay line tuning range, -20 V.

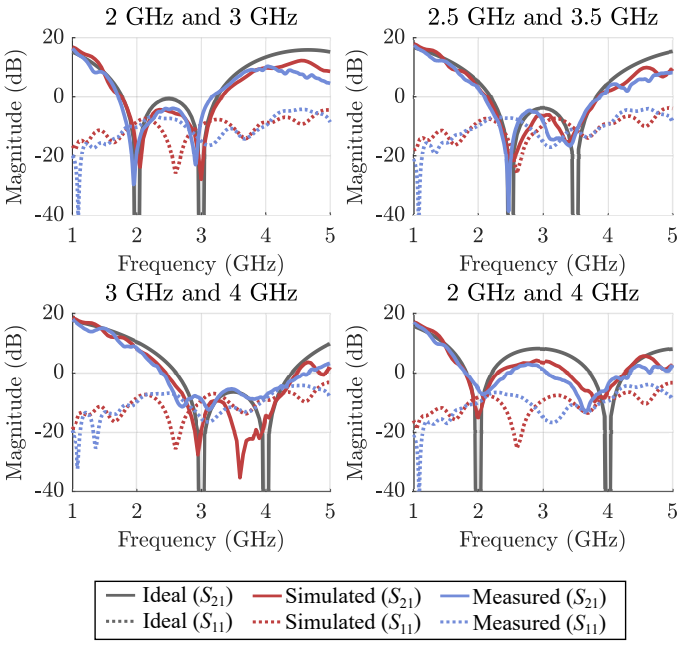

Fig. 6. Small signal scattering parameters of dual notch circuit with the notches set at the frequencies indicated in the plot title. Comparing an ideal circuit, simulated PCB, and measured PCB.

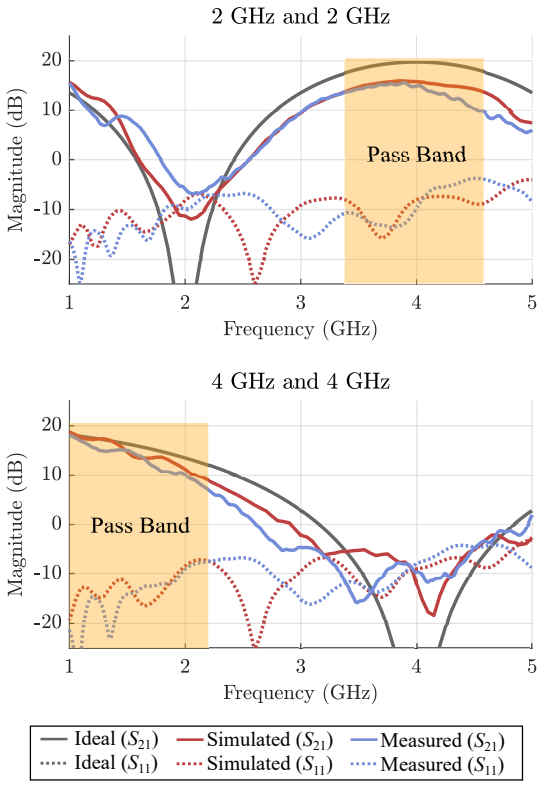

Fig. 7. Small-signal scattering parameters of dual notch circuit with the notches set at the same frequencies at the band edges as indicated in the plot title creating pass band regions. Comparing an ideal circuit, simulated circuit, and measured circuit.

V. Conclusion

An active tunable dual notch circuit for suppressing interfering signals in the 2–4 GHz octave band using a four-branch interferometer is presented. The circuit reduces the power of an interfering signals by at least 10 dB, while amplifying the desired signal by as much as 18 dB. The measured circuit agrees well with simulations and and idealized theory presented here. The noise figure ranges from 5–8.5 dB across the octave band and is comparable to similar active tunable circuits in a similar frequency range [9]. The LNAs in this work are off-the-shelf GaAs packaged circuits, but can be implemented in GaN for higher power handing and better linearity. Additionally, variable gain stages in the paths before the final combiner can help increase the signal suppression and noise performance.

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