
# Impact of pole-to-pole DC voltage on energy requirement of FB YY-MMC

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*Index Terms*—**Modular Multilevel Converters (MMC), grid-connected converter, high voltage power converters, energy requirement and losses estimation, submodule capacitor parameter design.**

*Abstract*—**The aim of this paper is to investigate the impact of pole-to-pole DC voltage on the energy requirements of a modular multilevel converter with full-bridge submodules (FB-MMC). With focus on energy-storage equipped FB-MMCs, the relation between the pole-to-pole voltage and the peak-to-peak energy variations in the MMC's arms is derived. Unlike MMC with half-bridge (HB) submodules (SM), in a FB-MMC the pole-to-pole DC voltage can be selected independently of the AC voltage; this allows for reduced energy requirements as well as lower number of FB SMs and capacitors for the same converter ratings. Furthermore, the impact of the converter's circulating current on the MMC's energy requirements is investigated. A guideline for the converter design is provided. Theoretical findings are validated via time-domain simulations.**

## I. Introduction

In recent years, Modular Multilevel Converters (MMCs) have become the utility standard for high-power and high-voltage grid applications. The wye- and delta-connected chain-link converters are used for reactive power compensation, while the YY-MMC topology that has a common DC-link is used in HVDC-transmission. The MMC provides a high efficiency, a relatively small footprint, an excellent dynamic performance and robustness when connected to weak grids [1], [2]. Moreover, YY-MMCs with Energy Storage (ES) connected to the DC-link have found grid applications, especially to favor integration of renewable energy sources. [3].

In a YY-MMC structure, each phase-leg consists of an upper and lower converter arm. Each arm has several series connected submodules (SM), which can be considered by either a half-bridge (HB) or full-bridge (FB) converter. Based on the required phase voltage, the SMs are inserted or bypassed dynamically to form a sinusoidal voltage at the MMC's terminal.

Studies have shown that YY-MMC topology has a number of challenges [4]. One of the challenges is to reduce the requirement for the SMs' capacitors size in the YY-MMC, as they account for nearly 50% of its total cost [5]. Most studies available in the literature dealing with capacitance energy reduction are focusing on injecting a circulating current or a third-order harmonic voltage in the MMC arms. For example, [6] has proposed a method for injecting a second order harmonic circulating current so the peak SM voltage coincides with the maximum requested arm voltage, resulting in a lower capacitance requirement. The impact of the third-order harmonic arm voltage injection on the capacitance requirement of YY-MMC has been analyzed in [7] and [8]. In [9], a hardware-based strategy to achieve a capacitance energy reduction of the YY-MMC has been proposed. However, a way to find the optimal pole-to-pole dc voltage for an ES-connected MMC which results in the lowest possible capacitors size in the SMs has not been presented yet.

Unlike the DC transmission application, the pole-to-pole DC voltage of the MMC is a design parameter in ES systems and can be selected in the design stage. For HB YY-MMCs, the AC grid voltage determines the minimum needed pole-to-pole DC voltage, which is not the case for a FB configuration, which do not have the restriction on a certain minimum pole-to-pole DC voltage. A controllable pole-to-pole DC voltage has the advantage of handling faults on the DC side. Moreover, the freedom to choose the pole-to-pole DC voltage enables the search for a minimum SM capacitor energy.

This paper investigates the optimal pole-to-pole DC voltage that reduces the capacitance energy requirement and will result in the minimum number of SMs for the same YY-MMC rating. Furthermore, the impact of the circulating current on the YY-MMC capacitance

requirements is explored. A guideline for the FB-based YY-MMC design based on an optimal pole-to-pole DC voltage selection is provided and theoretical findings are validated through time-domain simulations.

## II. Energy Variation in FB YY-MMC

The FB YY-MMC scheme is shown in Fig. 1. Each arm consists of $N$ SMs in series together with a filter reactor having the inductance and resistance $L$ and $R$, respectively. The AC side of the YY-MMC is connected to a three-phase grid with voltage of $v_{\mathrm{g}}$ and the DC side is connected to ES with pole-to-pole DC voltage of $V_{\mathrm{dc}}$ and current of $I_{\mathrm{dc}}$. The terms $v_{\mathrm{u}}$ and $v_{\mathrm{l}}$ are the upper and lower arm voltages of a generic phase, while $i_{\mathrm{u}}$ and $i_{\mathrm{l}}$ are the upper and lower arm currents, and $i_{\mathrm{g}}$ is the phase current.

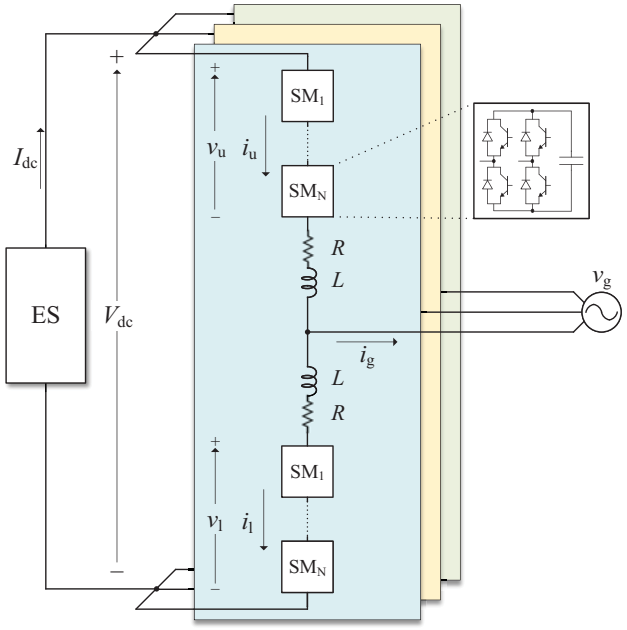


Fig. 1. Scheme of grid-connected FB YY-MMC.

Assuming inverter reference as in Fig. 1, a generic YY-MMC can be modeled as a voltage source, where $v_{\mathrm{s}}$ is the YY-MMC output voltage behind the filter and is written

$$v_{\mathrm{s}} = \frac{L}{2}\frac{di_{\mathrm{g}}}{dt} + \frac{R}{2}i_{\mathrm{g}} + v_{\mathrm{g}} \tag{1}$$

since the equivalent output filter of YY-MMC is half of the arm filter [2], and $v_{\mathrm{s}}$ is found to be

$$v_{\mathrm{s}} = \frac{v_{\mathrm{l}} - v_{\mathrm{u}}}{2} \tag{2}$$

From Fig. 1 and neglecting the DC voltage drop of the filter, the relation between $V_{\mathrm{dc}}$ and arm voltages can be found as

$$V_{\mathrm{dc}} = v_{\mathrm{l}} + v_{\mathrm{u}} \tag{3}$$

Combining (2) and (3), the arm voltages are derived as

$$\begin{aligned} v_{\mathrm{u}} &= \frac{V_{\mathrm{dc}}}{2} - v_{\mathrm{s}} \\ v_{\mathrm{l}} &= \frac{V_{\mathrm{dc}}}{2} + v_{\mathrm{s}} \end{aligned} \tag{4}$$

The next step is to find the upper and lower arm currents. The arm currents consist of three main terms [10]

$$\begin{aligned} i_{\mathrm{u}} &= I_{\mathrm{dc,arm}} + i_{\mathrm{f,arm}} + i_{\mathrm{cir}} \\ i_{\mathrm{l}} &= I_{\mathrm{dc,arm}} - i_{\mathrm{f,arm}} + i_{\mathrm{cir}} \end{aligned} \tag{5}$$

where $I_{\mathrm{dc,arm}}$ is the DC current flowing through the upper and lower arm and is 1/3 of $I_{\mathrm{dc}}$, $i_{\mathrm{f,arm}}$ is the current at fundamental frequency, which is responsible for exchanging active and reactive power between the YY-MMC and the grid and is assumed to be half of the phase current $i_{\mathrm{g}}$. The term $i_{\mathrm{cir}}$ is the circulating current resulting from the capacitors voltage ripple mismatch between the upper arm and lower arm. Here, it is assumed that the circulating current is well suppressed by the circulating current controller (CCC), thus $i_{\mathrm{cir}} = 0$. This implies that the CCC adds an extra term to the reference voltage of upper and lower arm in (4). However, since this term is very small, it is neglected in the analysis. As a result, the upper and lower arm currents can be rewritten as

$$\begin{aligned} i_{\mathrm{u}} &= \frac{I_{\mathrm{dc}}}{3} + \frac{i_{\mathrm{g}}}{2} \\ i_{\mathrm{l}} &= \frac{I_{\mathrm{dc}}}{3} - \frac{i_{\mathrm{g}}}{2} \end{aligned} \tag{6}$$

Considering a steady-state operation, it is assumed that

$$v_{\mathrm{g}} = \hat{V}_{\mathrm{g}}\cos(\omega t) \tag{7}$$

$$i_{\mathrm{g}} = \hat{I}_{\mathrm{g}}\cos(\omega t + \varphi) \tag{8}$$

Therefore, $v_{\mathrm{s}}$ can be found in phasor domain

$$\bar{V}_{\mathrm{s}} = \hat{V}_{\mathrm{s}}\angle\varphi_{\mathrm{s}} = \left(j\omega\frac{L}{2} + \frac{R}{2}\right)\bar{I}_{\mathrm{g}} + \bar{V}_{\mathrm{g}} \tag{9}$$

where $\bar{V}_{\mathrm{g}} = \widehat{V}_{\mathrm{g}}\angle 0$ and $\bar{I}_{\mathrm{g}} = \widehat{I}_{\mathrm{g}}\angle\varphi$ are the grid voltage and current phasors, respectively.

After the arms' voltage and current have been determined, the arm power and energy expressions can be found. The upper and lower arm instantaneous power are

$$p_{\mathrm{u,l}} = v_{\mathrm{u,l}}i_{\mathrm{u,l}} \tag{10}$$

replacing (4), (6), and (9) in (10) will result in

$$\begin{aligned} p_{\mathrm{u}} &= \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} + \frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4} \cos(\omega t + \varphi) - \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3} \cos(\omega t + \varphi_{\mathrm{s}}) \\ &\quad - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(2\omega t + \varphi + \varphi_{\mathrm{s}}) - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(\varphi - \varphi_{\mathrm{s}}) \\ p_{\mathrm{l}} &= \frac{V_{\mathrm{dc}} I_{\mathrm{dc}}}{6} - \frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4} \cos(\omega t + \varphi) + \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3} \cos(\omega t + \varphi_{\mathrm{s}}) \\ &\quad - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(2\omega t + \varphi + \varphi_{\mathrm{s}}) - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(\varphi - \varphi_{\mathrm{s}}) \end{aligned} \tag{11}$$

The active power balance between the DC and the AC sides of the YY-MMC is

$$V_{dc} I_{dc} = \frac{3}{2} \hat{V}_{\mathrm{s}} \hat{I}_{\mathrm{g}} \cos(\varphi - \varphi_{\mathrm{s}}) \tag{12}$$

Therefore, the DC terms in (11) are cancelled out. The instantaneous power in upper and lower arms become

$$\begin{aligned} p_u &= \frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4} \cos(\omega t + \varphi) - \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3} \cos(\omega t + \varphi_{\mathrm{s}}) \\ &\quad - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(2\omega t + \varphi + \varphi_{\mathrm{s}}) \\ p_l &= -\frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4} \cos(\omega t + \varphi) + \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3} \cos(\omega t + \varphi_{\mathrm{s}}) \\ &\quad - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{4} \cos(2\omega t + \varphi + \varphi_{\mathrm{s}}) \end{aligned} \tag{13}$$

The instantaneous variation of energy in upper and lower arm is determined by integrating the instantaneous power in each arm

$$\begin{aligned} w_{\mathrm{u}} &= \int p_{\mathrm{u}} dt = \frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4\omega} \sin(\omega t + \varphi) \\ &\quad - \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3\omega} \sin(\omega t + \varphi_{\mathrm{s}}) - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{8\omega} \sin(2\omega t + \varphi + \varphi_{\mathrm{s}}) \\ w_{\mathrm{l}} &= \int p_{\mathrm{l}} dt = -\frac{V_{\mathrm{dc}} \widehat{I}_{\mathrm{g}}}{4\omega} \sin(\omega t + \varphi) \\ &\quad + \frac{\widehat{V}_{\mathrm{s}} I_{\mathrm{dc}}}{3\omega} \sin(\omega t + \varphi_{\mathrm{s}}) - \frac{\widehat{V}_{\mathrm{s}} \widehat{I}_{\mathrm{g}}}{8\omega} \sin(2\omega t + \varphi + \varphi_{\mathrm{s}}) \end{aligned} \tag{14}$$

The energy variation of the capacitors in each arm will lead to a voltage modulation across the capacitor in each SM. The peak-to-peak energy value of the (14) is found using

$$W = \max(w_{\mathrm{u,l}}) - \min(w_{\mathrm{u,l}}) \tag{15}$$

where $W$ is the energy variation, which is a function of the $V_{\mathrm{dc}}$ and the active and reactive power exchange between the YY-MMC and the grid. Fig. 2 shows the energy variation expressed in seconds (energy divided by rated power) as a function of $V_{\mathrm{dc}}$ in pu and the output power angle $\varphi$, while keeping $\widehat{V}_{\mathrm{g}}$ and the apparent power to 1 pu. Fig. 3 displays $W$ versus $V_{\mathrm{dc}}$ for three different power angles: 0°, 60°, and 90°.

As shown in Fig. 2 and Fig. 3, there is a $V_{\mathrm{dc}}$ for every power angle that corresponds to a minimum energy variation. This pole-to-pole voltage and its corresponding energy variation are referred to as $V_{\mathrm{dc,min}}$ and $W_{\mathrm{min}}$. As an example, for the power angle of 90°, when only reactive power is injected to the grid, $V_{\mathrm{dc,min}} = 0$ and for the power angle of 0°, $V_{\mathrm{dc,min}} = 1.41$ pu. In case the active and reactive power have the same requirement, the highest energy variation between all the $V_{\mathrm{dc,min}}$s happens at the power angle of 60° and $V_{\mathrm{dc,min}} = 1.03$ pu. From Fig. 2, (14), and (15) it can be shown that while keeping the reactive power constant, the energy variation for the same amount of active power injection or absorption is equal. Furthermore, it is assumed that the converter only injects reactive power to the grid. Therefore, in Section III it is assumed that $0 \leq \varphi \leq \frac{\pi}{2}$.

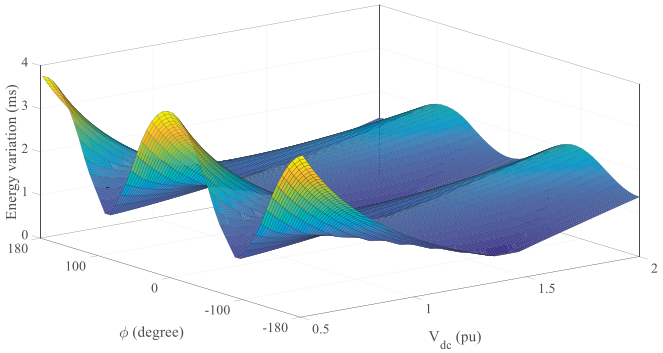


Fig. 2. Energy variation of YY-MMC for different pole-to-pole dc voltages and power angles.

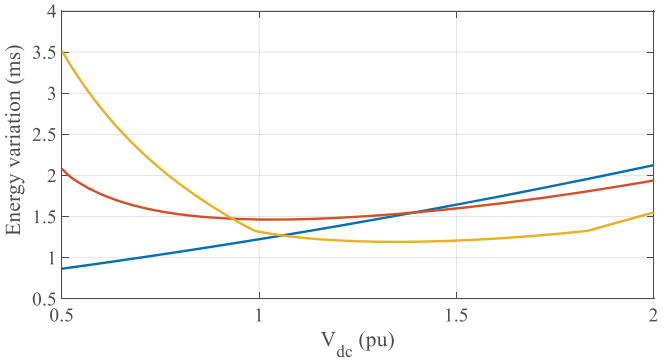


Fig. 3. Energy variation of YY-MMC for different pole-to-pole DC voltages when $\varphi = 90°$ (blue), $\varphi = 60°$ (red), and $\varphi = 0°$ (yellow).

An interesting range of pole-to-pole DC voltage is for values larger than 2 pu. As discussed in Section I, MMC SMs can be either HB or FB. HB SMs can only generate 0 and positive voltage; hence, the arm voltage should always be positive in a HB YY-MMC. Taking into account (4)

$$V_{\text{dc}} \geq 2\widehat{V}_{\text{s}} \tag{16}$$

and when neglecting the voltage drop over the filter reactor, the pole-to-pole DC voltage becomes

$$V_{\text{dc}} \geq 2 \text{ pu} \tag{17}$$

Therefore, the minimum pole-to-pole dc voltage is 2 pu for HB-MMC and is the usual choice for this kind of converters. Since FB SMs can generate negative voltages as well, there is no such limitation for $V_{\text{dc}}$ in FB-MMC. As it can be seen from Fig. 2 and Fig. 3, for every power angle, there is always a $V_{\text{dc,min}}$, lower than 2pu. Therefore, in case $V_{\text{dc,min}}$ is chosen as the ES DC voltage, the energy variation for FB-MMC is always lower than HB-MMC.

## III. FB YY-MMC Design

The design and sizing of the FB YY-MMC, based on the optimal selection of the pole-to-pole DC voltage to minimize the energy requirement of the YY-MMC is presented in this section. First, the design of components without dependence of $V_{\text{dc}}$ are presented. Next, a flow-chart that demonstrates how the optimal pole-to-pole DC voltage ($V_{\text{dc,opt}}$) should be selected is proposed. Finally, as $V_{\text{dc,opt}}$ is determined, the design of components that are dependent on $V_{\text{dc}}$ are analyzed.

The first component to be designed is the arm filter, which limits the line harmonics and enable current control. Moreover, it protects the SMs from transient currents and limits high-frequency components in the circulating current. A typical size of the arm filter is 0.10 to 0.20 pu [2], [11] and here it is assumed that the reactance is 10 times larger than the resistance. Here, the arm filter is chosen to 0.15 pu. The YY-MMC should provide the voltage reference generated by the current controller (CC). The maximum YY-MMC output voltage $\widehat{V}_{\text{s}}$ is determined as [12]

$$\widehat{V}_{\text{s}} = 1.05\widehat{V}_{\text{g}}(1 + \Delta V_{\text{g}} + I_{\text{pu}}\frac{Z_{\text{f}}}{2}) \tag{18}$$

where $\Delta V_{\text{g}}$ is the maximum grid voltage variation, $I_{\text{pu}}$ is the output current and equals 1 pu, and $Z_{\text{f}}$ is the arm filter impedance. Moreover, a 5% margin is added to guarantee a suitable dynamic response of the CC. Considering an arm filter of 0.15 pu and 10% maximum grid voltage variation, $\widehat{V}_{\text{s}}$ is found to be $1.23\widehat{V}_{\text{g}}$.

The next design consideration is the pole-to-pole DC voltage limit. From (12), the DC current equals

$$I_{\text{dc}} = \frac{3\hat{V}_{\text{s}}\hat{I}_{\text{g}}\cos(\varphi - \varphi_{\text{s}})}{2V_{\text{dc}}} \tag{19}$$

where $P$ is the active power to the grid. By decreasing $V_{\text{dc}}$, the arm current increases and semiconductors with larger rated current are required. Hence, $V_{\text{dc}}$ cannot decrease too much and a limit for $V_{\text{dc}}$, based on the rated current of the semiconductors ($I_{\text{n}}$), should be defined. The maximum current of the arm should be lower than the rated current of the semiconductors

$$\max(i_{\text{u}}, i_{\text{l}}) \leq I_{\text{n}} \tag{20}$$

From (6) and (8), the maximum upper and lower arm current are found to be

$$\max(i_{\text{au}}, i_{\text{al}}) = \frac{I_{\text{dc}}}{3} + \frac{\widehat{I}_{\text{g}}}{2} \tag{21}$$

combining (19), (20), (21) and assuming the apparent power to the grid equals $S = \frac{3}{2}\widehat{V}_{\text{g}}\widehat{I}_{\text{g}}$ when neglecting the voltage drop over the filter inductor, the limit for the pole-to-pole DC voltage can be written as

$$\frac{V_{\text{dc}}}{\widehat{V}_{\text{g}}} \geq \frac{P}{3\widehat{V}_{\text{g}}I_{\text{n}} - S} \tag{22}$$

Thus, the pu limit for the pole-to-pole DC voltage can be defined as

$$V_{\text{dclim,pu}} = \frac{P}{3\widehat{V}_{\text{g}}I_{\text{n}} - S} \tag{23}$$

The flowchart in Fig. 4 shows how $V_{\text{dcopt,pu}}$ and its corresponding energy requirement, which is called optimal energy requirement ($W_{\text{opt,pu}}$), should be chosen so that the least possible capacitor size is selected for the SMs and furthermore, the peak-to-peak voltage variations of SM's capacitors are held below a certain threshold for all the working points of the converter. The relation between the energy requirement and the capacitors and their voltage variations are discussed in the following paragraphs.

In the next step, the number of SMs are selected to guarantee that the YY-MMC is able to generate the needed voltage and does not enter in overmodulation during normal operations. Considering (4), (9) and assuming optimal values from the flow-chart, the maximum needed arm voltage becomes

$$\widehat{V}_{\text{arm}} = \max(v_{\text{au}}, v_{\text{al}}) = \frac{V_{\text{dcopt}}}{2} + \widehat{V}_{\text{s}} \tag{24}$$

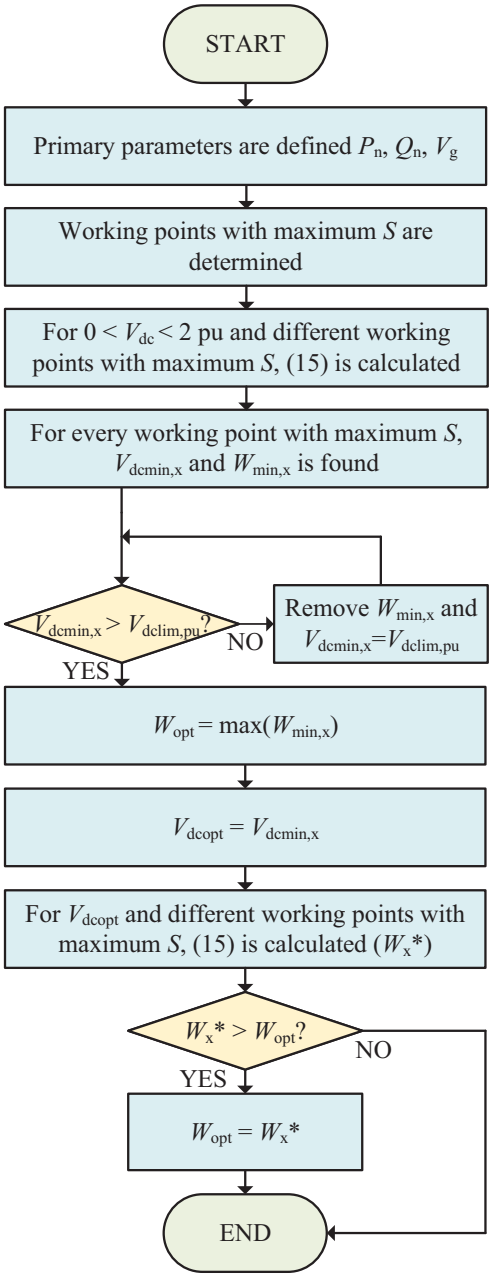


Fig. 4. Flowchart for $V_{dcopt}$ and $W_{opt}$ selection.

In order to find the number of SMs in each arm, the maximum arm voltage should be divided by the rated SM voltage $V_n$, which is chosen to fit the 100 FIT (100 failures in $10^9$ operating hours) value of the selected semiconductor device [12]. This voltage is inserted to the arm by each SM. Thus, the number of SMs in each arm become

$$N = \frac{\widehat{V}_{arm}}{V_n} \tag{25}$$

Finally, the energy requirement of the SM capacitor is determined. The energy requirement is defined as the peak-to-peak variation of the arm energy which originates from the voltage ripple of the capacitors. Considering that there are $N$ SMs in each arm, the total arm energy variation will be the sum of the energy variation of each SM capacitor. Selecting the optimal arm energy requirement found from the flow-chart in Fig. 4, the total arm energy variation can be determined as

$$\begin{aligned} W_{opt} &= \frac{N}{2} C \left(V_{cmax}^2 - V_{cmin}^2\right) \\ &= \frac{N}{2} C \left(V_{cmax} + V_{cmin}\right)\left(V_{cmax} - V_{cmin}\right) \end{aligned} \tag{26}$$

where $V_{cmax}$ and $V_{cmin}$ are the maximum and minimum capacitor voltage, respectively. Assuming $V_{cmax}+V_{cmin} \approx 2V_n$ and defining $\Delta V$ as the voltage ripple of the capacitor

$$\Delta V = \frac{V_{cmax} - V_{cmin}}{V_n} \tag{27}$$

and combining (26) and (27) and solving for $C$ results in

$$C = \frac{W_{opt}}{N \Delta V V_n^2} \tag{28}$$

## IV. Averaged Model and Control

In this section, the control blocks that are used for the time-domain simulations are introduced. Since studying voltage, currents, and switching events of of each SM is not of interest in this work, an averaged model of the YY-MMC has been investigated. The model used in this study is arm-level averaged model [2], in which each arm of the FB YY-MMC is modeled by a controllable voltage source. The capacitors of the SMs are modeled as a series connection of a controllable current source and a capacitor value of $C/N$, where $C$ is the SM capacitor value. The voltage and current sources are equal to

$$v_{av,u,l} = n_{u,l} v_{cm,u,l}^{\Sigma} \tag{29}$$

$$i_{av,u,l} = n_{u,l} i_{m,u,l} \tag{30}$$

where, as shown in Fig. 5, $v_{av,u}$, $v_{av,l}$, $i_{av,u}$, and $i_{av,l}$ are the voltages and currents of the upper and lower arm sources, $v_{cm,u}^{\Sigma}$ and $v_{cm,l}^{\Sigma}$ are the measured sum capacitor voltages of the upper and lower arm, $i_{m,u}$ and $i_{m,l}$ are the measured upper and lower arm currents, and $n_u$ and $n_l$ are upper and lower arm insertion indices, which are defined as

$$n_u = \frac{\frac{V_{m,dc}}{2} - v_{cc} - v_{ccc}}{v_{cr}^{\Sigma}} \tag{31}$$

$$n_l = \frac{\frac{V_{m,dc}}{2} + v_{cc} - v_{ccc}}{v_{cr}^{\Sigma}} \tag{32}$$

In (31) and (32) $V_{\mathrm{m,dc}}$ is the measured pole-to-pole DC voltage, $v_{\mathrm{cc}}$ is generated voltage reference by the CC, $v_{\mathrm{ccc}}$ is the voltage reference for circulating current suppression from the CCC, and $v_{\mathrm{cr}}^{\Sigma}$ is the reference sum capacitor voltage which is equal to $NV_{\mathrm{n}}$. For FB YY-MMC, the arm insertion indices is a number between $-1$ and 1 and shows in average how many SMs are inserted in each arm.

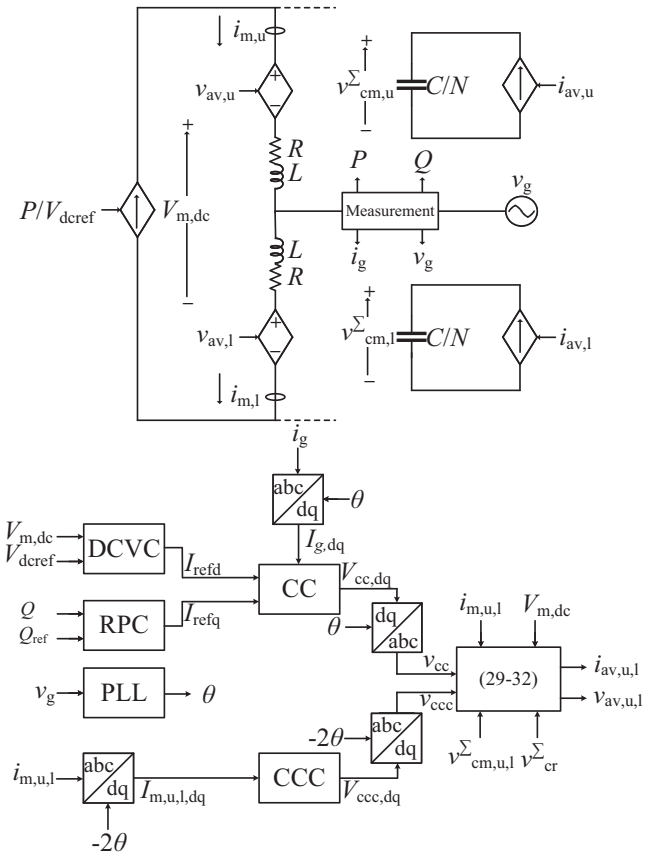


Fig. 5. FB YY-MMC arm-level averaged with controller.

The control system of the FB YY-MMC consists of a reactive power controller (RPC), a DC-link voltage controller (DCVC), a vector CC and a CCC as displayed in Fig. 5. The RPC is a PI controller generating the q-component of the reference current. The DCVC regulates the pole-to-pole DC voltage and provides the d-component of the reference current. A grid-following CC is used to regulate the YY-MMC output voltage and finally, a vector CCC is used to suppress the second-order harmonic in the circulating-current. The ES is modelled as a current source with the current equal to $P/V_{\mathrm{dc}}$. However, in actual applications, the voltage of the ES decreases as the state of charge of the storage becomes low. This decrease in the voltage will be reflected in the sum capacitors voltage which is neglected in this analysis.

## V. Case study and simulation results

In this section, based on the defined procedure, a FB YY-MMC with an ES is designed. The ES and grid specifications which are the primary design parameters of the FB YY-MMC are shown in TABLE I.

TABLE I
ES and grid specifications

| Parameter | Symbol | Unit | Value |
|---|---|---|---|
| ES rated active power | $P_{\mathrm{n}}$ | [MW] | 50 |
| Rated reactive power | $Q_{\mathrm{n}}$ | [MVar] | 100 |
| Rated apparent power | $S_{\mathrm{n}}$ | [MVA] | 112 |
| Line to line grid voltage | $V_{\mathrm{g}}$ | [kV] | 33 |
| Grid frequency | $f$ | [Hz] | 50 |

As explained in Section III, the two design parameters that are not dependent on $V_{\mathrm{dc}}$ are the arm filter reactor and $\widehat{V}_{\mathrm{s}}$ that are selected as 0.15 pu and $1.23\widehat{V}_{\mathrm{g}}$. By using the primary design parameters, the peak-to-peak energy value (15) can be found and is displayed in Fig. 6. Since there is only one operating point with a maximum apparent power, as shown in TABLE I, the most suitable candidate candidate for $V_{\mathrm{dcopt,pu}}$ is $V_{\mathrm{dcmin,pu}}$ which is found to be 0.98. For this value the max arm current from (21) is found to be 2016 A. Therefore, the selected semiconductor should have a current rating of at least 2016 A. Here, the semiconductor device with part number of 5SNA2000K450300 which has a rated current of 2500 A [12] is selected for the FB YY-MMC. Replacing $P$, $S$, and $\widehat{V}_{\mathrm{g}}$ from TABLE I and the semiconductor rated current in (23), the limit for pole-to-pole DC voltage is found. Considering the rated voltage of the chosen semiconductor device and the maximum voltage ripple of 10% for each SM capacitors, the other parameters of the FB YY-MMC are displayed in TABLE II.

The energy variation for the YY-MMC is simulated using the model presented in Section IV. In Fig. 7, the results are compared with the theoretical calculations for the apparent power exchange of 1 pu ($P$=50 MW and $Q$=100 MVar), as well as two other cases with different power ratings. As displayed, the simulation results are in agreement with the theoretical values. The maximum error is about 0.3% which is due to neglecting the voltage added by CCC in (4) and the assumption made in (26). Furthermore, as discussed before, while by regulating $V_{\mathrm{dc}}$, $W$ can be chosen as low as 1.46 ms for a FB

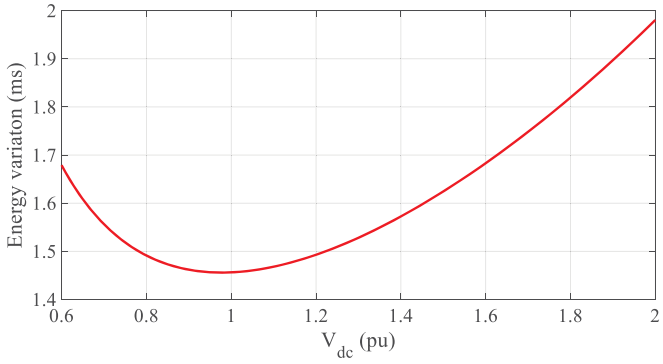


Fig. 6. Energy variation for the MMC with primary parameters in TABLE I.

TABLE II
FB YY-MMC DESIGN PARAMETERS

| Parameter | Symbol | Unit | Value |
|---|---|---|---|
| Arm filter | $Z_{\text{f}}$ | [pu] | 0.15 |
| MMC maximum output voltage | $V_{\text{s}}$ | [kV] | 33.14 |
| Maximum arm current | $I_{\text{max}}$ | [kA] | 2.02 |
| Semiconductor rated current | $I_{\text{n}}$ | [kA] | 2.5 |
| Pole-to-pole dc voltage limit | $V_{\text{dclim}}$ | [pu] | 0.56 |
| Pole-to-pole optimal dc voltage | $V_{\text{dcopt}}$ | [pu] | 0.98 |
| Optimal energy requirement | $W_{\text{opt}}$ | [ms] | 1.46 |
| Number of SMs per arm | $N$ | - | 23 |
| SM's maximum voltage ripple | $\Delta V$ | [%] | 10 |
| SM's rated voltage | $V_{\text{n}}$ | [kV] | 2.5 |
| SM's capacitance | $C$ | [mF] | 11.34 |

YY-MMC, according to (17), $V_{\text{dc}}$ has to be greater than 2 pu for a HB YY-MMC which results in a minimum energy requirement of 1.98 ms. As a result, the energy requirement for a FB YY-MMC is 26% lower than HB YY-MMC.

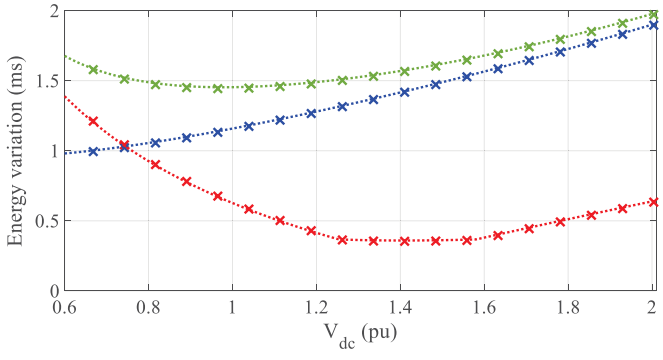


Fig. 7. The energy variation calculation (dotted lines) and simulation (crosses) for $P = 50$ MW and $Q = 100$ MVar (green), $P = 10$ MW and $Q = 100$ MVar (blue), and $P = 50$ MW and $Q = 10$ MVar (red).

Fig. 8 compares the $v^{\Sigma}_{\text{cm,u}}$ for the estimated optimal DC voltage ($V_{\text{dcopt}}$ = 0.98 pu), a lower value ($V_{\text{dc}}$ = 0.67 pu) and a higher value ($V_{dc}$ = 2 pu), which is the lowest possible value for HB-MMC. As mentioned in TABLE II, the maximum sum capacitor voltage ripple is designed to be 10% for $V_{\text{dcopt}}$, which is confirmed by the simulated value of 10.2%. Moreover, the voltage ripple for $V_{\text{dc}}$=0.67 pu and $V_{\text{dc}}$=2 pu are found to be 11.4% and 13.7%, respectively. Therefore, it is verified that $V_{\text{dcopt}}$ leads to the least voltage ripple.

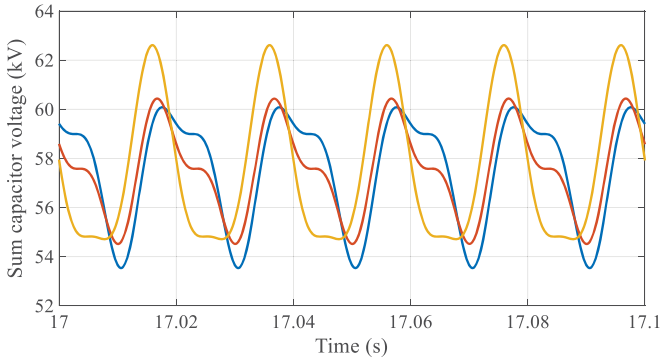


Fig. 8. Sum capacitor voltage ripples for $V_{\text{dc}} = 0.67$ (blue), $V_{\text{dc}} = 0.98$ (red), and $V_{\text{dc}} = 2$ (yellow).

Furthermore, $v^{\Sigma}_{\text{cm,u}}$ for the estimated optimal DC voltage ($V_{\text{dcopt}}$ = 0.98 pu) and the three different mentioned power exchange for Fig. 8 can be seen in Fig. 9. As discussed in Section III, the optimal DC voltage is chosen in a way that the capacitors voltage ripple do not exceed a certain threshold ($\Delta V = 10\%$ in this case study) for all the operating points. This is confirmed by the simulation which shows that the sum capacitors voltage ripple is 8% for $P = 10$ MW and $Q = 100$ MVar and 4.5% for $P = 50$ MW and $Q = 10$ MVar.

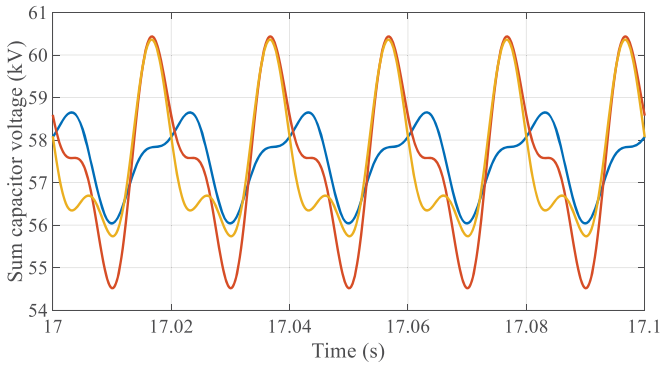


Fig. 9. Sum capacitor voltage ripple for $V_{\text{dc}} = 0.98$ pu and $P = 50$ MW and $Q = 10$ MVar (blue), $P = 50$ MW and $Q = 100$ MVar (red), and $P = 10$ MW and $Q = 100$ MVar (yellow).

Finally, the effect of the CCC on the energy variation for the FB YY-MMC is investigated. Fig. 10 shows the energy variation for the FB YY-MMC for three case studies: no CCC; proportional CCC; dq-based CCC as the one described in Fig. 5. When the second-order harmonic of the circulating current is completely suppressed by the dq-based CCC, the energy variation is at minimum with respect to the other two cases. For $V_{\text{dc}} = 0.98$ pu, the energy variation for the three cases is 1.73 ms, 1.49 ms, and 1.46 ms, respectively. Therefore, the proper suppression of the second-order circulating current leads to a reduction in the converter's energy requirement of 18%.

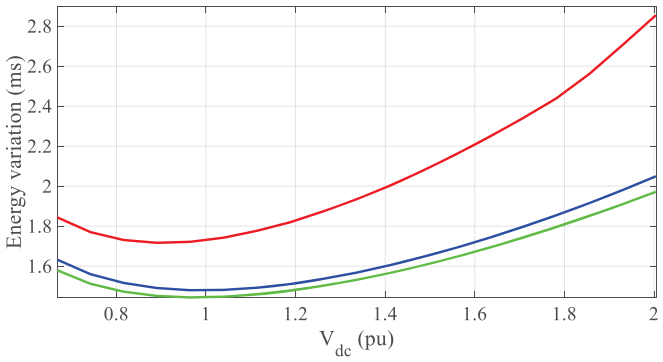


Fig. 10. The energy requirement in case no CCC (red), P controller (blue), and dq controller (green) is implemented.

## VI. Conclusion

In this paper, the impact of the pole-to-pole DC voltage on the capacitance requirement of the FB YY-MMC has been investigated. It has been found that there exists an optimal pole-to-pole DC voltage that minimizes the capacitance requirement of the converter. Based on this voltage, a design guideline for the FB YY-MMC has been presented. Furthermore, it has been demonstrated that with proper selection of pole-to-pole DC voltage reduction in capacitance requirement for the FB YY-MMC up to 26% with respect to the HB YY-MMC can be achieved.

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