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Abstract

Indium (In) is currently used to fabricate metal bumps on micro-light-emitting diode (Micro-LED) chips due to its excellent physical properties. However, as Micro-LED pixel size and pitch decrease, achieving high-quality In bumps on densely packed Micro-LED chips often presents more challenges. This paper describes the process of fabricating In bumps on micro-LEDs using thermal evaporation, highlighting an issue where In tends to grow laterally within the photoresist pattern, ultimately blocking the pattern and resulting in undersized and poorly dense In bumps on the Micro-LED chip. To address this issue, we conducted numerous experiments to study the height variation of In bumps within a range of photoresist aperture sizes (3 μm −7 μm) under two different resist thickness conditions (3.8 μm and 4.8 μm). The results showed that the resist thickness had a certain effect on the height of In bumps on the Micro-LED chip electrodes. Moreover, we found that, with the photoresist pattern size increasing under constant resist thickness conditions, the height and quality of the bumps significantly improved. Based on this finding, we rationalized the adjustment of the photoresist pattern size within a limited emission platform range to compensate for the height difference of In bumps caused by different resist thicknesses between the cathode and anode regions. Consequently, well-shaped and dense In bumps with a maximum height of up to 4.4 μm were fabricated on 8 μm pitch Micro-LED chips. Afterwards, we bonded the Micro-LED chip with indium bumps to the CMOS chip, and we found that we could successfully control the CMOS chip to drive the Micro-LED chip to display specific characters through the Flexible Printed Circuit (FPC). This work is of significant importance for the fabrication of In bumps on Micro-LED chips with pitches below 10 μm and subsequent bonding processes.

1. Introduction

In recent years, with the deep integration of display technology with emerging industries such as artificial intelligence, 5G communications, and the Internet of Things, the rise of the 'metaverse' concept has led to the emergence of new applications such as Augmented Reality (AR) and Virtual Reality (VR). The advent of AR/VR technologies has transformed human-computer interaction from simple screen viewing and touching to an unprecedented immersive experience [1–4]. In AR/VR technologies, near-eye display devices are the core equipment for conveying virtual information, placing extremely high demands on display technology [5, 6]. Micro-LED, as a new type of display technology, offers advantages over other display technologies, including

high brightness, high contrast, low power consumption, long lifespan, and fast response time [7]. In practical applications, these advantages ensure image clarity under near-eye conditions and reduce motion blur and latency, thereby enhancing users' visual comfort and immersion [8].

Since the concept of Micro-LED was introduced in 2000, it has been over 20 years [9]. In these two decades, Micro-LED display technology has experienced rapid development. Although the luminescence efficiency decreases with the reduction of pixel size due to size effects, and the technical difficulties increase with the reduction of pixel pitch, with the maturation and optimization of various manufacturing techniques, the pixel size of the chip has changed from the original 12 μm to the current 5 μm or even lower [10, 11]. For example, Wang *et al* used an ultralow-damage dry etching technique to fabricate GaN blue micro-LEDs [12–14]. They successfully fabricated a 3.5 $\times$ 3.5 μm^2 GaN blue micro-LED with negligible mesa sidewall nonradiative recombination compared with bulk nonradiative recombination of the epitaxial wafer, using the neutral beam etching (NBE) process [15]. Meanwhile, its pixel pitch has reduced from the original 50 μm to below 10 μm today. Wu *et al* even presented an active matrix micro Micro-LED display with a resolution of 1920 $\times$ 1080 and a high pixel density of 3200 pixels per inch [16]. Although there has been a lot of research on Micro-LED display technology now, how to further reduce pixel pitch and reduce the cost of manufacturing high-resolution Micro-LED screens remains a challenge.

The preparation of metal bumps on Micro-LED chips and the subsequent bonding with the driver chip CMOS are key steps in manufacturing high-resolution displays. There are currently many studies on bonding technology, such as Panigrahi *et al* demonstrated a novel mechanism to increase the diffusion across the bonding interface and also shows the CMOS in-line process flow compatible Sub 100 °C Cu–Cu bonding which is devoid of Cu surface treatment prior to bonding [17]. Zhao *et al* transferred the AlGaInP epitaxial layer onto a silicon substrate using In-Ag bonding technology and epitaxial layer stripping process [18]. The metal bump materials on Micro-LED chips are mainly composed of metals such as Au and Sn [19, 20]. This presents two issues. From a performance perspective, metals like Au and Sn have higher melting points. This places higher demands on our subsequent bonding temperature and pressure. During the bonding process, the Micro-LED chip and the CMOS chip can easily get damaged due to the high temperature and pressure, thereby affecting the performance of the Micro-LED chip [21]. From a cost perspective, metals like Au are also relatively expensive, which is not conducive to the industrialization of Micro-LED displays.

Due to its low melting point (156 °C) and excellent ductility among other physical and chemical properties, In is widely used for electrical interconnection in various semiconductor devices [22, 23]. The most common method for fabricating In bumps is by combining UV lithography with thermal evaporation. However, during the evaporation process, besides the vertical deposition of In in the pattern formed after lithography, In also grows horizontally within the pattern. As a result, the diameter of the pattern gradually decreases, leading to a situation where the evaporated In can no longer be deposited on the metal electrodes. At this point, even if the thickness of the surface indium film increases, the height of the indium column on the metal electrodes will not increase. Moreover, due to the significant size difference between the pattern at the peripheral marking location and the pattern in the pixel area, there is a substantial height difference between the In height at the marking location and the indium height in the pixel area. This is likely to cause some pixel areas of Micro LED chips unable to bond with CMOS, resulting in an insufficient bonding strength between the two chips and easy separation.

Currently, some articles have proposed solutions to the problem of insufficient bump height caused by In lateral growth blocking photolithography patterns. For instance, by cyclically using the methods of thermal evaporation and ion etching, the In blocking the photolithographic pattern is continuously etched away and re-evaporated, ultimately obtaining bumps of the desired height on the readout circuit of the infrared detector. There is also a method of two-step lithography and one-step etching, in which an In film is evaporated on the infrared detector readout circuit after the first step of lithography, and the position where the bump is to be formed is protected by the photoresist. The other parts are etched to obtain the required bump [24]. Both methods achieve the desired In bumps on the infrared detector readout circuit through etching. However, when trying to utilize the aforementioned method to fabricate high-quality In bumps on Micro-LED chips with smaller pixel pitch and higher densities, various other challenges will arise. Firstly, for the former method, repeated etching might significantly impact the surface morphology, quality, and uniformity of the bumps we require, introducing numerous unstable factors to the subsequent bonding process. As for the latter, the structure of small Micro-LED chips is more complex, and there's also a certain warping issue. This makes it challenging to form a uniform positive photoresist pattern on the indium film with poor flatness. For complex and high-density Micro-LED chips, we should simplify the process as much as possible. Continuously complicating certain process steps not only presents more challenges but can also adversely affect subsequent process steps.

This article mainly discusses the challenge encountered during the preparation of In bumps on 8 μm pitch Micro-LED chips, where indium grows laterally within the photoresist pattern, ultimately clogging it and

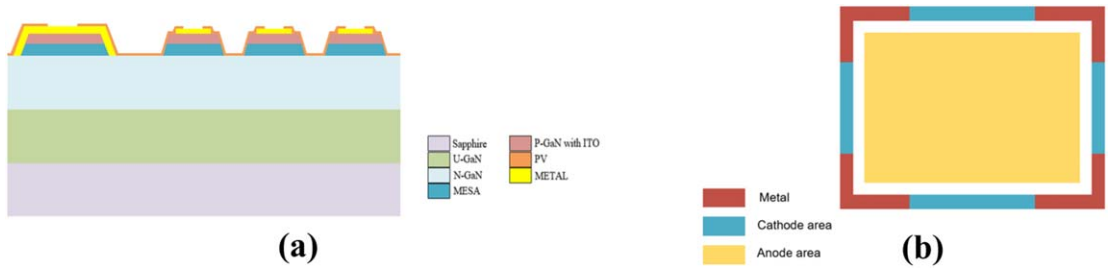

Figure 1. (a) The structure diagram of the Micro-LED chip; (b) The layout diagram of the Micro-LED chip.

resulting in undersized and poorly dense In bumps on the Micro-LED chip electrodes. To address this issue, the article utilized existing Micro-LED chips and conducted extensive experiments to study the effect of different photolithography aperture sizes and resist thicknesses on the height of In bumps. The results showed that the resist thickness had a certain impact on the height of In bumps on Micro-LED chip electrodes, and with the increase in photolithography pattern size under constant resist thickness, the height and quality of the bumps improved significantly. Based on this conclusion, the article adjusted the size of the photoresist mask area in the cathode and anode regions to control the height of In bumps after thermal evaporation. Experimental results demonstrated that this method could produce dense In bumps with a maximum height of 4.4 μm on high-density Micro-LED chips with an 8 μm pitch. Moreover, during the bump fabrication process, when faced with the issue of unequal heights between the cathode and anode metal bumps under the same conditions, we utilized the Indium (In) blockage phenomenon. By slightly increasing the size of the cathode photolithography pattern, a certain degree of height compensation was achieved for the In bumps on the cathode side, ensuring a consistent height between the cathode and anode In bumps. Afterwards, we bonded the Micro-LED chip with indium bumps to the CMOS chip, and we found that we could successfully control the CMOS chip to drive the Micro-LED chip to display specific characters through the FPC. Compared to existing articles on Micro-LED display screen fabrication, this article focuses on the growth process of In bumps, providing a detailed analysis of height variations within the 3 μm $-$7 μm photolithography aperture range. This work is significant for the fabrication and bonding of In bumps on Micro-LED chips with pitches below 10 μm.

2. Experiment procedure

2.1. Lithography

The chip used in this step is a common cathode Micro-LED chip with a resolution of 1920 $\times$ 1080 and a pixel pitch of 8 μm. In contrast to other Micro-LED chips, we first fabricate electrodes and then fabricate the insulating layer during the graphic preparation process. Its chip structure is shown in figure 1(a). The layout of the Micro LED chip is depicted in figure 1(b), where the central part represents the anode region, and there are four squares around it representing the cathode region, connected together by metal. Firstly, the Micro-LED chip undergoes thorough cleaning. The cleaning process involves initially rinsing with deionized water to remove surface particles, followed by the use of acetone and isopropanol to eliminate organic matter on the chip. After cleaning, a spin-coater is used to apply a 7 μm thick layer of negative photoresist AZ 2070 onto the chip surface. This is then baked at 100 °C for 50 s. Subsequently, the chip is exposed to ultraviolet light at 365 nm with intensities of 150 mJ/cm^2 and 365 nm with intensities of 220 mJ/cm^2. The purpose of the second exposure is to solidify the photoresist at the marked areas. After exposure, it's baked again at 100 °C for 50 s. This is followed by a 40 s development, resulting in a photolithography pattern on the chip surface with an aperture size of 5.3 μm and a distance from the electrode surface to the resist surface of 4.7 μm.

2.2. Thermal evaporation

After photolithography, the chip is treated with an oxygen plasma for 2 min to remove any residual photoresist and impurities from the pattern, enhancing the adhesion of the subsequently evaporated metal to the surface electrodes of the Micro-LED chip. The chip is then placed on the sample stage of the evaporation equipment. The stage is heated to 75 °C and maintained for 5 min to remove potential surface contaminants. Once the stage cools to room temperature, the heating process begins for the 10 g of In in the crucible. During the heating process, a film thickness monitor is used to check the evaporation rate of In. By controlling the heating current, the evaporation rate is maintained at around 10 Å s^{-1} to prevent issues related to insufficient density caused by a too high evaporation rate. Once all 10 g of In has been evaporated, the evaporated chip is immersed in a stripping solution for 24 h for photoresist removal.

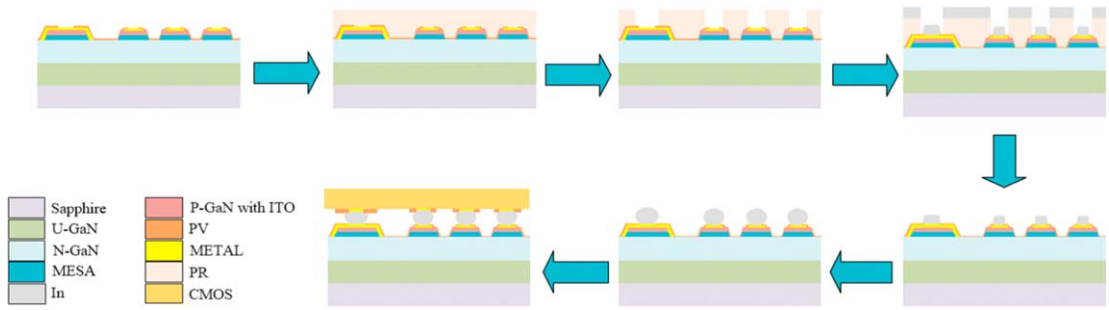

Figure 2. Process from In bump fabrication to bonding.

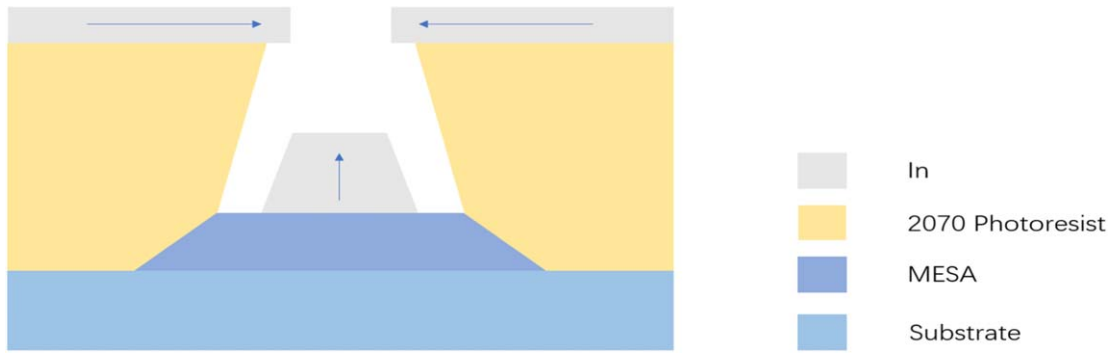

Figure 3. In bump growth process.

2.3. Reflow and bonding

After the lift-off process, we can obtain indium (In) bumps on the electrode surface of the Micro-LED chip that meet our size and height requirements. However, to achieve superior bump performance and enhance device reliability, a reflow process for the prepared In bumps is essential. The Micro-LED chip is reflowed in an environment with formic acid at 210 °C. After reflow, the Micro-LED chip, with its In bumps, is bonded to a CMOS chip under conditions of 180 °C temperature, 60 kg bonding force, and for a duration of 600 s. The entire process for In bump preparation and bonding is illustrated in figure 2.

2.4. Characterization

The uniformity and dimensions of the photolithography patterns and the bumps after the lift-off process were characterized using an optical microscope and a 3D measurement laser microscope (LEXT OLS4100). Additionally, the surface and cross-sectional morphology of the In bumps were observed using a Scanning Electron Microscope (SEM) assisted by a Focused Ion Beam (FIB; Helios G4 CX).

3. Results and discussion

3.1. The influence of the size of photolithography patterns on In bump fabrication

During the fabrication process of high-density Micro-LED In bumps, we utilize a thermal evaporation method. The specific procedure involves heating an evaporation boat inside a vacuum chamber, which causes In particles to adhere to our chip's electrodes, thereby forming the bumps. In the formation process of these bumps, In particles not only grow vertically on the chip electrodes but also continuously deposit on, and spread horizontally across, the surrounding photoresist. Consequently, the aperture of our photolithography pattern gradually reduces due to the horizontal growth of the In particles. This leads to the photolithography pattern eventually being completely blocked by the In film layer, preventing the In bumps on the chip electrodes from reaching the height required for our bonding. The growth schematic of the In bumps during the evaporation process can be seen in figure 3.

Through extensive experiments, it can be observed that the horizontal growth of In particles in the photolithography pattern during the evaporation process is inevitable. To determine the appropriate photolithography pattern size for fabricating In bumps on Micro-LED chips, we conducted a series of

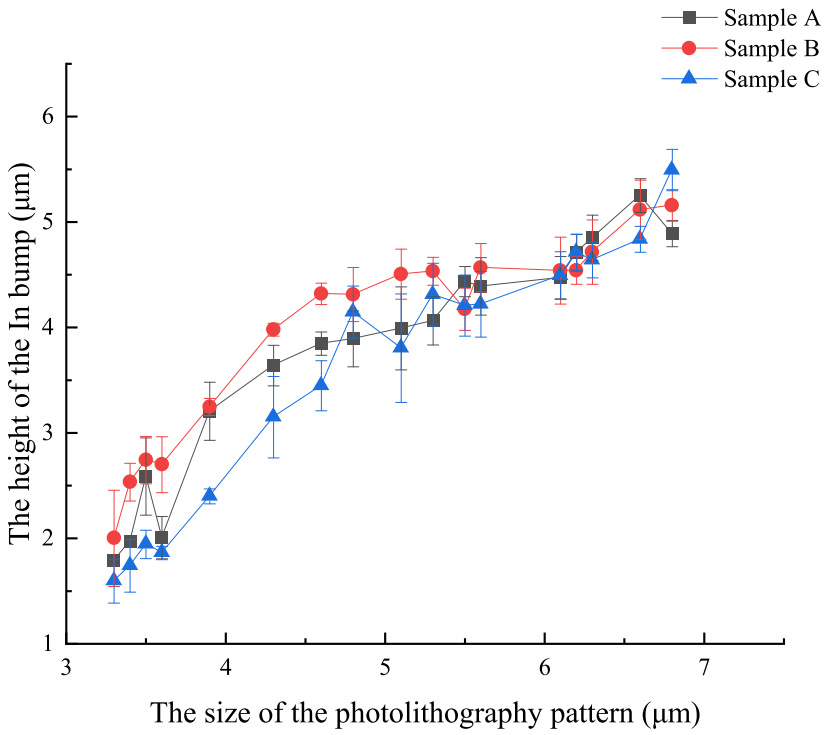

Figure 4. Relationship between the size of the photolithography pattern and the height of the In bump for samples A, B, and C.

experiments on gold-plated silicon wafers. We used AZ 2035 photoresist to achieve thicknesses of 3.8 μm and 4.8 μm on the gold-plated silicon wafers, approximating the actual distance from the Micro-LED chip electrode to the surface of the photoresist. Subsequently, through exposure and development steps, we formed a range of photolithography patterns with apertures ranging from 3.0 μm to 7.0 μm on the gold-plated silicon wafers. The wafers were then placed in the evaporation equipment and added with 10 g of In for the fabrication of In bumps. For this experiment, two samples were prepared: Sample A and Sample B, both with a photoresist thickness of 3.8 μm, and Sample C with a thickness of 4.8 μm. The final relationship between the photolithography pattern and the height of the In bump is shown in figure 4. From figure 4, it can be seen that as the aperture increases, the height of the In bump continues to rise. Based on these results, to further verify that the insufficient height of the In bump at smaller apertures is due to the horizontal growth of In particles, we created a photolithography pattern with an aperture size of 3.6 μm on the Micro-LED chip. It was then evaporated under conditions of 10 g In. After evaporation, it was directly observed under FIB. The observation results are shown in figure 5(a), where we can see that the photolithography pattern has been essentially blocked by the In film, resulting in a lower and less dense bump height on the electrode.

From the aforementioned analysis, we can deduce that the smaller the pattern formed after photolithography, the lower the subsequent evaporated In bump height. However, on the Micro-LED chip, this doesn't imply that we can indefinitely increase the size of the photolithographic pattern. As the pattern enlarges, the underlying aperture also continually grows, making it more likely for the In metal to bridge between adjacent pixels, preventing individual pixel operation. The result is illustrated in figure 5(b). Therefore, within a certain mesa range, it's crucial to select the right photolithographic aperture size. Based on numerous experiments, we created a photolithographic pattern with a diameter of 5.2 μm on the high-density Micro-LED chip. After evaporation, the height of the In bump reached approximately 4.4 μm. The evaporation outcomes are shown in figures 5(c) and (d).

3.2. Height compensation of In bumps at the cathode position

In the process of fabricating Micro-LED chips, there often exists an issue where the anode and cathode have unequal heights. This introduces many challenges for our bonding. Although we have addressed this by elevating the cathode using a platform, in subsequent bumping processes, discrepancies in the spin-coating plane and variances in the structure between some chip cathodes and anodes still result in a noticeable height difference between the cathode In-bumps and the anode In-bumps.

To address this issue and ensure a smoother bonding process in the future, we exploited the horizontal growth of In within the photolithography pattern. While maintaining the anode photolithography pattern

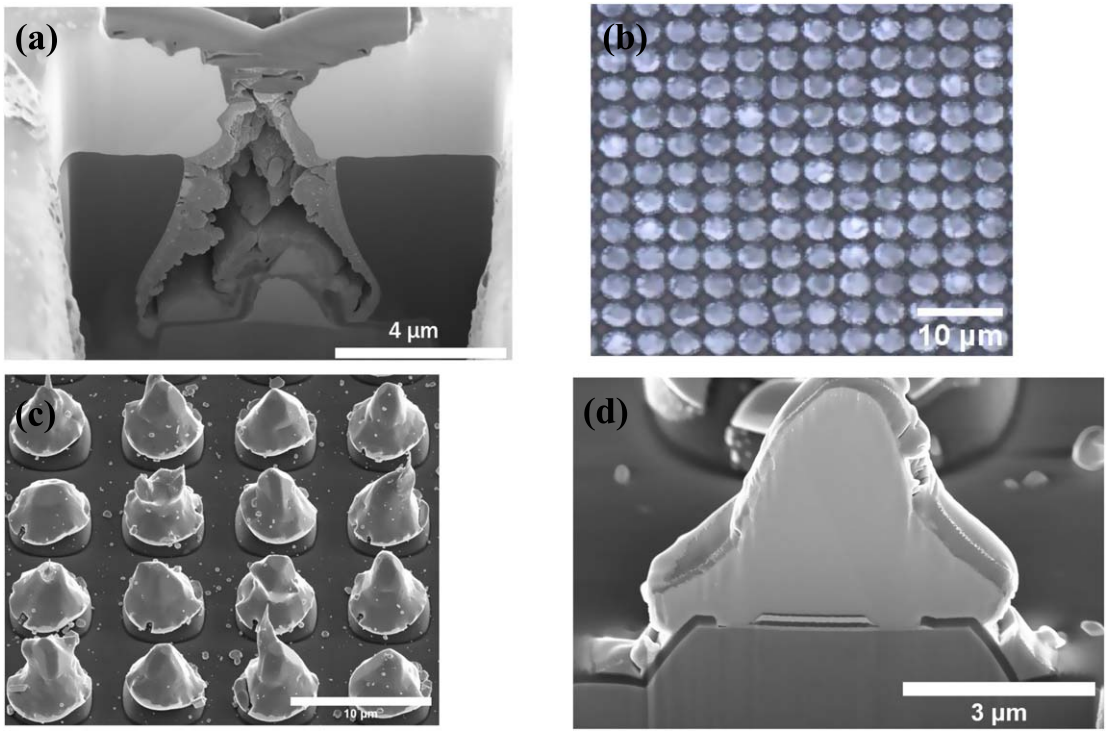

Figure 5. (a) Cross-sectional view of In bump after evaporation with a too small aperture; (b) In bumps connected due to excessive aperture size after evaporation; (c) Image of In bump under a 5.2 μm lithography pattern size; (d) Cross-sectional image of the In bump on a single pixel.

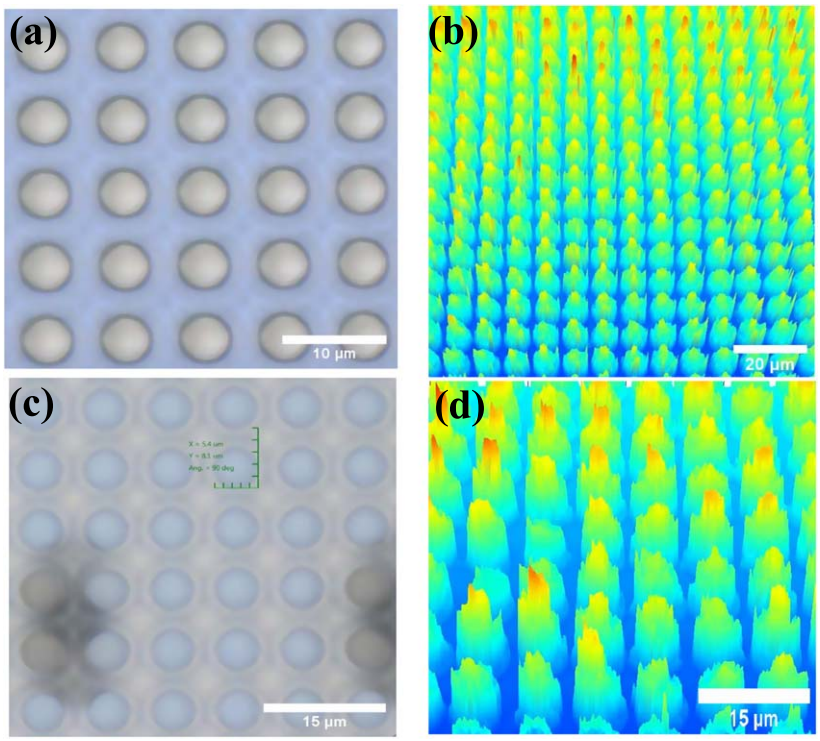

Figure 6. (a) Image of anode lithography pattern size at 4.9 μm; (b) Image of anode bump height at 3.0 μm; (c) Image of enlarged cathode lithography pattern size at 5.4 μm; (d) Image of cathode bump height at 3.2 μm.

aperture unchanged, we increased the aperture of the cathode photolithography pattern. This allowed us to compensate for the height of the In bumps at the cathode location, thus bringing the heights of the cathode and anode In bumps closer together. The results are illustrated in figures 6(a)–(d).

Figure 7. The image of the Micro-LED display shows specific characters.

3.3. Bonding results

After preparing the In bumps on the Micro-LED chip, we subjected them to reflow to remove surface oxides and improve the surface morphology of the In bumps. To successfully drive the Micro-LED chip, several additional processing steps are required after the reflow of the bumps: thermal compression bonding between the Micro-LED chip and the CMOS chip, underfill of the bonding interface, and wire bonding between the CMOS chip and the Flexible Printed Circuit (FPC). The main purpose of underfill is to solidify the bonding interface to prevent bond point fractures during subsequent processes, while wire bonding is necessary for driving the pixels on the Micro-LED chip through CMOS control via the FPC. After completing the above steps, we proceeded with powering on the Micro-LED chip for observation. The observation revealed that after indium bump bonding between the Micro-LED chip and the CMOS chip, a large area of pixels could not be driven. We believe that the possible reason for this result is the soft material of indium, which may cause interconnection between adjacent pixels' indium bumps during the bonding process, ultimately leading to abnormal operation of the micro-LED display. To further validate the feasibility of indium bump bonding on high-density Micro-LED chips, we replaced the bump material on the CMOS chip with Au. The results showed that the Micro-LED chip could display specific characters controlled by the FPC, as shown in the figure 7. Although there is still room for improvement in our current results, we can still see from the above experimental results that it is feasible to fabricate high-resolution Micro-LED displays using the approach described in the paper. We believe that further optimization of the results shown in figure 7 can be achieved through improvements in the bonding process.

4. Conclusion

This study focuses on the fabrication of high-density In bumps on Micro-LED chips with an 8 μm pixel pitch through thermal evaporation and the subsequent reflow and bonding with CMOS chips. Initially, photolithography and thermal evaporation were used to form In bumps on the Micro-LED chips. During the evaporation process, to address the issue of the lateral growth of In leading to blockage of the photolithography pattern, we adjusted the photolithography aperture size to its maximum within a confined range. This ensures the height meets reflow requirements while avoiding excessively large areas that could cause short circuits between pixels. Additionally, during the photolithography process, a second exposure was introduced to mask the pixel area, leaving the peripheral markers exposed to ultraviolet light. This prevented the issue of insufficient bonding due to the excessive height of the In metal around the edges. After the fabrication of the In bumps, they underwent reflow and were then bonded to the CMOS chip. Results indicated that the In bumps, fabricated on the 8 μm pixel pitch Micro-LED chips via thermal evaporation, exhibited good uniformity and compactness. Moreover, after reflowing the Micro-LED chips fabricated with indium bumps and bonding them to CMOS chips, the Micro-LED chips can display the characters we set.

Based on the comprehensive analysis of the experimental results, we have achieved our experimental objectives to a large extent. Reflecting on the entire experimental process, there is still room for improvement in the results we have obtained. In future research, we will further optimize our experimental procedures to achieve a better yield for the fabrication of 8μm pitch Micro-LED displays. Additionally, we will continue investigating the bonding between Micro-LED chips and CMOS chips with In bumps. Despite certain issues encountered in previous experiments, we believe that these results can be improved through optimization of the bonding process. We are confident that this work potentially paves the way for further cost reductions in high-density Micro-LED displays, pushing Micro-LED technology a step closer to industrialization.

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Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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