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Integration of BCH Encoder in SiGe Driver System

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Abstract: We implement a 56-Gbps BCH encoder in a 130-nm SiGe technology suitable for VCSEL drivers for short-reach optical communication. We show that encoder-driver integration can reduce total power consumption in addition to reducing manufacturing cost.
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1. Introduction

Short fiber-optic communication links commonly based on vertical-cavity surface-emitting lasers (VCSELs) are essential components of global communication systems. To push the data rate further and maintain the same bit error rate (BER), forward error correction (FEC) will likely be required [1], which introduces hardware overheads. Suitable FECs, however, can reduce energy consumption for the whole fiber system [2]. This is because improved BER performance due to FEC relaxes the optical modulation amplitude (OMA) requirement at the receiver, resulting in a more energy-optimal operating point for the driver and VCSEL. Fougstedt et al. [3] demonstrated a low-power BCH FEC in a 28-nm CMOS process technology which offered a 25% total system power reduction.

Although CMOS technology is key to area and power efficiency for digital circuits, silicon-germanium (SiGe) BiCMOS technology with its mix of MOSFET and BJT transistors has emerged as the common choice for high data rate VCSEL drivers [4]. Despite SiGe is not offering the same CMOS logic density, it is still possible to integrate limited digital functionality, such as a FEC encoder, close to the driver with low hardware overhead, improving encoder-driver communication and lowering manufacturing cost. Therefore, we investigate the use of parallel Bose-Chaudhuri-Hocquenghem (BCH) 56-Gbps encoders on a 130-nm SiGe BiCMOS technology used for VCSEL drivers. With a power estimation model based on [5–7], we demonstrate that the introduction of a SiGe encoder can in fact reduce total system power consumption.

2. Encoder and Driver in SiGe Technology

Binary BCH(n,k,t) code is an important subclass of BCH code in Galois fields [8] which can correct at most t random errors, where n is block length and k is message length. Since the code is linear, a parallel BCH encoder [9] component can be built by $U(T+m) = F^m \cdot (U(T)+X(T+m))$, enabling low latency and high throughput. Here, $U(T+m)$ and $U(T)$ are the states of the remainder registers at time T and $T+m$, respectively, $X(T+m)$ represents the input messages of length p_{in}, where $p_{in} = m$, at time $T+m$, and F^m is the generator matrix. Since exclusive OR (XOR) gates can realize the field's addition, the encoder is a symmetric XOR tree based on F^m. An encoder with a high throughput can be built by arranging the encoder components in a p_{cp} parallel computing configuration.

Digital logic, such as FEC circuitry, benefits from implementation in an advanced CMOS process node. Since it offers excellent energy efficiency, CMOS is a common choice for drivers with moderate data rates. However, it is challenging to provide the required swing for the driver with CMOS; a problem which is exacerbated in harsh environments with high temperatures. SiGe, on the other hand, offers superior drive capability, higher supply, and higher switching speeds. The 130-nm SiGe technology used here has BJTs with an f_T of around 300 GHz, which paves the way for very high data rate transmission. The 1.2-V CMOS logic of this SiGe technology is not as dense as in state-of-the-art CMOS technologies. However, due to the simplicity of the FEC encoder logic, the encoder and driver can be integrated into the same technology, making this a promising approach.

3. Power Estimation Model

Introducing FEC can improve the BER performance, resulting in a lower OMA requirement at the receiver. This in turn relaxes the requirements on the VCSEL, possibly enabling a reduction of the transceiver's total power consumption. Szczerba et al. [3] proposed a post-FEC BER model with a VCSEL operating at 20 Gbps, which assumes that the laser and driver consume the same power, resulting in a decrease on the receiver OMA of 1 dB. To evaluate an operation at 56 Gbps, we propose post-FEC BER models based on the 55-Gbps VCSEL data from [10]. To minimize the power overhead of the encoder, we implement BCH codes with $t = 1$, also known as Hamming codes. Figure 1 shows that at 55 Gbps, the possible OMA reductions improve to around 2 dB for a BER of 10^{-12}. The 2 dB reduction on the receiver side will lead to the same reduction on the transmitter side. Hence, to save power, the introduced power of FEC P_{fec}, including the encoder and decoder, must be less than the reduction of total fiber system power ΔP_{total} before introducing FEC. In this paper, three ΔP_{total} cases based on the results [5–7] are investigated for an OMA reduction of 2 dB. As the receiver does not have a VCSEL-dependent voltage swing requirement, we use the result from [3] with an energy per bit (EPB) of 0.025 pJ/bit to estimate the decoder power in a 28-nm CMOS process technology.

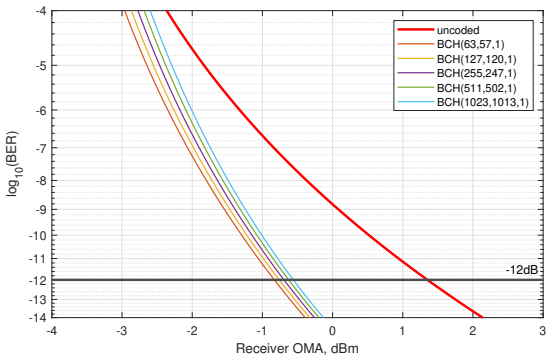

Fig. 1: Post-FEC BER as a function of the receiver OMA at 55 Gbps

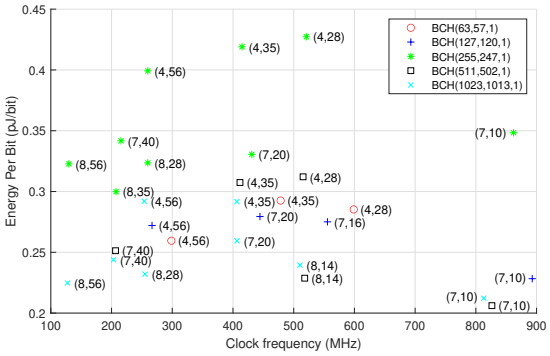

Fig. 2: Encoder EPB for different configurations in (p_{in}, p_{cp}) parallelism

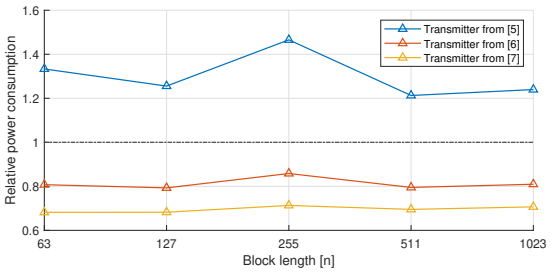

Fig. 3: Relative system power consumption after adding FEC, based on minimal-EPB configuration for each n

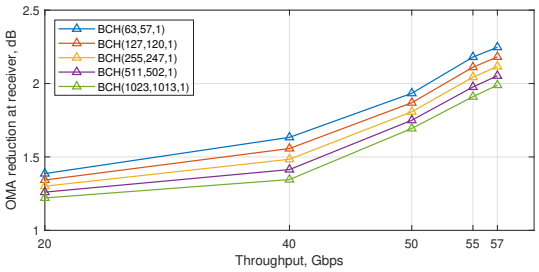

Fig. 4: Receiver OMA reduction as a function of different throughput of VCSELs

4. Results and Analysis

To determine the configuration with the lowest power consumption at an overall throughput of 56 Gbps, we implemented various combinations of block length n, input parallelism p_{in} and computing parallelism p_{cp}. Figure 2 shows that the configuration BCH(511,502,1) with $p_{in} = 7$ and $p_{cp} = 10$ has the lowest EPB of around 0.21 pJ/bit. The performance of the encoder is significantly influenced by the logic depth and maximum fanout features of F^m, which are denoted as $\lceil \log_2(count_{row}) \rceil + 1$ XOR gates and $count_{col}$, respectively. Here, $count_{row}$ and $count_{col}$ are the summation of elements for each row and column. The above lowest power candidate has the shallowest logic depth (three logic levels) and the lowest maximum fanout (three). The code rate k/n also influences the EPB, since a lower code rate will need a higher clock frequency or parallelism to maintain the throughput.

Figure 3 shows the relative power dissipation of a system *with FEC* over a system *without FEC* for different FEC block lengths under the 2-dB OMA relaxation. Clearly, introducing FEC to an ultra-low power transmitter system [5] will increase total power consumption. However, FEC can help to reduce total power, when the transmitter consumes more power, such as in high-throughput transceivers. Figure 3 shows that the best FEC candidate offers a 32% power saving or a 60-mW power reduction for the case with the highest transmitter power consumption. The OMA reductions in Figure 4 assume the VCSEL data in [2,10,11]. As we can see from this figure, introducing FEC becomes more beneficial when the throughput increases. Furthermore, designing a decoder in a more advanced CMOS technology will also help to reduce the power.

In conclusion, it is an advantage in terms of encoder-driver communication and manufacturing cost to integrate digital encoder circuitry next to the driver. Here, we showed that integrating a 56-Gbps BCH encoder in a 130-nm SiGe driver system also can reduce the system's total power consumption and that this integration becomes more beneficial in higher throughput systems.

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