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A 25-40 GHz Three-Way Power Amplifier with No Load Modulation Achieving Broadband Deep Power Back-Off Efficiency Enhancement

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***Abstract*— This paper presents a millimeter-wave (mm-Wave) power amplifier (PA) topology that avoids the trade-off between bandwidth and load modulation. The proposed topology uses three PA paths and can achieve efficiency enhancement at power back-off without load modulation. With a 100 MHz 5G NR FR2 1-CC 64-QAM signal, this PA achieves P_{AVG} and PAE_{AVG} of 6.45 - 12.61 dBm and 5.9 - 16.4% from 25 - 40 GHz, respectively. With a 200 MHz, signal, P_{AVG} and PAE_{AVG} are 5.58 - 11.1 dBm and 4.8 - 13.3%, respectively.**

***Keywords*— 5G, CMOS, Mm-Wave, Power amplifiers.**

I. Introduction

The use of complex and spectrally efficient modulation schemes (e.g., 64-QAM and higher) is a pre-requisite for multi-Gbps data rates in next-generation wireless communication systems. However, these signals have a high peak-to-average power ratio (PAPR) requiring the power amplifier (PA) to often operate in power back-off (PBO). For example, a 5G NR FR2 1-CC 64-QAM signal has PAPR of approximately 9.6 dB, which is often considered as "deep" PBO. This signifies the importance of deep PBO efficiency enhancement for advanced PA designs [1]. Furthermore, different countries around the world are allocated different FR2 bands, so a broadband PA design covering all FR2 bands will greatly benefit the RF frontend flexibility and cost.

Recently, there have been multiple PA architectures reported that address PBO efficiency enhancement. The load-modulated balanced amplifier (LMBA) is both wideband and efficient at PBO but is difficult to implement on chip due to the required large quadrature coupler and the need for additional baluns to interface this coupler with differential PAs [2]. The Doherty architecture achieves PBO efficiency enhancement by using an auxiliary PA path to perform active load modulation. This architecture requires a $\lambda/4$ impedance inverter, which inherently limits the load modulation bandwidth. In addition to bandwidth limitations, load modulation also results in degraded AM-AM and AM-PM linearity when deviating from the center frequency [3]. Moreover, deep PBO efficiency enhancement demands multi-way Doherty PAs with high impedance transformation ratios and large ranges of load modulation, which further degrades the output passive efficiency while also severely limiting bandwidth and linearity [4], [5], [6]. Recently, a broadband parallel-series architecture has been reported [7].

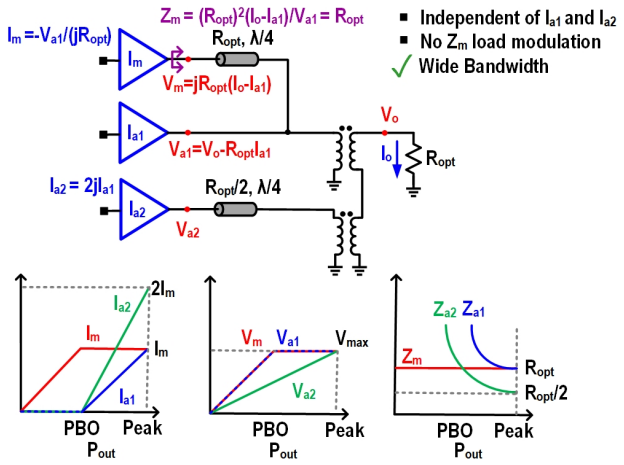

Fig. 1. Schematic of the non-load modulated PA output network.

However, this design is not instantaneously broadband since it requires mode switching. Furthermore, this design exhibits large gain variations across the operating frequency, and requires a large area overhead due to the four PA paths.

Yet another way of achieving broadband PBO efficiency enhancement is to remove the load modulation entirely [8], [9]. The distributed efficient PA (DEPA) architecture utilizes a unique auxiliary PA control and combiner design, resulting in constant PA load impedance vs PBO. This removes the bandwidth limitation due to the load modulation in all load-modulated PAs. However, the architecture in [8] is challenging for CMOS designs, as the required six auxiliary paths are extremely area intensive and complex to coordinate. Additionally, the Main PA is placed furthest from the output, incurring the full loss of the output network, thereby reducing the PA efficiency particularly at deep PBO. In [9], the same no load modulation concept is demonstrated with only two auxiliary paths, but this design has a much smaller fractional bandwidth (33%) compared to [8] (71%).

To address these challenges, this paper presents a new PA topology with no load modulation that is simultaneously broadband and efficient at deep PBO. It uses only two auxiliary PAs and one Main PA, drastically reducing the complexity compared to [8], and has a greater -3dB S_{21} fractional bandwidth (45%) compared to [9].

* equal contribution

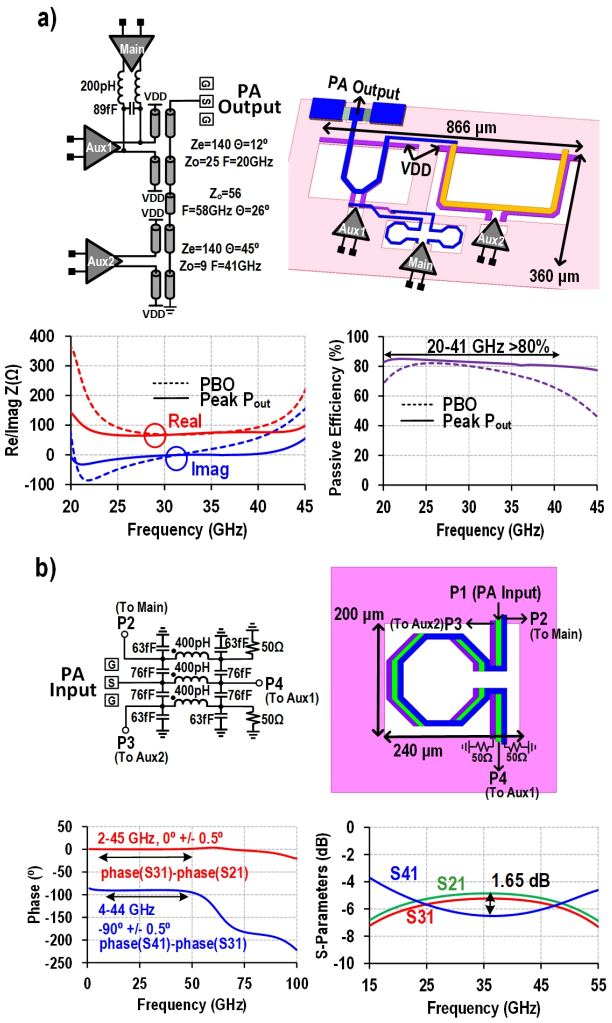

Fig. 2. (a) EM model of the output combiner, simulated passive efficiency, and simulated impedance presented to the Main PA at PBO and peak P_{out}. (b) EM model of the 1:3 quadrature coupler with simulated phase shift and power splitting.

II. Proposed Non-Load Modulated Architecture

As seen in Fig. 1, the proposed PA architecture uses three amplifier paths, which are the Main, auxiliary 1 (Aux1), and auxiliary 2 (Aux2). The Main and Aux1 are parallel combined, then both are series combined with Aux2, with a Main:Aux1:Aux2 sizing ratio of 1:1:2. At PBO, only the Main is turned on, which sees an impedance of R_{opt}. As the input drive increases, Aux1 and Aux2 are turned on at the same time. At peak P_{out} Aux1 and Aux2 see impedances of R_{opt} and $\frac{R_{opt}}{2}$, respectively. However, different than a Doherty PA, here the Main PA sees a constant load all the time. Shown in Fig. 1, the Main sees a Z_m which is independent of the Aux currents I_{a1} and I_{a2}. This is due to the fact that the current and voltage swing at the drain of the Main PA reaches their maximum at PBO, which also ensures PBO efficiency enhancement.

The 3D electromagnetic (EM) model of the output combiner is shown in Fig. 2. For the on-chip realization of this output combiner, low loss coupled-line based baluns are used

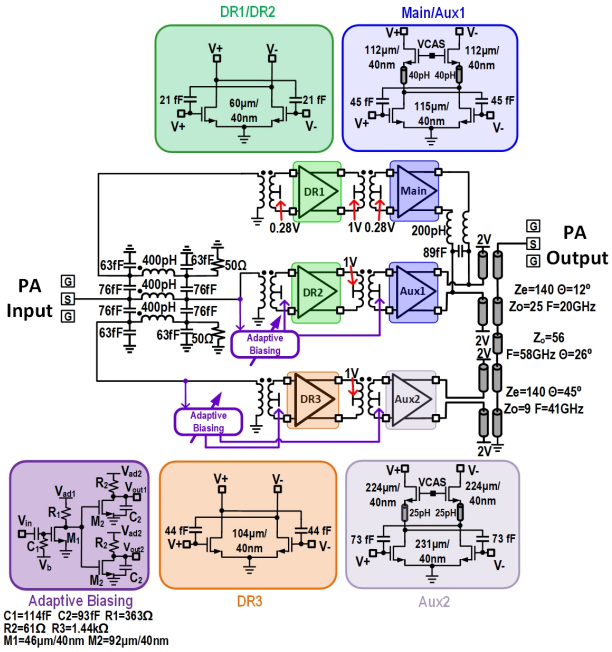

Fig. 3. Full schematic of the proposed PA.

in series to connect the Aux paths, and the Main is connected using an LC-based $\lambda/4$ line. The resulting Main PA load impedance stays almost constant at both peak power and PBO from 25-40 GHz, verifying the absence of load modulation (Fig. 2(a)). Additionally, the passive efficiency of the output network is shown across frequency and is >80% at peak P_{out}. Notably, this output network has the Main path much closer to the load compared to that of the DEPA implementation in [8], enabling a higher passive efficiency.

On the other hand, the input network for this PA needs to achieve proper three-way power splitting, phase shifting, and input matching across the full bandwidth. Shown in Fig. 2(b), a 1:3 coupled-inductor quadrature coupler is used to achieve this goal. This coupler fits into a single inductor footprint. Compared to the input networks of other three-way Doherty PAs, which often utilize a complex cascade of power dividers, 90° couplers and lengthy transmission lines ([5], [6]), the proposed input network is very compact. By taking the Main PA as the reference, the simulated phases of the input to Aux1/Aux2 are -90°/0° over 4-44 GHz with a maximum deviation of only $\pm$ 0.5°. Furthermore, the network also shows the split of input power to the three paths with a maximum difference of 1.65 dB across 25-45 GHz.

III. Circuit Schematic

A schematic of the full circuit is shown in Fig. 3. Each of the three paths consists of a driver and a power stage. First, the RF signal is appropriately split and phase shifted by the 1:3 quadrature coupler at the input. Then, a transformer balun is used to convert the single-ended signal to differential. Both the driver and power stage are differential with capacitative neutralization. The power stage is cascoded so that a higher

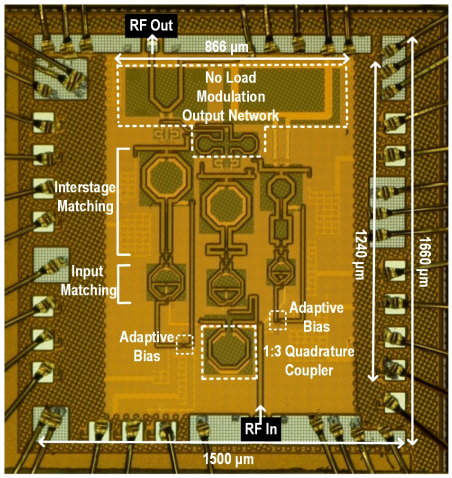

Fig. 4. PA die photo. The total area is 2.49 mm^2, and the core area is 1.07 mm^2.

voltage supply can be used. An inductor between the common source (CS) and common gate (CG) stages is used to absorb the interstage parasitic of the transistors, ensuring that the current from the CS device is transferred to the CG device with minimal loss.

An adaptive biasing circuit is used on both Aux paths, which serves a few purposes. First, at deep PBO when only the Main path is on, both the driver and the power stage of the Aux1 and Aux2 paths are kept off to reduce unnecessary DC power consumption. Second, the adaptive bias ramp-ups the V_{gs} of the Aux paths so that at peak P_{out} all PA paths have the same gate bias, maintaining the drive profiles described in Fig. 1. The simulated bandwidth of the adaptive biasing circuit is approximately 2.2 GHz, which is sufficient for supporting signals with modulation bandwidth up to around 700 MHz.

IV. Measurement Results

The PA is fabricated in the GF 45nm RFSOI CMOS process, and the chip photo is shown in Fig. 4. The total area including pads is 2.49 mm^2, with a core area of 1.07 mm^2. The die is attached to a PCB and wirebonded. RF input/output are measured by on-chip probing. The driver stage/power stage use a V_{DD} of 1V/2V, respectively. The measured s-parameters, stability factor, and large signal continuous-wave (CW) results across frequency are shown in Fig. 5.

Shown in Fig. 5(a), the S_{21} -3dB bandwidth is 25 - 41 GHz, with S_{11} < -10dB from 25 - 30 GHz and 35 - 50 GHz. From 30 - 35 GHz, the S_{11} is <-8.7 dB. Additionally, the K-Δ stability factor is shown from 100 MHz to 50 GHz, showing unconditional stability across all frequencies (Fig. 5(b)). With a large-signal CW test, the PA achieves an OP_{1dB} of 18.7 - 22.2 dBm, PAE_{OP1dB} of 20.9 - 37.6%, power gain of 12 - 15 dB, and $PAE_{9dB,PBO}$ of 8.8 - 18.2% from 25 - 40 GHz (Fig. 5(c)-(g)). Efficiency enhancement at deep PBO is clearly shown across frequency, verifying the simultaneous broadband and deep PBO efficiency enhancement capabilities.

Furthermore, the PA is tested using 5G NR FR2 1-CC 64-QAM signals with bandwidths of both 100 MHz and 200

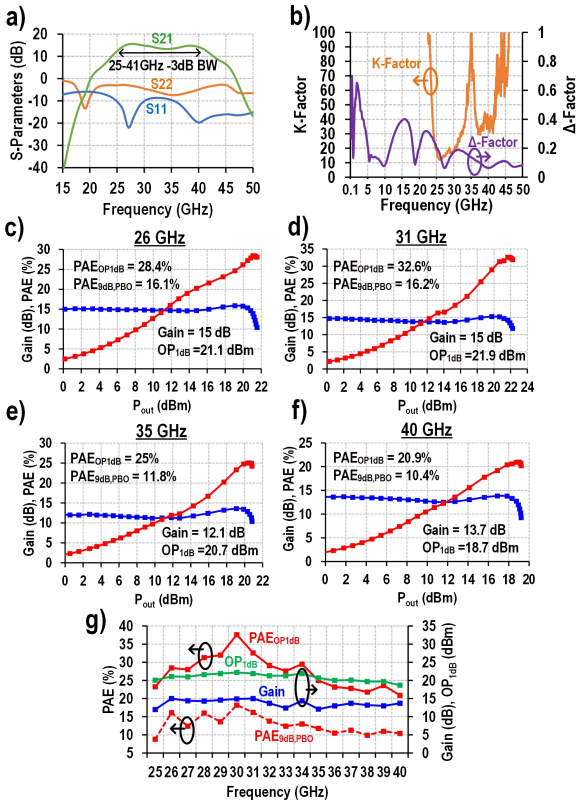

Fig. 5. Measured results for (a) S-parameter (b) k-factor and (c) - (g) large signal CW from 25 - 40 GHz.

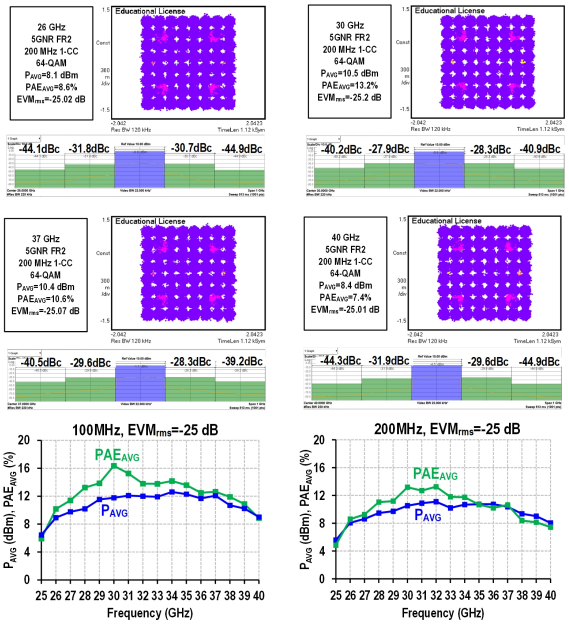

Fig. 6. Measured results with modulated signals.

MHz (Fig. 6). With a 100 MHz signal, the PA achieves an average P_{out} and PAE of 6.45 dBm - 12.61 dBm and 5.9% - 16.4% at an EVM_{rms} of -25 dB from 25 - 40 GHz. With a 200 MHz signal, the PA achieves an average P_{out} and PAE

Table 1. Comparison with PBO efficiency enhancement PAs from 20 - 40 GHz.

	This Work				Ma [5] ISSCC 2022	Zhang [6] JSSC 2023		Mortazavi [10] JSSC 2022	Hu [11] ISSC 2017			Chappidi [12] VLSI 2019			Huang [13] ISSCC 2021				Liu [7] JSSC 2023			
Technology	45nm SOI CMOS				55nm CMOS	40nm CMOS		40nm CMOS	130nm SiGe			65nm CMOS			45nm SOI CMOS				45nm SOI CMOS			
Architecture	3-Way Parallel-Series with No Main PA Load Modulation				Transformer-based 3-way Parallel -Series Doherty	Coupled-Inductor-based 3-Way Doherty		Digital Polar TX	Multiband Doherty			Broadband Doherty-Like Multi-Port			Continuous Coupler				Coupler Based Parallel-Series Doherty			
Supply (V)	2				2.4	1.8		1	1.5			1.1			2				2			
-3dB S_{21} BW (GHz)	25-41 (48%)				25.9-32.6 (23%)	35.9-39.5 (10%)		24-31 (26%)	23.3-39.7 (52%)			N/A			N/A				N/A			
Core Area (mm^2)	1.07				0.54	1.4		0.55[b]	1.76(incl. pads)			1.35 (incl. pads)			0.62				1.55			
Freq (GHz)	26	30	37	40	28	38		29.5	28	37	39	28	37	39	26	32.5	37.5	40	26	33	38	40
Gain (dB)	14.5	14.9	13.7	13.7	16.1	15		N/A	18.2	17.1	16.6	15*	16*	17.5*	11*	16*	N/A	N/A	12*	15*	12*	13*
P_{SAT} (dBm)	21.4	22.6	20.2	19.1	25.5	18.9		18.7	16.8	17.1	17	19	19.6	19.2	20.8	22	21.8	21.8	23.5	24.1	22.8	22.7
OP_{1dB} (dBm)	21.1	22.2	20.1	18.7	24.3	18.4		N/A	15.2	15.5	15.4	19	16	18.1	18.3	21.5	20*	20*	22.8	23.9	22.7	22.5
PAE_{1dB} (%)	28.4	37.6	22.8	20.9	24.4	23		36[c] (PAE_{max})	19.5	21.6	20.7	21.6	21.9	21.7	20.4	39.9	30*	25*	27.6	38.2	26.8	26.2
PAE@9dB PBO (%)	16.1	18.2	11.3	10.4	18*	13.7**		26[c]*	13*^	17.5*^	15*^	7*	13*	12*	8*	23*	N/A	N/A	18*	29*	15*	12*
Modulation	5G NR FR2 1-CC 64-QAM OFDM				Single-Carrier 64-QAM	5G NR FR2 1-CC 64-QAM OFDM	5G NR FR2 2-CC 64-QAM OFDM	64-QAM OFDM (/w DPD)	Single-Carrier 64-QAM			64-QAM OFDM			5G NR FR2 1-CC 64-QAM OFDM				5G NR 1-CC 64-QAM		5G NR 1-CC 16-QAM	
PAPR (dB)	9.64				6	9.64	11.85	10.7	6			N/A			9.64				9.64		9.64	
Bandwidth(MHz)	100/200				250	100	100	300	500			1000	2000		200				100		400	
Freq. (GHz)	28	30	37	40	28	38		29.5	28	37	39	28	37	39	27.5	30	32.5	40	33		35	
EVMrms (dB)	-25				-25.2	-25	-25.1	-27.58	-27[a]	-30.3[a]	-28.7[a]	-22	-24	-23	-25	-25	-25	-25	-25.2		-20	
$Pout_{avg}$ (dBm)	10.2/9.5	11.8/10.5	12.1/10.4	9/8.04	17.7	11.3	10	7.9	9.2	9.5	9.3	7.5	9.8	9.1	7*	8*	9.5	8.9	14.3		16.55	
PAE_{avg} (%)	13.2/11	16.4/13.2	12.6/10.6	8.9/7.4	17.5	14.7	13.4	18[c]	18.5^	19.2^	17.2^	5.1	10.2	8.5	6*	8*	15.5	10.5	25.2		26.4	

*Estimated from figures ^Collector Efficiency [a]EVM normalized to peak signal
**9.6 dB PBO [c]Drain Efficiency [b]Core Area consisting of I/Q splitter, DPM, DPA, and SDC

of 5.58 dBm - 11.1 dBm and 4.8% - 13.3% at an EVM_{rms} of -25 dB from 25 - 40 GHz.

V. Conclusion

This paper describes a PA architecture that achieves broadband and deep PBO efficiency enhancement. From Table 1, previous works using higher-order output networks at mm-Wave are mostly narrowband. Other works that are broadband do not have deep PBO efficiency enhancement. In comparison, this work can achieve both. As demonstrated with 5G NR FR2 64-QAM signals, this PA is suitable for use in the 5G n257 - 261 bands.

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