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***Abstract* — This paper presents a $10-14$ GHz Doherty power amplifier (PA) implemented in GaN on SiC MMIC process aimed for future 6G FR3 centimeter-wave (cmWave) applications. We propose the theory and design of the continuous-mode (CM) operations to extend Doherty PA bandwidth. To demonstrate the viability of the concept, a prototype GaN MMIC CM Doherty PA was fabricated and fully characterized. Experimental results exhibit a peak power added efficiency (PAE) of $28\%-38\%$ and back-off PAE of $21\%-31\%$, respectively, with an output power higher than 34 dBm across the operating frequencies.**

***Keywords* — Continuous mode, Doherty, 6G, gallium nitride (GaN), load modulation, MMIC, power amplifier (PA), wideband.**

I. Introduction

In the evolution toward the sixth generation (6G) wireless communications, the FR3 band ($7-24$ GHz) is anticipated to play an important role due to its superior balance between transmission capacity and coverage area [1]. Specifically, the international mobile telecommunications (IMT) has identified new spectrums within the FR3 band, including the $10.7-13.25$ GHz and the $14-15.35$ GHz, etc., that are vital for future developments in the telecommunications industry [1], [2]. In this context, the design and development of power amplifiers (PA) for use in handsets, access points, and base stations present significant challenges. These PAs are expected to deliver peak output power within $30-35$ dBm [3], [4], a requirement that surpasses those for the fifth-generation (5G) millimeter-wave PAs, attributed to the anticipated increase in cell size within the 6G arrays. Furthermore, the evolution toward more complex modulation schemes, required by higher data throughput in 6G mobile wireless communication systems, has resulted in signals with large peak-to-average-power ratios (PAPR).

Load-modulated PA architectures have been widely adopted to enhance system energy efficiency when transmitting high PAPR signals. Key developments include outphasing and Doherty PAs, with recent advancements introducing the load modulated balanced amplifier (LMBA) [5], distributed efficient PA (DEPA) [6], and circulator load modulated amplifier (CLMA) [7], [8]. Despite the emergence of these novel architectures, the Doherty PA remains the most widely employed technique in cellular base stations because of its simple topology and proven reliability, making it a preferred choice for monolithic microwave integrated circuits (MMIC) applications demanding high efficiency and simplicity. In recent years, expanding the bandwidth of

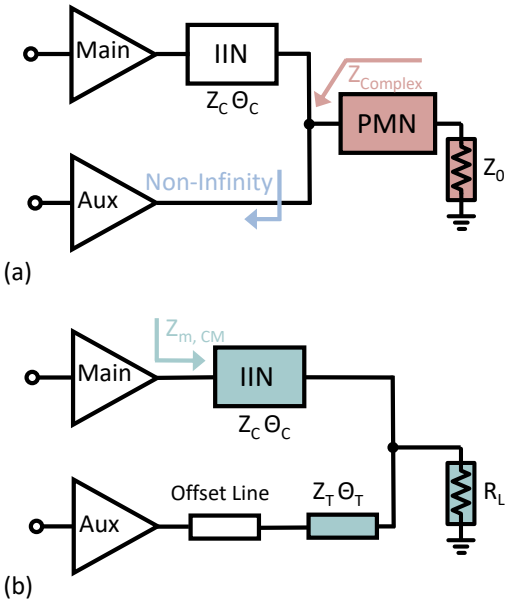

Fig. 1. (a) The conventional CM Doherty PA architecture utilizing the post-matching network or auxiliary non-infinite output impedance and (b) the proposed CM Doherty PA topology.

Doherty PAs has emerged as a key research area. Prior research has effectively incorporated the continuous-mode (CM) technique [9] into Doherty PA designs, achieving bandwidth extension through methods including post-matching in combining networks [10], [11] and employing non-infinite auxiliary output impedance [12] for CM Doherty PAs.

This paper elaborates on the theory and design of a $10-14$ GHz CM Doherty PA, incorporating a novel output combiner network. Fabricated using a 150 nm GaN on SiC process, this PA is tailored for potential 6G FR3 frequency applications. The following sections demonstrate the theory, design, and characterization of the proposed CM Doherty PA, highlighting its bandwidth performance enhancements.

II. Theory

The CM PA operation, analogous to class-B operation, was introduced to expand the design space for the PA output matching network [9]. It allows a range of impedances to yield identical output power and efficiency levels for the PA. Consequently, CM operation facilitates a broader design space without sacrificing RF performance, enabling the development of wideband PAs beyond the constraints of the class-B

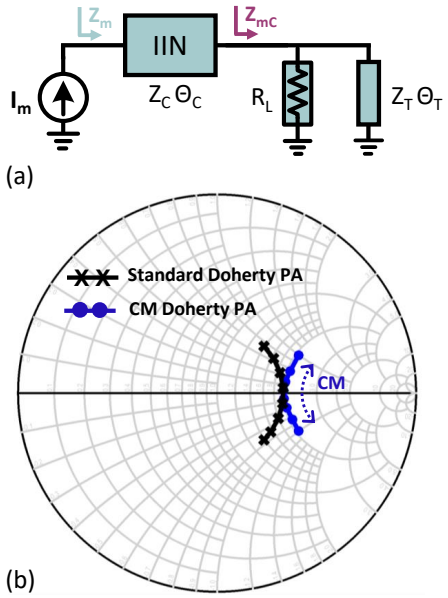

Fig. 2. (a) Theoretical block diagram of the proposed CM Doherty PA at back-off power. (b) Simulated back-off impedance of the standard and CM Doherty PA across 50% normalized fractional bandwidth at their main current source generator plane.

operation. The load impedance for the CM mode PA can be expressed as [9]

$$Z_{\mathrm{f_0}} = R_{\mathrm{opt}}\left(1 - j\gamma\right) \tag{1}$$

$$Z_{\mathrm{2f_0}} = j\gamma\frac{3\pi}{8}R_{\mathrm{opt}} \tag{2}$$

where $-1{\leq}\gamma{\leq}1$, and R_{opt} is the class-B optimal impedance.

In conventional CM Doherty PAs, the combination of output power from the main and auxiliary amplifiers is facilitated through an impedance inverting network (IIN). Fig. 1 demonstrates that to attain CM impedance at back-off power levels, one can utilize the auxiliary amplifier's non-infinite output impedance, altering the combining load into a complex value for conversion to CM impedance, as proposed in [12]. An alternative strategy involves a post-matching network to directly achieve complex impedances at the combining node, introduced in [11]. However, the dependency on a standard quarter-wavelength (λ/4) transformer for the load modulation network in conventional CM Doherty PAs inevitably limits the design space, as it necessitates the use of either non-infinite output impedance or a post-matching network to achieve complex impedances.

To further expand the design space of CM Doherty PAs, we introduce a novel output combiner topology, as shown in Fig. 1(b). Unlike the conventional CM Doherty PA, the proposed combiner network provides the CM complex impedance at the back-off power level, enhancing design flexibility and performance. As demonstrated in Fig. 2(a), at the back-off level, an offset line or matching network from the auxiliary path can transform the auxiliary output impedance to exhibit short circuit behavior at the desired point. Consequently, the load resistance at the combining node, R_{L}, and the remaining transmission line, with impedance Z_{T} and electrical length θ_{T} are effectively in parallel combining. The resulting impedance Z_{mC} is defined as

$$Z_{\mathrm{mC}} = \frac{R_{\mathrm{L}}Z_{\mathrm{T}}\tan\left(\theta_{\mathrm{T}}\right)}{Z_{\mathrm{T}}\tan\left(\theta_{\mathrm{T}}\right) - jR_{\mathrm{L}}} \tag{3}$$

Meanwhile, the impedance at the main current source plane, Z_{m}, can be expressed as [13]

$$Z_{\mathrm{m}} = Z_{\mathrm{C}}\frac{Z_{\mathrm{mC}} + jZ_{\mathrm{C}}\tan\left(\theta_{\mathrm{C}}\right)}{Z_{\mathrm{C}} + jZ_{\mathrm{mC}}\tan\left(\theta_{\mathrm{C}}\right)} \tag{4}$$

Assuming the IIN functions as λ/4 transmission line, the required characteristic impedance Z_C is determined by [14]

$$Z_{\mathrm{C}} = \sqrt{\frac{R_{\mathrm{opt}}R_{\mathrm{L}}}{\beta_{\mathrm{B}}}} \tag{5}$$

where β_{B}, when set to 0.5, represents the back-off level for a symmetrical Doherty PA targeting a 6-dB back-off efficiency enhancement. With these considerations, the impedance Z_{m} can be calculated as

$$Z_{\mathrm{m}} = \frac{Z_{\mathrm{C}}^2}{Z_{\mathrm{mC}}} = \frac{R_{\mathrm{opt}}}{\beta_{\mathrm{B}}}\left(1 - j\frac{R_{\mathrm{L}}}{Z_{\mathrm{T}}\tan\left(\theta_{\mathrm{T}}\right)}\right). \tag{6}$$

Equation (6) reveals that the proposed Doherty combiner topology effectively exhibits CM operation at the back-off power level, which is further illustrated in Fig. 2(b).

III. Prototype Design

The developed CM Doherty PA, fabricated using a 150 nm GaN on SiC MMIC process from WIN Semiconductors (NP15-00), is a two-stage design with dedicated driver amplifiers for both main and auxiliary paths. To achieve a peak output power beyond 34 dBm, 8×100 μm devices are selected for the final power stage, with 4×100 μm devices employed for the driver stages. The main amplifiers are set to operate in Class-AB, whereas the auxiliary amplifiers are configured in Class-C mode, all biased with a 20 V drain supply voltage.

The block diagram of the designed CM Doherty PA is illustrated in Fig. 3(a). Note that all passive networks were EM simulated using ADS Momentum. A Wilkinson power splitter and a phase shifter were designed and employed at the Doherty PA's input to ensure appropriate signal and phase alignment for both amplifier paths. The design of the output combiner network was initiated with load-pull simulations to determine the optimal load impedance for the final-stage devices, thus optimizing power and efficiency over the targeted frequency range. The simulations facilitated the extraction of equivalent output optimal resistance and parasitic capacitance for subsequent modeling. Building on the insights gained, the output combiner network was then designed following the theoretical analysis presented earlier. Furthermore, the inter-stage matching network (ISMN) incorporates a design approach, as proposed in [15], [16], employing a filter-based matching network. This ISMN design optimizes matching conditions, substantially reducing in-band loss and ripples, which in turn improves the bandwidth performance of the PA.

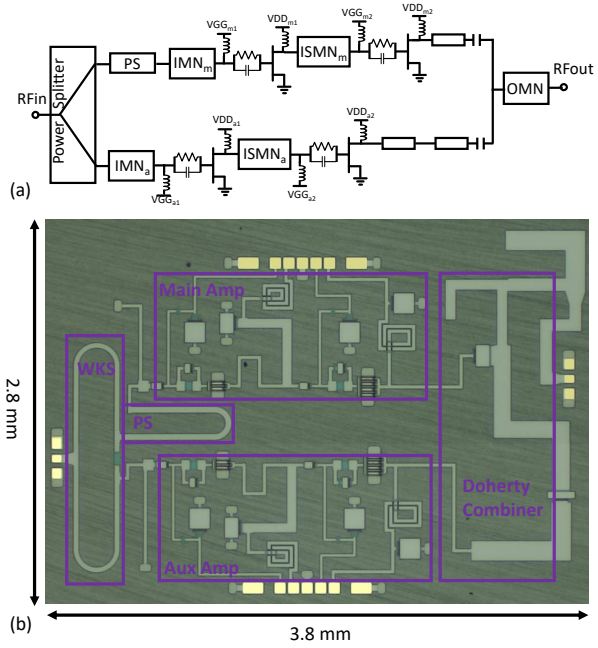

Fig. 3. (a) The circuit block diagram and (b) chip photograph of the fabricated GaN MMIC CM Doherty PA (Total chip area: 2.8 mm × 3.8 mm including DC and RF pads).

The stability of the circuit was carefully simulated using Winslow Stability (WS) probes at all gate and drain terminals, employing various loop gain approaches to test the PA stability. Parallel RC networks were implemented at the gates of both the driver and final stages to mitigate instability across different DC bias bond wire inductances. To counter low-frequency instabilities, a parallel LR network was integrated between the DC pad and the bypass capacitor on the drain bias line. Additionally, series resistors were incorporated into the gate bias lines to enhance stability for similar considerations.

IV. Measurement Results

A photograph of the fabricated CM Doherty PA prototype is shown in Fig. 3(b), which occupies a compact chip area of 2.8 mm3.8 mm including the DC and RF pads. The chip was further mounted on a customized printed circuit board (PCB), with the DC pads of the PA connected to decoupling capacitors through wire bonds. Small signal measurements were performed using a vector network analyzer with the calibration reference plane de-embedded to the GSG pads. Large signal testing employed a signal generator to produce static signals and the output power was measured with a power meter and spectrum analyzer.

A. Small Signal Measurement

In Fig. 4, we present the small signal characterization of the prototype circuit, alongside a comparison with simulation results. We observe good agreement between the measured and simulated results of both the input and output return loss. Additionally, the measured small signal gain closely matches the simulated predictions, with minor deviations occurring only at the edge frequencies. It is worth mentioning that the

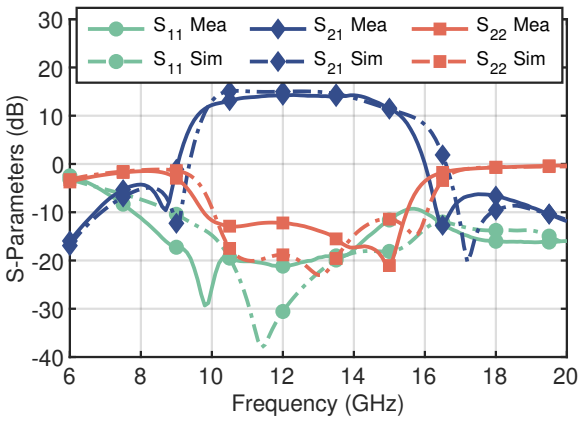

Fig. 4. Measured (solid line) and simulated (dashed line) small-signal results of the fabricated prototype Doherty PA circuit.

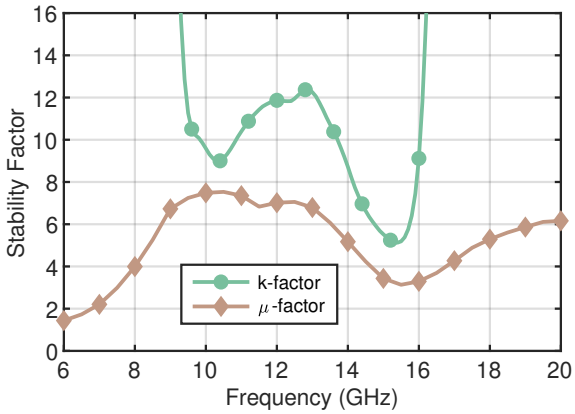

Fig. 5. Measured stability factors of the prototype Doherty PA circuit.

measured 3 dB bandwidth of the small signal gain is across 9.6 – 15.1 GHz and the prototype achieves an ultra-flat gain response within the operating frequencies. Furthermore, the prototype circuit is unconditionally stable as shown in Fig. 5.

B. Large Signal Measurement

Fig. 6 illustrates the measured power added efficiency (PAE) versus the output power at 11 GHz and 13 GHz, demonstrating the prototype's smooth compression behavior without parametric oscillations. The static measured results in terms of peak power, peak- and 6-dB back-off PAE are further presented versus frequency in Fig. 7. It can be observed that a peak output power of 34.2-36.1 dBm is measured across the entire band within 10-14 GHz. Correspondingly, the measured peak PAE is 28-38%, while the measured PAE at 6-dB back-off power level is 21-31%.

The performance of the fabricated PA is then presented and compared with the state-of-the-art load modulated MMIC PAs in Table I. The comparison reveals that our prototype achieves excellent PAE at both peak and back-off levels compared to existing MMIC PAs designed for back-off efficiency enhancement. Furthermore, the prototype maintains competitive performance over a wide frequency range.

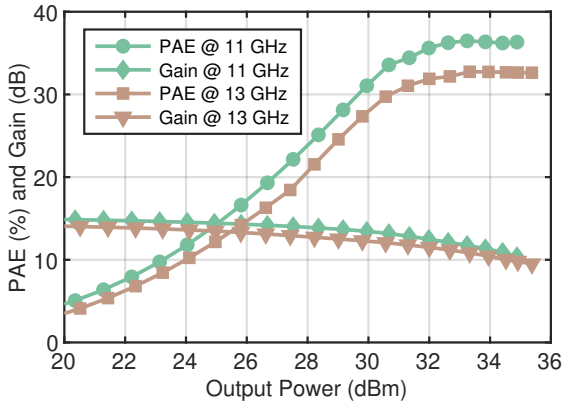

Fig. 6. Measured PAE and gain of the prototype versus output power.

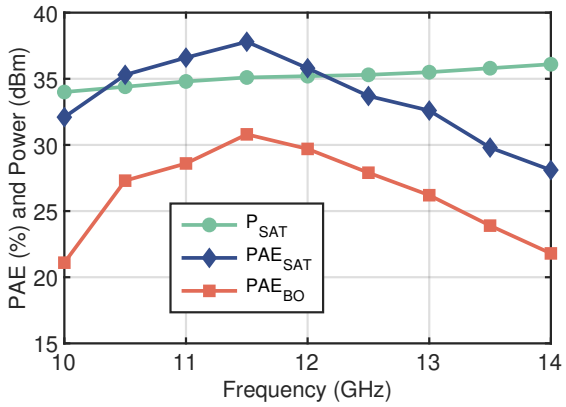

Fig. 7. Measured power and PAE of the prototype versus frequency.

V. Conclusion

This work proposes a novel output combiner network for CM Doherty PA designs, aimed at expanding the bandwidth of Doherty architectures. We present a two-stage, GaN on SiC, CM Doherty PA, capable of delivering over 34 dBm of power across the 10–14 GHz with a 33% fractional bandwidth. Furthermore, the prototype demonstrates PAE at peak and 6-dB back-off levels of $28\% - 38\%$ and $21\% - 31\%$, respectively. To the best of our knowledge, this represents the first GaN MMIC CM Doherty PA designed for the FR3 cmWave band, highlighting its potential for 6G applications.

Acknowledgment

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Table 1. Summary of Load Modulated MMIC PAs.

Ref.	Arch.	BW (GHz)	BW (%)	PAE_B (%)	PAE_S (%)	P_{SAT} (dBm)
[17]'22	2-DPA	16.3-20.3	22	19-21	23-31	36
[18]'23	3-DPA	27.5-29.5	7	19-21	23-31	34
[19]'17	2-DPA	13.7-15.3	11	16*-28*	29*-39*	35
[20]'19	LMBA	10.8	N.A.	26	38	35
[11]'22	2-DPA	4.1-5.6	32	32-39	41-49	35
T.W.	**2-DPA**	**10.0-14.0**	**33**	**21-31**	**28-38**	**34**

$*$ drain efficiency reported, PAE_B and PAE_S denotes PAE at the back-off and peak power, respectively, and P_{SAT} denotes minimum peak power level.

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