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Deliberate Source/Load Mismatch for Linearity and Efficiency of Discrete Supply Modulated GaN PAs

Connor Nogales, *Student Member, IEEE,* Paul Flaten, *Student Member, IEEE,*
Morten Olavsbråten, *Member, IEEE,* Zoya Popović, *Fellow, IEEE* and Gregor Lasser, *Member, IEEE,*

***Abstract*—The effect of source (gate-side) and load (drain-side) impedance match on the linearity and efficiency of an envelope-tracked power amplifier (PA) is investigated. Conventionally designed GaN PAs exhibit an increasing gain magnitude and phase with increasing drain supply voltage. When this supply voltage is dynamically modulated in discrete levels for efficiency enhancement, the changing gain distorts the output signal and degrades linearity. The dependency of the PA gain on drain supply voltage can be minimized, however, through proper selection of the source and load impedances. This is illustrated through source/load pull simulations of a $8\times100\,\mu$m GaN HEMT, which reveal impedances that result in low gain magnitude and phase variation. Three PA design (matching) cases are then chosen and their performances are evaluated with an ideal dynamically changing supply. For the comparison, envelope simulations with a 67.5 MHz 64 QAM signal are performed and show that dynamic supply modulation of the mismatched PA design improves linearity and efficiency over a conventional PA designed for maximum efficiency/gain. The simulation results are validated through measurements of a deliberately mismatched, 6.2 to 12.6 GHz, 5-W GaN MMIC PA envelope-tracked with a GaN MMIC 4-level supply modulator. Compared to a static supply, the dynamic results show improvement in average efficiency and a small penalty in linearity without using DPD.**

***Index Terms*—Envelope Tracking, GaN, Linearity, Supply Modulation, Power Amplifier**

I. Introduction

MODERN communication and electronic warfare wireless systems require front-end transmitters utilizing signals with a high peak-to-average power ratio (PAPR). These transmitters demand high efficiency, large RF and baseband bandwidths, and have stringent linearity requirements. However, in a conventional power amplifier (PA) efficiency and linearity are at odds [1]. To improve linearity, digital and analog techniques have been adopted [2], such as a hybrid analog/digital feedforward method [3], dynamic gate biasing [4], and analog pre-distortion [5]. Additionally, AM-AM and AM-PM non-linearities can be minimized through a mismatch of the matching networks [6], [7]. However, none of these techniques improve the efficiency directly. One technique to improve PA efficiency is supply modulation (envelope tracking) where the drain supply voltage is dynamically changed in accordance with the input signal envelope [8], which can be done in a continuous [9] or discretized [10] manner. By reducing the drain bias voltage at backed-off input power levels, the PA can be saturated across a range of power levels and the average efficiency is improved. However, GaN PAs exhibit an expansive gain magnitude and phase dependence on drain voltage (V_d) which can vary by as much as 7.5 dB and 40° as reported in [11], [12], [13]. The origin of this variation comes from the transconductance and input/output impedance dependence on V_d [14] highlighted in Fig. 1a.

Supply modulation itself can also be used as an analog linearization technique. By taking advantage of the PAs gain magnitude expansion with drain voltage, the power-dependent

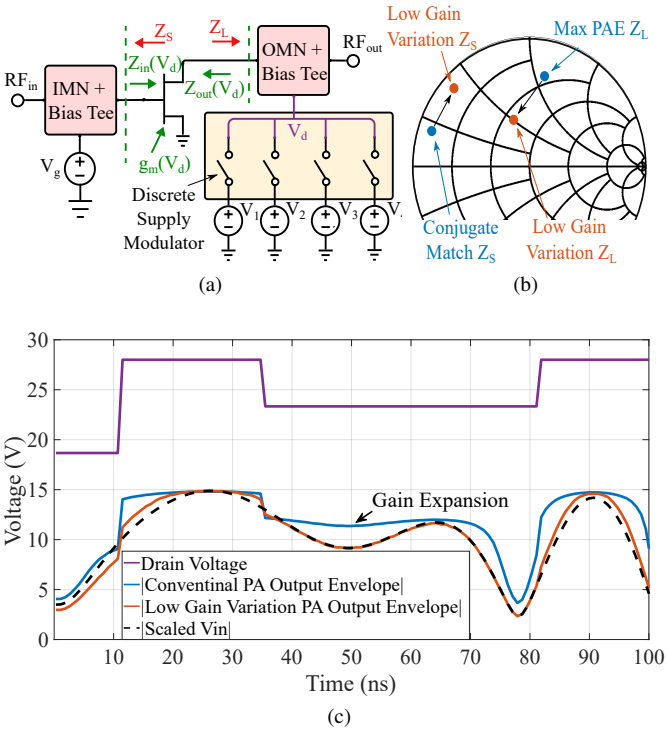

Fig. 1. (a) Block diagram of a PA with a dynamically changing discrete drain supply voltage. (b) Potential source/load impedances for low gain variation across drain voltage and conventional PA design impedances. (c) Time domain simulation comparing the conventional PA design to the deliberately mismatched PA designed to reduce the gain dependence on drain voltage.

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Connor Nogales, Paul Flaten, and Zoya Popović are with the University of Colorado Boulder, Boulder, CO (email: connor.nogales@colorado.edu, paul.a.flaten.civ@us.navy.mil, and zoya.popovic@colorado.edu). Morten Olavsbråten is with the Department of Electronic Systems, Norwegian University of Science and Technology, Trondheim 7491, Norway (e-mail: morten.olavsbraten@iet.ntnu.no) Gregor Lasser is with Chalmers University of Technology, Sweden (e-mail: gregor.lasser@chalmers.se). *(Corresponding author: Connor Nogales)*

gain compression can be compensated, resulting in a linear AM-AM response often referred to as "flat gain" [9], [15]–[18]. This is achieved by tailoring a shaping function (drain voltage to input power relationship) so that the gain is constant across output power. This often results in reduced efficiency from shaping functions targeting maximum efficiency. For instance, in [9], the PAE is reduced by 1.9% points. However, the ACPR is improved by $5.1\,\mathrm{dB}$ with a $10\,\mathrm{MHz}$ LTE signal. While the AM-AM response of a PA can be linearized through a flat gain shaping function, the AM-PM response remains distorted due to the gain's phase dependence on drain voltage and input power. Furthermore, since most GaN PAs exhibit an expansive phase as a function of drain voltage and power, it is challenging if not impossible to linearize the phase response through a shaping function. Examples of analog compensation of the phase dependence on drain voltage have been demonstrated through an input phase shifter with the control voltage tied to the PA drain voltage [19] or mismatch of the input matching network [20], both of which result in a reduced PA gain.

For continuous supply modulation (CSM) systems, the PA can be designed to minimize gain phase variation to improve AM-PM linearity and the AM-AM response can be linearized using a "flat-gain" shaping function. Thus for CSM, the degree of gain magnitude variation is insignificant. However, in systems with high signal bandwidths where the total system efficiency is important, a discrete supply modulation (DSM) topology is often adopted [10], [21]. In contrast to CSM, DSM consists of discrete voltage levels which the modulator switches between to approximate the CSM case. The advantage of DSM is that the supply modulator has higher efficiency since it has fewer switching instances than a switched-mode power converter such as a buck converter [22].

The PA's gain as a function of drain voltage is a key characteristic for discrete supply modulation. Since DSM has a limited number of levels and is often bandwidth-limited, the drain voltage deviates from the CSM shaping function at instances where the supply does not have enough levels or is not fast enough to follow the continuous shaping function. At these instances, the PA is dynamically moving between backed-off approximate small signal and large signal operation as the drain voltage and input power are changed. Therefore, if the PA has a high small-signal gain variation with regard to supply voltage, the output signal is distorted, resulting in degraded linearity. The gain variation can be reduced through a deliberate mismatch of the input and output impedances as shown in Fig. 1b. The improvement in linearity from this mismatch is illustrated in Fig. 1c, where the output envelope is compared between a conventionally designed PA and a low-gain variation PA with DSM. At $50\,\mathrm{ns}$, we see a gain expansion for the conventional PA design when the envelope drops but the supply voltage remains constant. In contrast, the low gain variation PA amplifies the signal with less distortion. Additionally, upon each switching instance, the discrete supply introduces voltage ringing which mixes with the PA and degrades linearity metrics [22]–[24]. This distortion is in addition to known AM-AM and AM-PM compression behavior prevalent in GaN PAs [25], [26], [27]. Any distortion of the output signal degrades out-of-band linearity metrics, such as adjacent channel power ratio (ACPR), and in-band metrics, such as error vector magnitude (EVM). With discrete supply modulation, the linearity is degraded further while the supply is in a transient state, switching voltage levels. This distortion is in addition to gain magnitude/phase dependence on drain voltage and compression-based non-linearities. Applying DPD to compensate for these distortions is demonstrated in [28]. However, this adds additional complexity, requires more computational power, degrades system efficiency, and has limitations for large signal bandwidths [29], [30]. The work presented in this paper focuses on improving the intrinsic linearity of the PA without the use of DPD.

Mismatching PAs for reduced gain variation was demonstrated for the phase of the gain in [20], [31] and for the magnitude of the gain in [32]. However, an in-depth analysis of the linearity and efficiency trade-offs of different load/source impedances with a dynamically changing discrete drain supply has not been discussed in the literature to the best of the author's knowledge.

The paper is organized as follows, First, simulations of source and load pull are shown in Section II for different loading cases and investigated with both continuous and discrete supply modulation. The source and load impedances with minimal gain variation over supply voltage are then realized in the final stage of an experimental PA presented in III. Next, the design and characterization of a two-stage 6 to $12\,\mathrm{GHz}$ bandwidth $5\,\mathrm{W}$ PA is presented. The measured CW data of the PA is used to predict the dynamic drain bias results using the custom envelope simulator. The PA is measured with a dynamic drain signal and compared with envelope simulation results showing good agreement and validating the results of the envelope simulator.

II. Simulation Study

The small-signal gain variation of a GaN MMIC device is investigated through source/load pull simulations. Three different loading cases are identified: a conventional PA design; a design with the input mismatch to minimize the small-signal gain phase variation while maintaining a minimum of $10\,\mathrm{dB}$; and a design that mismatches the source and load for minimal gain magnitude variation. The three cases are then simulated with continuous and discrete supply modulation.

A. Device Source and Load Pull

The source/load pull simulations are performed with a single transistor at $9\,\mathrm{GHz}$ with a drain bias ranging from 14 to $28\,\mathrm{V}$ and a fixed gate bias. The WIN Semiconductors NP15 $150\,\mathrm{nm}$ GaN-on-SiC process is used for this analysis and for the fabricated MMIC. A device size of $8\times100\,\mu\mathrm{m}$ is chosen to achieve a minimum output power of $34\,\mathrm{dBm}$ at $28\,\mathrm{V}$. This device is biased with a gate voltage of $-1.57\,\mathrm{V}$ corresponding to 80 mA of quiescent current at the maximum drain voltage ($28\,\mathrm{V}$). The two-port S-parameters of the transistor are extracted at three drain voltages of 14, 21, and $28\,\mathrm{V}$ from the non-linear model provided by WIN Semiconductors. The load and source pull simulations are performed at each drain voltage using linear

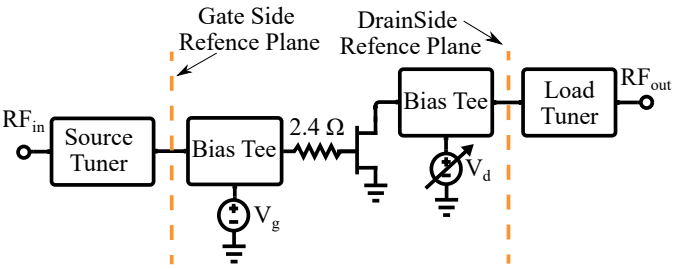


Fig. 2. Source/load pull schematic. The $2.4\,\Omega$ resistor is added to stabilize the transistor.

network analysis, cascading the transistor S-parameters with the input and output impedances. The standalone transistor is not unconditionally stable. Therefore, loss must be added to the input to stabilize the device as shown in Fig. 2 where a $2.4\,\Omega$ resistor is added. The schematic of the load/source pull simulation is shown in Fig. 2 with the corresponding reference planes. At each load/source impedance, the gain magnitude and phase of the overall cascaded network is calculated at the three previously stated drain voltages. The gain magnitude variation ($\Delta|G|$), gain phase variation ($\Delta\phi$), and complex gain variation (ΔG) are defined as:

$$\Delta|G| = max(|G(V_{\mathrm{d}m})|/|G(V_{\mathrm{d}n})|) \quad \forall m \neq n, \tag{1}$$

$$\Delta\phi = max(\angle G(V_{\mathrm{d}m}) - \angle G(V_{\mathrm{d}n})) \quad \forall m \neq n, \tag{2}$$

$$\Delta G = max\left(\frac{|G(V_{\mathrm{d}m}) - G(V_{\mathrm{d}n})|}{|G(V_{\mathrm{d}2})|}\right) \quad \forall m \neq n, \tag{3}$$

where $G(V_{\mathrm{d}m}) = |G(V_{\mathrm{d}m})|\exp\left[j\angle G(V_{\mathrm{d}m})\right]$ is the small signal complex gain at a drain voltage index m.

Load pull simulations of the $8\times100\,\mu$m device $\Delta|G|$, $\Delta\phi$, and ΔG are shown in Figs. 3a, 3b, and 3c, respectively. At each load impedance, the input is conjugate matched at a drain voltage of 28 V. The maximum PAE impedance for each drain voltage is shown, along with PAE contours where the efficiency drops by 5 percentage points (pp) from its peak value. Additionally, the impedance which results in the maximum 1 dB compression output power is labeled as well. The 2^{nd} and 3^{rd} harmonics are terminated with an open circuit to yield high efficiency. An analysis of the 2^{nd} and 3^{rd} harmonic termination with this MMIC process is presented in [33]. The labeled point $Z_{L1,2}$ shows the maximum PAE impedance at 28 V and Z_{L3} shows the load impedance presented to the output stage of the realized PA, which is a compromise between efficiency and $\Delta|G|$. In Fig. 3a, it is apparent that the $\Delta|G|$ can be reduced by matching the output for maximum PAE at the lower drain voltages. However, the $\Delta\phi$ is increased at these impedances, and the overall ΔG is nearly the same. By aggressively de-tuning the load impedance each of these parameters can be improved as shown in Z_{L3}, however, this reduces the efficiency. The tradeoffs between these impedances and their effect on PA performance will be further investigated in section II-B. The $\Delta|G|$ and $\Delta\phi$ can be completely nulled through extreme de-tuning of the load impedance, however, this comes at a significant cost to efficiency and gain. Therefore, the load impedance chosen for the realized PA (Z_{L3}) is a trade-off between improving the $\Delta|G|$ and $\Delta\phi$ while maintaining acceptable gain and PAE.

Source pull simulations of the $\Delta|G|$, $\Delta\phi$, and ΔG are shown in Fig. 4 with the load impedance fixed for maximum PAE at 28 V ($Z_{L1,2}$). The corresponding conjugate match points at each drain voltage are plotted when the output is loaded with the maximum PAE impedance for the three drain voltages. The labeled point Z_{S1} is the conjugate match at 28 V. Z_{S2} is the mismatched source impedance which results in minimal $\Delta\phi$ while maintaining 10 dB of gain at the lowest drain voltage. The point Z_{S3} is the source impedance presented to the output stage of the realized PA. Interestingly, the region of low $\Delta|G|$ (Fig. 4a) near a short circuit, corresponds to a region of high $\Delta\phi$ (Fig. 4b).

B. Envelope Simulations of a Single Device

To investigate the impact that different loading conditions have on efficiency, gain, and linearity, three matching cases are identified:

- **Case 1:** A conventional PA design where the load impedance is chosen to maximize PAE at 28 V ($Z_{L1,2}$) with the source impedance conjugate matched (Z_{S1});
- **Case 2:** Similar to the design in [20] where the load impedance maximizes PAE at 28 V ($Z_{L1,2}$) but the source impedance is mismatched to minimize $\Delta\phi$ while maintaining a minimum gain of 10 dB at the lowest drain voltage of 14 V (Z_{S2}); and
- **Case 3:** A low gain variation design where the load and source impedances are significantly mismatched from the conventional design and use the same impedances presented to the final stage of the realized PA presented in section III (Z_{L3} and Z_{S3}).

TABLE I
$\Delta|G|$, $\Delta\phi$, AND ΔG OF THE THREE MATCHING CASES.

Case	Z_{L}	Z_{S}	$\Delta\lvert G\rvert$ (dB)	$\Delta\phi$ (deg.)	ΔG
1	Z_{L1}	Z_{S1}	7.5	41.4	1.0
2	Z_{L2}	Z_{S2}	5.4	16.7	0.67
3	Z_{L3}	Z_{S3}	4.6	13.1	0.54

The simulated $\Delta|G|$, $\Delta\phi$, and ΔG values for these matching conditions are summarized in Table I. The simulations are performed in Cadence AWR Microwave Office using ideal input and output tuners with identical device sizes and bias points as presented in section II-A. The simulated CW PAE, gain magnitude, and gain phase are shown in Fig. 5 for each of the three cases, across drain voltages ranging from 14 to 28 V. These figures also show the continuous and discrete PAE, gain, and phase resulting from max PAE shaping functions.

Since the shaping function is mapped from a continuous range of input powers, there is a discontinuity in gain and output power when switching to higher discrete drain voltages, which degrades linearity. In addition, the bandwidth limitations of the dynamic supply cause deviations from this shaping

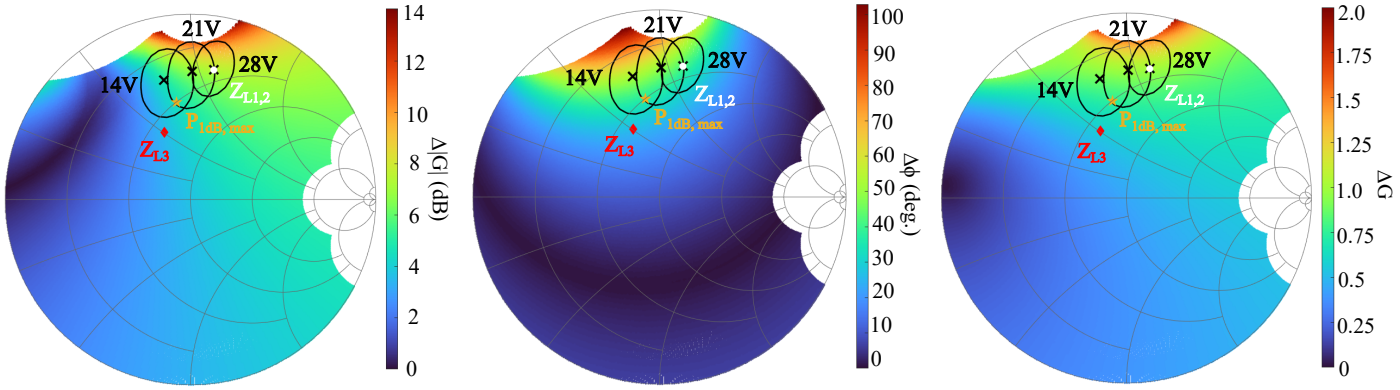


Fig. 3. Load pull at 9 GHz of a single $8\times100\,\mu$m device in the WIN NP15 GaN on SiC 150 nm process showing small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) across drain voltages of 14, 21, and 28 V. The PAE contours indicate impedances where the PAE is reduced by 5% from the peak PAE at each drain voltage. Additionally, the impedance which results in the maximum 1 dB compression output power is labeled.

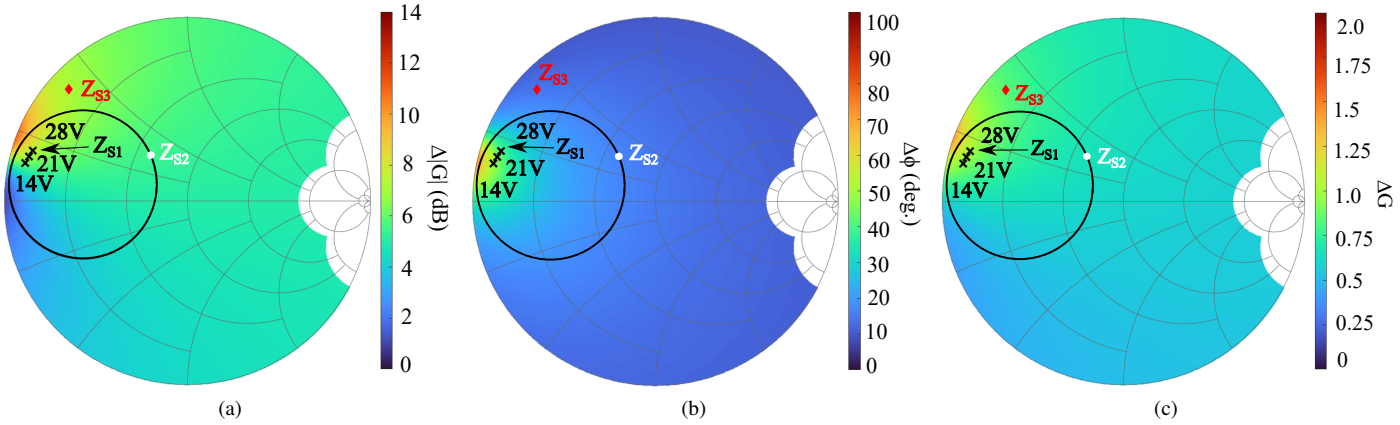


Fig. 4. Source pull at 9 GHz of a single $8\times100\,\mu$m device in the WIN NP15 GaN on SiC 150 nm process showing small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) across drain voltages of 14, 21, and 28 V. The load impedance is fixed at the maximum PAE point for a drain voltage of 28 V ($Z_{L1,2}$). The conjugate match points at each drain voltage are labeled along with the 10 dB small signal gain contour at 14 V.

function and the PA is constantly switched between small- and large-signal operation. This distortion can be minimized by reducing the gain magnitude variation of the PA.

The PAE shown for a conventional PA design (Case 1) shown in Fig. 5a is nearly identical to the mismatched source impedance design (Case 2) shown in Fig. 5b with peak PAE occurring at 28 V, while the PAE of Case 3 (Fig. 5c) peaks at 14 V. Furthermore, the $\Delta|G|$ is highest in Case 1 and lowest in Case 3. The advantage of de-tuning the source impedance in Case 2 can be seen clearly in Figs. 5h and 5i where Cases 2 and 3 have much improved $\Delta\phi$.

To evaluate the performance of each of these cases under dynamic supply modulation conditions, a behavioral model of the PAs is created in MATLAB using the CW PAE, gain magnitude, and phase as a function of input power and drain voltage. The behavioral model is a look-up table of the CW performance that is linearly interpolated across power and drain voltage. Using this model, the time domain envelope simulator applies the PA AM-AM and AM-PM non-linearities point by point to the baseband signal, predicting the PAE, gain, and linearity. The envelope simulator does not include memory effects such as trapping, thermal dependence, and bias line effects. However, the AM-AM and AM-PM distortion is the dominant non-linearity in GaN HEMT PAs. Therefore, this behavioral model works as a first-order approximation of the non-linearities including the complex gain variations due to supply modulation [13], [34].

Each case is evaluated with three different drain voltage modulation signals. The first is a continuous drain supply with no bandwidth limitations shown in Fig. 6a, the second and third are four-level discrete signals with minimum pulse widths limited to 10 ns (100 MHz) and 40 ns (25 MHz) shown in Figs. 6b and 6c. Parasitics in the switching devices and circuit layout reduce the slew rate of voltage transitions and set the upper limit on switching frequency. When the signal envelope bandwidth approaches or exceeds this maximum switching frequency, the DSM deviates from the desired continuous shaping function and has reduced efficiency and linearity [35]. At such points, the drain voltage is higher than the desired shaping function to avoid clipping the signal, and the PA

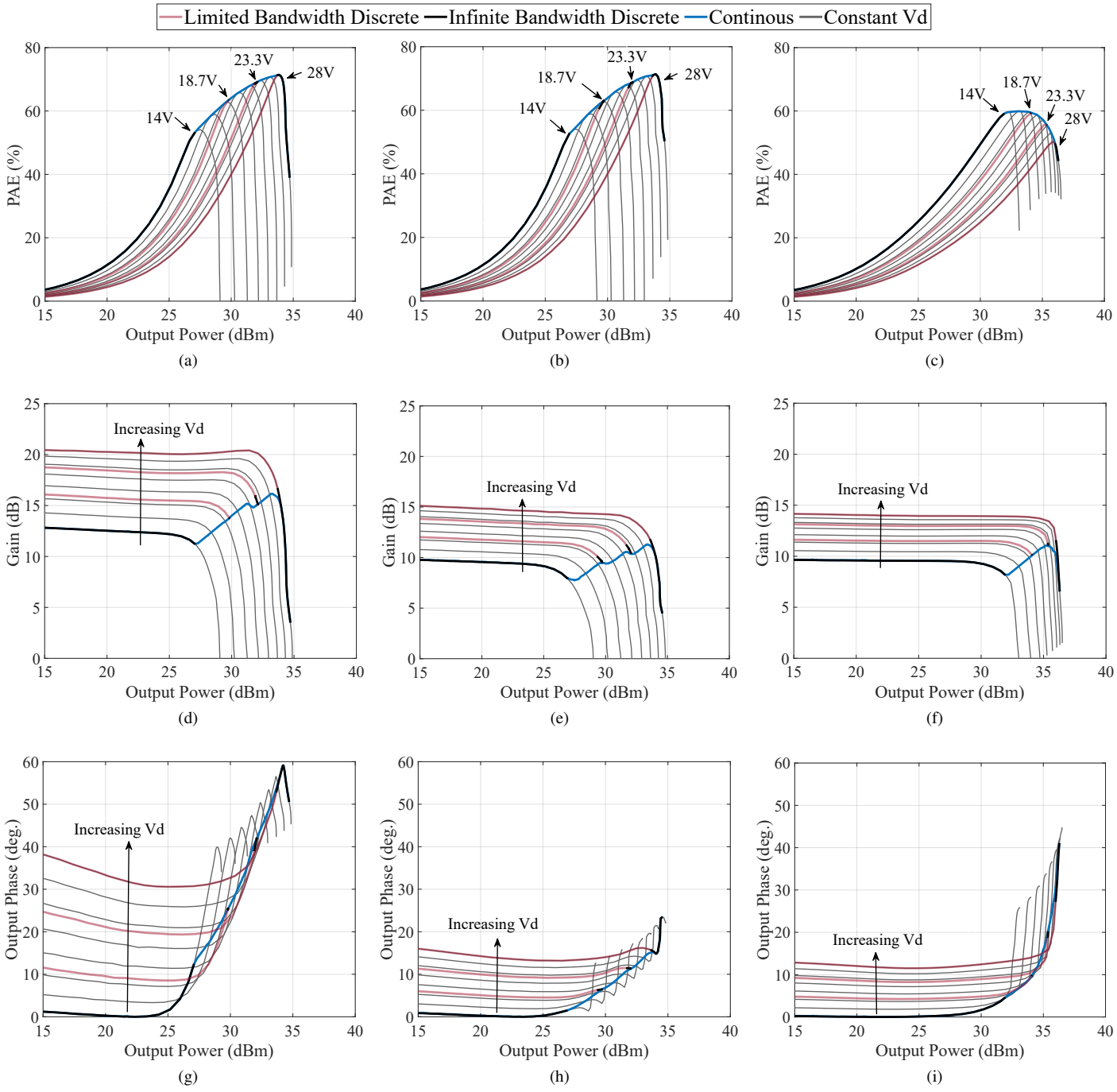


Fig. 5. CW PAE, gain magnitude and phase plotted vs. output power for three different loading conditions at 9 GHz. The loading conditions are: (a) conventional PA design (Case 1) (b) mismatched input impedance for minimal $\Delta\phi$ (Case 2) and (c) PA designed for low gain variation with the source and load mismatched (Case 3). Additionally, the PAE, gain magnitude, and phase resulting from the max PAE shaping function are plotted with an infinite bandwidth supply utilizing continuous (blue) and discrete (black) voltage levels. The performance resulting from bandwidth limitations in the discrete supply (red) is shown where the PA operates in the small and large signal regions.

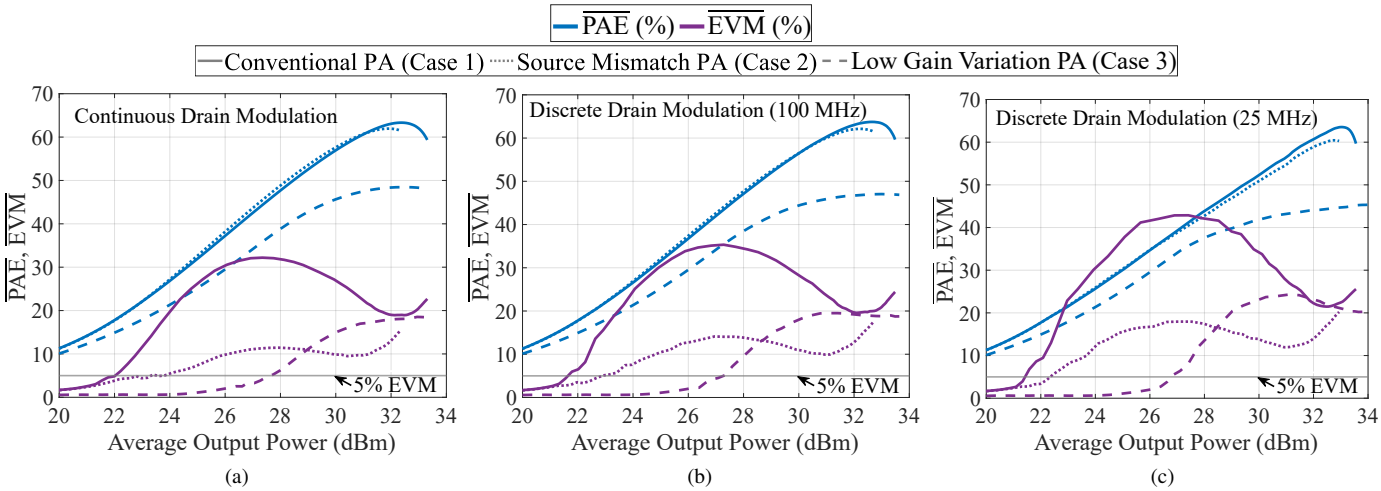


Fig. 6. Simulated comparison between the three loading conditions in terms of average PAE, Gain, and EVM vs average output power at 9 GHz with (a) continuous supply modulation (b) four-level discrete supply modulator with a maximum switching frequency of 100 MHz and (c) DSM with a maximum switching frequency of 25 MHz. Each scenario is evaluated with a 67.5 MHz 64-QAM signal.

operates in the backed-off approximate small signal regime. There is a gain expansion at these instances where the discrete supply is not fast enough to follow the signal envelope or does not have enough levels, which is a direct consequence of the small signal gain variation $\Delta|G|$, and when minimized can improve linearity.

The amplified signal uses a 64-QAM modulation scheme with a baud rate of 50 Msymbols/sec, an initial root-raised cosine filter with a roll-off factor of 0.35 is applied before the signal is amplified, and this digital filter is applied a second time to the sampled output signal. The filtering expands the bandwidth to 67.5 MHz. The signal length is 1000 symbols and the PAPR is 7 dB. The PAE, gain, and error vector magnitude (EVM) are averaged across one signal period and plotted in Fig. 6 as a function of average output power for each of the three cases. Here the maximum PAE shaping function shown in Fig. 5 is used.

Comparing cases 1 and 2, we can see the advantage of mismatching for minimum $\Delta\phi$. Here the EVM is significantly improved without any drop in PAE and a small reduction in gain. If we compare cases 2 and 3 we can see the advantage of mismatching the source and load impedances. Case 3 shows the best EVM, with a reduction in PAE and gain due to the mismatch in the source and load impedance. However, to achieve an EVM of 5% with the Case 2 design, it would be necessary to back the PA off by over 4 dB from the output power of Case 3. At an EVM of 5%, Case 3 has a PAE 14% points greater than the PAE of Case 2. Additionally, the performance of Case 3 is less affected by supply modulator bandwidth limitations. At 27.0 dBm of output power, limiting the discrete switching speed to 25 MHz degrades the EVM of Case 1 and 2 by 10.3% points and 6.8% points when compared to the continuous drain voltage, alternatively the EVM of Case 3 is reduced by only 2.2% points. The PAE, gain, P_{out}, and EVM values are summarized in Table II and evaluated using two criteria. The first is with a fixed output power of 27 dBm and the second is a fixed EVM of 5%. Note that the signal bandwidth is almost three times greater than the switching frequency of 25 MHz, and these results are obtained without the use of DPD.

TABLE II
SIMULATED AVERAGE PAE, GAIN, P_{out}, AND EVM FOR THE THREE CASES WITH STATIC 28 V, CONTINUOUS, AND DISCRETE DRAIN SUPPLIES. THE VALUES ARE OBTAINED AT A FIXED OUTPUT POWER OF 27 dBm (LEFT) AND A FIXED EVM OF 5% (RIGHT).

	Fixed P_{out} of 27 dBm			Fixed EVM of 5%		
Case	$\overline{\boldsymbol{PAE}}$	$\overline{\boldsymbol{Gain}}$	$\overline{\boldsymbol{EVM}}$	$\overline{\boldsymbol{PAE}}$	$\overline{\boldsymbol{Gain}}$	$\overline{\boldsymbol{P_{\text{out}}}}$
Static 28 V Drain Supply						
1	21.1	20.2	4.2	23.4	20.2	27.5
2	21.5	14.3	2.2	31.6	14.0	29.0
3	15.9	13.9	0.9	31.5	13.7	31.5
Continuous Drain Modulation						
1	42.6	13.7	32.2	17.8	12.2	22.0
2	43.7	9.3	11.1	26.3	8.8	23.8
3	34.2	9.3	3.3	36.6	9.25	27.5
Discrete 4-level 100 MHz Drain Modulation						
1	42.1	14.2	35.2	16.1	12.3	21.6
2	42.7	10.2	14.0	21.6	9.2	22.9
3	34.3	9.3	4.0	34.5	9.3	27.1
Discrete 4-level 25 MHz Drain Modulation						
1	39.2	15.0	42.5	15.3	12.3	21.3
2	38.7	10.8	17.8	18.5	9.2	22.2
3	33.9	9.4	5.5	32.4	9.4	26.6

The discrete drain voltage amplitude statistics are a function of average input power. At low power levels, the PA operates at its lowest drain voltage level only switching to higher voltages when necessary. At medium average powers, all four voltage levels are used so the PA sees the full range of gain magnitude and phase variation. Here, the EVM peaks and then drops at higher power levels where the PA operates at the highest voltage for the majority of the time, converging to the static 28 V supply case. However, at these high average power levels, the EVM is beyond an acceptable value.

A comparison between the conventional PA design (Case 1)

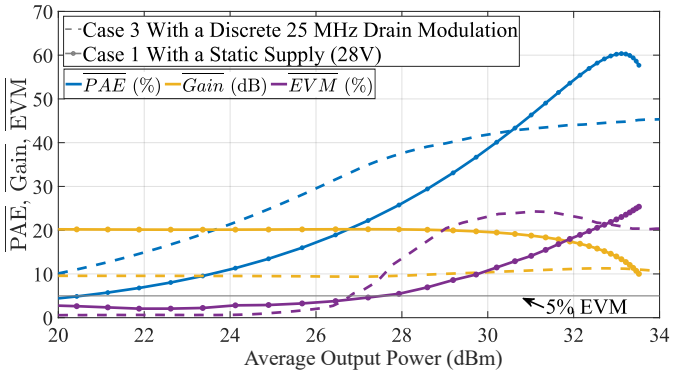


Fig. 7. Simulated comparison between a conventional PA design (Case 1) with a static drain supply, and a low gain variation PA design (Case 3) with a discretely supply modulated supply at a carrier frequency of 9 GHz. The dynamic supply has a maximum switching of 25 MHz. Each scenario is evaluated with a 67.5 MHz 64-QAM signal.

with a static 28 V supply and a low gain variation design (Case 3) with discrete 25 MHz drain modulation is shown in Fig. 7. At 27 dBm of average output power both cases show the same EVM however the PAE of Case 3 is 12.4% points higher. This demonstrates that a PA that is deliberately mismatched for linearity can beat a conventional, efficiency optimized, static supply PA using discrete supply modulation.

III. PA Design and Characterization

A. PA Design

The deliberate mismatch approach of the previous sections is now used to design a two-stage GaN MMIC PA covering 6 to 12 GHz with a minimum of 5 W of peak CW output power across the band. Furthermore, since Case 3 gives the best trade-off between PAE and EVM as shown in section II-B, the source and load impedances of the final stage are chosen to minimize small signal $\Delta|G|$ and thus are identical to the impedances of Case 3 at 9 GHz. The source/load pull procedure is repeated at frequencies of 6 GHz and 12 GHz. A parallel RC circuit is fit to the optimal load impedances and matched across the bandwidth. For the source impedance, a simple RC circuit did not approximate the impedances sufficiently. Therefore, a higher-order network consisting of an LC tee network in parallel with a resistor is fit to the source impedances.

The MMIC PA is designed in the WIN Semiconductors NP15 process and is shown in Fig. 9. This process targets mm-wave power applications through 40GHz. The gate length is 0.15 um and is manufactured on 100 um SiC substrates. A source-coupled field plate design is used to provide the high breakdown voltage required for reliable operation at a V_{ds} of 28 V. This process features two interconnect metal layers, high-reliability MIM capacitors, precision TaN resistors, and through-substrate vias for low inductance ground connections. The periphery of the first stage is a single $8\times50\,\mu$m device biased near class-B operation with 8 mA of quiescent current at a fixed drain voltage of 28 V. The second stage consists of two reactively combined $8\times100\,\mu$m devices, each biased with a current of 80 mA. The staging ratio is 4:1. The PA is designed to have the first stage operate with a fixed drain voltage while the second stage drain is supply modulated from 14 to 28 V. Supply modulating only the output stage improves the PA $\Delta|G|$ and $\Delta\phi$. The efficiency is improved by biasing the first stage in deep class-B and reducing the current consumption at backed-off power levels. In addition, by including a first stage with a fixed drain supply, this allows the second stage input to be mismatched through the inter-stage matching network, and the first stage input matched to 50 Ω. Therefore, the total PA is well matched to 50 Ω with an overall low gain magnitude/phase variation. The devices are reactively matched using lumped capacitors and transmission lines. The octave bandwidth output matching network (OMN) is designed using a filter synthesis matching technique which results in minimal insertion loss and incorporates the drain bias line and blocking capacitor into the OMN as described in [36] [37]. A series resistor is placed at the gate of the first-stage transistor to improve stability and input return loss. The second stage has a parallel RC stability network at the gate of each transistor with an added small series resistor at the gate manifold. Additionally, an odd-mode stability resistor is placed between the gates of these two devices. These resistors improve PA stability across the range of drain voltages and power levels with a slight reduction in gain and PAE. The stability of the PA is evaluated using the Nyquist stability criterion at the gate and drain plane of the transistors in the first and second stages. The PA is determined to be stable from 1 MHz to 40 GHz and across drain voltages from 10 V to 28 V.

B. Small-Signal Simulations and Measurements

The measured and simulated S-parameters of the PA in Fig. 10 at a drain voltage of 28 V show good agreement. The measured $|S_{21}|$ peaks at 7.7 GHz with 25.7 dB of gain, and remains above 15 dB from 5.9 to 12.5 GHz. The measured $|S_{11}|$ is less than -10 dB from 5.6 to 12.7 GHz. Additionally, the simulated and measured gain variation for a supply voltage sweep of 14 to 28 V is shown in Fig. 8. Overall, the simulated and measured trends match across frequency, with the simulated gain variation typically higher than measured. At lower frequencies, the $\Delta|G|$ is particularly low and remains below 1 dB from 6 to 7.5 GHz, however, at these frequencies, the $\Delta\phi$ is high. From 8.9 to 13 GHz, the $\Delta\phi$ is low ($<15°$), however the $\Delta|G|$ is higher (>2.2 dB). This seemingly inverse relationship between $\Delta|G|$ and $\Delta\phi$ is consistent with source-pull results in Fig. 4 and results in an approximately flat ΔG across frequency as shown in Fig. 8c. To validate the source/load pull approach presented in section II-A, the $\Delta|G|$, $\Delta\phi$, and ΔG are predicted from the simulated input and output impedances presented to the final stage of a single device. These results are compared to the simulated gain variation from the total two-stage PA in Fig. 8. The impedances are determined by replacing the final stage PA transistors with simulation ports at the gate and drain side. Since the final stage is power combined, the impedance must be determined assuming a symmetrical power split and even mode excitation [38]. Once the impedances are simulated they are implemented

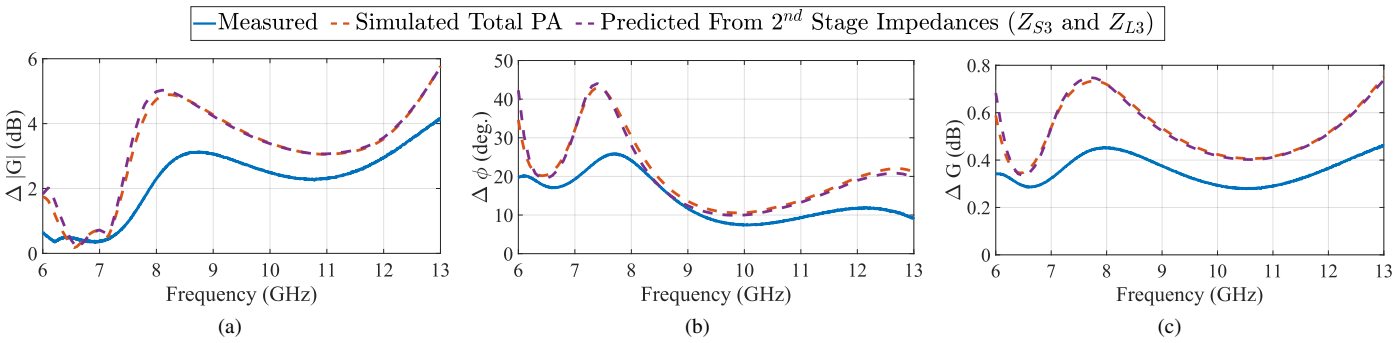


Fig. 8. Measured and simulated small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) vs frequency over a 14 to 28 V range. The predicted gain variation is calculated by implementing the input/output impedance as ideal tuners and cascading them with S-parameters of the final stage transistor at multiple drain voltages as described in section II-A.

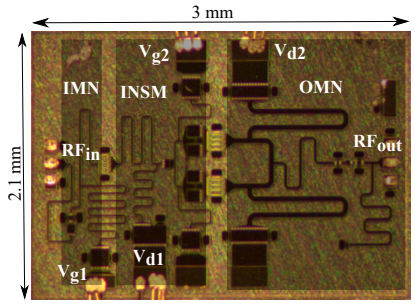


Fig. 9. Photograph of 6 to 12 GHz MMIC PA fabricated in the WIN Semiconductor GaN on SiC NP15 150 nm process.

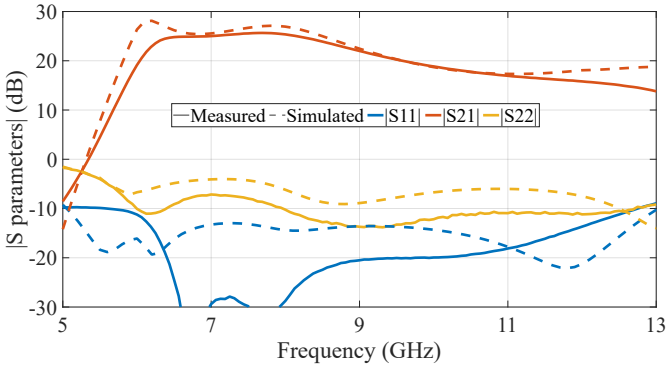


Fig. 10. Measured and simulated S-parameters of the fabricated low gain variation PA at a drain voltage of 28 V

as ideal tuners, and cascaded with the transistor S-parameters at multiple drain voltages as demonstrated in section II-A. The input stability network is separately simulated and cascaded so that the loss can be added appropriately and the PAs stabilized. The $\Delta|G|$, $\Delta\phi$, and ΔG are then determined from the total cascaded network. Since the first-stage drain bias is fixed, it does not contribute to the gain variation. The results obtained from this approach are practically identical to the gain variation found from the total simulated S_{21} of the PA (Fig. 8), with the small deviations likely caused by the asymmetry in the interstage and output matching networks.

C. Large-Signal Simulations and Measurements

The PA is mounted on a copper-molybdenum (CuMo) carrier and measured on a probe station. Large-signal amplitude

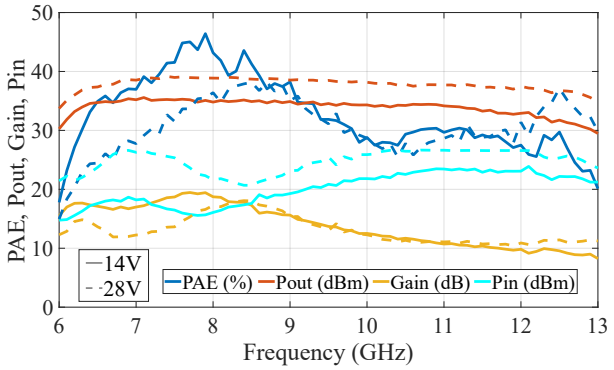
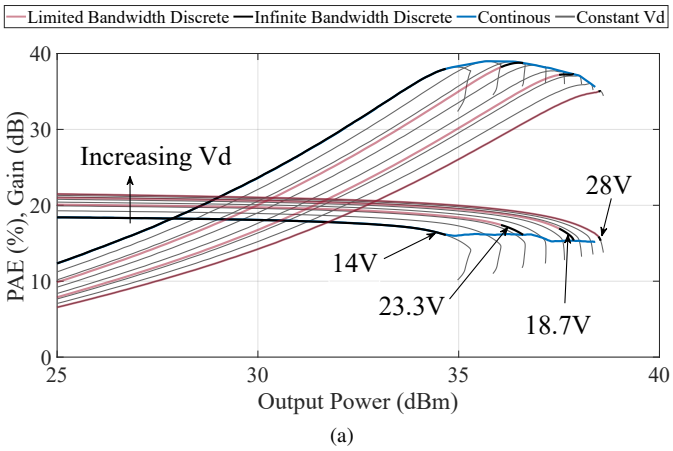


Fig. 11. PAE, gain, output power, and input power vs frequency at drain voltages of 14 and 28 V. Here the input power is selected to yield the highest PAE at each frequency point.

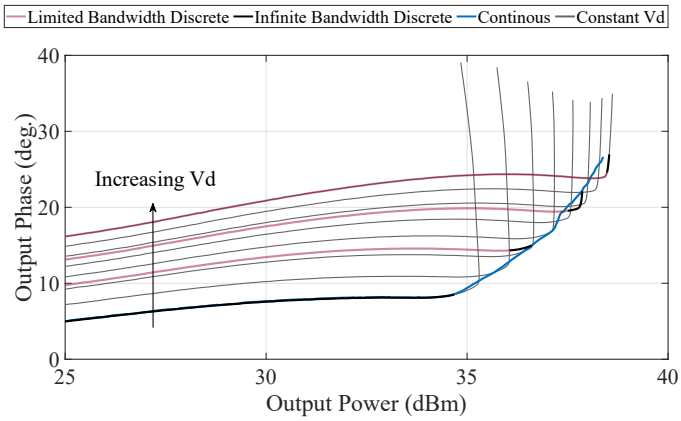
and phase measurements from 6 to 13 GHz are performed in 0.1 GHz steps as a function of input power and drain voltage. The PAE, Gain, output power, and input power are shown vs. frequency in Fig. 11 at drain voltages of 14 and 28 V. From 6.2 to 12.6 GHz, the PAE exceeds 25.6% at 14 V, with a peak PAE of 46.4% at 7.9 GHz and the output power is greater than 36.0 dBm at 28 V. The PAE and gain are plotted vs. output power with multiple drain voltages at 9 GHz in Fig. 12a when a max-PAE shaping function is applied. Additionally, the phase is plotted vs. output power in Fig. 12b also at 9 GHz. In Fig. 12a, the PAE peaks at 39.0% at a drain voltage of 16 V, here the PAE peaks at a low drain voltage due to the load mismatch. Small-signal trends in $\Delta\phi$ are a good predictor for large-signal behavior, although the large-signal $\Delta\phi$ at 9 GHz of 24.9° is higher than the small-signal value.

IV. Modulated Drain Voltage Measurements and Experimental Validation

The PA is next integrated with a discrete 4-level MMIC supply modulator fabricated in the same WIN GaN on SiC process, similar to the architecture in [39]. This discrete supply modulator is a multi-level architecture that uses transistor switches to apply four different externally generated voltage levels with over 80% efficiency. The high electron mobility and low parasitics in the MMIC process provide higher switching speeds than commercial off-the-shelf transistors, thus enabling the modulator to track higher signal bandwidths. The device size of each switch is $23\times100\,\mu$m, chosen as a tradeoff between R_{on} and the input/output capacitance while being large



(a)



(b)

Fig. 12. Measured CW PAE, gain, and phase plotted vs output power at 9 GHz and drain voltages ranging from 14 to 28 V in 2 V steps.

enough to supply a maximum current of 1 A. The modulator is designed to be integrated with a 10 W PA with a maximum drain voltage of 28 V. The supply modulator provides a low output impedance past 100 MHz to avoid a linearity penalty due to self-modulation. A block diagram of the testbench with a photo of the MMIC supply modulator is shown in Fig. 13. The maximum PAE discrete shaping functions chosen for this PA and used for the measurements reported in the next section are plotted in Fig. 14 at 6.5, 9, and 11.5 GHz. Since the large signal performance of the PA changes across the bandwidth, the shaping function must be regenerated at each frequency.

A 67.5 MHz 64-QAM signal is generated using an arbitrary waveform generator (AWG), this baseband signal is then upconverted through a vector signal generator (VSG), amplified with a driver, and applied to the input of the PA. Directional couplers on the input and output allow for the power, spectrum, and IQ baseband waveforms to be measured. The dynamic drain voltage is programmed into a bit pattern generator that controls the switches of the discrete supply modulator. The output of the supply modulator is connected to the second-stage drain supply of the PA through a low inductance/capacitance interconnect. Additionally, the baseband signal and drain voltage waveforms are aligned by applying a delay to the trigger of the AWG. Details on the alignment process can be found in [4]. The PA is mounted on a CuMo carrier with 50 Ω alumina lines on the input/output. These

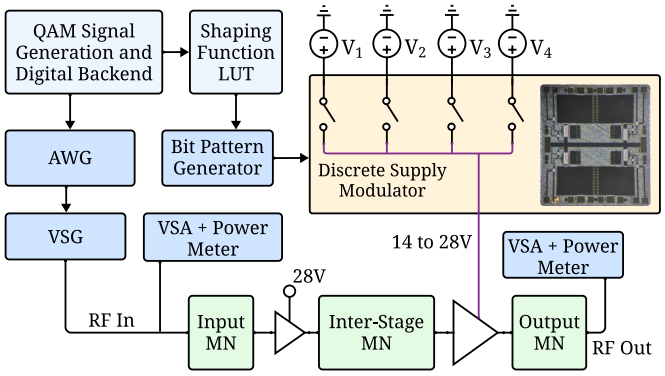


Fig. 13. System block diagram of the measurement system

alumina lines extend to the edge of the CuMo carrier where micro-strip-to-coax transitions connect. The loss and mismatch due to the alumina lines, bond wires, and transitions result in approximately 1 dB lower gain than when measured on the probe station.

A. Discrete Supply Modulated Results

The PA is measured with a dynamic drain voltage and compared to the case of a static 28 V drain voltage using the 67.5 MHz 64-QAM signal from section II-B. The efficiency, gain, EVM, and right-side adjacent channel power ratio (ACPR) are shown in Fig. 15 plotted vs. output power with the maximum switching frequency of the supply modulator set to 100 MHz. The ACPR is calculated using a 8.85 MHz guard band between 50 MHz channels. The composite power added efficiency (CPAE) takes into account the efficiency of the supply modulator and the PA, and the PAE refers to the efficiency of the PA with the supply modulator losses de-embedded. Both efficiencies are averaged over one signal period. With a dynamic drain supply, the peak PAE and CPAE improvement is 10.6% points and 6.8% points occurring at an output power of 31 dBm while the gain, EVM, and ACPR are degraded by 2.8 dB, 1.7% points, and 3.7 dB, respectively.

Using the custom envelope simulator presented in section II-B the PAE, gain, output power, EVM, and ACPR can be predicted with a high accuracy. Here, the envelope simulator

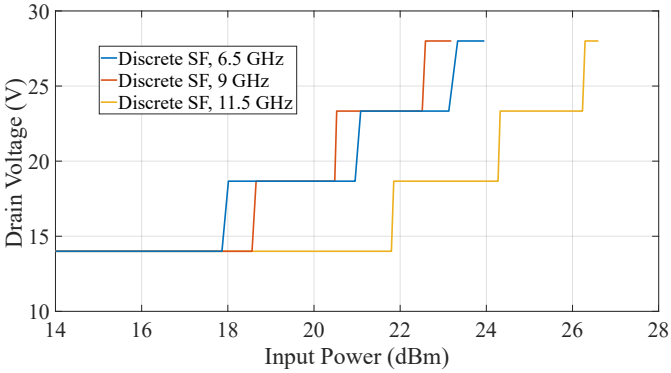


Fig. 14. Discrete shaping functions of the PA at 6.5, 9, and 11.5 GHz.

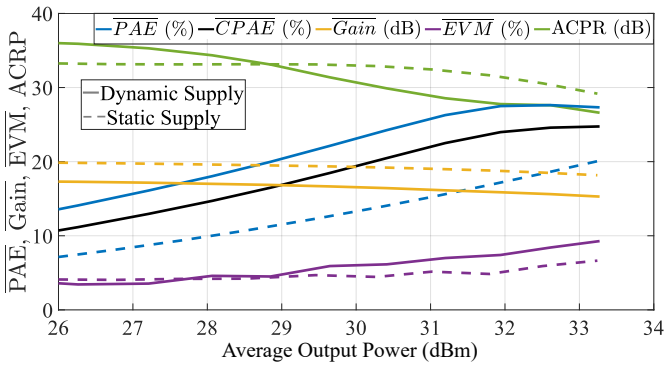


Fig. 15. Measured PA performance comparing a static 28 V supply and a dynamically changing supply at 9 GHz. The CPAE is the power-added efficiency with the losses in the supply modulator included.

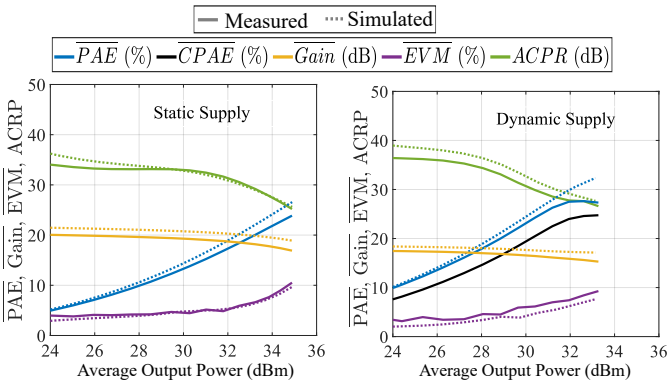


Fig. 16. Comparison of predicted and measured PA efficiency and linearity at 9 GHz amplifying a 67.5 MHz 64-QAM signal with (a) static 28 V supply and (b) dynamically changing four-level supply with a maximum switching frequency of 100 MHz.

uses measured CW large-signal probe-station data presented in section III-C. The measured and predicted PAE, Gain, EVM, and ACPR are compared to a static 28 V supply in Fig. 16a, and dynamic supply switching at a maximum of 100 MHz in Fig. 16b. In both cases, we see good agreement between the predicted and measured linearity and PAE. Since the simulated results are derived from large-signal on-wafer measurements, the gain is slightly higher than the measured data which uses a wire-bonded coaxially-connected MMIC PA.

The envelope simulator is used to predict supply modulation results from 6 to 13 GHz as shown in Fig. 17. Across frequency, the input power is adjusted to obtain a constant output power of 31 dBm. The discrete supply modulator is limited to maximum switching frequencies of 100 MHz (greater than the signal bandwidth) and 25 MHz (about three times lower than the signal bandwidth). The EVM and ACPR are shown in Fig. 17a. The PAE and gain are shown in Fig. 17b. Additionally, the measured points are plotted at frequencies of 6.5, 9, and 11.5 GHz for the static and dynamic drain voltage cases. In Fig. 17 we see that with a switching frequency of 100 MHz the EVM is nearly the same as the static supply case across the band, and at some frequencies shows an improvement in EVM without the use of DPD. The PAE is nearly the same for the two switching speeds and is improved at all frequencies over the static case with the largest improvement occurring at the lower frequencies (6 to 9 GHz). The EVM however is degraded with the slower switching speed but remains below 10% across the band. Additionally, the gain with a dynamic supply is lower than the static supply gain from 8 to 13 GHz.

Conclusion

In transmitters that use discrete supply modulation for efficiency enhancement, the bandwidth of the drain supply modulator is often limited. The limited switching speed and discretized voltage of the supply modulator distorts the PA gain magnitude and phase which adds to AM-AM and AM-PM non-linearities. Here we demonstrate that the distortion can be reduced by mismatching the input and output impedance. This is first shown in the simulated source/load pull of a standalone transistor from which three different matching cases are examined through simulations. Comparing these cases in simulation using a custom behavioral model and a 64-QAM signal, it is shown that a PA with intentionally mismatched input and output impedances is more efficient than a conventional PA when using discrete, bandwidth–limited supply modulation for the same 5% EVM limit. Additionally, envelope simulations reveal that bandwidth limitations on the supply have a larger impact on error vector magnitude than on PAE, gain, and output power. The comparison between the three cases shows that non-linearities created from bandwidth limitations in the supply can be reduced through mismatching for low gain variation.

To validate simulation results and the advantage of designing for low gain variation, a two-stage 5 W GaN on SiC MMIC PA is fabricated covering a bandwidth of 6.2 to 12.6 GHz with intentionally mismatched source and load impedances of the final stage. S-parameter measurements show low small signal gain variation across drain voltage which holds for the entire bandwidth and is accurately predicted from the input/output impedances presented to the final stage of the PA. The PA is measured with a 67.5 MHz 64-QAM signal with a dynamic drain voltage generated from a four-level discrete GaN MMIC supply modulator. The measured PAE, gain, and linearity are compared to predicted results from the behavioral model envelope simulator showing good agreement. In conclusion, matching PAs for low gain magnitude and phase variation instead of maximum PAE and gain can improve the linearity and efficiency of a transmitter with discrete supply modulation even for signals that have a high bandwidth relative to that of the supply modulator and without the aid of DPD.

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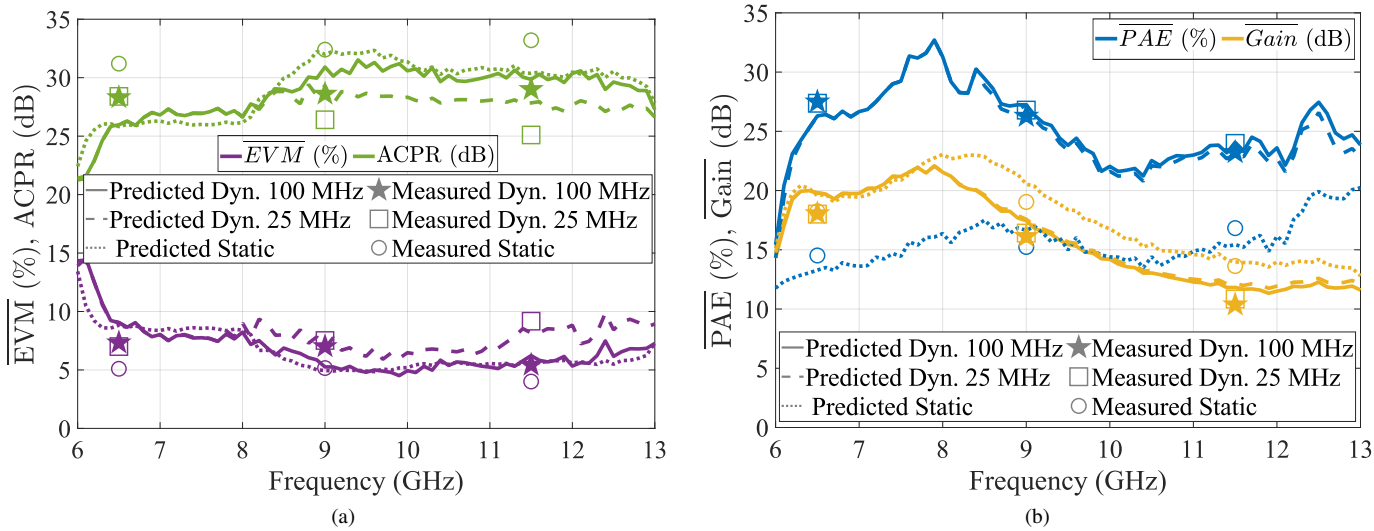

Fig. 17. Measured and predicted results comparing a static 28 V supply to a dynamically changing drain supply with two maximum switching frequencies of 100 MHz and 25 MHz in terms of (a) linearity and (b) PAE and gain, for a constant output power of 31 dBm. The measured points are plotted at frequencies of 6.5, 9, and 11.5 GHz for the static (circle symbols) and dynamic 100 MHz (star symbol) and 25 MHz (square symbol) drain voltage cases.

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