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A Multiport Power Electronic Transformer Based on Three-Phase Four-Arm Full-bridge Modular Multilevel Converter

Sizhao Lu, *Member*, *IEEE*, Jian Deng, Siqi Li, *Member*, *IEEE* , Yumeng Shao and Kai Li, *Member*, *IEEE*

***Abstract*-This paper presents a multiport power electronic transformer (PET) based on a three-phase four-arm full-bridge modular multilevel converter (MMC), which is suitable for the hybrid AC/DC distribution grid because it can provide four ports, including medium-voltage AC and DC ports, low voltage DC and AC ports. Compared with the conventional MMC-based PET, which adopts three-phase six arms MMC with full-bridge submodules (FBSMs), the proposed PET uses three-phase four arms MMC with FBSMs, which can reduce the number of submodules. Meanwhile, the modulation index can be increased and the DC-bus voltage utilization can be improved. In addition, the concentrated capacitor on the medium-voltage DC port is eliminated in the proposed PET, so high transient discharging current from the concentrated capacitor can be avoided under the DC-bus short-circuit condition. The operating principle, applied control strategy and PWM scheme are presented in detail. The proposed PET is investigated and simulated in a hybrid 10 kV AC/±10 kV DC distribution grid. A scale down experimental test is also performed. Simulation and experimental results confirm the feasibility and validity of the proposed PET and control method.**

***Index Terms*-Power electronic transformer, modular multilevel converter, hybrid AC/DC distribution grid, modulation index, DC-bus short-circuit protection.**

I. Introduction

In order to reduce the environmental unfriendliness of fossil fuels, more and more renewable energies, such as solar and wind power, are integrated into the distribution grid. The hybrid AC/DC distribution grid is promoted to cope with the challenges induced by integrating of large-scale renewable energy into the distribution grid [1]. Power electronic transformers (PETs) are considered to be suitable for the hybrid AC/DC distribution grid [2], because it is a multiport equipment and it can integrate functions such as power regulation and control, voltage conversion, electrical isolation and renewable energy integration [3]. A typical hybrid AC/DC distribution grid based on the multiport PET is shown in Fig. 1 [4-6], in which multiport PET provides medium-voltage AC (MVAC) port, MVDC port, low voltage DC (LVDC) port and LVAC port. In Fig.1, the optional distributed energy storage device (DESD) and distributed renewable energy resources (DRERs) can be integrated into LVDC port.

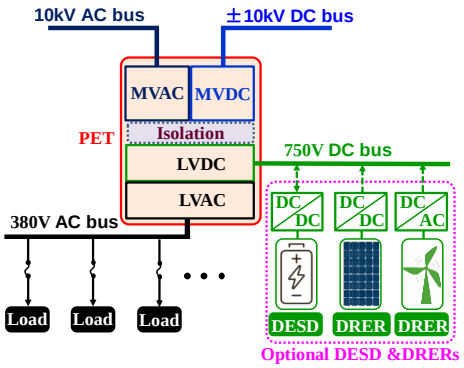

Fig. 1. Typical hybrid AC/DC distribution grid based on the multiport PET.

There are numerous PET topologies which are mainly divided into single-stage, two-stage and three-stage. Three-stage PET topology become the most popular for field application because it is superior to one stage and two-stage topology with regard to voltage regulation, current limit, protection, and power factor [3]. Three-stage PET topology can be mainly categorized as the PET based on cascaded H-bridge (CHB) and the PET based on the modular multilevel converter (MMC) [7, 8]. The CHB-based PET lacks the MVDC port, which make it not applicable to a hybrid AC/DC distribution grid [2]. The MMC-based PET intrinsically provides an additional MVDC port, so it can provide MVAC and MVDC ports, LVDC and LVAC ports. MVDC port can be connected to the DC distribution grid [9, 10] or integrate high-power distributed energy systems, such as the photovoltaic farm, wind power plants and battery energy storage systems [1], which make it applicable for hybrid AC/DC distribution grid [2].

For the MMC-based PET, the isolated DC-DC converter (IDDC) can be directly connected to the submodules (SMs) [11, 12]. The disadvantage of this structure is a large number of SMs and IDDCs as well as medium-frequency transformers are employed. If only the number of SMs are considered, it employs four times the number of SMs of the CHB-based PET case [8]. An alternative topology is proposed in [13] by directly connecting the IDDCs to the MVDC port, which can

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S. Lu, J. Deng and S. Li are with the Department of Electrical Engineering, Kunming University of Science and Technology, Kunming 650500, China (email: lusz10@kust.edu.cn; dengjian2100@163.com; lisiqi@kust.edu.cn).

Y. Shao is with the School of Electrical Engineering, Chalmers University of Technology, Gothenburg, 41296, Sweden (e-mail: yumengs@student.chalmers.se).

Kai Li is with the School of Electrical Engineering, Beijing Jiaotong University, Beijing 100044, China (e-mail: kaili@bjtu.edu.cn).

significantly reduce the number of IDDCs and medium-frequency transformers. Consequently, the medium-frequency transformers can be reduced by 44% and the number of total power devices can be reduced by 16 compared with the CHB-based PET case [14, 15]. To improve the power density of the PET, an effective method is reducing the number of SMs [15]. In [16], an MMC with a reduced number of arms is proposed, which is composed of only four arms and considered as a good potential to improve the fault tolerance of the MMC [17]. However, its generated phase voltage is only 57.7% of the conventional three-phase six-arm MMC [16] and the DC-bus voltage utilization is low.

To improve the DC-bus voltage utilization, the half-bridge SMs (HBSMs) can be replaced by the full-bridge SMs (FBSMs) in the MMC, which can achieve a modulation index greater than 1 [18]. The other advantage of FBSM-based MMC is the energy storage requirements of the SM capacitor can be significantly reduced [19]. In [20], the relationship between the FBSM capacitor voltage ripple and the modulation index under suppressed circulating current is derived, which shows the minimum voltage ripple is achieved when the modulation index is equal to 1.414. However, the modulation index and the DC-bus utilization are still low when the three-phase six-arm MMC is employed in some applications, such as the hybrid 10 kV AC/±10 kV DC distribution grid, in which the voltage class is specified by Chinese standard GB/T 40097-2021 [21] and GB/T 35727-2017 [22]. It should be noticed that ±10 kV DC voltage means 20kV DC voltage between P and N in Fig. 2.

To improve the reliability of the hybrid AC/DC distribution grid, PETs which can provide MVDC port short-circuit protection are preferred. However, the MMC based on the HBSMs cannot realize the DC-bus short-circuit handling and ride through capability [23]. Many alternative SM structures are presented to deal with this issue [24], such as the FBSM, the clamp-double SM, the cross-connected SM and the diode clamp SM [25]. Among these SM structures, the FBSM is popular because it does not only overcome the limitations of the HBSM but also provide reactive power support to the AC grid during the DC-bus fault conditions [23]. For the MMC-based PET with directly connecting the IDDCs to the MVDC port [13, 15], even if FBSM-based MMC is employed, the DC-bus short-circuit protection is not easy to realize because the concentrated capacitor will be discharged under the DC-bus short-circuit condition [26, 27], which generates a high transient current. This high transient current should be limited, otherwise the capacitors and the equipment in the circuit would be damaged. In [28], a PET based on a three-phase four-arm MMC is presented, in which the concentrated capacitor is avoided by using indirect connection of the IDDCs. However, IDDCs in [28] are operated with a fixed duty-cycle of 50%. Consequently, the average dc input voltage of the IDDC is only half of the capacitor voltage. Therefore, either the voltage ratings of the input capacitor and primary side power devices are doubled compared with other SMs, or the number of IDDCs is doubled by using the same voltage rating capacitors and power devices as other SMs.

Comparisons of the existing MMC-based three-stage PET topologies for the hybrid 10kV AC/±10 KV DC distribution grid is tabulated in Table I, in which similar voltage rating power devices and DC capacitors are employed. The topologies presented in [13] and [11] are based on the MMC with HBSMs, which employ fewer power devices in the MMC. However, due to the freewheeling effect of diodes in HBSMs [29], these topologies cannot realize DC-bus short-circuit protection because the dc-fault current cannot be immediately cutoff by turning off all power devices. The similar phenomenon also happens in the topologies proposed by [28] with HBSMs and [1] even with FBSMs. To realize DC-bus short-circuit protection, FBSMs are employed in MMCs and the concentrated capacitor introduced by IDDCs should be avoid. However, these requirements usually lead to a large number of FBSMs, a significant increase in the total of power devices, an increased number of transformers and a large number of DC capacitors.

To address aforementioned issues, this paper proposes a multiport PET for a hybrid AC/DC distribution grid based on a three-phase four-arm full-bridge MMC (TFFMMC). It can improve the modulation index and DC-bus utilization, reduce the number of SMs, reduce SM voltage ripple and realize the DC-bus short-circuit protection. The rest of this paper is organized as follows. Section II introduces the structure of the proposed PET and its operating principles. Section III presents the characteristics of the proposed PET. Simulated results based on a hybrid 10 kV AC/±10 kV DC distribution grid are presented in Section IV and the experimental results based on the proposed PET prototype are given in Section V. The conclusions are drawn in Section VI.

TABLE I
COMPARISONS OF EXISTING MMC-BASED THREE-STAGE PET TOPOLOGIES FOR THE HYBRID 10 KV AC/±10 KV DC DISTRIBUTION GRID

Topologies	Number of MMC SMs		Number of FBSM in DC-DC stage	Number of total power devices	Number of total trans.	Number of total DC Cap.	DC-bus short-circuit protection
	FBSMs	HBSMs					
CAS 2012 [13]	0	10×6=60	10×2=20	60×2+20×4+6=206	10	60+20=80	No
MGU 2013 [11]	0	10×6=60	10×6×2=120	60×2+120*4+6=606	60	60+60=120	No
SEU 2017 [28]*†	0	14×4=56	28×2=56	56×2+56×4+6=342	28	56+56=112	No
SEU 2017 [28]※	12×4=48	0	20×2=40	48×4+40×4+6=358	20	48+40=88	Yes
NEPU 2020 [1]	12×6=72	0	12×6=72	72×4+72×4+6=582	72	12×6=72	No
TSFMMC based PET ‡	10×6=60	0	12×2=24	60×4+24×4+6=342	12	60+12=72	Yes
This work	12×4=48	0	12×2=24	48×4+24×4+6=294	12	48+12=60	Yes

* TFFMMC with HBSM. † The DC-bus voltage is increased to 30kV to generate 10kV AC voltage. ※ TFFMMC with FBSM. ‡ The isolation stage is same as this paper.

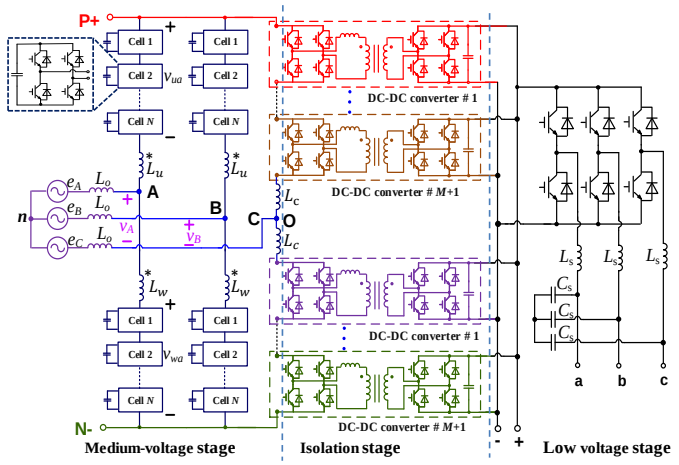


Fig. 2. Topology of the proposed PET.

II. Proposed PET and Its Operating Principles

A. Topology of the proposed PET

The proposed PET topology for the hybrid AC/DC distribution grid is shown in Fig. 2. It includes a MV stage, isolation stage and low voltage stage, which can provide MVAC and MVDC ports, and LVDC and LVAC ports. The MV stage uses the TFFMMC. Each of the three phases includes an upper arm and a lower arm. The upper and lower arms are connected by arm inductors. The arms of phase A and phase B are formed by connecting a series of N identical FBSMs. The third terminal of the MVAC port is led out by the midpoint of the isolation stage. It should be noticed that points 'C' and 'O' represent same point in Fig. 2. Phase-shifted full-bridge converters are employed in the isolation stage, which can avoid the concentrated capacitors on the DC-bus. The isolation stage is divided into an upper arm and a lower arm. Each arm is composed of M+1 power modules (PMs) and these PMs are connected as an input-series-output-parallel converter. The power conversion between the LVDC port and the LVAC port are achieved by an inverter, which consists of six IGBTs. In Fig. 2, e_A, e_B, and e_C represent grid voltage, L_u and L_w are coupled arm inductor for phase A and B, L_c is the arm inductor of phase C and L_o is the input inductor.

B. Mathematic Model of TFFMMC

Assuming the coupled inductor is fully coupled (i.e., L_u=L_w=M_c), the equivalent circuit of phase A or B is shown in Fig. 3(a), where x is equal to A or B. Take phase A as an example, the upper arm voltage and the lower arm voltage can be expressed as

$$\begin{cases} v_{uA} = \dfrac{V_{dc}}{2} - v_{AO} - (L_{uA} + M_c)\dfrac{di_{uA}}{dt} \\ v_{wA} = \dfrac{V_{dc}}{2} + v_{AO} - (L_{wA} + M_c)\dfrac{di_{wA}}{dt} \end{cases} \tag{1}$$

where the v_{AO} is the output voltage of phase A.

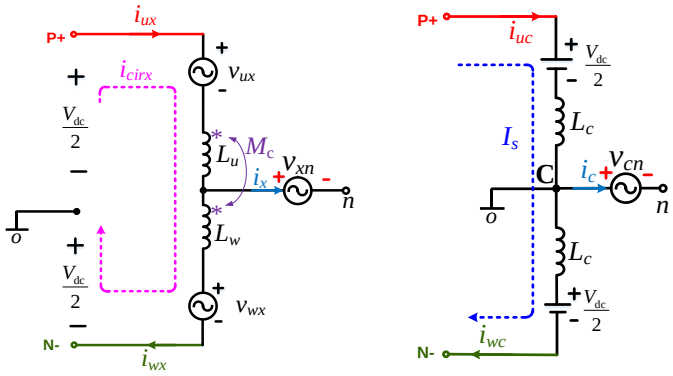


Fig. 3. The equivalent circuit of TFFMMC. (a)The equivalent circuit of phase A or B. (b) The equivalent circuit of phase C.

The upper arm current and the lower arm current can be expressed as

$$\begin{cases} i_{uA} = i_{cirA} + \dfrac{1}{2} i_A \\ i_{wA} = i_{cirA} - \dfrac{1}{2} i_A \end{cases} \tag{2}$$

where i_{cirA} represents the circulating current and i_A represents the output current.

The equivalent circuit of phase C is shown in Fig. 3(b). The upper arm voltage and the lower arm voltage are equal to $V_{dc}/2$, which is guaranteed by the isolation stage. The upper arm current and the lower arm current can be expressed as

$$\begin{cases} i_{uC} = I_s + \dfrac{1}{2} i_C \\ i_{wC} = I_s - \dfrac{1}{2} i_C \end{cases} \tag{3}$$

where i_C represents the output current of phase C, and I_s is the dc bias which represents the transferring power between the MVDC port and the LVDC port.

C. Operating Principle of MV Stage

The MV stage of PET has only four arms and can only form two controllable phase voltages. However, the MVAC port is a three-phase symmetrical 120° system. Therefore, the two-phase reference phase voltages of TFFMMC are different from that of the traditional three-phase six-arm MMC. In Fig. 2, points 'C' and 'O' represent same point, so the phasor diagram for line-to-line voltages and phase voltages are shown in Fig. 4. In Fig. 4, $\dot{V}_{An}$, $\dot{V}_{Bn}$ and $\dot{V}_{Cn}$ are phasors of grid phase voltages, $\dot{V}_{AC}$ and $\dot{V}_{BC}$ are phasors of line-to-line voltages, $\dot{I}_A$, $\dot{I}_C$ and $\dot{I}_C$ are phasors of grid currents, φ is phase angle between the grid phase voltage and the grid current, γ_1 is phase angle between $\dot{V}_{AC}$ and $\dot{I}_A$, γ_2 is phase angle between $\dot{V}_{BC}$ and $\dot{I}_B$.

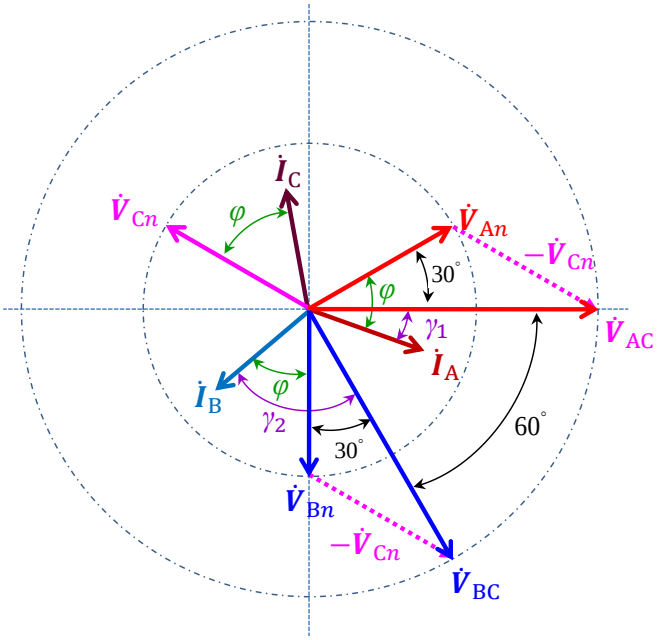


Fig. 4. Phasor diagram for line-to-line voltages and phase voltages.

Assuming the phase of line-to-line voltage $\dot{V}_{AC}$ is zero, then the following equation can be expressed

$$\begin{cases} v_{AC} = v_{AO} = \sqrt{3}V_m \sin(\omega t) \\ i_A = I_m \sin(\omega t - \gamma_1) \\ \gamma_1 = \varphi - \pi/6 \\ \gamma_2 = \varphi + \pi/6 \end{cases} \tag{4}$$

where V_m and I_m is the magnitude of the grid phase voltage and current, ω is the angular frequency of the grid voltage.

Consequently, the grid phase voltages can be expressed as

$$\begin{cases} v_{An} = V_m \sin(\omega t + \pi/6) \\ v_{Bn} = V_m \sin(\omega t - \pi/2) \\ v_{Cn} = V_m \sin(\omega t + 5\pi/6) \end{cases} \tag{5}$$

In the TFFMMC as shown in Fig. 2, the line-to-line voltages are controlled by phase A and phase B, so the two-phase reference phase voltages, v_A and v_B, are given by

$$\begin{cases} v_A = v_{AC} = v_{AO} = \sqrt{3}V_m \sin(\omega t) \\ v_B = v_{BC} = v_{BO} = \sqrt{3}V_m \sin(\omega t - \dfrac{\pi}{6}) \end{cases} \tag{6}$$

It should be noticed that the phase difference between v_A and v_B is 60°, which can be named as the 60° system. According to (5) and (6), the transformation from the three-phase symmetrical 120°system to the 60° system is given by

$$T_{abc/AB} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix} \tag{7}$$

Compared with the grid phase voltages v_{An}, v_{Bn} and v_{Cn} in a three-phase symmetrical system, the amplitudes of the phase voltages v_A and v_B in the equivalent 60° system are 1.732 times of v_{An}, v_{Bn} and v_{Cn}. This is because the phase voltages v_A and v_B are line-to-line voltage of v_{An}, v_{Bn} and v_{Cn}. It should be noticed that the point O in Fig. 2 is floating, so it doesn't mean a grid interfacing transformer must always be installed on MVAC side when AC grid is effectively grounded.

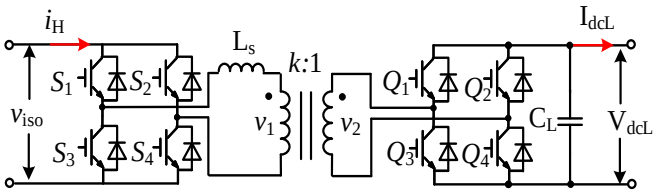


Fig. 5. Circuit diagram of the isolation stage PM.

D. Operating Principle of Isolation Stage and Low Voltage Stage

The circuit diagram of the isolation stage PM is shown in Fig. 5, which consists of two full-bridges, a high-frequency isolation transformer and a LVDC side capacitor. In Fig. 5, v_{iso} represents the input side voltage of the isolation stage PM, and V_{dcL} is the voltage on the LVDC side. L_s is the primary equivalent leakage inductance, v_1 and v_2 represent the primary and secondary side voltages of the isolation transformer, i_H is the input current of the isolation stage PM and I_{dcL} is the output current on the LVDC side.

The modulation scheme of the isolation stage PM is given in Fig. 6, where T_s is the switching period. The LVDC side full-bridge (Q_1-Q_4) adopts the phase-shifted carrier PWM scheme. Two carriers C_1 and C_2 are employed and the phase-shifted angle between these two carriers is δ. The gate signals for Q_1 and Q_2 are generated by comparing the carrier C_1 and C_2 with the duty cycle D. Q_3 and Q_4 are complementarily switched with Q_1 and Q_2, respectively. For the input side full-bridge (S_1-S_4), one carrier C_s is used and a phase-shifted angle δ_s is employed which can be expressed as

$$\delta_s = \frac{\delta}{2} \tag{8}$$

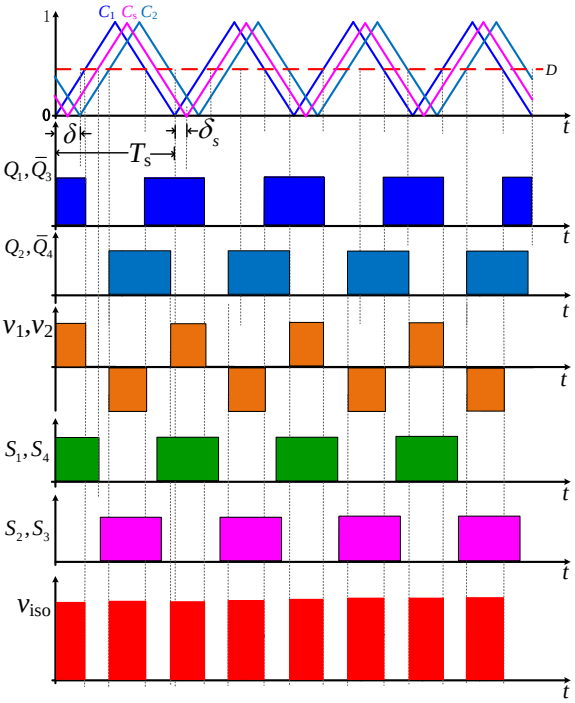


Fig. 6. The modulation scheme of the isolation stage PM.

According to Fig. 6, the input side voltage of each isolation stage PM v_{iso} is a square wave, whose frequency is $2f_s$ (f_s=1/T_s). Its duty cycle can be obtained as

$$d_{PM} = 2\frac{(1-D)T_s - \delta}{T_s} \tag{9}$$

It is obvious that the duty cycle of the PM input side voltage can be changed by controlling the phase-shifted angle δ.

The magnitude of v_{iso} is given by

$$v_{iso\_m} = V_{dcL}\,k \tag{10}$$

where k is the turn ratio of the transformer.

The average voltage of v_{iso} can be expressed as

$$v_{iso\_av} = d_{PM} V_{dcL}\,k \tag{11}$$

The isolation stage is divided into an upper arm and a lower arm, each arm is composed of (M+1) PMs. These PMs are connected as an input-series-output-parallel converter. Meanwhile, according to Fig. 3(b), the upper arm voltage and the lower arm voltage of the isolation stage should be controlled to be equal to V_{dc}/2. Therefore, the operating principle of the isolation stage is illustrated in Fig. 7. In Fig. 7, v_{iso_i} (i=1, 2, …, M, M+1) are the input side voltages of PMs in one arm, ϕ is the phase-shifted angle between two PMs, V_H is the summation of all input side arm voltage, which is equal to V_{dc}/2. At any time, M PMs are engaged and one PM is bypassed, so the duty cycle of the PM input side voltage can also be expressed as

$$d_{PM} = \frac{M}{M+1} \tag{12}$$

The magnitude of the PM input side voltage is given by

$$v_{isom\_i} = \frac{V_{dc}}{2M} \tag{13}$$

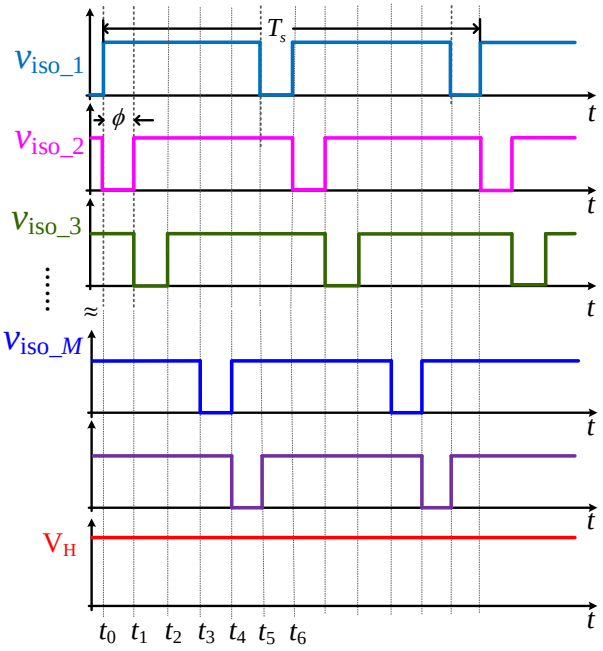


Fig. 7. Operating principle of the isolation stage.

The phase-shifted angle is given by

$$\phi = \frac{1-d_{PM}}{2}T_s = \frac{T_s}{2(M+1)} \tag{14}$$

According to (8) and (11), the following equation can be derived.

$$\delta = \left(1 - D - \frac{M}{2(M+1)}\right)T_s \tag{15}$$

The phase-shifted angles ϕ and δ can be adjusted according to (14) and (15), which can ensure that each arm has M PMs engaged and one PM is bypassed.

According to (10) and (13), the DC voltage ratio can be obtained as

$$\frac{V_{dc}}{V_{dcL}} = 2Mk \tag{16}$$

For the low voltage stage, a three-phase inverter is employed to convert the LVDC to the LV AC. The traditional dq decoupling control strategy and sinusoidal PWM scheme can be applied. Meanwhile, DESD and DRERs can be optionally integrated into LVDC port. During the stand-alone mode, DESD regulates the LVDC bus voltage while it is on power balancing mode during the MV grid-connected mode. DRERs are always on MPPT mode during both the stand-alone mode and the MV grid-connected mode.

E. Power management for the proposed PET

The primary objective of a multiport inverter is to achieve desired power flow among MVAC and MVDC ports, and LVDC and LVAC ports. The power allocations among ports are based on the control commands from the superior dispatch center. According to the control commands, the proposed PET can control power flow among MVAC and MVDC ports, and LVDC and LVAC ports.

Currently, most of load are AC loads, so a typical operation principle of the proposed PET is shown in Fig. 8. The MVAC and MVDC ports can realize bi-directional power flow with a rated power of 7.5MW. The LVAC can output 2.5MW power to the AC loads. A 2.5MW DESD and DERE can be optionally integrated into LVDC port, which can support LVAC loads or the MVAC and MVDC ports. When the DESD and DRERs are not integrated into LVDC port, the AC loads have to draw power from the MVAC and MVDC ports.

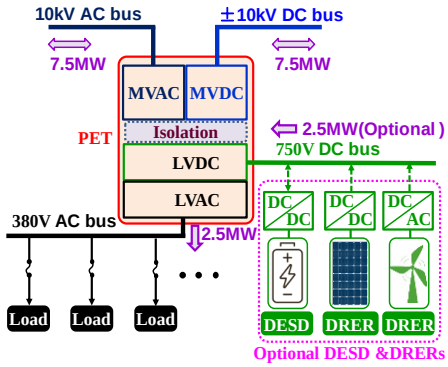


Fig. 8. A typical operation principle of the proposed PET.

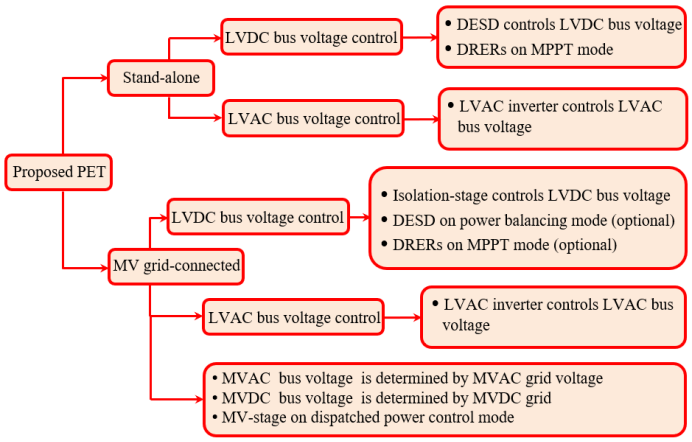


Fig. 9. The power management scheme for the proposed PET.

The power management scheme for the proposed PET is given Fig. 9. When MVAC grid and MVDC grid are not available, DESD and DRERs should be integrated into LVDC bus and the proposed PET is operated at stand-alone mode. DESD controls LVDC bus voltage and DRERs are on maximum power point tracking (MPPT) mode. LVAC bus voltage is controlled by the LVAC inverter. When the proposed PET is connected to MVAC grid and MVDC grid, it is operated at MV grid-connected mode. MVAC bus voltage and MVDC bus voltage are determined by MVAC grid and MVDC grid, respectively. MV stage is on dispatched power control mode. The dispatched power is given by the superior dispatch center. LVDC bus voltage is controlled by the isolation-stage. LVAC bus voltage is still controlled by the LVAC inverter. In MV grid-connected mode, DESD and DRERs are optional. If DESD and DRERs are integrated into LVDC bus. DESD is on power balancing mode and DRERs are on MPPT mode.

F. Control Method of the Proposed PET

The proposed PET includes MV stage, isolation stage and low voltage stage. The isolation stage is operated in open-loop mode as illustrated in Fig. 6 and Fig. 7, where the phase-shifted angles ϕ and δ are determined by (14) and (15). The control block diagrams for the MV stage, TFFMMC, are illustrated in Fig. 10. Fig.10(a) shows the TFFMMC system-level control block diagram, where i_{d}^{*} and i_{q}^{*} are the active reference current and reactive reference current of the HVAC port. i_{d}^{*} and i_{q}^{*} are transferred to i_{A}^{*}, i_{B}^{*} and i_{C}^{*} by a dq/abc transformation. Then three current loops based on dead-beat control [30] are employed to regulate the MVAC port current to follow their commands. Consequently, the voltage commands of the phase A and phase B are generated by using the transformation given by (7). The DC capacitor voltage averaging control of the TFFMMC is illustrated in Fig. 10(b). The average dc capacitor voltage is given by

$$v_{\mathrm{cx}} = \frac{1}{2N}\left(\sum_{j=1}^{N} v_{cujx} + \sum_{j=1}^{N} v_{cwjx}\right) \tag{15}$$

Then DC component of v_{cx} is obtained by using a moving average filter. A PI controller is employed to control the DC component of v_{cx} to follow its command v_{c}^{*}. The DC circulating current command is i_{Zx}^{*}, which is also regulated by a PI controller. Meanwhile, a repetitive controller [31] is employed to suppress the harmonic components in the circulating current. To balance the DC capacitor voltage among the different FBSM, a DC capacitor voltage individual control described in [32] is employed as shown in Fig. 10(c), which regulates the individual DC capacitor voltage follow its command v_{c}^{*}. Moreover, an arm-balancing control is used to ensure that the average voltages of the upper arm $\overline{v}_{cux}$ and lower arm $\overline{v}_{cwx}$ are same [32], which is shown in Fig. 10 (d). The voltage command of each arm is synthesized as shown in Fig. 10(e), where v_{refx} is given by the system-level control as shown in Fig. 10(a). The voltage commands v_{Pjx}^{*} and v_{Njx}^{*} are normalized by each DC capacitor voltage command v_{c}^{*} and a phase-shifted modulation scheme is employed for the TFFMMC.

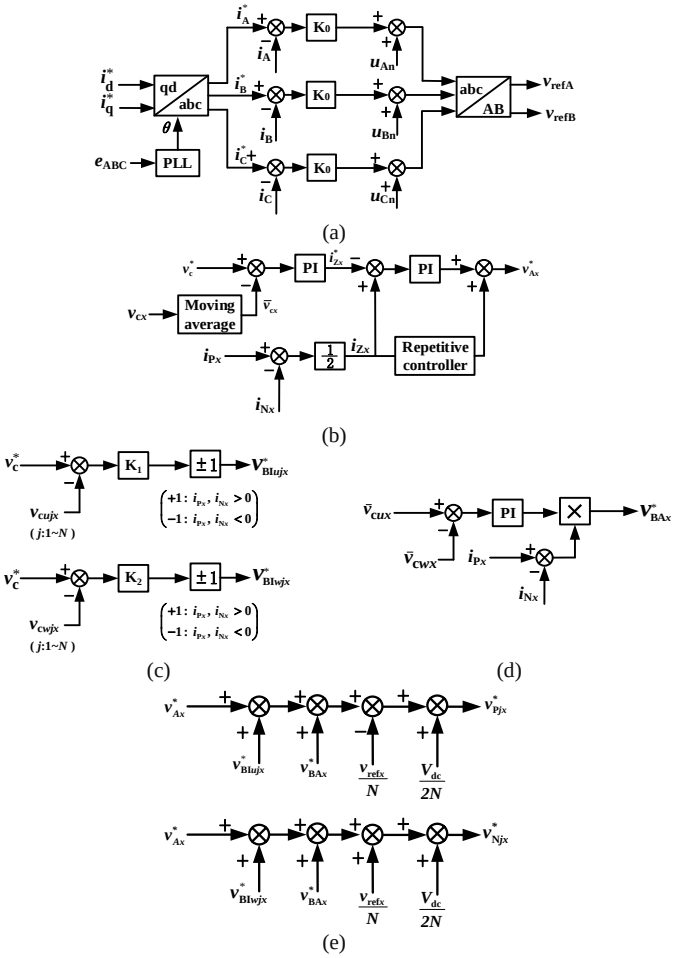


Fig. 10. Control block diagrams for the TFFMMC. (a)TFFMMC system-level control. (b)TFFMMC DC capacitor voltage averaging control. (c) TFFMMC DC capacitor voltage individual control. (d) TFFMMC arm-balancing control. (e) TFFMMC voltage command of each arm.

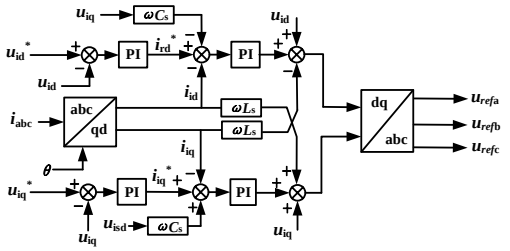
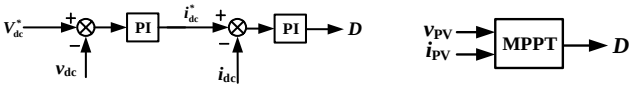


Fig. 11. Control block diagram for the LVAC inverter.



(a) (b)

Fig. 12. A general structure of the control block diagram for the optional DESD and PV-based DRER. (a) Control block diagram for the DESD. (b) Control block diagram for the PV-based DRER.

For the LVAC inverter, the traditional *dq* decoupling control strategy is applied. The control block diagram is shown in Fig. 11, where two outer voltage control loops and two inner current control loops (using d-q axis current control) are employed to regulate the LVAC inverter output voltages and currents. When the LVAC inverter is connected to LVAC grid, only inner current control loops are needed.

When DESD and DRERs are integrated into LVDC port. During the stand-alone mode, DESD regulates the LVDC bus voltage by using an outer voltage control loop and an inner current control loop as shown in Fig. 12(a), where the DC current command i_{dc}^{*} is generated by the outer voltage control loop. During the MV grid-connected mode, the LVDC bus voltage is controlled by the isolation stage, so only an inner current control loop is employed to realize the power balancing control. Therefore, the DC current command i_{dc}^{*} is set according to the power balancing requirement. DRERs are always on MPPT mode during both the stand-alone mode and the MV grid-connected mode. Fig. 12(b) shows MPPT control block diagram of the PV-based DRER.

III. Characteristics of The proposed PET

A. Modulation Index and DC-bus Voltage Utilization Improvement

Based on the operating principle of MMC, the modulation index of the three-phase six-arm full-bridge MMC (TSFMMC) and the TFFMMC can be derived as

$$m_1 = \frac{2V_m}{V_{dc}} \tag{17}$$

$$m_2 = \frac{2V_m}{V_{dc}} = \frac{6V_m}{\sqrt{3}V_{dc}} \tag{18}$$

where m_1 and m_2 are the modulation indexes of the TSFMMC and the TFFMMC, respectively.

In order to validate the characteristics of the proposed PET for the 10 kV AC/±10 kV DC hybrid distribution grid, the system specification is given in Table II. According to (17) and (18), the modulation index for TSFMMC and TFFMMC is calculated as

$$m_1 = \frac{2\times 8165}{20000} = 0.816 \tag{19}$$

$$m_2 = \frac{8165}{20000}\times\frac{6}{\sqrt{3}} = 1.414 \tag{20}$$

From (19) and (20), it can be seen that the modulation index is increased from 0.816 to 1.414 by using TFFMMC. Consequently, the DC-bus voltage utilization is also improved. It should be pointed out that the modulation index of TFFMMC is equal to 1.414, which is a good choice because it can reduce the SM capacitor voltage ripple. The detailed analysis will be presented in part C.

B. Number of SMs Reduction

Regardless of the redundancy SMs for fault tolerance, at the same DC-bus voltage, the number of SMs in each arm can be expressed as [20]

$$\begin{cases} N = \dfrac{V_{dc}}{V_c}, m \le 1 \\ N = \dfrac{(1+m)}{2}\dfrac{V_{dc}}{V_c}, m > 1 \end{cases} \tag{21}$$

where V_c is the voltage of the SM capacitor, and m is the modulation index. It can be seen that the number of SMs is not only determined by the voltage of the SM capacitor, but also by the modulation index.

According to (17) and (18), with the same DC-bus voltage and the same output AC voltage, the following equation can be obtained.

$$\frac{m_1}{m_2} = \frac{1}{\sqrt{3}} \tag{22}$$

Because the FBSM is employed, the modulation index can be greater than 1, so the number of SM in each arm can be expressed as three cases.

The first case is $m_2 \le 1$ and $m_1 \le \sqrt{3}/3$. In this case, the DC-bus utilization is too low, which is not preferred in a real engineering project.

The second case is $m_2 > 1$ and $m_1 \le 1$. In this case, the number of SM for TSFMMC and TFFMMC can be expressed as

$$\begin{cases} N_1 = 6\dfrac{V_{dc}}{V_c}, m_1 \le 1 \\ N_2 = 4\dfrac{(1+m_2)}{2}\dfrac{V_{dc}}{V_c}, m_2 > 1 \end{cases} \tag{23}$$

where N_1 is the number of SM for TSFMMC, and N_2 is the number of SM for TFFMMC. When N_2 is smaller than N_1, it means the number of SM for TFFMMC is fewer than that of the TSFMMC. Therefore, the modulation index range for TFFMMC to use fewer SMs is derived from

$$N_2 - N_1 = 4\frac{(1+m_2)}{2}\frac{V_{dc}}{V_c} - 6\frac{V_{dc}}{V_c} < 0 \tag{24}$$

Consequently, the following equation can be obtained.

$$1 < m_2 < 2 \tag{25}$$

The third case is m_2>1 and m_1>1. In this case, the number of SM for TSFMMC and TFFMMC can be expressed as

$$\begin{cases} N_1 = 6\dfrac{(1+m_1)}{2}\dfrac{V_{dc}}{V_c}, m_1 > 1 \\ N_2 = 4\dfrac{(1+m_2)}{2}\dfrac{V_{dc}}{V_c}, m_2 > 1 \end{cases} \tag{26}$$

The modulation index range for TFFMMC to use fewer SMs is derived from

$$N_2 - N_1 = 4\frac{(1+m_2)}{2}\frac{V_{dc}}{V_c} - 6\frac{(1+m_1)}{2}\frac{V_{dc}}{V_c} < 0 \tag{27}$$

Consequently, the following equation can be obtained.

$$1 < m_2 < 1/(2-\sqrt{3}) \tag{28}$$

From (25) and (28), it can be concluded that the number of SM for TFFMMC is fewer than that of the TSFMMC when $1 < m_2 < 2$.

Therefore, according to (21) and Table II, the SM reduction ratio is calculated by

$$\varepsilon = \frac{[6 - 2\times(1+1.414)]\dfrac{V_{dc}}{V_c}}{6\dfrac{V_{dc}}{V_c}} \approx 20\% \tag{29}$$

It can be seen that the SM number of MMC can be reduced by 20% when TFFMMC is employed in the 10 kV AC/±10 kV DC hybrid distribution grid. This result has also been illustrated in Table I. According to Table I, the number of MMC FBSMs in the TSFMMC based PET is 60, while the number of MMC FBSMs in the proposed PET is 48, so the SM number of MMC can be reduced by 20%.

C. SM Voltage Ripple Reduction

The capacitor voltage ripple for TSFMMC under suppressed circulating current is calculated in [20]. The capacitor voltage fluctuation of the SM is related to the instantaneous power of the arm. Ignoring the voltages on the AC inductors, according to (1) and (4), the upper arm voltage of phase A can be expressed as

$$v_{uA} = (\frac{V_{dc}}{2} - v_{AO}) = \frac{V_{dc}}{2}\left(1 - m_2\sin\omega t\right) \tag{30}$$

Meanwhile, a control strategy is employed to suppress the circulating current harmonic to reduce the RMS value of the arm current. Then, the circulating current of TFFMMC only contains the DC component. According to the definitions illustrated in Fig. 3, the arm current of phase A can be expressed as

$$i_{uA} = I_{cirA} + \frac{1}{2}i_A = I_{cir}\left[1 + \frac{2\sin(\omega t - \gamma_1)}{m_2\cos\gamma_1}\right] \tag{31}$$

where I_{cirA} is the DC component of the circulating current. It is given by

$$I_{cirA} = \frac{(3V_m I_m/2)\cos\gamma_1}{\sqrt{3}V_{dc}} = \frac{S\cos\gamma_1}{\sqrt{3}V_{dc}} \tag{32}$$

where S is the TFFMMC power transmission capacity. The output current is given by

$$i_A = \frac{I_{cirA}}{\cos\gamma_1}\times\frac{4}{m_2}\sin(\omega t - \gamma_1) \tag{33}$$

From (30), (31), (32) and (33), the instantaneous power of the upper arm in phase A can be obtained as

$$p_{uA} = v_{uA}i_{uA} = \frac{S\cos\gamma_1}{2\sqrt{3}}(1 - m_2\sin\omega t)\left[1 + \frac{2\sin(\omega t - \gamma_1)}{m_2\cos\gamma_1}\right] \tag{34}$$

Therefore, the ripple energy stored in the arm capacitors are calculated as

$$\begin{aligned}\Delta E &= \int |p_{uA}| dt \\ &= \int \left|\frac{S\cos\gamma_1}{2\sqrt{3}\omega}(1 - m_2\sin\omega t)\left[1 + \frac{2\sin(\omega t - \gamma_1)}{m_2\cos\gamma_1}\right]\right| d(\omega t)\end{aligned} \tag{35}$$

To calculate ΔE, the zero-crossing points of p_{uA} should be determined first. For TFFMMC, when $m_2 \le 1$, p_{uA} has two zero-crossing points which are defined as θ_1 and θ_2. When m_2>1 and ($m_2\cos\gamma_1$)/2≥1, p_{uA} has two zero-crossing points which are defined as θ_3 and θ_4. When m_2>1 and ($m_2\cos\gamma_1$)/2<1, p_{uA} has four zero-crossing points. These crossing-points are given by

$$\begin{cases} \theta_1 = \pi + \arcsin(m_2\cos\gamma_1/2) + \gamma_1 \\ \theta_2 = 2\pi - \arcsin(m_2\cos\gamma_1/2) + \gamma_1 \\ \theta_3 = \arcsin(1/m_2) \\ \theta_4 = \pi - \arcsin(1/m_2) \end{cases} \tag{36}$$

According to [20], the capacitor voltage ripple ξ is given by

$$\xi = \frac{\Delta E}{2NCV_c^2} \tag{37}$$

where N is given by (21).

The capacitor voltage ripple for TFFMMC under suppressed circulating current is given by

$$\xi = \begin{cases} \dfrac{S}{\sqrt{3}CV_cV_{dc}\omega m}\left[1 - \left(\dfrac{m_2\cos\gamma_1}{2}\right)^2\right]^{1.5} & m_2 \le 1 \\ \dfrac{S}{\sqrt{3}CV_cV_{dc}\omega(1+m_2)}\max\left\{\dfrac{2}{m_2}\left[1 - \left(\dfrac{m_2\cos\gamma_1}{2}\right)^2\right]^{1.5}, \right. & \\ \qquad \left. m_2\cos\gamma_1\left(1 - \dfrac{1}{m_2}\right)^{1.5}\right\} & m_2 > 1,\ m_2\cos\gamma_1/2 < 1 \\ \dfrac{S\cos\gamma_1}{\sqrt{3}CV_cV_{dc}\omega(1+m_2)}m_2\left(1 - \dfrac{1}{m_2}\right)^{1.5} & m_2 > 1,\ m_2\cos\gamma_1/2 \ge 1 \end{cases} \tag{38}$$

According to [20] and (38), the relationship between the SM capacitor voltage ripples and the modulation index under unity power factor ($\cos\varphi$=1, $\cos\gamma_1$=0.866) is shown in Fig. 13. The modulation indices for TSFMMC and TFFMMC are calculated in (19) and (20), which are equal to 0.816 and 1.414, respectively. As shown in Fig. 13, compared with TSFMMC with m_1=0.816 (i.e., point A), TFFMMC with m_2=1.414 (i.e., point B) can reduce the SM capacitor voltage ripple ξ to 54.1%. It means the SM capacitance can be reduced to 54.1% with the same ξ.

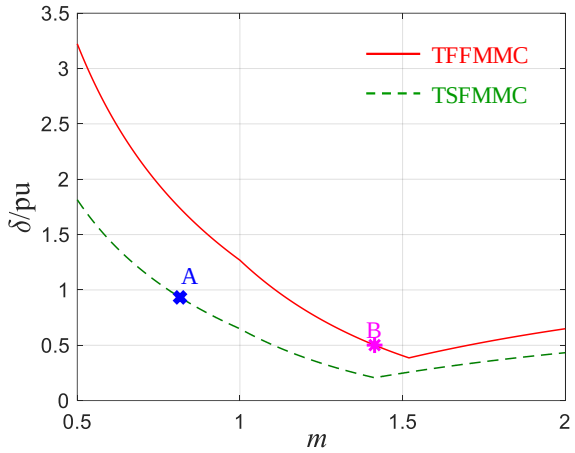


Fig. 13. The relationship between the SM capacitor voltage ripples and the modulation index under unity power factor.

D. DC-bus Short-circuit Protection

Based on the structure and the operating principle of the isolation stage, the concentrated capacitor on the MV DC-bus is eliminated, so a high transient discharging current from the concentrated capacitor can be avoided under DC-bus short-circuit condition. When a DC-bus short-circuit fault occurs, all the power devices are turned off after the fault is detected. The fault current path of the proposed PET is shown in Fig. 14, where the grid voltages are $e_A>0$, $e_B<0$, and $e_C<0$. Because FBSMs are employed in the TFFMMC, the output voltages of the FBSMs are opposite to the grid voltage. The voltages of the phase A upper arm and the phase B lower arm can be expressed as

$$V_{uarmA} = V_{warmB} = -NV_c \tag{39}$$

There are two fault current paths, that is, *n*-A-P-N-B-*n* and *n*-A-P-N-C-*n*. To limit the fault current in the first path, the following equation should be satisfied.

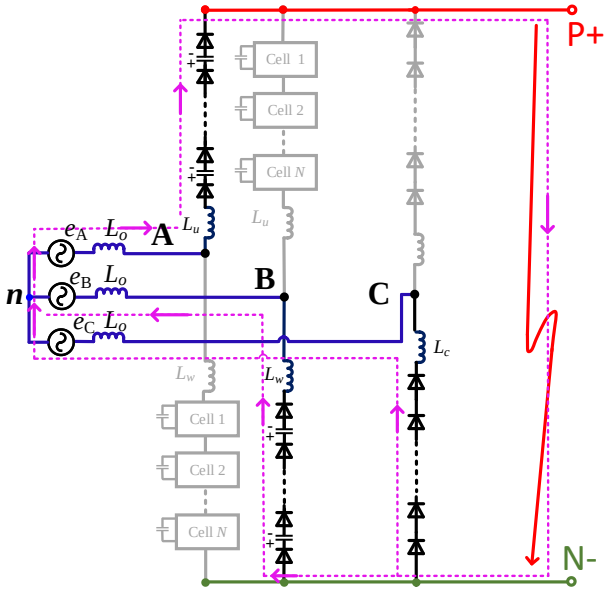


Fig. 14. The fault current path of the proposed PET under DC-bus short-circuit condition.

$$2NV_c > \max(e_A - e_B) = \sqrt{3}V_m \tag{40}$$

To limit the fault current in the second path, the following equation should be satisfied.

$$NV_c > \max(e_A - e_C) = \sqrt{3}V_m \tag{41}$$

According to (18), (21) and (41), the following equation can be derived.

$$NV_c = \frac{1+m}{m}\sqrt{3}V_m > \sqrt{3}V_m \tag{42}$$

The modulation index of the TFFMMC is 1.414, so equation (42) is always satisfied. It means the proposed PET can protect against the DC-bus short-circuit. The energy stored in the inductor will be absorbed by the FBSM capacitor in the arm. Consequently, the fault current is limited and gradually reduced to zero.

IV. Simulation and Calculation Results

In order to verify the validity of the proposed PET, a simulation model is built in MATLAB/Simulink. The optional DESD and DRERs are not integrated in the simulation model because the main focus of this paper is the topology as shown in Fig. 2. System specifications are tabulated in Table II. The number of FBSM employed in the TFFMMC is 48 (12 per arm), while TSFMMC requires 60 FBSMs for the same system.

The voltage and current waveforms of the MVDC port and MVAC port are shown in Fig.15. The MVDC voltage is 20 kV and the input rated DC current is 375 A, so the input power of the system can be calculated as 7.5 MW. The line-to-line voltage waveforms of the TFFMMC and the grid currents are shown in Fig. 15(c) and Fig. 15(d). The grid line-to-line voltage is set to 10 kV, so the modulation index of the TFFMMC is 1.414. The RMS value of the grid current is 288.6 A, so the output power of the MVAC is 5 MW. The FBSM capacitor voltage waveforms, arm currents and the

TABLE II
SYSTEM SPECIFICATIONS

Parameter	Symbol	Value
Rated power	P	7.5 MW
MVDC port voltage	V_{dc}	±10 kV
MVAC port voltage (line-to-line RMS)	V_{ac}	10 kV
The power factor for MVAC port	η	1
Rated line frequency	ω	50 Hz
FBSM voltage	V_c	2185 V
FBSM capacitance	C_{sm}	2.35 mF
Coupled arm inductance	L_u, L_w	5 mH
Arm inductance	L_c	2 mH
MVAC input inductance	L_o	3.3 mH
Number of FBSMs per arm	N	12
Number of PMs per arm	M+1	6
LVDC port voltage	V_{dcL}	750 V
Switching frequency of TFFMMC	f_s	400Hz
Switching frequency of the isolation stage	f_{iso}	2 kHz
Transformer turns ratio	k	20:7.5
Switching frequency of LVAC converter	f_{inv}	5 kHz
LVAC output inductor	L_{LVAC}	0.1 mH
MVAC output power	P_{MVAC}	5 MW
LVAC output power	P_{LVAC}	2.5 MW

circulating current are given in Fig. 16. The average value of the FBSM capacitor voltage is 2185 V and the fluctuation of the FBSM capacitor voltage is about 148 V, which agrees with (38) and the Fig. 13. The arm currents are two sinusoidal with a DC bias. The circulating current is a DC current without the two-order harmonic.

The transformer primary side current waveforms in one isolation SM at the upper arm and lower arm and arm currents of phase C are shown in Fig. 17(a) and Fig. 17(b), where the outer envelope is the arm current of phase C. The LVDC voltage waveform and the LVAC output currents are shown in Fig. 17(c) and Fig. 17(d). The LVDC voltage is 750 V and the RMS value of the output current of the LVAC port is 3680 A. The LVAC is connected to a 380 V AC grid, so the calculated power of the LVAC port is 2.43 MW, which is a little smaller than 2.5MW. This is because a 0.001Ω equivalent resistor is implemented in the IGBT simulation model and the LVAC output inductor, respectively.

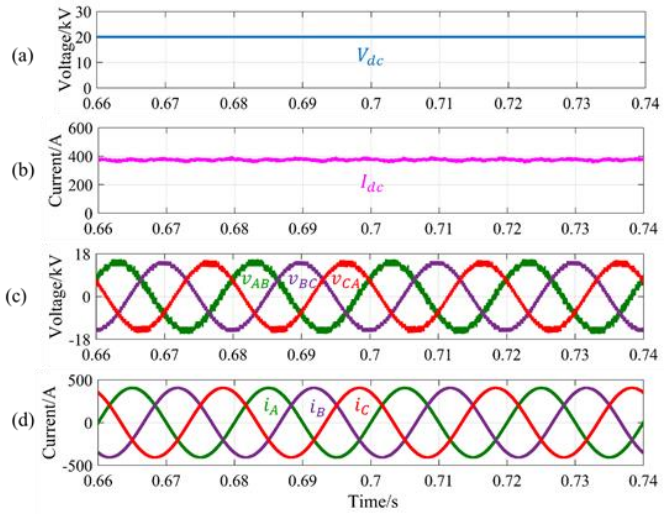


Fig. 15. The voltage and current waveforms of the MVDC port and MVAC port. (a)MVDC voltage waveform. (b) MVDC current waveform. (c) MVAC line-to-line voltage waveforms. (d) MVAC current waveforms.

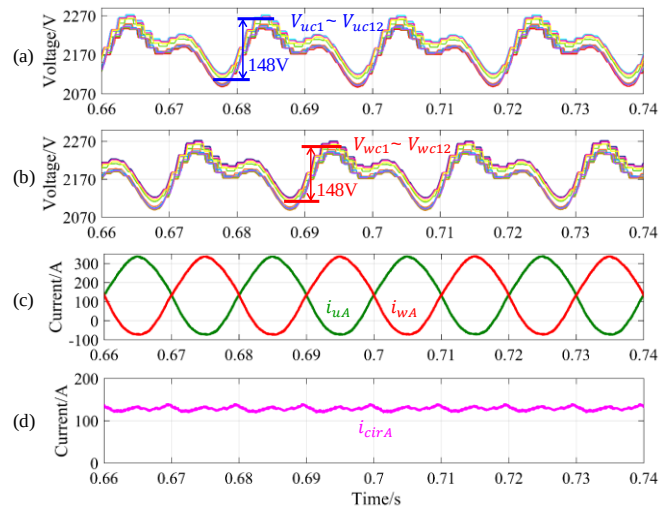


Fig. 16. The FBSM capacitor voltage waveforms, arm currents and the circulating current. (a)Upper arm FBSM capacitor voltage waveforms. (b) Lower arm FBSM capacitor voltage waveforms. (c)Arm current waveforms. (d) Circulating current waveform.

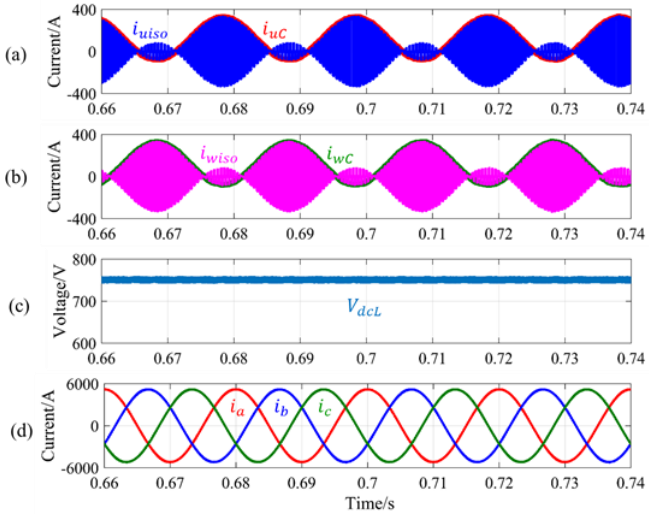


Fig. 17. The transformer primary side current waveforms, arm currents of phase C, LVDC voltage waveform and LVAC current waveforms. (a)The upper arm transformer primary side current and arm current waveforms. (b) The lower arm transformer primary side current and arm current waveforms. (c) LVDC voltage waveform. (b) LVAC current waveforms.

To verify the effectiveness of the proposed PET structure for DC-bus short-circuit protection, the MV stage works in the rectifier mode and a DC-bus short-circuit is simulated at the moment t_{sc}=0.6 s. The short-circuit resistor is set as R_{sc}=12 Ω. After 100 us later, the drive signals of all switches in the PET are blocked. The voltage and current waveforms of the MVDC port is shown in Fig.18. It can be seen that when a short circuit fault occurs, the DC-bus voltage drops rapidly and the current on the MVDC side rises instantaneously. After the converter is

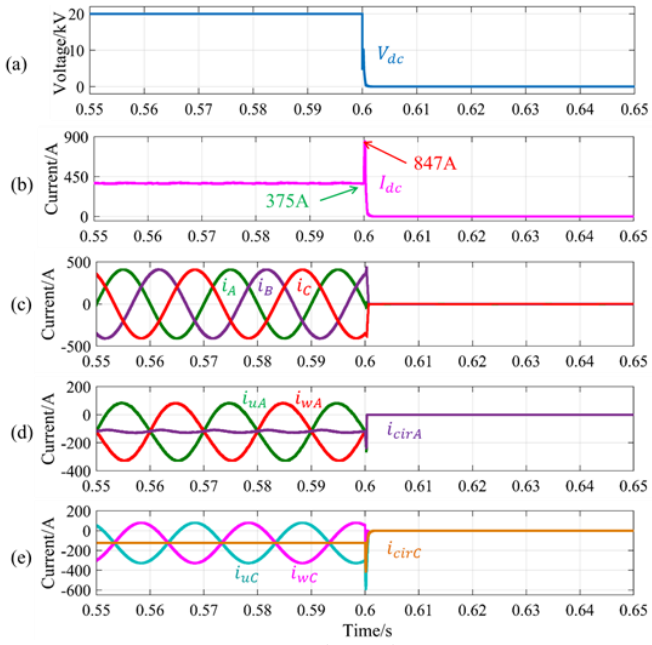


Fig. 18. The voltage and current waveforms of MVDC port under DC-bus short-circuit condition. (a)MVDC voltage waveform. (b) MVDC current waveform. (c) MVAC current waveform. (d) Arm currents waveform of phase A. (e) Arm currents waveform of phase C.

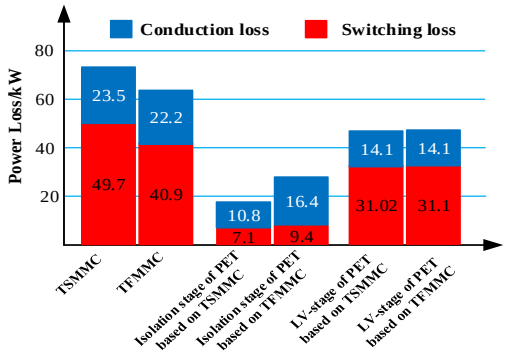


Fig. 19. Power device losses comparisons of TFFMMC-based PET and TSMMC-based PET.

blocked, the fault current on the MVDC port is gradually reduced to zero. The peak value of the inrush current is 847A as shown in Fig. 18(b), which is about 2.26 times the rated DC current. Meanwhile, IGBT module, FZ825R33HE4D, is employed in the MV stage and isolation stage. The repetitive peak collector current of FZ825R33HE4D is up to 1650A. Therefore, the proposed PET can survive from the DC-bus short-circuit. This proves that the proposed PET can deal with the DC-bus short-circuit fault.

To highlight the loss reduction advantage of the proposed PET, a simple loss calculation method is employed [33]. The loss calculation is embedded into the MATALB/Simulink simulation model. The main parameters of the simulation model are given in Table II. Meanwhile, four IGBT modules, FF1800R12IE5, are paralleled to boost the current rating of the power device in the LVAC inverter. The parameters extracted from the datasheets of the IGBT module are employed in the calculation. At the power level of 7.5MW, the power device losses comparisons are illustrated in Fig. 19. For the MV stage, the device loss of the TFFMMC is 63.1kW, which is reduced by 13.80% compared with the TSMMC because fewer FBSMs are employed in the TFFMMC. For the isolation stage, the device loss of the TFFMMC-based PET is higher than that of the TSMMC-based PET because the arm current of phase C in the TFFMMC contains a line frequency current component, which induces higher device losses. For the LVAC inverter, the TFFMMC-based PET has the similar device losses as the TSMMC-based PET. Consequently, the total device loss of the proposed PET is reduced by 1.6% compared with the TSMMC-based PET.

V. Experimental Results

To verify the effectiveness of the proposed PET, an experimental setup is built as shown in Fig. 20. The specification of the experimental setup is tabulated in Table III. The rated power of the experimental setup is 1kW. The experimental waveforms are shown in Fig. 21 to Fig. 24. In Fig. 21(a), the MVDC port voltage and current waveforms are given. The DC voltage is 200 V and the DC current is about 5.2 A. The TFFMMC outputs line-to-line voltage waveforms are shown in Fig. 21(b), which are multilevel waveforms. The voltage and current waveforms of the MVAC port are shown in Fig. 22(a). The RMS value of MVAC port line-to-line voltage is 141 V, so the modulation index of TFMMC is around 1.414. The currents of MVAC port are good sinusoidal waveforms. The capacitor voltages of FBSMs in the phase A are shown in Fig. 22(a), which are well balanced. The average value of the FBSM capacitor voltage is about 131V. The arm currents and circulating current of phase A are also shown in Fig. 22(b). The arm current is a sinusoidal waveform with a DC bias. The circulating current is a DC current because the odd-order harmonic is suppressed by the repetitive controller as shown in Fig. 10(b).

The transformer primary side current waveforms in one isolation SM at the upper arm and lower arm and arm currents of phase C are shown in Fig. 23(a) and Fig. 23(b), respectively. The outer envelope of the transformer primary side current is the AC component of the phase C arm current. It should be noticed that there is a DC bias in the phase C arm current as shown in Fig. 23(b), which represents the transferring power between the MVDC port and the LVDC port. The current of phase C is calculated by (3) and it is a good sinusoidal current waveform as shown in Fig. 23(b). The LVDC voltage

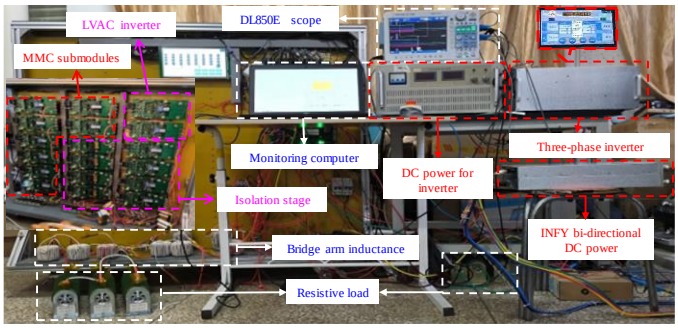


Fig. 20. Picture of the experimental setup.

TABLE III
SPECIFICATIONS OF PROPOSED PET PROTOTYPE

Parameter	Symbol	Value
Rated power	P	1kW
MVDC port voltage	V_{dc}	±100 V
MVAC port voltage (line-to-line RMS)	V_{ac}	100 V
The power factor for MVAC port	η	1
Rated line frequency	ω	50 Hz
Rated FBSM voltage	V_c	131 V
FBSM capacitance	C_{sm}	2.35 mF
Coupled arm inductance	L_u, L_w	1 mH
Arm inductance	L_c	0.1 mH
MVAC input inductance	L_o	1.5 mH
Number of FBSMs per arm	N	2
Number of PMs per arm	M+1	2
LVDC port voltage	V_{dcL}	100 V
Switching frequency of TFFMMC	f_s	5 kHz
Switching frequency of the isolation stage	f_{iso}	10 kHz
Transformer turns ratio	k	1:1
Switching frequency of LVAC converter	f_{inv}	20 kHz
LVAC output inductor	L_{LVAC}	1 mH

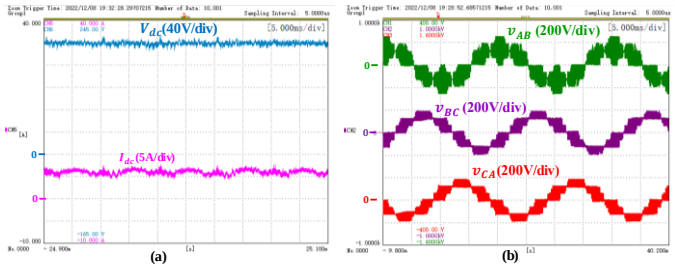


Fig. 21. The voltage and current waveforms of the MVDC port and MVAC port. (a)MVDC voltage and current waveforms. (b) MVAC port output line-to-line voltage waveforms.

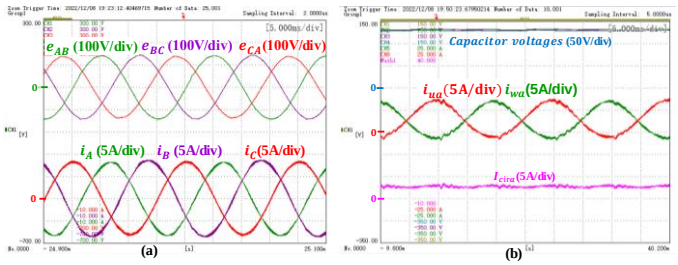


Fig. 22. The voltage and current waveforms of MVAC port, capacitor voltage waveforms, arm currents and the circulating current. (a)MVAC grid-side line-to-line voltage and current waveforms. (b) capacitor voltage waveforms, arm currents and the circulating current.

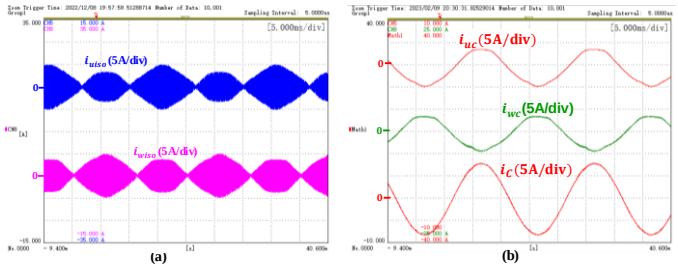


Fig. 23. The voltage and current waveforms of the isolation stage. (a) Transformer primary side current waveforms in one isolation SM at the upper arm and lower arm. (b) Arm and output current waveforms of phase C.

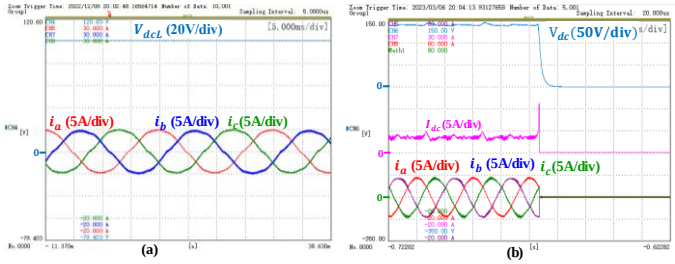


Fig. 24. The voltage and current waveforms of the LVDC port, LVAC port and MVDC port. (a) LVDC port voltage and LVAC port output current waveforms. (b) MVDC port voltage and current waveforms under DC-bus short-circuit condition.

waveform and the LVAC inverter output currents are shown in Fig. 24(a). It can be seen that the LVDC voltage is stable and its value equals to 100 V, and the LVAC inverter output currents are sinusoidal waveform.

The DC-bus short-circuit protection is illustrated in Fig. 24(b), where the TFFMMC works in the rectifier mode and a DC-bus short-circuit is simulated by switching the DC-bus to a resistor R_{sc}=5 Ω. After the short circuit fault occurs, the DC-bus voltage drops rapidly and the current on the MVDC side rises instantaneously. After 240 *us* later, the drive signals of all switches in the proposed PET are blocked, and the fault current on the MVDC port is gradually reduced to zero. It can be seen that the proposed PET has ability to deal with the DC-bus short-circuit fault. The current distortion in Fig. 24 is mainly induced by the control because the non-ideal factors in the hardware prototype.

VI. Conclusion

A multiport PET based on TFFMMC and its operating principles are presented in this paper. The advantages of the proposed PET include improving the modulation index and DC-bus voltage utilization, reducing the number of submodules by 20%, reducing the SM voltage ripple and protecting against the DC-bus short-circuit. Simulations based on a 10 kV AC/±10 kV DC hybrid distribution grid and tests based on a scale down experimental setup are performed, which confirm the feasibility and validity of the proposed PET and control method.

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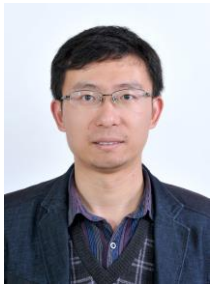
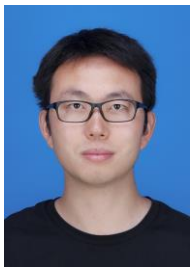
Sizhao Lu (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2008 and 2010, respectively, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2016. He became an Associate Professor at the Department of Electrical Engineering, Kunming University of Science and Technology, Kunming, China, in 2019. He was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, from February 2012 to November 2013. His research interests include modular multilevel converters (MMCs), solid-state transformers, and high-frequency high-power three-level dc–dc converters.

Jian Deng received the B.S. degree in motors and appliances in 2017 from the School of Electrical and Control Engineering, North University of China, Shanxi, China. He is currently working toward the M.S. degree in electrical engineering, Kunming University of Science and Technology, Kuming, China. His main research interests include modular multilevel converters (MMCs), solid-state transformers, dc–dc converters, and wireless power transfer.



Siqi Li (Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2004 and 2010, respectively. He was a Postdoctoral Fellow with the University of Michigan, Dearborn, MI, USA, from 2011 to 2013. He was a Visiting Scholar at San Diego State University, San Diego, CA, USA, from 2018 to 2019. In 2013, he joined the Faculty of Electric Power Engineering, Kunming University of Science and Technology (KUST), Kunming, China, where he is currently a Professor in the Department of Electrical Engineering. He is also the Director of the Advanced Power Electronics and New Energy Laboratory, KUST. His research interest focuses on battery management systems, high-performance wired, wireless battery chargers for electric vehicles, and solid-state transformers.

Yumeng Shao received the B.S. degree in electrical engineering from Shandong University of Technology, Zibo, China, in 2016, and the M.S. degree in electrical engineering from Kunming University of Science and Technology, Kuming, China, in 2021. She is currently studying at Chalmers University of Technology, Gothenburg, Sweden. Her research interests include modular multilevel converters, solid-state transformers, and the application of power electronics in electric drive systems.



Kai Li (Member, IEEE) received the B.S. degree in electrical engineering from Wuhan University, Wuhan, China, in 2011, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2017. He was a Visiting Scholar with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, from 2013 to 2015. He was a Post-Doctoral Fellow with Tsinghua University, from 2017 to 2019. In 2019, he joined the School of Electrical Engineering, Beijing Jiaotong University, Beijing, where he is currently an Associated Professor with the School of Electrical Engineering. His current research interests include solid-state transformer, railway electrification system, modular multilevel converters, and electrolytic hydrogen production converters.