Electrodes for High-κ Molecular Crystal Antimony Trioxide Gate Dielectrics for 2D Electronics

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Electrodes for High-κ Molecular Crystal Antimony Trioxide Gate Dielectrics for 2D Electronics

Alok Ranjan, Lunjie Zeng, and Eva Olsson**

Wafer-scale deposition of high-κ gate dielectrics compatible with atomically thin van der Waals layered semiconductors (e.g., MoS_2, WS_2, WSe_2) is urgently needed for practical applications of field effect transistors based on 2D materials. A study on a high-κ molecular crystal antimony trioxide (Sb_2O_3) gate dielectric examined the role of electrode material on dielectric degradation and breakdown. It is demonstrated that the thin films of Sb_2O_3 can be uniformly deposited on a wafer scale. The current–voltage (I–V) curves show tightly controlled distributions of both leakage current and breakdown voltage. Electrical measurements reveal that defects are generated gradually upon electrical stressing. The evaluation of degradation is based on charge trapping, stress-induced leakage current, and dielectric breakdown measurements. The breakdown voltage distribution follows a tight monomodal Weibull distribution suggesting a high quality of the film. Comparing Ti and Au as gate electrodes, both the breakdown field and the tunnel current are affected by the choice of electrode material. Transmission electron microscopy reveals that the chemistry at the electrode/Sb_2O_3 interface plays an important role and that Ti scavenges oxygen from the Sb_2O_3, forming a defective oxide layer at the Ti/Sb_2O_3 interface. For the Au electrode, this interfacial reaction is completely absent, improving the dielectric performance.

1. Introduction

There has been a continuous improvement in the performance of the field effect transistor (FET) in the last few decades.[1] Silicon has been a material of choice as a channel due to its modest carrier mobility and ability to form a high-quality semiconductor-dielectric interface.[2,3] The state-of-the-art gate-all-around nanosheet FET has been introduced at the 5 nm technology node, where only a handful of atoms in the channel control its performance.[4,5] With the FETs reaching the physical limits of scaling, new materials and device architectures are actively explored. Atomically thin van der Waals layered materials (also called two dimensional (2D) material) have demonstrated an enormous potential to realize energy-efficient and ultrafast electronic and optical devices.[6–10] FETs based on the 2D semiconductors (e.g., MoS_2, WS_2, WSe_2) have a higher intrinsic carrier mobility[11,12] compared to Si and they have also been shown to mitigate the short channel effects in ultra-scaled devices.[13,14] The successful integration of transistors based on the 2D materials in integrated circuits requires engineering the growth of high-quality 2D crystals on a wafer scale, understanding the physics of the semiconductor-dielectric interfaces, understanding the contact at the semiconductor-bulk metal interface, and addressing the reliability of the devices. One immediate challenge is to find a suitable gate dielectric, which could be seamlessly integrated with these emerging 2D semiconductors.[15–17]

Hexagonal Boron Nitride[18] (h-BN) is an interesting material since it has been used as an atomically flat substrate,[19] an encapsulating layer,[12,20] and a gate dielectric in the prototype devices.[21–24] The h-BN forms a clean and defect-free van der Waals interface with the majority of the reported 2D semiconductors.[20] However, h-BN fails to meet the stringent requirements when 2D material-based transistors are scaled down.[16,17] This is because the gate dielectric thickness must be proportionately scaled as the transistor dimensions shrink in order to provide the capacitance effect. It has been found that the off-state leakage current becomes prohibitively higher in ultra-scaled devices, rendering h-BN unsuitable to be used as an effective gate dielectric. For example, the physical thickness of h-BN is ≈1.3 nm at the effective oxide thickness (EOT) of 1 nm and the leakage current density (J) exceeds ≈10 A m^{-2} (at 1 V) due to direct tunneling.[17] An alternate strategy is to use a high-κ dielectric, akin to Si technology,[3] as a physically thick dielectric can be used for the sub-1 nm EOT-scaled FETs.

There have been efforts to grow the high-κ gate dielectrics, e.g., HfO_2, Al_2O_3, etc. directly on the 2D layered materials using atomic layer deposition (ALD).[25] The resulting dielectric films are inhomogeneous and also have poor coverage. This is because

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202400205

DOI: 10.1002/aelm.202400205

the surface of 2D materials is chemically inert to the ALD process, inhibiting the promotion of minimum nucleation sites required to grow a continuous thin film. Surface modification of the 2D materials through plasma[26] and ozone[27] treatment has shown improvements in the quality of the ALD-deposited dielectric films. However, exposure to either plasma or ozone also affects the crystallinity of the atomically thin 2D semiconductors and severely reduces their carrier mobility.

An interfacial seeding layer[28] deposited prior to ALD has been shown to promote the density of nucleation sites on the 2D semiconductors. These seeding layers typically have a low-κ dielectric constant and therefore the overall dielectric constant achieved is then lower than that of the pristine ALD dielectric films. Alternatively, native oxides have been also grown directly on the 2D materials.[29–32] For example, the Bi_2SeO_5 dielectric grown on the $Bi_2O_2Se_2$ semiconductor shows a semiconductor/dielectric interface that is atomically sharp.[29] This approach, however, is limited to a specific substrate at present, and a different strategy for the deposition of high-κ gate dielectrics on 2D surfaces is required. The choice of the molecular crystal high-κ ($\kappa = 11.5$) antimony trioxide (Sb_2O_3) as a gate dielectric is promising[33,34] as Sb_2O_3 can be grown directly on the surfaces of 2D crystals (e.g., MoS_2, Graphene) using standard thermal evaporation deposition (STED).[33] The deposition process is scalable and the thickness of the Sb_2O_3 films can be precisely controlled down to a nanometer thickness over a 3″ wafer. Using Sb_2O_3 as a top gate dielectric, prototype MoS_2 FET shows an on/off ratio of 10^8 and a record sub-threshold swing of 64 mV/decade at 300 K.[33]

In this work, we study the defect generation and evaluate the role of electrode material on the performance and dielectric breakdown of Sb_2O_3 films by combining electrical measurements and nanoscale analysis using transmission electron microscopy (TEM). Comparing Ti and Au electrodes, we show that the choice of electrode affects the tunnel current and the dielectric breakdown strength of the Sb_2O_3. The results show that the leakage current increases by 3–4 orders of magnitude for the Ti electrode compared to the Au. By using an Au electrode, the breakdown field strength can be increased by ≈1 MV cm^{-1} compared to Ti. The energy dispersive X-ray spectroscopy (EDXS) shows that the Ti scavenges oxygen from the Sb_2O_3 and forms non-stoichiometric oxides and defects at the interface. The growth of the interfacial layer is absent for the Au electrode.

2. Results

2.1. Test Structure and Experimental Methods

The test structure consists of $Ti/Sb_2O_3/n^{++}Si$ and $Au/Sb_2O_3/n^{++}Si$ capacitors as schematically shown in **Figure 1a**. $n^{++}Si$ is used as a global bottom electrode as it provides an atomically flat surface for the deposition of Sb_2O_3 films on 3″ Si wafers. Capacitors of areas 50 × 50, 75 × 75, 100 × 100, and 150 × 150 μm^2 are fabricated and the details of Sb_2O_3 film deposition, and the device fabrication can be found in the Experimental Section. The electrical measurements are carried out at room temperature using a semiconductor parameter analyzer connected to a probe station. This measurement setup serves two important purposes: i) enables the measurement of current in the logarithmic range from pA to mA range and, ii) limits the current flow immediately when dielectric breakdown occurs. This is important for the study of dielectric breakdown since it provides access to different stages of dielectric degradation including charge trapping, stress-induced leakage current (SILC), and dielectric breakdown for a holistic electrical characterization.

We use transmission electron microscopy (TEM) to determine the film thickness and crystalline quality of the Sb_2O_3 films in the prepared capacitors as shown in Figure 1b,c. The results show that the Sb_2O_3 films are continuous, and the thickness of the film varies between ≈7.5 and 8.0 nm. The Sb_2O_3 films are polycrystalline, and the size of nanocrystals is of the same order as the Sb_2O_3 film thickness. A 3.0–3.3 nm thick interfacial SiO_x layer is also present between the $n^{++}Si$ substrate and the Sb_2O_3 film.

2.2. Time-Dependent Dielectric Breakdown and Random Telegraph Noise

We evaluate the integrity of the dielectric by carrying out time-dependent dielectric breakdown (TDDB) measurements. TDDB tests are standard dielectric reliability tests used to probe the temporal evolution of stress-induced defects and their impact on the tunneling current. In TDDB measurements, an electric field is applied, and the current is monitored as a function of time until breakdown occurs. The choice of applied electric field is arbitrary and typically ranges between 50% and 80% of the breakdown field, to accelerate the degradation in the dielectric and complete the measurements within a reasonable time. TDDB measurements on 150 × 150 μm^2 capacitors subjected to a bias of 1.5 V are shown in **Figures 2a** and S1 (Supporting Information). The current increases progressively with time until breakdown occurs. Various stages of dielectric degradation are identifiable, including charge trapping, stress-induced leakage current (SILC), and multiple successive breakdown events.[35,36] The first stage is charge trapping where the tunnel current drops to ≈15% of the initial value. This initial reduction in current is due to pre-existing defects in the Sb_2O_3. The charge trapping component of the current can be better visualized by subtracting the current at t = 0 sec from the overall TDDB current as shown in Figure 2b. This initial reduction in the current is linear and has also been observed for other gate dielectrics like SiO_2[37] and h-BN.[22] Following charge trapping, the SILC stage initiates and the tunnel current increases with time until breakdown occurs. It is considered that the continued electrical stress leads to the dilation of the created breakdown path and results in the formation of additional multiple breakdown paths.[36] The discrete jumps in the measured current that can be seen in Figure 2a are consistent with this assumption.

These pre-existing defects in Sb_2O_3 also give rise to random telegraph noise (RTN),[38] where examples are shown in Figure 2c–e. RTN in gate dielectrics is associated with the capture and emission of charge carriers at the individual defect sites which manifests in the fluctuations of tunnel current between well-defined levels at random time intervals.[39,40] The RTN is observed when an electron is captured at the defect site as it increases the local potential barrier for the incoming charge carriers to tunnel and hence leads to a reduction in the current. The current recovers its original value when the captured

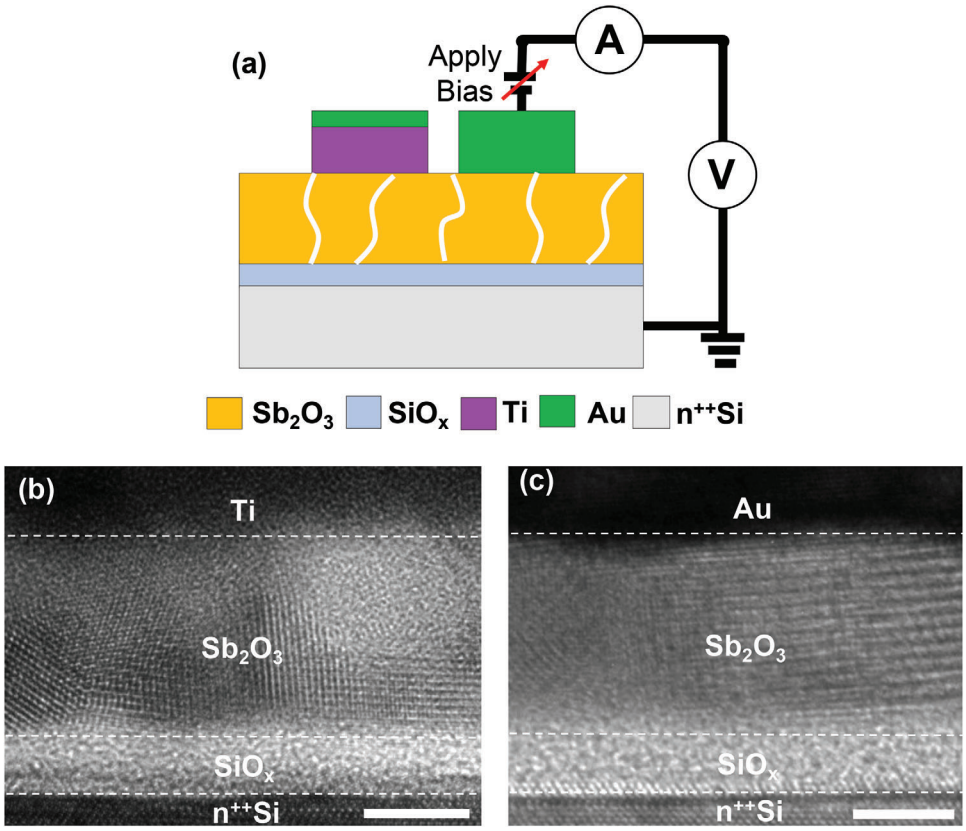

Figure 1. a) Schematic showing the cross-section of the capacitor test structure and the electrical connections for the charge transport measurements. Capacitors with both Ti and Au as top electrodes are fabricated. The capacitor areas are 50 × 50, 75 × 75, 100 × 100, and 150 × 150 μm^2. The bias is applied to the top electrode and $n^{++}Si$ is grounded during the electrical measurements. b) TEM micrograph showing a cross-section of the as-prepared capacitor with Ti. c) TEM micrograph showing a cross-section of the as-prepared capacitor with Au electrode. The Ti is capped with a thin layer of Au to prevent oxidation. The Sb_2O_3 film is continuous and has a thickness of 7.5–8.0 nm. The Sb_2O_3 film is polycrystalline as evidenced by the presence of lattice fringes observed in (b) and (c). An interfacial SiO_x layer of thickness 3.0–3.3 nm is also present. The scale bars in (b) and (c) are 5 nm.

electron is emitted from the defect site. For each current fluctuation, the time for which the current remains high and low is known as the time to capture (τ_c) and time to emit (τ_c) respectively, as shown in Figure 2d. For the measurement of RTN, a small bias (typically < 20% of the breakdown field) is applied and the tunnel current is measured as a function of time. RTN is sensitive to the applied electric field and hence the bias is changed only in small steps to obtain statistical trends.

RTNs are readily observed across capacitors with Ti electrodes. For the data shown in Figure 2c–e, a 2-level RTN is consistently observed for an applied voltage range of 25–75 mV. Here, only a small portion of the data is plotted for brevity and the complete RTN spectra are shown in Figure S2 (Supporting Information). Both τ_c and τ_e are extracted from each RTN spectrum and analyzed further. Both τ_c and τ_e show exponential distributions for all the RTNs as shown by the histogram in Figures S3 and S4 (Supporting Information). The exponential distribution of the time constants has also been observed for RTNs in other gate dielectrics.[38,39,41] Interestingly, we also observe that when the time constants (τ_c and τ_e) for all the RTN data are plotted on the same exponential plot, all the distributions overlap as shown in Figure S5 (Supporting Information). This overlap of the distributions of all six RTN spectra highlights that a single defect is associated with all the RTNs measured here.[42] Additionally, multi-level RTN is also observed, and an example is shown in Figure S6 (Supporting Information).

2.3. Role of Electrodes on Dielectric Breakdown

In this section, we discuss the role of electrodes on the dielectric breakdown in Sb_2O_3. Tunnel current and breakdown field (E_{BD}) are two critical parameters affecting the reliability of a gate dielectric and hence we evaluate these for Sb_2O_3 in this section. The tunnel current measured for capacitors of area 50 × 50 μm^2 with Ti electrodes is plotted in Figure S7 (Supporting Information). Here, the tunnel current is measured by applying a ramp voltage stress (RVS) between −250 and +250 mV. The measurements are also carried out on capacitors of areas 75 × 75 and 100 × 100 μm^2 and the current density (J) is obtained by dividing the measured tunnel current by the capacitor area. The current density versus voltage (J–V) plot for all three capacitor areas is shown in Figure S8 (Supporting Information). The J–V plots for all the capacitors overlap suggesting that the tunnel current scales with the area of the capacitor and no bulk structural defects, such as pinholes, are present in the Sb_2O_3 film. This agrees with the TEM analysis in

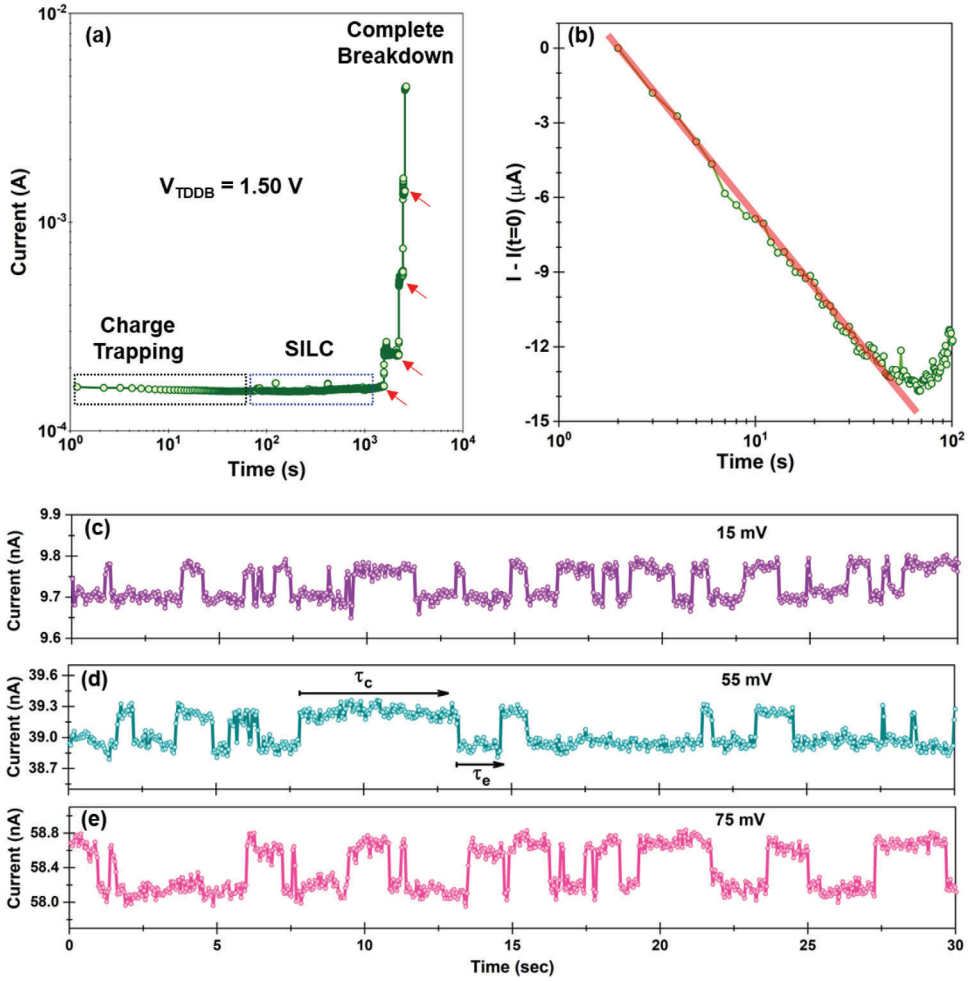

Figure 2. a) Time-dependent dielectric breakdown (TDDB) measurements showing the different stages of dielectric degradation including charge trapping, stress-induced leakage current (SILC), and breakdown in Ti/Sb_2O_3/n^{++}Si capacitors. Multiple breakdowns can be observed as indicated by the red arrows. b) The charge trapping component can be extracted from the TDDB current (i.e., I(t)) by subtracting the time zero current (i.e., I(t = 0)). The reduction in the charge-trapping current fits a linear curve on the log-normal scale. c–e) Random telegraph noise originating from the pre-existing defects in Sb_2O_3. The complete RTN spectra are shown in Figure S2 (Supporting Information). The capture (τ_c) and emission time (τ_e) are labeled in (d).

Figure 1b,c which shows that the Sb_2O_3 film is continuous with a uniform thickness.

We now evaluate the breakdown voltage of the capacitors by applying an RVS until breakdown occurs and a current compliance of ≈1 mA is reached. The representative breakdown current–voltage (*I*–*V*) curves measured on five different capacitors of 50 × 50 μm^2 area are shown in **Figure 3a**. A sudden increase in current is observed at the onset of breakdown. The post-breakdown *I*–*V* in Figure S9 (Supporting Information) shows that the resistance is ≈7.5 kΩ. The low resistance after the breakdown and the ohmic behavior of the post-breakdown *I*–*V* curve suggest that a metallic conducting filament has been formed. In our analysis, we define the breakdown voltage (V_{BD}) as the voltage at which the current compliance reaches ≈1 mA and this is used to extract the breakdown field (E_{BD}). The average value of the V_{BD} of Sb_2O_3 with Ti electrode is 1.9 V as obtained from the Weibull analysis shown in Figure 3d. E_{BD} is obtained by dividing V_{BD} by the dielectric thickness ($t_{dielectric}$) and we use the total dielectric thickness of ≈11.3 nm (i.e., 8.0 nm Sb_2O_3 + 3.3 nm SiO_x) by considering both the Sb_2O_3 thickness and the interfacial SiO_x layer. It should be noted that this represents a worst-case scenario and provides a lower bound on the estimates of E_{BD} as interfacial oxides are defective. The calculated E_{BD} for Ti electrodes is ≈1.7 MV cm^{-1} and we find that the values are lower by ≈1.0 MV cm^{-1} compared to InAu electrodes.[33]

To investigate the origin of this reduction in the breakdown field, we carried out a breakdown analysis on capacitors with Au electrodes. The representative breakdown *I*–*V* curves on 50 × 50 μm^2 capacitors are shown in Figure 3b. There are two distinct observations: a) there is a large reduction in the tunnel current, and b) the breakdown voltage is increased for capacitors with Au electrodes. For the quantitative analysis, the current density for capacitors with both Ti and Au electrodes for three different areas of 50 × 50, 75 × 75, and 100 × 100 μm^2 at 1 V is plotted in Figure 3c. We observe that while the current density distribution

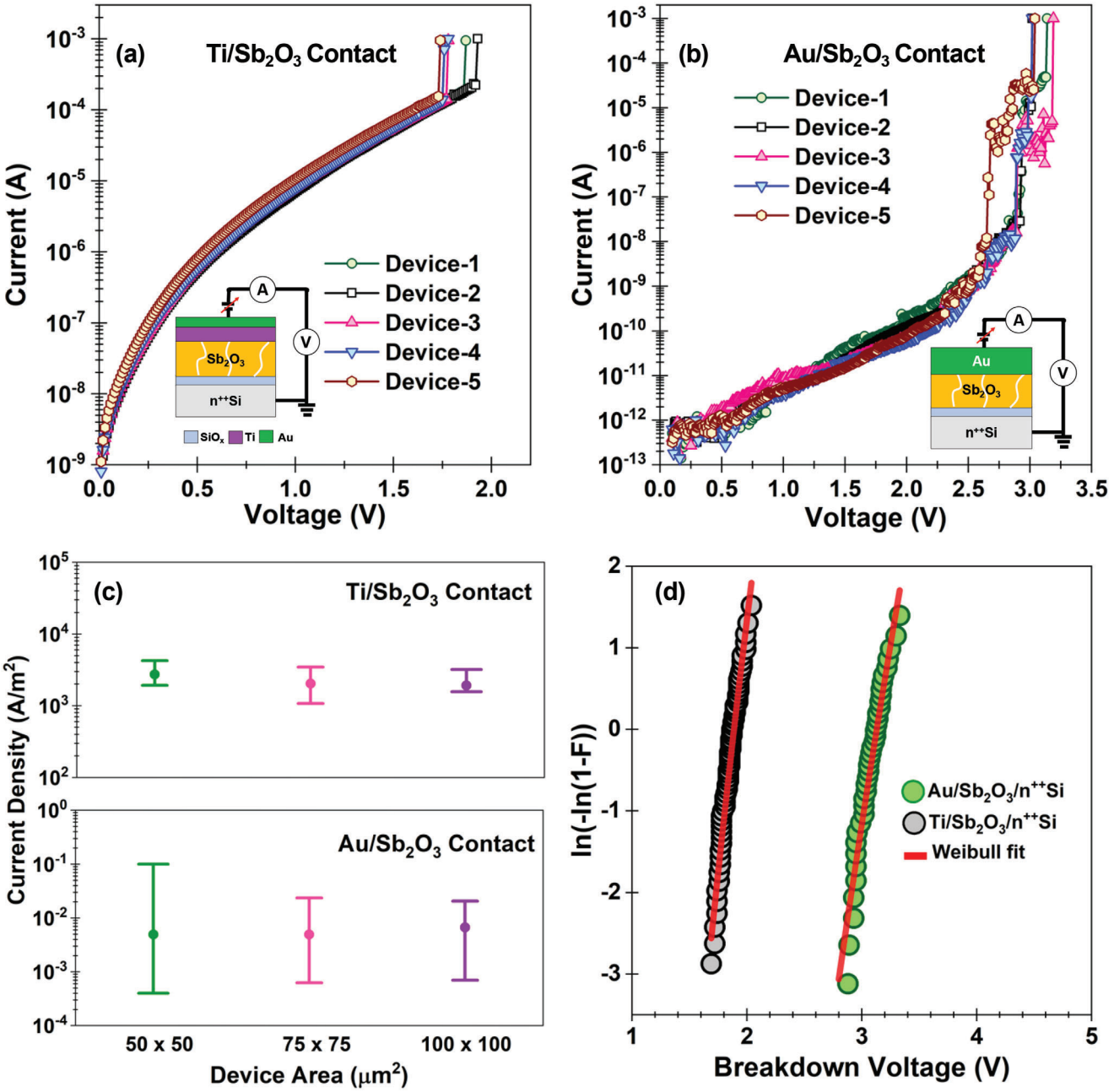

Figure 3. Breakdown current–voltage (*I*–*V*) curves measured on Sb_2O_3 film with a) a Ti and b) an Au electrode. c) The plot of current density for the three different capacitor areas of 50 × 50, 75 × 75, and 100 × 100 μm^2 for Ti and Au electrodes measured at a bias of 1 V. At least 10 devices have been measured for each capacitor area to obtain the boxplot shown in (c). d) Plot of breakdown voltage for both Ti and Au electrodes on Sb_2O_3 on a Weibull scale. The breakdown is defined as the voltage at which the current reaches a compliance of ≈1 mA. At least 40 capacitors have been measured for the Ti and the Au electrodes each to obtain the statistical plot shown in (d). The areas of the capacitors in (a), (b), and (d) are 50 × 50 μm^2.

is narrow for the Ti electrodes, their absolute value reduces by at least four orders of magnitude for Au electrodes.

V_{BD} values for Sb_2O_3 capacitors with both Ti and Au electrodes are extracted following the procedure discussed above. Following the standard failure reliability approaches, V_{BD} data are plotted on a Weibull scale[43,44] as shown in Figure 3d. We note that breakdown distribution for capacitors with both Ti and Au electrodes follows a linear Weibull model. The Weibull slope (β) is an important fitting parameter that gives an estimation about the spread in the breakdown voltage. Generally, $\beta < 1$ indicates that the breakdown is caused by extrinsic defects.[45] Therefore, $\beta > 1$ indicates that the intrinsic defects determine the breakdown. A larger value of β indicates a higher uniformity in the thickness of the dielectric film. The extracted values of β for both Ti and Au electrodes are 27.5 and 24.5 respectively. We also note that the values of β in the Sb_2O_3 are comparable to a VLSI quality 3 nm thick SiO_2

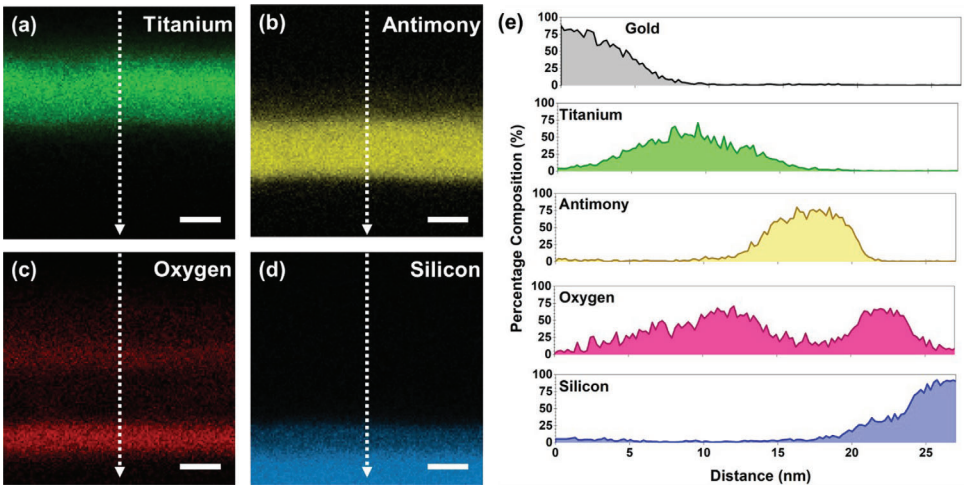

Figure 4. EDXS chemical analysis of the Ti/Sb_2O_3/n^{++}Si capacitors: a–d) EDXS elemental maps showing the elemental distribution of Ti, Sb, O, and Si along the white arrow. Ti is capped with Au to prevent oxidation from the ambient. The Au elemental map is not shown here for brevity. e) Line profiles across the white arrows in (a–d) showing the atomic percentage of all elements. The line profiles are obtained by averaging across 20 pixels to show the average trends. Here, each pixel is 0.18 nm wide. It should be noted that there is an accumulation of oxygen at the Ti/Sb_2O_3 interface and a simultaneous decrease in the oxygen concentration of the Sb_2O_3 layer. The scale bars in (a–d) are 5 nm.

film.[46] The mean values of breakdown voltage (τ_{BD}) obtained from the Weibull fitting for Ti and Au electrodes are ≈1.90 and ≈3.13 V, respectively. The measured E_{BD} for Au electrode is ≈2.76 MV cm^{-1} (compared to ≈1.68 MV cm^{-1} for Ti electrode) and we discuss the origin of the differences in the electrical behavior below.

2.4. Chemical Analysis of Ti and Au Electrodes with Sb_2O_3

We use scanning transmission electron microscopy (STEM) along with electron energy loss spectroscopy (EELS) and EDXS to decipher the origin of the differences observed for Ti and Au electrodes. Cross-section TEM lamellae are prepared from both Ti/Sb_2O_3/n^{++}Si and Au/Sb_2O_3/n^{++}Si capacitors prior to electrical stress and the results of the analyses are shown in **Figures** 4 and 5. EDXS data of Ti, Sb, O, and Si are plotted in Figure 4a–d which shows the distribution of the elements in the different layers. A line profile showing the elemental distribution of Ti, Sb, O, and Si in a capacitor with a Ti electrode is shown in Figure 4e and we find that there is a significant redistribution of oxygen both at the Ti/Sb_2O_3 interface and in the Sb_2O_3 bulk. The quantitative analysis of the EDXS data in Figure 4e shows that the ratio of oxygen to antimony content at the Sb_2O_3 bulk region of the film is drastically reduced to 0.26 compared to the ideal stoichiometric Sb_2O_3 (which has a ratio of 1.5). The concentration profiles in Figure 4e show that there is a formation of a TiO_x layer at the Ti/Sb_2O_3 interface. During the

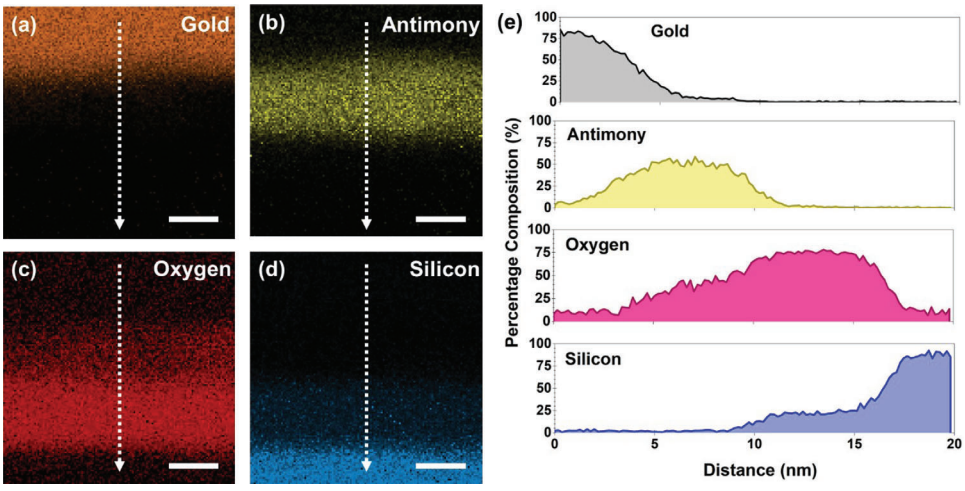

Figure 5. EDXS chemical analysis of the Au/Sb_2O_3/n^{++}Si capacitors: a–d) EDXS elemental maps show the elemental distribution of Au, Sb, O, and Si along the white arrow. e) Line profiles across the white arrows in (a–d) showing the atomic percentage of all elements. The line profiles are obtained by averaging across 20 pixels to show the average trends. Here, each pixel is 0.20 nm wide. Unlike Ti electrodes, there is no accumulation of oxygen at the Au/Sb_2O_3 interface. The scale bars in (a–d) are 5 nm.

formation of the TiO_x layer, the Sb_2O_3 layer loses oxygen leading to the formation of a sub-stoichiometric Sb_2O_3, deficient in oxygen.

Additional evidence for the formation of TiO_x is also provided by the EELS analysis as shown in Figure S10 (Supporting Information). The onset of the core-loss EELS edge and the energy loss near edge fine structure (ELNES) are sensitive to the chemical environment in the material, and they can be used as an indicator to probe if and how the oxygen is chemically bonded to Ti. We observe that the Ti L-edge EELS signal at the Ti/Sb_2O_3 interface shows a positive shift in the onset of the edge by ≈1.5 eV when compared to the bulk Ti. The Ti-L ELNES is consistent with titanium oxides (TiO_x, where $x < 2$).[47,48] It is challenging to quantify the value of x as there is a gradual change in the oxygen concentration in the Ti film, with the highest oxygen concentration at the Ti/Sb_2O_3 interface as shown in Figure 4e.

A similar elemental analysis for capacitors with Au electrodes is shown in Figure 5a–d and the distribution of elements agrees with the fabrication process. A line profile showing the distributions of Au, Sb, O, and Si is plotted in Figure 5e. The analysis of the EDXS data shows that the elemental ratio of oxygen to antimony content at the Sb_2O_3 bulk region of the film is 0.79. We note that the oxygen content in the Sb_2O_3 bulk with the Au electrode is about three times higher as compared to the Ti electrode. However, the Sb_2O_3 films with Au electrodes are also non-stoichiometric and oxygen-deficient.

2.5. Discussion

The general trend of the time-dependent dielectric degradation in Sb_2O_3 shown in Figure 2a is similar to other types of gate dielectrics (e.g., SiO_2, HfO_2, and h-BN). The various stages of dielectric degradation including charge trapping, SILC, and breakdown are clearly identifiable. We find that the oxygen-deficient Sb_2O_3 film causes charge trapping, and the effect is readily visible in the initial stages of TDDB where the tunnel current can drop and decrease can be up to ≈6% of the initial value. This charge-trapping effect is especially dominant for the capacitors where Ti is used as a top electrode. The Ti scavenges oxygen from Sb_2O_3 forming a defective interfacial layer. These pre-existing defects in the oxygen vacancy-rich Sb_2O_3 film also lead to RTN current fluctuations. Both 2-level and multi-level RTNs are readily observed in the Sb_2O_3. The RTN defects in Sb_2O_3 are stable at room temperature and hence long-term RTN spectra can be measured. Although this RTN is a reliability challenge for the FETs, these oxygen-deficient Sb_2O_3 layers have potential for applications in cryptography as sources of RTN generators since they offer the possibility of controlled tunability of oxygen vacancies.[49]

A critical finding of this study is that the interfacial reaction at the dielectric/electrode interface plays a crucial role in the overall performance of the Sb_2O_3. We demonstrate this by comparing the two commonly used electrodes Ti and Au. The tunnel current is significantly higher for Ti as compared to Au. Given that the Sb_2O_3 layer thickness is the same for both the Ti and Au electrodes, the 3–4 orders of increase in the tunnel current for Ti electrodes cannot be accounted for considering the lower work function of Ti ($\phi_{Ti} = 4.33$ eV) compared to Au ($\phi_{Au} = 5.20$ eV). Critical insights emerge from the cross-sectional TEM analysis of the fabricated capacitors which shows that there is a significantly higher concentration of oxygen present at the Ti/Sb_2O_3 interfaces. This suggests the oxidation of Ti and the formation of an oxygen-deficient non-stoichiometric Sb_2O_3. This is further corroborated by the EELS analysis of Ti which shows that the onset for the L-edge is delayed at the interface as compared to the metallic Ti electrode, indicating the formation of Ti—O bonds at the interface. Ti-L ELNES further confirms the formation of a TiO_x phase at the interface. In contrast, we do not observe the formation of any interfacial oxide at the Au/Sb_2O_3 interface. This absence of the interfacial oxide formation at the Au electrode also increases the breakdown field of Sb_2O_3 to 2.7 MV cm^{-1}. This value agrees with the breakdown field strength of Sb_2O_3 of 2.7 MV cm^{-1} measured previously using an InAu electrode.[33] We note that the deposited Sb_2O_3 films in all the cases are non-stoichiometric and oxygen deficient, and the improvement in the deposition process has the potential to increase the breakdown field strength.

This work also addresses another key practical aspect for the successful integration of the high-κ Sb_2O_3 films into the fabrication process. We demonstrate that a continuous, homogeneous, and defect-free (e.g., with any pinholes) Sb_2O_3 film can be deposited on a wafer scale for the fabrication of devices. The electrical measurements carried out on the capacitors show that tunnel current variations from device to device have a narrow distribution as shown in Figure S7 (Supporting Information). Given that the tunnel current is highly sensitive to the dielectric thickness, it can be also used as an indirect indication of the uniformity of the Sb_2O_3 thickness across the 3″ inch Si wafer. Direct evidence of the uniform thickness is also provided by the TEM measurements in Figure 1b,c which shows a uniformity of the Sb_2O_3 layer.

These initial results are promising for further consideration of Sb_2O_3 as a gate dielectric for 2D material-based transistors. However, there are many questions related to the material growth, metal/dielectric interfaces, physics of charge transport, and dielectric breakdown that remain to be understood. For example, it is not clear at present why the Sb_2O_3 film is polycrystalline, and non-stoichiometric, and how the crystallinity is affected by the growth substrate. It would also be important to further investigate the metal/dielectric interfaces for other commonly used gate electrodes. Future studies should also focus on understanding the atomic structure and improving the Sb_2O_3 deposition process to obtain stoichiometric films. Considering the different process steps in the fabrication process, the thermal stability of Sb_2O_3 is another crucial aspect and would be subject to future work.

Optimizing the electrical contacts presents a significant challenge when introducing new materials in the devices. For example, there have been significant efforts undertaken to understand and engineer the 2D semiconductor-metal contact interface to meet the technology requirements.[50] The challenge with the new emerging gate dielectrics is to identify a suitable contact metal that is chemically inert as well as relevant for applications. Insights gained from the previous works on 2D semiconductor-metal contact interfaces can be applied to optimize the contacts for the emerging gate dielectrics.[51] It is important to point out that the use of noble elements like Au or InAu as a contact material would have limited application for large-scale technology due to requirements from semiconductor fabrication. It is important to explore alternative pathways for improving the contact property. One promising approach is to use a diffusion barrier

layer (e.g., TiN) between the dielectric and the contact layer, which could prevent the chemical reaction from taking place at the dielectric/metal interface.

3. Conclusion

In this work, we have investigated the defect generation, degradation, and breakdown in high-κ molecular crystal antimony trioxide (Sb_2O_3) gate dielectrics. Electrical measurements show that the Sb_2O_3 undergoes various stages of degradation including charge trapping and stress-induced leakage current prior to dielectric breakdown. The pre-existing atomic defects in Sb_2O_3 give rise to random telegraph noise and both two-level and muti-level RTNs are observed. We show that the choice of electrode material is critical for the realization of the full potential of Sb_2O_3 as a gate dielectric. Using Ti and Au as electrodes, we show that the chemistry at the Sb_2O_3/electrode interface dictates the tunnel current and the dielectric breakdown strength. EDXS and EELS analysis confirm that Ti scavenges oxygen from Sb_2O_3. This results in the formation of both an oxygen-deficient Sb_2O_3 oxide at the interface as well as a defective TiO_x layer. This non-stoichiometric TiO_x/Sb_2O_{3-x} bi-layer has a high leakage current and a reduced breakdown voltage. This interfacial reaction is absent when Au is used as an electrode material highlighting the importance of selecting appropriate electrode materials for transistor applications.

4. Experimental Section

Sb_2O_3 Thin Film Deposition: A total of 3″ n^{++}Si wafers ($\rho < 0.025$ Ω;-cm) were pre-cleaned in acetone and IPA to remove surface contaminants. The wafers were immersed in hydrofluoric acid for 30 s to remove any native oxide. The Sb_2O_3 film was deposited using standard thermal evaporation (Nexdep, Angstrom Engineering) in a high vacuum (10^{-6} Torr) following the procedure described in previously published work.[33] The thickness of the Sb_2O_3 film was precisely controlled using an in situ crystal quartz monitor.

Device Fabrication: Small pieces of ≈2 cm × 2 cm were diced from the 3″ wafers and the top electrodes were patterned by electron beam lithography (EBL). Briefly, a 200 nm thick PMMA A4 resist was spin-coated on the sample at 4,000 rpm for 60 s and the sample was baked at 180 °C for 5 min prior to lithography. EBL was carried out using a JEOL JBX 9300FS at an acceleration voltage of 100 kV. The patterns were developed in MIBK-IPA (2:1) for 2.20 min, cleaned in IPA for 30 s, and dried in N_2. The top metal electrode was deposited using Kurt J. Lesker's Physical Vapor Deposition System under high vacuum conditions at room temperature. For bilayer electrodes (e.g., Ti/Au), metal layers were deposited without breaking the vacuum to avoid any oxidation. The lift-off was carried out in acetone for ≈20 min at 50 °C. The sample was cleaned in IPA and vacuum dried for ≈3–4 h prior to any measurements.

Electrical Measurements: Electrical measurements were carried out using an Agilent B1400 semiconductor parameter analyzer connected to a probe station. The probe station was equipped with four independent source measurement units and the base noise for the current measurements was ≈1 pA. During all the measurements, bias was applied to the top electrode, and the bottom n^{++}Si substrate was electrically grounded. All the measurements were carried out at room temperature. For RVS measurements, a ramp rate of 0.4 V s^{-1} was used and for RTN measurements a sampling rate of 500 points s^{-1} was used.

Focused Ion Beam Sample Preparation: Cross-section samples for the TEM analysis were prepared using a FEI Versa 3D FIB-SEM. A few µm thick Pt protection layer was first deposited using the electron beam and subsequently using the Ga ion beam. Lift-out was carried out to prepare a ≈5 µm long TEM lamella. Final milling was carried out at an accelerating voltage of 5 and 2 kV respectively, to diminish amorphous layers and beam damage on the sample surface.

Transmission Electron Microscopy: TEM measurements were carried out at 300 kV using a FEI Titan microscope. Scanning TEM (STEM) measurements were carried out at 200 kV on a JEOL Monochromated ARM200F microscope equipped with a CEOS GmbH probe corrector, a double silicon drift detector (SDD) for energy dispersive X-ray spectroscopy (EDXS), and a Gatan Imaging Filter Continuum for electron energy loss spectroscopy (EELS).

Quantification of the EDXS data: Given the overlap of the O and Sb EELS edges, EDXS was used for the chemical analysis in Figures 4 and 5. EDXS composition quantification was carried out using the Gatan Microscopy Suite (GMS 3.40) software, with background subtraction using the Kramers model, theoretical K-factor, Casnati cross-section model, and thickness correction. The thickness was estimated using EELS data and the log ratio (relative) routine available in GMS. The result from the analysis is obtained in units of inelastic mean free path (IMFP) of the electrons, t/λ. Here, t is the sample thickness, and the λ is the IMFP of electrons in the material. The IMFP of the electrons measured in the Si substrate, at the region of the sample where the EDXS data were acquired, varies between 0.64 and 0.88 (mean = 0.76) and 1.25–1.58 (mean = 1.42) for Au and Ti electrodes respectively. Considering that the IMFP of electrons at 200 keV in Si is ≈145 nm,[52] the estimated mean thickness of the TEM lamellae with Au and Ti electrodes are ≈110 and ≈206 nm respectively. Electron beam broadening can affect the quantitative analysis of the EDXS data at the interfaces. For the quantitative analysis of Sb_2O_3 films, therefore selected the regions where the EDXS signal is not affected by the beam broadening and the average values are provided.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

A.R. and E.O. acknowledge funding from the 2D Tech Vinnova Competence Centre (2019.00068) at Chalmers University of Technology. E.O. and L.Z. acknowledge the funding from the Knut and Alice Wallenberg Foundation (2019.0140). The authors would like to acknowledge Prof. Tianyou Zhai and Dr. Kailang Liu at Huazhong University of Science and Technology, China for the discussion and for providing the Sb_2O_3 thin films used in this work. This work was performed in part at the Myfab Chalmers, the Measurements Laboratory at the Microtechnology and Nanoscience (MC2) department at Chalmers, and the Chalmers Materials Analysis Laboratory (CMAL).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D materials, gate dielectric, high-κ, molecular crystal, reliability, Sb_2O_3

Received: March 11, 2024
Revised: May 24, 2024
Published online: August 21, 2024

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