THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Epitaxial optimization of InP High Electron Mobility Transistors in Low-Noise Amplifiers for Qubit Readout

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Cover pictures: Left: A 4-8 GHz hybrid cryogenic InP HEMT LNA. Middle: InP HEMT mounted in the LNA via bond-wires. Right: STEM cross-section of a 100-nm gate in an InP HEMT.

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To my beloved parents and friends

Abstract

The indium phosphide high electron mobility transistor (InP HEMT) is used in cryogenic low-noise amplifiers (LNAs) at C-band (4-8 GHz) for qubit readout in superconducting quantum computing. Improving the LNA performance with respect to noise, gain and dc power consumption is essential to meet future demands when upscaling quantum processors to handle thousands of qubits. Still, the noise temperature of today's best C-band LNAs remains nearly an order of magnitude higher than that of a quantum-noise-limited amplifier. This motivates further studies into the noise reduction mechanisms of the InP HEMT. This thesis provides evidence of the importance of epitaxial optimization in reducing noise in cryogenic InP HEMTs for LNAs in quantum computing. A 100-nm gate-length InP HEMT process was refined to a recess-first approach to mitigate electrochemical etching deterioration. The correlation between the subthreshold swing and noise temperature of the LNA observed at 4 K implied that the subthreshold swing served as an indicator of the amount of carrier fluctuations in the InP HEMT channel giving rise to noise. The noise of a C-band three-stage hybrid LNA was investigated by varying the spacer thickness (1 to 7 nm) and channel indium content (53% to 70%) in the InAlAs/InGaAs heterostructure of the 100-nm InP HEMT at 4 K. At the optimum noise bias, the 5 nm spacer InP HEMT LNA exhibited a 1.4 K average noise temperature with 6.1 mW dc power consumption. The best performance achieved with 60% indium content, yielding an average noise temperature and an average gain of 3.3 K and 21 dB, respectively, at 108 μW dc power, represents a new state of the art. Channel noise, expressed as a sum of thermal and excess noise measured from 4 K to 300 K, showed excess noise dominance at 4 K, independent of temperature. Excess noise was observed to vary with the channel indium content even with the same drain current and gate length, suggesting that channel noise cannot be described solely by suppressed shot noise. Additional channel noise contributions were proposed to originate from real-space transfer and impact ionization.

Keywords: Channel noise, channel indium content, cryogenic, InP HEMT, low-noise amplifier, noise temperature, quantum computing, spacer thickness, subthreshold swing.

List of Publications

This thesis is based on the following appended publications:

[A] **J. Li**, A. Pourkabirian, J. Bergsten, N. Wadefalk, and J. Grahn, "On the Relation between rf Noise and Subthreshold Swing in InP HEMTs for cryogenic LNAs," in Proceedings of the *34th Asia-Pacific Microwave Conference*, Yokohama, Japan, November 29 - December 2, 2022, DOI: 10.23919/APMC55665.2022.9999771.

[B] **J. Li**, A. Pourkabirian, J. Bergsten, N. Wadefalk, and J. Grahn, "Influence of Spacer Thickness on the Noise Performance in InP HEMTs for Cryogenic LNAs", *IEEE Electron Device Letters*, vol. 43, no. 7, pp. 1029-1032, July 2022, DOI: 10.1109/LED.2022.3178613.

[C] **J. Li**, J. Bergsten, A. Pourkabirian, and J. Grahn, "Investigation of noise properties in the InP HEMT for LNAs in qubit amplification: Effects from channel indium content," *IEEE Journal of the Electron Devices Society*, vol. 12, pp. 243-248, February 2024, DOI: 110.1109/JEDS.2024.3371905.

[D] **J. Li**, J. Chen, A. Minnich, and J. Grahn, "Noise Performance of $In_xGa_{1-x}As$ channels in InP HEMTs from 4 to 300 K," in manuscript, 2024.

Other publications not appended in this thesis:

[a] **J. Li**, A. Pourkabirian, J. Bergsten, E. Cha, A. Alexei Kalaboukhov, N. Wadefalk, and J. Grahn, "Reduction of Noise Temperature in Cryogenic InP HEMT Low Noise Amplifiers with Increased Spacer Thickness in InAlAs-InGaAs-InP Heterostructures," *Compound Semiconductor Week 2021*, Online, May 9–13, 2021.

[b] E. Cha, N. Wadefalk, G. Moschetti, A. Pourkabirian, J Stenarson, **J. Li**, D-H. Kim, and J. Grahn, "Optimization of channel structures in InP HEMT technology for cryogenic low-noise and low-power operation", *IEEE Trans. Electron Devices*, vol. 70, no. 5, pp. 2431-2436, 2023, DOI: 0.1109/TED.2023.3255160.

[c] **J. Li**, J. Bergsten, A. Pourkabirian, N. Wadefalk, and J. Grahn, "Epitaxial Optimization of the InP HEMT for Cryogenic Low-Noise Amplifiers", *Swedish Microwave Days 2023*, 23 – 25 May 2023, Stockholm, Sweden.

[d] **J. Li**, J. Bergsten, A. Pourkabirian, N. Wadefalk, and J. Grahn, "Optimization of InGaAs Channel for Cryogenic InP HEMT Low-Noise Amplifiers", *Compound Semiconductor Week 2023*, May 29 - June 2 2023, Jeju, Korea.

[e] Y. Zeng, **J. Li**, J Stenarson, P Sobis, and J. Grahn, "100-μW Cryogenic HEMT LNAs for Quantum Computing", *2023 18th European Microwave Integrated Circuits Conference (EuMIC)*, Berlin, Germany, pp. 71-74,2023, DOI: 10.23919/EuMIC58042.2023.10288982.

[f] **J. Li**, J. Chen, A. Minnich, and J. Grahn, "Investigation of Noise Performance in InP HEMTs with Varying Indium Channel Composition from 80 K to 300 K", *Compound Semiconductor Week 2024*, 3-6 June 2024, Lund, Sweden.

[g] **J. Li**, "Design and Fabrication of InP High Electron Mobility Transistors for Cryogenic Low Noise Amplifiers", *Licentiate thesis, Department of Microtechnology and Nanoscience, Chalmers University of Technology*, Nov 2022, https://research.chalmers.se/en/publication/520245.

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [g]. Figures, tables and text in [g] might therefore be fully or partly reproduced in this thesis.

Abbreviations

2DEG	Two-Dimensional Electron Gas
ALD	Atomic Layer Deposition
CMOS	Complementary Metal-Oxide Semiconductor
FET	Field-Effect Transistor
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HF	Hydrofluoric Acid
LNA	Low-Noise Amplifier
mHEMT	Metamorphic High Electron Mobility Transistor
NDR	Negative Differential Resistance
PECVD	Plasma Enhanced Chemical Vapor Deposition
PSD	Power Spectral Density
QC	Quantum Computing
RST	Real-Space Transfer
SEM	Scanning Electron Microscope
SSNM	Small-Signal Noise Model
STEM	Scanning Transmission Electron Microscope
TWPA	Traveling Wave Parametric Amplifier

Notations

C_{gs}	gate-source capacitance
C_{gd}	gate-drain capacitance
C_{ds}	drain-source capacitance
C_{pg}	gate pad capacitance
C_{pd}	drain pad capacitance
d_{sp}	spacer thickness
f	frequency
F	Fano factor
f_t	cut-off frequency
f_{max}	maximum oscillation frequency
g_m	transconductance
g_{ds0}	output conductance at 0 V drain voltage
g_{ds}	output conductance
G	conductance
G_{avg}	average gain
k_B	Boltzmann's constant
L_g	gate length
I_d	device drain current
I_D	LNA drain current
I_g	device gate current
n_s	sheet carrier concentration
P_{LNA}	dc power consumption for LNA
q	electron charge
R_c	contact resistance
R_d	drain resistance
R_g	gate resistance
R_i	intrinsic gate-source resistance
R_j	intrinsic gate-drain resistance
R_s	source resistance
R_{sh}	sheet resistance
S_i	noise current power spectral density
S_{id}	channel noise current power spectral density

$S_{id,th}$	thermal noise current power spectral density
$S_{id,ex}$	excess noise current power spectral density
S_{shot}	shot noise current power spectral density
SS_{avg}	average subthreshold swing
T_a	ambient temperature
T_e	electron temperature
T_d	drain noise temperature
$T_{e,avg}$	average noise temperature
T_g	gate noise temperature
T_{min}	minimum noise temperature
T_{50}	noise temperature measured with 50 Ohm impedance
V_{ds}	device drain voltage
V_{DS}	LNA drain voltage
V_{gs}	device gate voltage
V_{th}	threshold voltage
V_{ov}	overdrive voltage
W	gate width
Φ_{Bn}	Schottky Barrier height
ψ_{bi}	built-in potential
τ	transit time
ΔE_c	conduction band offset
η	hot electron fraction
ϵ_s	dielectric permittivity
μ	Hall electron mobility
γ	noise coefficient
ϵ_0	permittivity of free space
h	Planck's constant

Contents

CHAPTER 1

Introduction

1.1 Background

The invention of the high electron mobility transistor (HEMT) by T. Mimura in 1980 marked a significant milestone in semiconductor technology [1]. This breakthrough was one of the outcomes of the *first quantum revolution*, which brought quantum mechanics from theoretical foundations to practical applications in electronic systems [2]. Mimura's original HEMTs utilized a heterojunction of AlGaAs/GaAs. This creates a high electron mobility channel at the interface, where the electrons are confined to a two-dimensional electron gas (2DEG) in a quantum well. The confinement reduces charge carrier scattering and enhances electron velocity, leading to lower noise and higher gain [3]. Over the following decade, the development of the InAlAs/InGaAs/InP HEMT (InP HEMT) was demonstrated with excellent microwave noise performance because of its higher mobility and larger conduction-band discontinuity than the original Mimura's AlGaAs/GaAs HEMT [4]. At low temperatures around 5-15 K, the InP HEMT exhibits the lowest noise temperature among all transistor technologies [5], [6]. As a result, the InP HEMT is the natural choice in the design of a cryogenic low-noise amplifier (LNA) for the

detection of the weakest microwave or mm-wave signals [7]. Applications are found in high-speed communication, space communication, radio astronomy and physics [8]–[10].

In recent years, the InP HEMT LNA has become essential in quantum computing (QC) for the upcoming *second quantum revolution* [2]. In QC, information is represented by quantum bits (qubits), which must be amplified and read out from the quantum processor at the 10 mK stage. Given that a qubit typically has a signal power of -120 dBm, the amplifiers must be designed with the highest gain and lowest noise [6], [7]. InP HEMT LNAs operating in the 4-8 GHz frequency band (C-band) are currently used in the QC [11]. Normally, the InP HEMT LNA is found at the 4 K stage following a first-stage superconducting amplifier located in close proximity to the quantum processor. The first stage can be a Josephson parametric amplifier or a traveling wave parametric amplifier (TWPA) at around 10 mK ambient temperature. However, proposals suggest that the InP HEMT LNA can be used without a first-stage superconducting amplifier [12]. Also, the InP HEMT can serve as switching elements in routing circuits, as depicted in Fig.1.1 [13]. All this would be highly beneficial when upscaling future quantum systems, handling massive number of qubits. The importance of the InP HEMT LNA is therefore expected to increase in future QC.

This thesis presents progress in InP HEMT technology for detecting weak microwave signals in superconducting quantum computing. This implies that the device technology is meant for an application at 4 K ambient temperature. The main focus has been to optimize the heterostructure forming the 2DEG to understand what limits further noise reduction in the active channel of the InP HEMT. State-of-the-art results in InP HEMT LNAs for qubit readout are demonstrated.

1.2 State of the Art

Today, the 4-8 GHz 100-nm gate-length InP HEMT LNA used in the QC readout system achieves an average noise temperature $T_{e,avg}$ of 1.5 K with more than 40 dB gain at 4 K and 7.8 mW dc power [15]. Efforts to improve the noise performance of the LNAs under low-power bias have also seen significant advancements: a $T_{e,avg}$ of 2.8 K and 27 dB gain at 300 μW has been achieved in a C-band cryogenic LNA [11]. Still, the noise temperature for the best

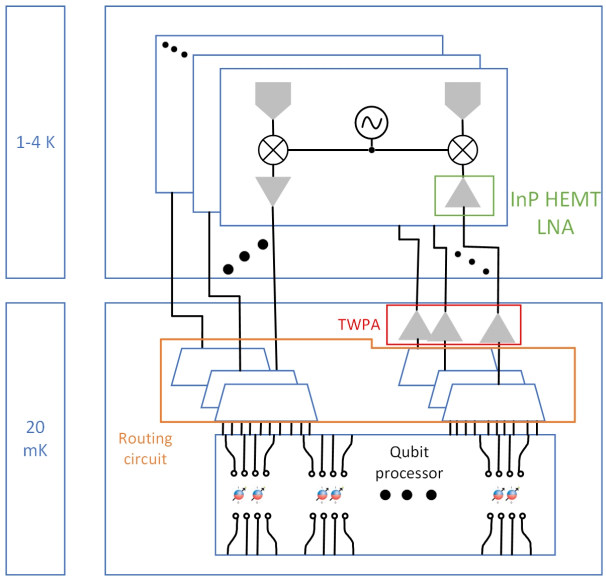

Figure 1.1: Schematic for a possible large-scale quantum computing system modified from [14]. The InP HEMT emerges as the most promising RF electronics for routing and readout a large number of qubit signals.

InP HEMT cryogenic LNA is nearly an order of magnitude higher than a quantum-noise-limited amplifier [16]. In addition, gain and noise will quickly degrade when running the device at lower dc power. This raises questions on the ultimate limit in noise reduction for the InP HEMT.

Alternative technologies to the InP HEMT are being explored for qubit readout amplifiers. Notably, a 4-8 GHz 50-nm gate-length metamorphic HEMT (mHEMT) LNA was reported with a $T_{e,avg}$ of 2.7 K and 31 dB gain with 7.78 mW dc power consumption at 10 K [17]. SiGe heterojunction bipolar transistor (HBT) has also shown promising noise and gain at low-power bias: $T_{e,avg}$ = 2.6 K for the SiGe LNA with 37 dB gain and 1.6 mW dc power consumption at 3-6 GHz [18]. Additionally, a cryogenic complementary metal-oxide semiconductor (CMOS) LNA has demonstrated a $T_{e,avg}$ of 39 K at 4.2 mW dc power consumption at 6-8 GHz [19]. Although SiGe HBT and CMOS technologies offer potential for large-scale integration, they have not yet surpassed the noise and low-power performance of the InP HEMT due to its superior

electron transport properties and low parasitic resistances.

A comparison of the cryogenic LNA noise performance at 4-20 K between different technologies for qubit readout frequencies is illustrated in Fig.1.2. It is observed that in comparison with the InP HEMT, only the superconducting TWPA is comparable in noise and dc power with a $T_{e,avg}$ of 1.9 K in the 3.5-5.5 GHz range at 100-μW dc bias [20]. However, linearity and bandwidth constraints typically limit the gain of TWPAs below 20 dB [21]. Overall, InP HEMTs exhibit superior noise performance among semiconductor devices for cryogenic LNAs in qubit readout. The design of the LNA must be made for the lowest noise under cryogenic conditions [22]. Ultimately, the performance of such LNAs depends on the device properties of the transistor technology used in the circuit design. Still, there is room to improve the InP HEMT noise performance in the LNAs for qubit readout. Further research is needed to optimize the InP HEMT with respect to noise, gain and power dissipation in the LNA for applications in future QC.

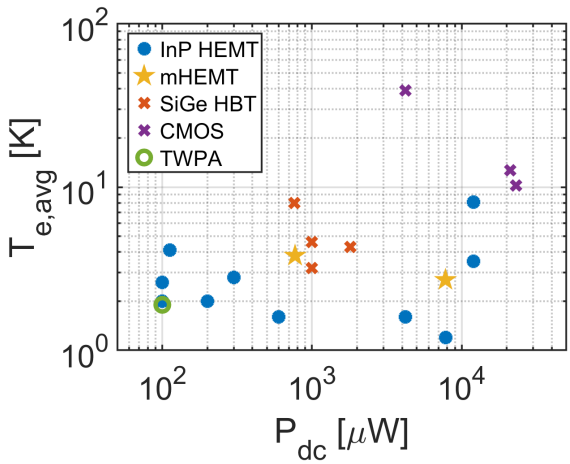

Figure 1.2: Comparison of noise performance as a function of dc power consumption at 4- 20 K for state-of-the-art amplifiers designed for qubit readout frequencies [6], [11], [17]–[20], [22]–[25].

1.3 Motivation

While current state-of-the-art InP HEMT LNAs meet the current requirements of the qubit readout in QC, further reduction in noise and dc power may be necessary to support the future upscaling quantum systems. Lower noise level allows for easier trade-off with gain and dc power consumption, two essential parameters in the LNA for qubit readout. It has been shown that modifications of the epitaxial structure in the HEMT will influence the final noise of the LNA [26], [27]. The majority of epitaxial optimization studies of InP HEMT have been driven by device scaling in order to maximize the current gain cut-off frequency f_t and maximum oscillation frequency f_{max} at room temperature, typically under relatively high dc bias at peak transconductance g_m [28], [29]. Indeed, it has been recently reported that the enhancements in f_t and f_{max} do not necessarily correlate with reduced noise for the InP HEMT [30]. The different electrical properties of the InP HEMT at cryogenic temperatures compared to room temperature add further complexity in transistor optimization for a qubit readout application at typically 4 K.

This thesis is dedicated to the epitaxial optimization of InP HEMTs in cryogenic C-band LNAs, with an overall aim to achieve lower noise temperature in the amplification of qubits in future QC applications. The epitaxial structure of these devices comprises several layers, with particular attention in this work given to the two critical layers: the InAlAs barrier/spacer and the InGaAs channel. The spacer layer which separates the delta doping in the barrier from the channel plays a crucial role in 2DEG transport properties responsible for the output current [3], [31]. The design of the spacer thickness in the InP HEMT has not been reported before this thesis under conditions used in cryogenic LNAs. Several different channel designs have been studied [26], [27], but the underlying physical noise mechanisms in the channels are yet to be clarified. In this thesis, channel noise has been studied for different indium content channels. Additionally, to fabricate and characterize the InP HEMT with the designed epitaxial structures, a process development turned out necessary to conduct the experiments needed for this work.

1.4 Scope of Dissertation

This thesis is organized in the following way:

Chapter 2: Noise Theory and Characterization Methods

A review of the theoretical microwave electronic noise sources in the InP HEMT, specifically in the channel, is presented. InP HEMT noise characterization methods are covered, including the principles of small-signal noise modeling of the InP HEMT. These tools and methods will be used in the subsequent chapters.

Chapter 3: InP HEMT Technology for LNAs in Qubit Readout

The key steps of the InP HEMT fabrication process will be described. The development of the process technology for the InP HEMT targeted for cryogenic LNAs in QC is presented. The motivation for the modified recess process is included. Finally, the subthreshold swing is proposed as a noise indicator for the InP HEMT cryogenic LNA.

Chapter 4: Investigation of Spacer Thickness

This Chapter investigates the spacer thickness in the InP HEMT with respect to noise in the cryogenic LNAs. The different noise observed for InP HEMTs with varied spacer thickness is proposed to be due to the noise generation via injection of a small fraction of electrons from the channel to the barrier.

Chapter 5: Investigation of Channel Indium Content

The noise performance for InP HEMTs with different channel indium content is presented. The observation of the optimum noise channel indium content is demonstrated. A state-of-the-art performance of cryogenic noise temperature and power dissipation of a hybrid 4-8 GHz LNA using the optimized InP HEMTs is presented. A physical interpretation of the channel noise is proposed.

Chapter 6: Conclusion and Outlook

The main conclusions are summarized. Suggestions for future research are given.

CHAPTER 2

Noise Theory and Characterization Methods

This chapter presents a brief review of the microwave electronic noise in the InP HEMT, focusing on the noise generated from the 2DEG channel at high frequency. Low-frequency noise sources such as $1/f$ noise are also present in the InP HEMTs [32]. However, $1/f$ noise is not of relevance for the high-frequency noise properties in the LNAs used for qubit readout.

Noise characterization requires an elaborate setup and complex calibration from cryogenic to room temperatures. Therefore, two noise characterization methods for HEMTs and LNAs are described for different temperature conditions.

2.1 InP HEMT microwave noise

RF and microwave signals are typically accompanied by various types of noise, such as thermal noise, shot noise, generation-recombination noise and hot-electron noise. In a field-effect transistor (FET), the noise is considered to be thermal noise generated from the resistors part except the channel. Several physics mechanisms are ongoing in the channel which contribute to the noise in the InP HEMT at different temperatures and bias conditions. The noise

mechanisms in a HEMT are significant as they determine the lowest limit of the magnitude of the electrical signal that can be amplified without loss of signal quality. This section will focus on possible noise sources in the channel. Physically, such noise sources originate from spontaneous fluctuations in the current and voltage.

2.1.1 Thermal noise

Thermal noise, also known as Johnson or Nyquist noise, is attributed to the random thermal motion of charge carriers within a conductive medium. Assuming thermal equilibrium, the thermal noise can be expressed as a current power spectral density (PSD):

$$S_i = 4k_B T_a G, \tag{2.1}$$

where k_B is the Boltzmann constant, T_a is the ambient temperature and G is the conductance of the conductive medium.

In a cryogenic HEMT, thermal noise primarily originates from the channel resistance and the associated fluctuations in the drain current. The channel thermal noise PSD at zero drain voltage $V_{ds} = 0$ V can be modeled as [33]:

$$S_{id} = 4k_B T_a g_{ds0}, \tag{2.2}$$

where g_{ds0} is the output conductance at $V_{ds} = 0$ V. Under bias, the channel can be in non-equilibrium, giving rise to diffusion current. Assuming that Einstein's relation holds, the diffusion noise can then be regarded as thermal noise, as proven by Van der Ziel [34].

The actual channel noise will be higher than the pure thermal noise [35]. HEMTs are non-linear devices in which current is not always linear with voltage. Therefore, Eq. 2.2 cannot be applied directly. It is possible to divide the HEMT channel into microscopic segments and each segment will produce thermal noise $4kT_a g(x)$ as long as the carriers are in thermal equilibrium or near-equilibrium at the channel position x, where $g(x)$ is the local conductance per unit length at x. The total noise generated by the device can then be found by integrating the contribution of each segment along the channel. Van der Ziel introduced the noise coefficient γ to characterize the channel thermal noise [12]:

$$S_{id} = \gamma 4 k_B T_a g_{ds0}. \tag{2.3}$$

When V_{ds} is 0 V or close to 0 V, the channel behaves like a linear resistor, which leads to $\gamma = 1$. When V_{ds} is further increased, the HEMT will gradually reach saturation and γ will be 2/3 if the channel length is long enough. However, as scaling the channel length below 100 nm, various short-channel effects and other noise mechanisms have appeared, undermining the theoretical foundation of the long-channel value of γ. γ becomes rather an empirical fitting parameter without a solid analytical expression in some of the noise models [35].

2.1.2 Shot noise

As the thermal noise model cannot predict the noise in short channel devices, shot noise has been proposed as the fundamental noise source [36], [37]. Shot noise is a quantum mechanical phenomenon that arises due to the discrete nature of charge carriers and their statistical fluctuations during transport across a potential barrier. In semiconductor devices like HEMTs, shot noise is significant in the regions where carrier transport occurs via tunneling or through potential barriers, such as the potential barrier at the gate or near the source. Shot noise becomes more pronounced at smaller gate lengths due to increased electric fields. The channel shot noise PSD is given by:

$$S_{shot} = F 2 q I_d, \tag{2.4}$$

where q is the electron charge. The shot noise suppression Fano factor F is introduced to describe the level of suppression caused by various scattering mechanisms on the drain current noise. Normally, F is dependent on the channel length [36]. When the channel length approaches 0, F becomes 1, which means pure shot noise.

2.1.3 Relation of thermal and shot noise

While thermal noise dominates at room temperatures and equilibrium conditions, shot noise becomes more prominent at low temperatures or under non-equilibrium conditions. Normally, the two noise mechanisms are considered to be independent of each other. In a short-gate-length device, an intense

electric field and altered charge carrier transport are present. Thermal and shot noise can be regarded as specific forms of a general noise source in mesoscopic physics [38], [39].

2.1.4 Hot-electron noise

Hot-electron noise arises when electrons gain enough kinetic energy from the electric field to deviate from their equilibrium or quasi-equilibrium distribution in the 2DEG. This condition increases scattering and interactions between carriers and lattice, thereby adding noise. In nano-scale devices such as short-channel HEMTs, the electrons travel at saturated speed along the majority of the channel and will thus be 'hot'.

Real-space transfer (RST) refers to the phenomenon where high-energy electrons are scattered from the quantum well to the barrier in a HEMT structure [40]. RST noise has earlier been proposed to occur in the GaAs HEMT [41] and InAlAs/InGaAs/InAlAs/InP quantum well [42]. This scattering leads to a spatial separation of charge carriers and a fluctuation in the channel current, thereby contributing to an increased level of noise PSD [43]:

$$S_{RST} = \frac{2e^2 n_{s2} v_{d1}^2 W \tau}{L_g}, \tag{2.5}$$

where n_{s2} is the barrier electron sheet density, v_{d1} is the saturation velocity in the channel, W is the gate width, τ is the characteristic time of electrons to transfer from InGaAs channel to InAlAs layer, L_g is the gate length. n_{s2} is determined by the hot electron fraction η. In Ref. [43], it is proposed that the fraction of hot electron transfer from the channel to the barrier in a HEMT is determined by the channel-barrier conduction band discontinuity ΔE_c and gate-source voltage V_{gs}. However, a HEMT at a gate bias below threshold voltage V_{th} cannot experience RST. When comparing different devices, it is overdrive voltage $V_{ov} = V_{gs} - V_{th}$ which controls the fraction of transferred electrons via RST. Therefore, compared to Ref. [43], a modified equation is proposed to describe the hot electron fraction η taking the varying threshold voltage into account:

$$\eta = e^{-[\Delta E_c - q(V_{gs} - V_{th})]/k_B T_e}, \tag{2.6}$$

where T_e is the electron temperature.

Impact ionization noise, also known as avalanche noise, is another source for hot electron noise, which occurs when electrons acquire enough energy to ionize atoms, generating electron-hole pairs and leading to considerable current fluctuations. The PSD for noise due to impact ionization can be estimated by [44], [45]:

$$S_{ii} = 2qI_M\alpha, \tag{2.7}$$

where I_M is the mean current due to impact ionization, and α is the ionization coefficient, which depends on the electric field, material properties and temperature [46].

2.1.5 Gate noise

The noise current generated in the channel also affects the gate voltage fluctuations and vice versa. The gate noise of the HEMT can be modeled in two parts. The first part is the thermal noise in the gate resistance R_g. The noise voltage PSD can be expressed as [47]:

$$S_{vg} = 4k_BT_gR_g, \tag{2.8}$$

where T_g is the gate noise temperature. The dependence between the drain and gate noise can be described by a correlation coefficient [47], [48].

The second part is due to the gate leakage current I_g which can also have an impact on the HEMT's total noise at a few GHz range via shot noise [38], [49]:

$$S_{shot} = 2qI_g. \tag{2.9}$$

2.2 Noise characterisation

This thesis employed two methods for measuring HEMT noise: a direct method of measuring transistor noise carried out on-wafer and an indirect method of measuring a hybrid 4-8 GHz three-stage LNA equipped with the HEMTs. The applicability of these methods is discussed below.

2.2.1 Direct noise determination

In an on-wafer measurement, the cryogenic probe station has a temperature sensor positioned in close proximity to the discrete InP HEMTs, as shown in Fig. 2.1. The noise temperature was measured with a 50-Ohm generator impedance T_{50} by the Y-factor method covering a frequency range of 4.0-7.2 GHz, as demonstrated in Fig. 2.2. When T_a is above 40 K, T_{50} has a value higher than 10 K, which gives the measurement uncertainty of around 20%. At $T_a = 300$ K, the uncertainty can be determined to be around 15% [50]. The repeatability of the T_{50} measurements was ∼0.5 K at $T_a = 80$ K and ∼1 K at $T_a = 300$ K.

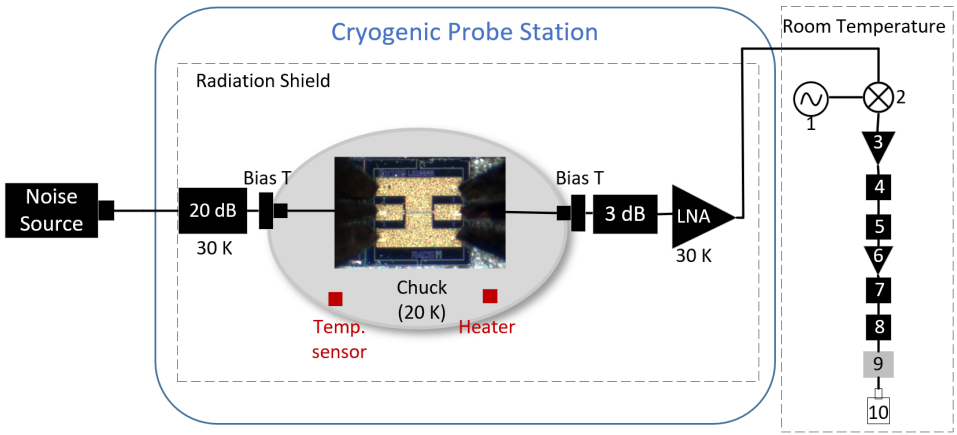

Figure 2.1: Schematic of the on-wafer noise measurement in a cryogenic probe station. The room temperature parts are: 1. HMC-T2100 local oscillator, 2. M1-0220-P Mixer, 3. ZFL-500LN+ low noise amplifier, 4. 20 dB attenuator, 5. SLP-1000+ low pass filter, 6. ZFL-100H+ low noise amplifier, 7. SLP-250+ high pass filter, 8. SHP-25+ high pass filter, 9. variable attenuator, 10. U8481A USB thermocouple power sensor

2.2.2 Indirect noise determination

At temperatures below 40 K, the noise of the InP HEMT was too small to be estimated with high accuracy using the on-wafer measurement. The most

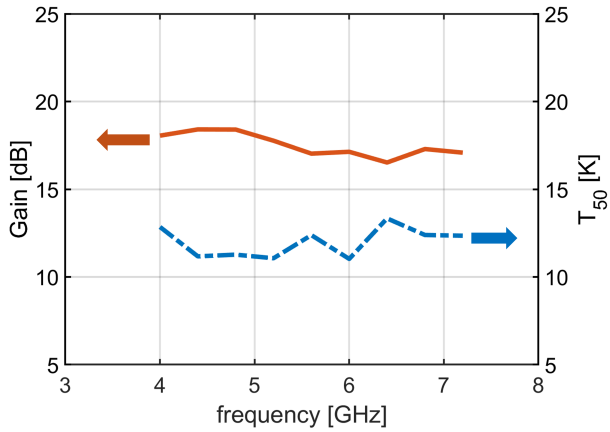

Figure 2.2: Noise and gain as a function of frequency using the direct on-wafer noise method at 80 K. The sample was a 100-nm gate-length InP HEMT based upon an epitaxial structure in Paper C with 60% indium channel content.

reliable method requires the insertion of discrete devices in a hybrid LNA designed for the lowest noise [51]. As illustrated in Fig. 2.3, a diced individual transistor was mounted by wire-bounding in the LNA. Noise temperature for the LNA was measured by the Y-factor method using a cold attenuator setup, shown in Fig. 2.4. A typical result is illustrated in Fig. 2.5. At 4 K, the absolute noise value of the InP HEMT LNA is less than 1.5 K. Provided the LNA gain was higher than 40 dB, the measurement uncertainty for the LNA $T_{e,avg}$ was determined to be less than 0.3 K (∼20%) [52]. The repeatability of the measurements was better than 0.05 K. As a result, the noise difference between the cryogenic LNAs could be attributed to the noise difference between the InP HEMTs.

The temperature gradient in the cryogenic measurement increased when the ambient temperature T_a became higher than 4 K. In the setup, the temperature sensor in the cryogenic box was attached to the attenuator, which could not provide an accurate temperature of the InP HEMT in the LNA, which gives rise to the error of the noise measurement [51]. At higher temperatures, the noise contribution from the temperature-sensitive components in the circuit also increased making the calibration of the LNA difficult. As a result,

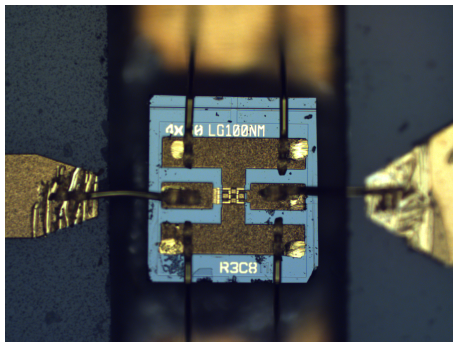

Figure 2.3: A 4×50 μm InP HEMT mounted by bond-wires in the 4–8 GHz hybrid LNA.

accuracy in noise extraction for the InP HEMT degraded at temperatures above 4 K. In this thesis, the majority of InP HEMT noise estimations using the indirect method were done at 4 K.

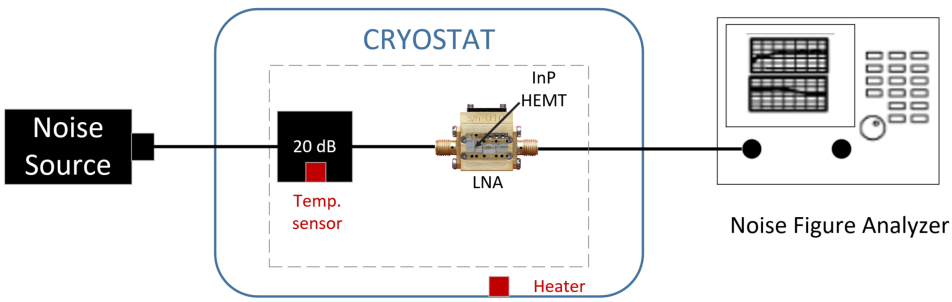

Figure 2.4: Schematic of the noise measurement using an amplifier module in a cryogenic box.

2.2.3 Small-signal noise model

To understand the difference in noise level between the investigated InP HEMTs, Pospieszalski's small-signal noise model (SSNM), depicted in Fig. 2.6, can be used [53]. The equivalent circuit of SSNM is derived from S-

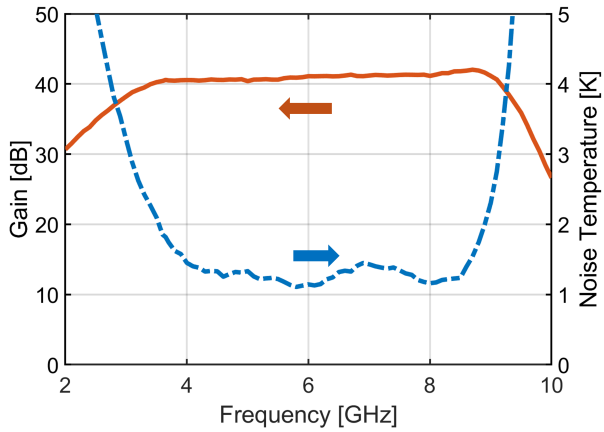

Figure 2.5: Noise and gain as a function of frequency using the indirect method at 4 K. The device was an LNA with 100-nm gate-length, 60% indium content channel InP HEMT based upon an epitaxial structure in Paper C .

parameters described in Ref. [54]. The circuit includes extrinsic elements such as parasitic capacitances (C_{pg}, C_{pd}), inductances (L_g, L_s, L_d) and resistances (R_g, R_s, R_d), along with intrinsic components representing the active region of the HEMT: capacitances (C_{gs}, C_{ds}, C_{gd}), resistances (R_i, R_{gd}, R_{ds}) and g_m. Except for the channel resistance R_{ds} and corresponding conductance g_{ds}, which are assumed to be at an elevated temperature under bias and are modeled with drain noise temperature T_d, all resistances are considered to be at ambient temperature [53]. The channel noise PSD can be calculated by:

$$S_{id} = 4k_B T_a g_{ds}. \tag{2.10}$$

The SSNM expresses the minimum noise temperature $T_{\min}$ for the HEMT as:

$$T_{\min} \approx 2\frac{f}{f_t}\sqrt{R_t T_g g_{ds} T_d}, \tag{2.11}$$

where $R_t = R_s + R_g + R_i$ and f is the frequency. Thus, the objective of both noise measurement methodologies is to determine T_d for the InP HEMT.

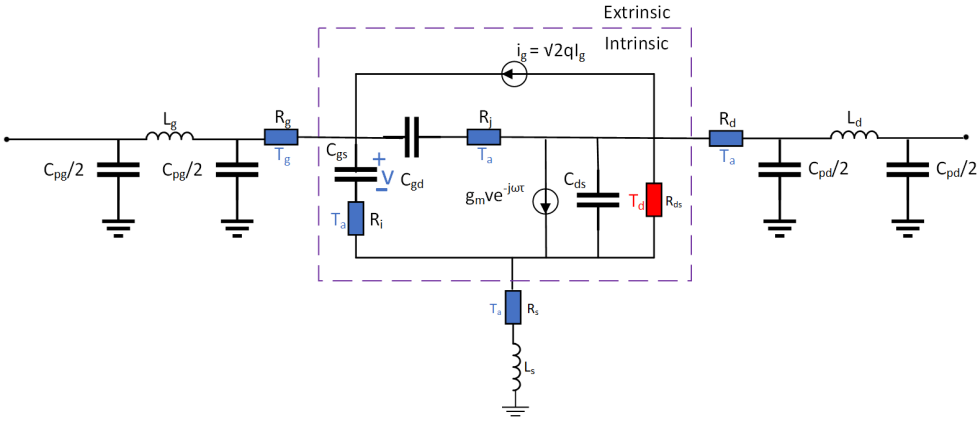

Figure 2.6: The SSNM of the InP HEMT consists of two parts: the intrinsic part, which represents the active region of the HEMT under the gate, and the extrinsic part, which accounts for the parasitic elements [54].

This parameter can be extracted using either the $T_{e,avg}$ model of the LNA circuit or the T_{50} model for on-wafer measurement. For $T_a \leq 10$ K, the T_g in Pospieszalski's noise model was set to 10 K, thus taking device self-heating into account [55]. Above 10 K, T_g was set equal to T_a.

Based on the SSNM, the AWR Microwave Office software circuit simulator can isolate each noise source by setting all others to zero [56]. Fig. 2.7 displays the relative contributions for each noise source at the optimum noise bias in a typical InP HEMT LNA at 6 GHz, where all simulations were conducted at 5 K. The bar chart reveals that elements such as the matching network, R_g and R_i contribute marginally to the total cryogenic LNA noise. Instead, the g_{ds} stands out as the primary factor for the total LNA noise temperature, highlighting the importance of channel noise in the InP HEMT. Consequently, T_d (the equivalent noise temperature for g_{ds}) is the most indicative parameter of the noise level for InP HEMT used in cryogenic LNAs at microwave frequencies. For the InP HEMT at cryogenic temperature, a proper noise measurement will mainly record the nature of electron fluctuations in the intrinsic transistor and not by the parasitic noise sources. This is due to the high mobility of electrons in the InP HEMT at low temperatures, which makes access resistances very small.

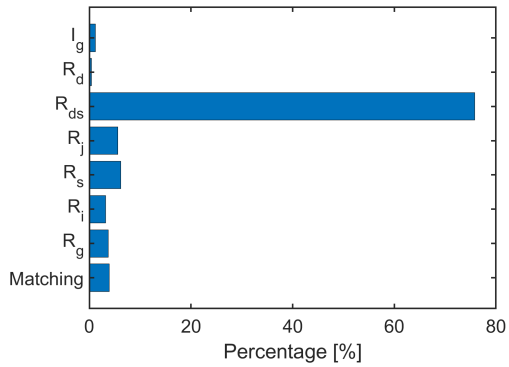

Figure 2.7: Simulated contribution for each noise source at the optimum noise bias in a three-stage InP HEMT LNA at 6 GHz and 5 K. The noise in the cryogenic InP HEMT LNA is dominated by the properties of the HEMT channel.

This chapter briefly described different types of noise sources in the InP HEMT responsible for high-frequency noise. The channel noise for the InP HEMTs was here extracted by two different noise characterization methods. It was concluded that the InP HEMT used in qubit readout is dominated by channel noise. Therefore, the T_d is a crucial parameter to extract and analyze in this thesis. As will be seen in the rest of the thesis, T_d will be strongly affected by the design of the epitaxial structure in the cryogenic InP HEMT.

CHAPTER 3

InP HEMT Technology for LNAs in Qubit Readout

The HEMT LNA has found many applications where low noise figure is a key property, such as in space communication, sensor systems and radio astronomy [8]–[10]. However, reported record results for cryogenic HEMT LNAs are normally based on InP HEMT technology originally developed for room-temperature applications [5]. This means that the full potential of the InP HEMT for the lowest noise is not fully exploited. In this Chapter, the development of the process technology for the InP HEMT specifically targeted for cryogenic LNAs in qubit readout is described. The results of using the subthreshold swing as a rapid noise indicator for cryogenic InP HEMTs are also reported.

3.1 InP HEMT technology

In this thesis, the InP HEMT was based on an epitaxial stack presented in Fig. 3.1. The epitaxial layers were grown by an external vendor using molecular beam epitaxy [57]. The heterostructure was grown on a semi-insulating InP substrate, followed by a 500 nm thick $In_{0.52}Al_{0.48}As$ buffer, an $In_xGa_{1-x}As$ channel and an $In_{0.52}Al_{0.48}As$ spacer/barrier layer including a Si δ-doping

plane. The $In_{0.52}Al_{0.48}As$ spacer layer between the δ-doping plane and the $In_xGa_{1-x}As$ channel separated the Si dopants from the free electrons in the 2DEG. The thicknesses of the channel, spacer and barrier layers were adjusted in these investigations, see Tables. 4.1 and 5.1 for numbers. On top of the barrier, a 4 nm thick InP etch stop layer and a 20 nm thick n^+ $In_{0.53}Ga_{0.47}As$ cap layer was grown. The InP etch stop layer was introduced to improve etch selectivity between the cap and the barrier, as well as to passivate electrically active surface traps present on the $In_{0.52}Al_{0.48}As$ barrier [58].

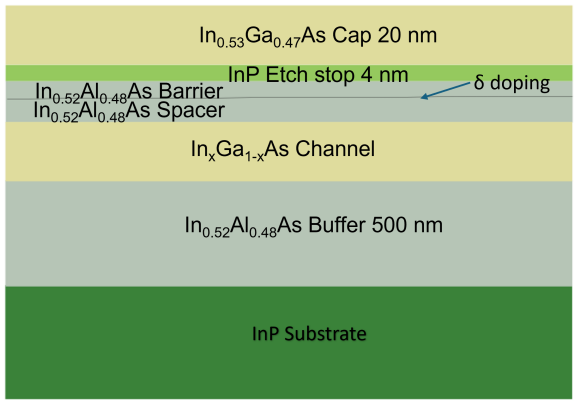

Figure 3.1: Schematic of the epitaxial stack used in InP HEMT fabrication. The Si δ-doping plane is between the InAlAs barrier and spacer layers.

Fig. 3.2 (a) illustrates a schematic of the T-shaped gate InP HEMT. The cross-section scanning transmission electron microscope (STEM) image in Fig. 3.2 (b) shows a homogeneous lateral gate recess of an InP HEMT with a gate length of 100 nm. The main process steps were mesa etch, source and drain contact formation, gate contact formation, passivation, pad metallization, air-bridge formation, thinning and dicing [59]. In this thesis work, two process modules were developed to improve the InP HEMT technology in cryogenic applications. First, the gate recess formation responsible for the gate-to-channel distance was developed. Second, different device passivations were examined. Both these modules affect the final noise properties of the InP HEMT in the LNA for qubit readout.

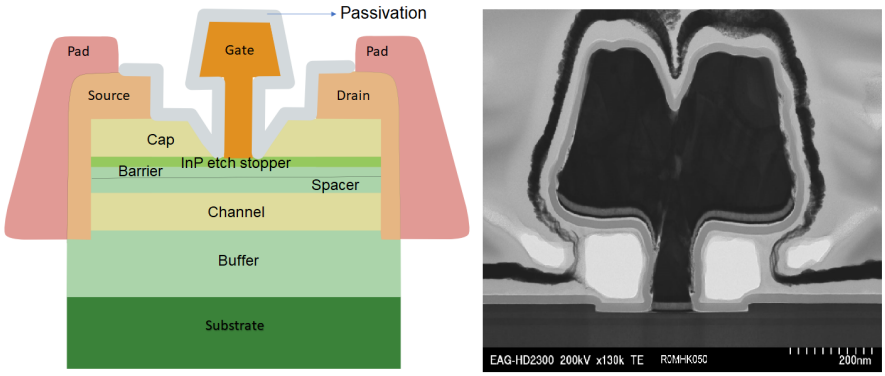

Figure 3.2: (a) Schematic of the processed InP HEMT. (b) Cross-section STEM image of the 100-nm gate-length InP HEMT in the gate region [From paper A].

3.2 Gate recess formation

The most critical step in HEMT fabrication is the gate recess formation since the HEMTs are surface-controlled devices: all types of electrical active defects associated with a surface etch process such as the gate recess may end up as non-ideal electrical characteristics for the transistor. This becomes even more severe under cryogenic device operation. The main purpose of the recess etch is to remove the cap layer and create a well-defined gate-to-channel distance. The InP layer here serves as an etch stop layer for the gate recess. In addition, InP electrically passivates the underlying InAlAs barrier surface, which is prone to oxidation and thus suppresses surface defects. The other critical dimension is the recess width. It must be wider than the gate foot to ensure that the gate has no contact with the drain and source regions. Moreover, the gate width must be sufficiently large to avoid elevated parasitic capacitances. However, a too-wide recess will increase the access resistance of the InP HEMT. In summary, the gate recess formation must be able to provide a constant recess width and depth with a low density of surface defects, regardless of the HEMT position on the wafer and the material structure in the epitaxial stack.

A traditional wet etch process was here employed in the gate recess forma-

tion. The width of the recess was determined by electron beam lithography, etch solution and etch time. The citric acid/H_2O_2 etch solution has been reported to have a high selectivity between $In_xGa_{1-x}As$ and InP [60]. The etch mixing ratio and etch time are determined by the relative concentration of acid and oxidizer in the solution. Since H_2O_2 rapidly decomposes into water [61], it is essential to keep track of the H_2O_2 with respect to aging and exposure in air. In this work, the best standard practices were established for mixing citric acid and H_2O_2 etch solutions meaning that the gate recess etch conditions were almost identical from run to run.

3.2.1 Recess-first InP HEMT process

In the standard InP HEMT process, the source and drain ohmic contact formation is defined prior to the gate recess etch, see Fig. 3.3(a). This process flow is here denoted as the recess-last method. After a homogeneous gate recess is formed, the gate metal stack of Pt/Ti/Pt/Au can be deposited to form the T-shaped gate contact.

During the inspection of the InP HEMTs fabricated in this thesis work, it was observed that the recessed surface was uneven for many devices. An example is given in Fig. 3.4. In Fig. 3.4(a), a top-view scanning electron microscope (SEM) photo illustrates that the recess in the center is different from the recess at the edge. This will cause a poor Schottky contact as demonstrated in the cross-section in Fig. 3.4(b).

A similar gate recess etch problem was noted for HEMTs based on variations in the underlying epitaxial stack. Fig. 3.5(a) presents top-view SEM images of the recess region using an identical recess etch procedure for HEMTs with channel indium content varying from 53% to 70%. The recess width measured by SEM is plotted in Fig. 3.6 (blue line). The recess width exhibits an unexpected variation of more than a factor of two as a function of channel indium content. This observation together with the unexpected erosion shown in Fig. 3.5 indicated an abnormal etching occurring for the traditional recess-last method.

A plausible explanation of the abnormal gate recess etch behavior is electrochemical etching in semiconductor layers adjacent to the pre-deposited metal [62]. An electrochemical potential is established between two different materials exposed to an electrolytic solution. The electrochemical reaction accelerates the oxidation of the semiconductor surface in the periphery of

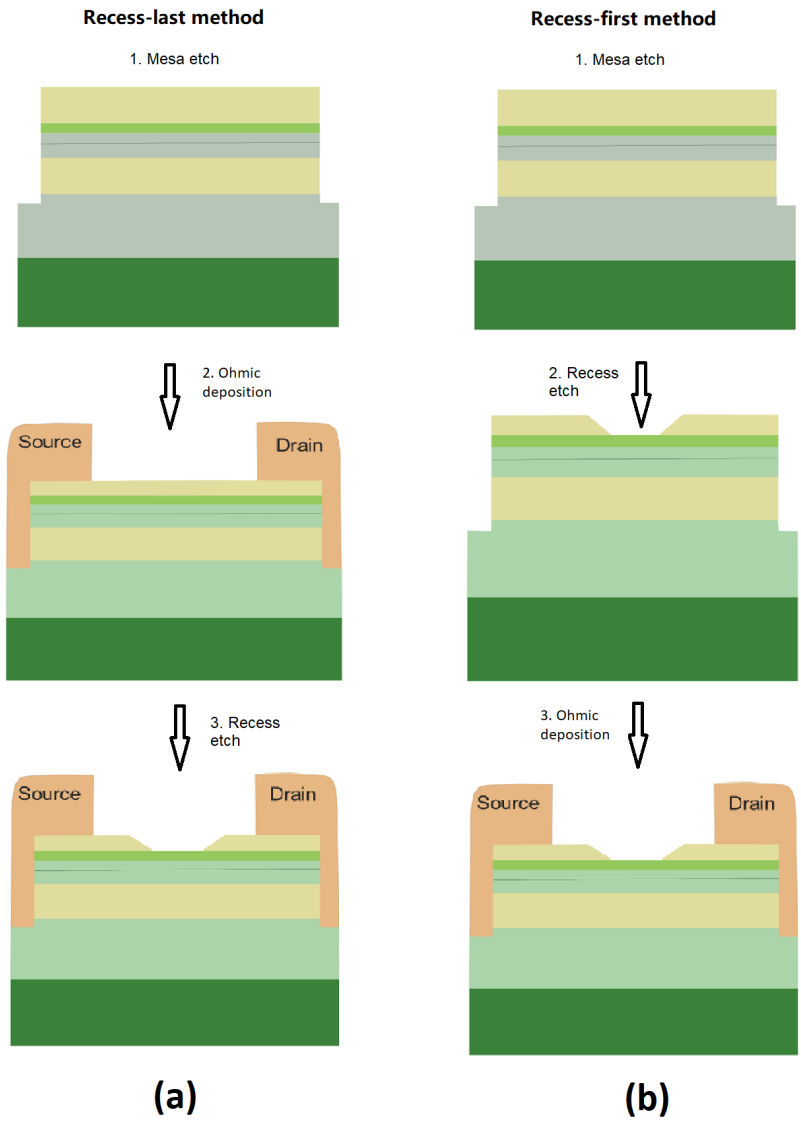

Figure 3.3: (a) Recess-last and (b) recess-first process flow schematically illustrating the order of the ohmic deposition and the gate recess.

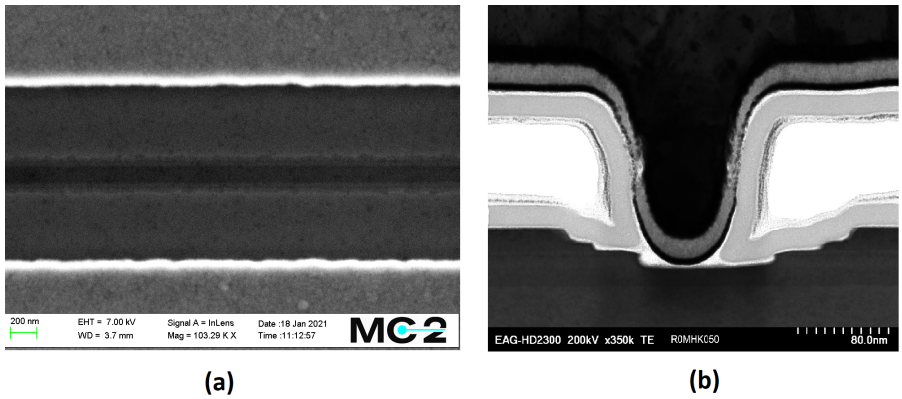

Figure 3.4: (a) Top-view SEM and (b) cross-section STEM image of the abnormal gate recess.

metals even in the presence of deionized water [63]. Evidence has been presented in the literature that electrochemical etching affects the wet-chemical processing of GaAs and related compound semiconductors [64]. The different work functions between the metal and semiconductor will result in different etch rates and selectivities of the semiconductors [65]. The lateral and vertical etch rates of InAlAs and InGaAs with Ni/Pt surface metal in a non-alloyed ohmic electrode were reported to strongly deviate from the etch rate of the bulk without metal. The deviation was attributed to electrochemical etching [64]. This also seems to apply to the InP HEMTs here using alloyed metal deposition immersed in citric acid etch solution. Therefore, it will be difficult to adjust the etch solution to achieve the required control of lateral and vertical gate recess distances by the recess-last method. In particular, this becomes problematic when processing different epitaxial layers in the same InP HEMT batch.

To alleviate the detrimental effect of electrochemical etching, the InP HEMT fabrication was modified according to the process flow shown in Fig. 3.3(b). The gate recess was etched prior to the ohmic deposition and annealing. The method is here denoted recess-first as opposed to the standard recess-last method illustrated in Fig. 3.3(a). The SEM images for the recess-first method using different channel indium content are shown in Fig. 3.5(b). In Fig. 3.6, it is observed that the measured recess width (red line) is substantially more stable for the recess-first method compared with the recess-last process (blue

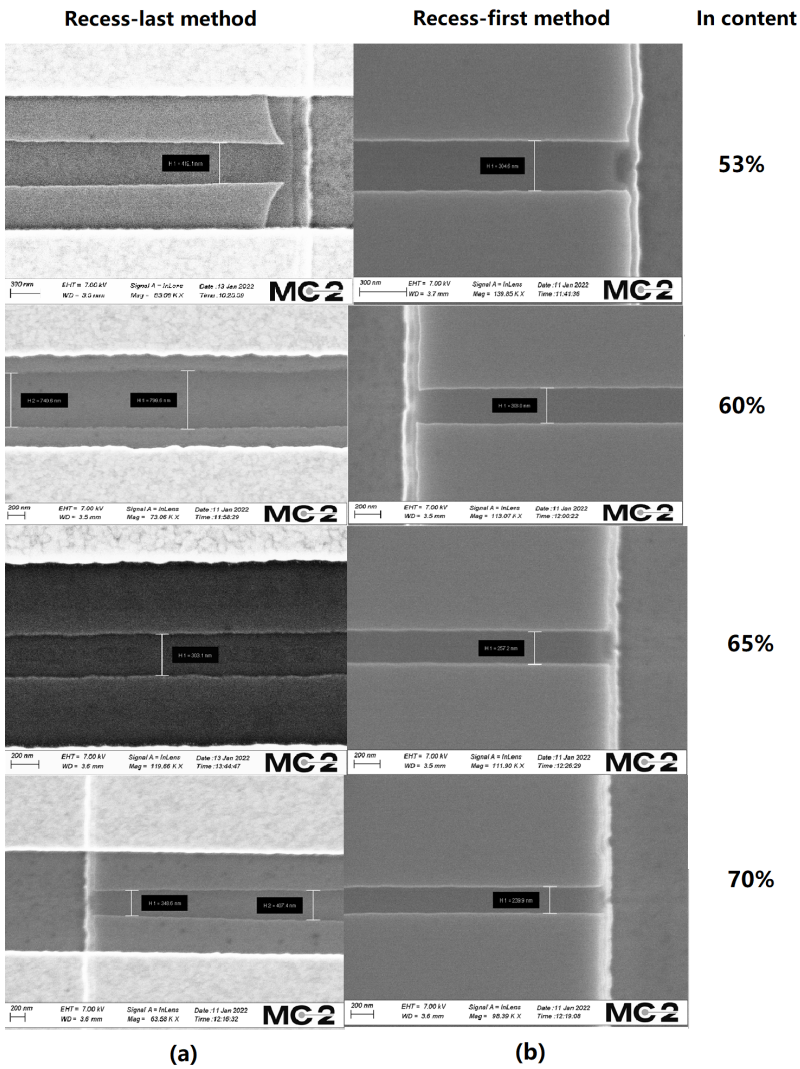

Figure 3.5: Top-view SEM images after gate recess etch using (a) recess-last and (b) recess-first method. Channel indium content from top to bottom is 53%, 60%, 65% and 70%. The gate recess etch process is identical for all samples.

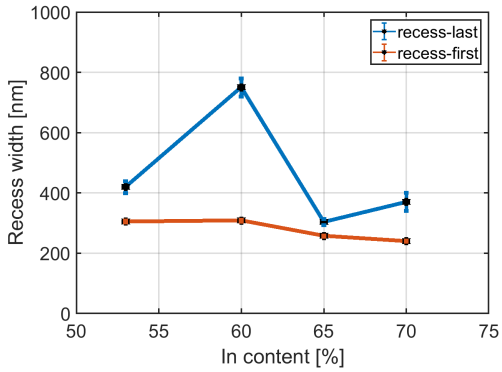

Figure 3.6: The measured gate recess width from Fig. 3.5 versus In channel content for recess-last (blue) and recess-first (red) method.

line). However, the recess-first method will sacrifice the accurate alignment between the gate recess and gate metal. This can be compensated by using more alignment marks in the electron beam lithography step. Since stability in device dimensions between different InP HEMT epitaxial structures was crucial in this research work, the recess-first method was here selected for device fabrication.

3.3 Influence of the passivation

After the gate recess etch, the exposed surface contains many defects which may affect the electric performance of the InP HEMT. The InP etch stop layer serves as the passivation for the InAlAs barrier layer which helps to eliminate the well-known kink effect in the output characteristics when measured under cryogenic conditions [58]. InP is much less reactive than InAlAs. Nonetheless, defects and contaminants may still exist on the surface after processing the InP HEMT. This makes passivation using a dielectric thin film deposition necessary for long-term stability and to prevent contamination of the recess surface. The conventional passivation is either Si_xN_y by plasma enhanced chemical vapor deposition (PECVD) or Al_2O_3 by atomic layer deposition (ALD). However, the passivation itself may introduce problems. Fig. 3.7 shows the undesirable increase in I_g caused by passivation using either

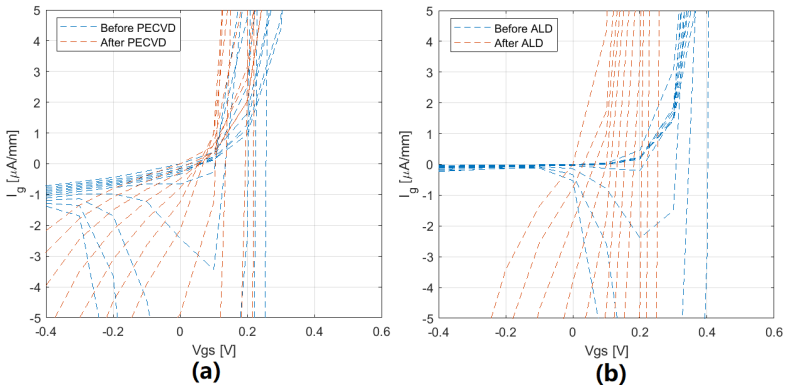

Figure 3.7: Gate current versus gate voltage at 300 K for 2 x 100 μm-width, 100 nm-length InP HEMTs before (blue) and after (red) passivation of (a) PECVD Si_xN_y and (b) ALD Al_2O_3. The drain voltage is 0 - 1 V with steps of 0.1 V.

PECVD Si_xN_y or ALD Al_2O_3. Such enhancement in I_g is detrimental to the noise of the InP HEMT LNA, in particular for lower frequencies of a few GHz [23], [66].

The increase of the I_g by a factor of ten following passivation appeared for both PECVD and ALD regardless of dielectric; See Fig. 3.7. Gate leakage related to the thermal nature of the depositions was excluded. Experimentally, this was confirmed by exposing the devices in the PECVD chamber at 300°C without depositing Si_xN_y. No increase in I_g was recorded. Al_2O_3 can be easily removed by hydrofluoric acid (HF). The I_g for Al_2O_3 passivated InP HEMTs recovered to the same level after removing the Al_2O_3.

Based on these observations, the I_g increase was deduced to unwanted residuals on the surface prior to the passivation. This could potentially aggravate electrically active defects and create current paths between the gate and source during passivation. It has previously been observed by photoluminescence that interfacial defects are induced on the InP surface by the dielectric depending on the surface treatment before the deposition [67]. Therefore, an oxygen plasma cleaning with 50 W power for 20 s at room temperature was introduced before the passivation. Fig. 3.8(a) confirms that the I_g decreased more than ten times for both Al_2O_3 and Si_xN_y passivation compared with no plasma cleaning at 300 K (Fig. 3.7). The I_g will be even lower at 5 K as

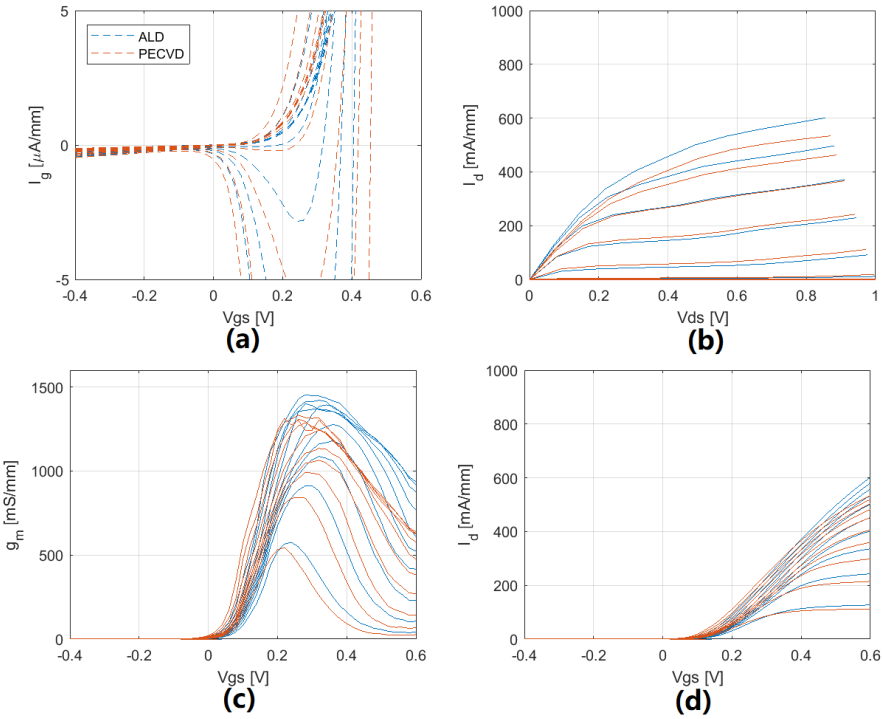

Figure 3.8: dc characterization of 4 x 50 μm InP HEMTs at 300 K using passivation of PECVD Si_xN_y (red) and ALD Al_2O_3 (blue) with a plasma cleaning process. (a) Gate current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (b) Drain current versus drain voltage, with gate voltage -0.4 - 0.6 V in steps of 0.1 V. (c) Transconductance versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (d) Drain current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V.

depicted in Fig. 3.9(a).

Nonetheless, the plasma cleaning will create surface traps in the recess area. This can be seen from the kink effect in the output curves at cryogenic temperature, as shown in Fig. 3.9(b). The kink effect occurs only at high gate bias (above $V_{gs} = 0.6$ V), which is far from the low-noise bias used for the LNA (around $V_{gs} = 0.2$ V). In order to mitigate the undesired kink phenomenon, the oxygen plasma process can be replaced by a wet cleaning step using a

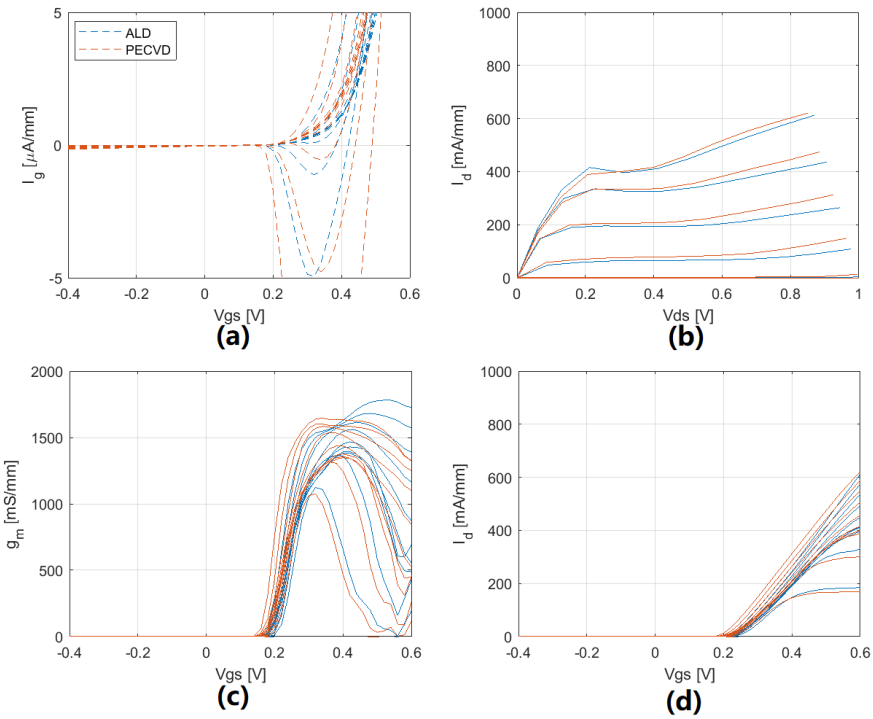

Figure 3.9: dc characterisation of 4 x 50 μm InP HEMTs at 5 K using passivation of PECVD Si_xN_y (blue) and ALD Al_2O_3 (red). (a) Gate current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (b) Drain current versus drain voltage, with gate voltage -0.4 - 0.6 V in steps of 0.1 V. (c) Transconductance versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V. (d) Drain current versus gate voltage, with drain voltage 0 - 1 V in steps of 0.1 V.

remover solution.

Figs. 3.8(b) and (c) show slightly higher current driving ability and g_m for the InP HEMTs with ALD Al_2O_3 at 300 K than for the InP HEMT with PECVD Si_xN_y. In contrast, the current driving ability and g_m become very similar at 5 K; See Figs. 3.9(b) and (c). The V_{th} is almost identical for InP HEMTs with both passivation methods at 300 K and 5 K, as demonstrated in Fig. 3.8(d) and Fig. 3.9(d). Fig. 3.10 presents the noise and gain of 4-8

GHz LNAs at 5 K using the indirect method described in Chapter 2.2.2. The HEMT LNA were equipped with the transistors passivated with either ALD Al_2O_3 or PECVD Si_xN_y. The average gain and $T_{e,avg}$ is 46 dB and 1.3 K, respectively, for both ALD Al_2O_3-based and PECVD Si_xN_y-based LNAs. It is concluded that no significant difference with respect to noise and gain in the cryogenic LNA is seen for the two passivation methods used in the fabrication of InP HEMTs. The better suppression of the kink effect by ALD Al_2O_3 than for the PECVD Si_xN_y reported previously [49] was not observed here. This may be due to the usage of an InP etch stop layer in this thesis work. Such an InP layer will serve as a strong passivation for the InAlAs surface and thus change the conditions for the subsequent dielectric deposition.

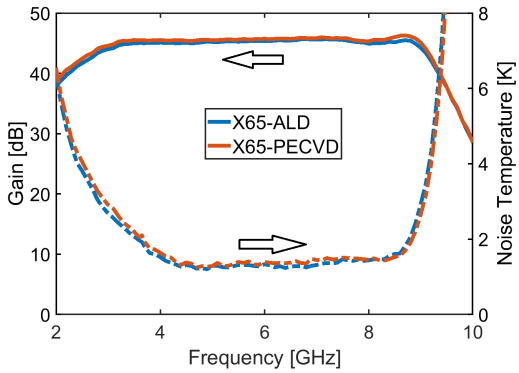

Figure 3.10: The measured gain (solid) and noise temperature (dashed) of a three-stage 4-8 GHz hybrid LNAs integrated with InP HEMT passivated by PECVD Si_xN_y (red) and ALD Al_2O_3 (blue). V_D = 0.7 V, I_D = 15 mA at 5 K.

3.4 Cryogenic LNA noise indicator

In the mapping of noise properties for the InP HEMT and its corresponding dc properties, all measured at 5 K, an interesting correlation was observed between $T_{e,avg}$ and the subthreshold swing (SS). SS depicts the slope of the transfer characteristics in the subthreshold region. The average SS (SS_{avg}) was calculated from the average drain current with V_{ds} from 0.025 to 1 V ver-

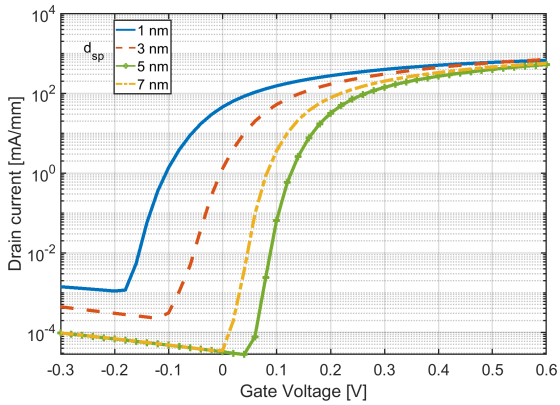

Figure 3.11: The average drain current (V_{ds} = 0.025 - 1 V) in the subthreshold region versus gate voltage of the InP HEMT at 5 K with d_{sp} = 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) [From paper A].

sus gate voltage shown in Fig. 3.11. From the curves, the SS_{avg} was obtained to be 25, 23, 14 and 15 mV/dec for InP HEMTs with different spacer thickness d_{sp} = 1, 3, 5 and 7 nm, respectively. The latter values of SS are among the lowest reported for cryogenic FETs yet still much beyond the theoretical Boltzmann limit $(k_BT/q)\ln(10)$ [3]. The deviation from the Boltzmann limit occurs at 110 K for InP HEMTs with d_{sp} = 1 and 3 nm and 70 K for d_{sp} = 5 and 7 nm. $T_{e,avg}$, $\sqrt{I_d}/g_m$ and SS_{avg} versus d_{sp} for InP HEMTs measured at 5 K are plotted in Fig. 3.12. $T_{e,avg}$ reflects the rf properties of the transistor as depicted in Fig. 3.12 (a). The widely used noise indicator $\sqrt{I_d}/g_m$ plotted in Fig. 3.12 (b) does not show a fully consistent relation with $T_{e,avg}$ as a function of d_{sp} at the optimum noise bias. Finally, SS_{avg} in Fig. 3.12 (c) is another dc property which monitors the I_d/g_m ratio. This is similar to the $\sqrt{I_{ds}}/g_m$ but at a lower bias [68].

Out of the two dc parameters $\sqrt{I_d}/g_m$ and SS_{avg}, it appears that the latter better reflects the difference in noise between the cryogenic InP HEMTs. The saturation of the SS at low temperatures is indicative of intrinsic mechanisms related to electron scattering in the 2DEG when approaching 0 K [69]. According to the model in ref. [69], the higher saturation SS in InP HEMTs at cryogenic temperature indicates a larger band-tail extension. As a result,

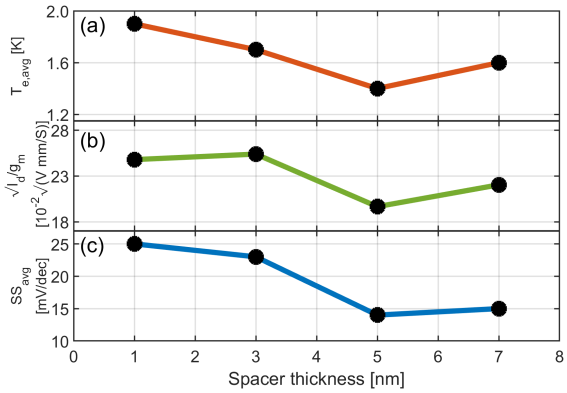

Figure 3.12: (a) The $T_{e,avg}$ (red) of the InP HEMT LNAs extracted at optimum noise bias. (b) $\sqrt{I_d}/g_m$ (green) at optimum noise bias of the InP HEMTs. (c) The SS_{avg} (blue) of the InP HEMTs extracted at V_{ds}=0.1 V. All data points were based on measurements at 5 K. [From paper A]

the 2DEG in the channel will be affected by the increase of the electron density in the conduction-band tail. A recent follow-up study demonstrated that potential fluctuations within the channel affect the cryogenic SS, which hypothetically can be related to random variations in the 2DEG responsible for channel noise [70]. This may explain the better correspondence between SS_{avg} and $T_{e,avg}$ compared to $\sqrt{I_d}/g_m$ and $T_{e,avg}$. Since the noise performance of the InP HEMT at low temperature cannot be measured directly on-wafer with high accuracy, this suggests that SS for the InP HEMT (measured at the same low temperature) may serve as a useful and swift indicator for the expected rf noise in the cryogenic InP HEMT LNA.

In conclusion, the InP HEMT fabrication scheme was successfully developed to a recess-first process to mitigate the electrochemical etching. A comparison of two different device passivation methods of Al_2O_3 and Si_xN_y did not reveal any significant difference neither in gain nor noise for the InP HEMT cryogenic LNA. The SS of the InP HEMT was proposed as a swift indicator for the noise performance of cryogenic InP HEMT LNAs.

CHAPTER 4

Investigation of Spacer Thickness

This thesis is focused on the relation between epitaxial design in the InP HEMT and the final noise properties of the InP HEMT LNA used for qubit readout. In this Chapter, the optimization of d_{sp} in the InP HEMT with respect to noise in a cryogenic LNA is described.

The spacer layer is one of the key features that determine the 2DEG formation in the InP HEMT. The spacer separates the doping impurities from the 2DEG. For a given quantum well heterostructure, the d_{sp} and the number of dopants influence the shape, density and location of the 2DEG. The carrier concentration and associated scattering of electrons have been reported to depend on d_{sp} [3], [31]. It is therefore evident that the optimization of d_{sp} is also needed to improve the InP HEMT noise performance. Prior to this work, such an optimization had not been carried out for InP HEMTs aimed for cryogenic LNAs.

Since variation in the d_{sp} introduces a minimum amount of modifications in the heterostructure, the optimization of the d_{sp} may provide information on the impact of device noise from the 2DEG itself without taking material imperfections such as increased lattice strain or defect density into account. Changing the d_{sp} may therefore potentially reveal insights into the noise mech-

anisms in the channel of the InP HEMT.

4.1 Epitaxial design

The transistor technology was a 100-nm gate-length InP HEMT with 15 nm 65% channel indium content using the recess-last process and ALD Al_2O_3 passivation described in Chapter 3. The experiment was based on variations in d_{sp} of the epitaxial structure for the InP HEMTs. Four epitaxial structures with d_{sp} of 1, 3, 5 and 7 nm were designed; see epitaxial structure in Table. 4.1. The total thickness of the barrier and spacer layer was kept constant at a value of 9 nm. The δ-doping level was adjusted to have the sheet carrier concentration n_s constant of 2.5×10^{12} cm^{-2} for all samples to keep the same channel condition for all the devices.

Table 4.1: The spacer and barrier thickness of the investigated structures in Fig. 3.1.

Spacer (nm)	*Barrier* (nm)
1	8
3	6
5	4
7	2

4.2 Hall measurements

Before fabricating InP HEMT devices, Hall measurement served as an assessment tool for the transport properties of the channel electrons, offering a means of verifying the quality of the epitaxial layers. Hall measurement provides critical data on electron mobility μ, sheet resistivity R_{sh}, and n_s. The Hall measurements were carried out using Hall bars shown in Fig. 4.1. Measurements were conducted under a constant magnetic field of 1 T, varying the temperature from 300 K down to 5 K.

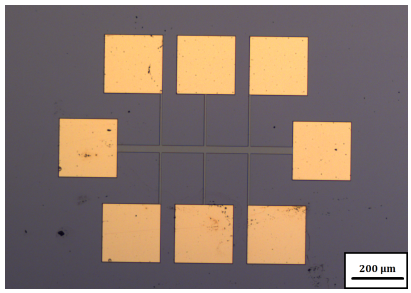

Figure 4.1: Photo of the Hall bar structure.

The values for μ, R_{sh}, and n_s are plotted in Fig. 4.2. Here, the parameter μ is observed to increase steeply with reduced temperature and flattens out below 50 K. In this region, the difference in μ between d_{sp} = 5 (and 7) nm and d_{sp} = 1 nm is almost a factor of 3. The strong dependence of μ on the d_{sp} at 5 K is due to various degrees of scattering in the channel electrons caused by different d_{sp}. In contrast, at 300 K, the μ was almost similar showing typical values of μ ranging from 9,500 and 14,000 cm^2/Vs. The difference in μ is reflected in the R_{sh} behavior which is plotted against temperature in Fig. 4.2(b). Finally, it is seen in Fig. 4.2(c) that n_s exhibited only a $\pm$10% dependence on d_{sp} with no temperature variation. The data in Fig. 4.2 demonstrated that the epitaxial materials used for InP HEMT experiments in this thesis were of high quality and showed the expected differences with respect to d_{sp}.

4.3 DC and RF characterization

The dc and rf properties of InP HEMTs with the epitaxial structures described in Section 4.1 were characterized on-wafer at 5 K. In Fig. 4.3, the output $I-V$ curves are presented for different V_{ov} [71]. The maximum drain current level at V_{ds} = 0.8 V with an V_{ov} of 0.7 V is around 900 mA/mm at 5 K for all InP HEMTs but for d_{sp} = 1 nm. The latter was due to its lower μ; see Fig. 4.2(a).

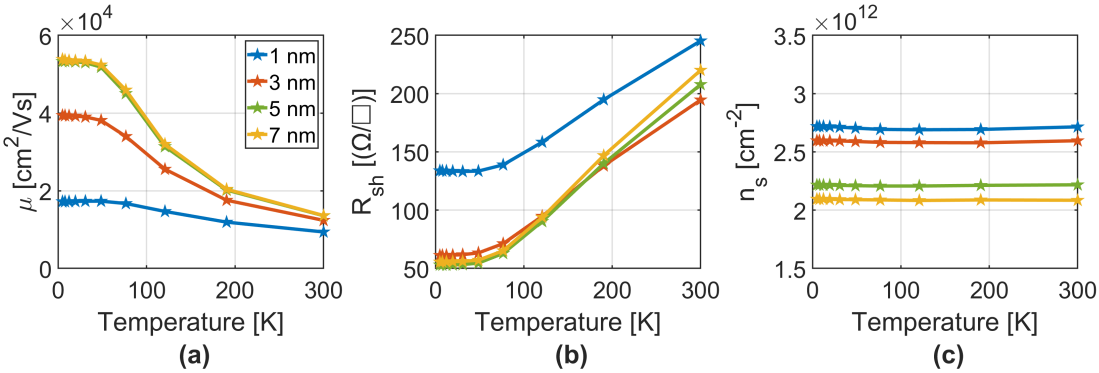

Figure 4.2: The (a) μ, (b) R_{sh} and (c) n_s of the epitaxial structures with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow).

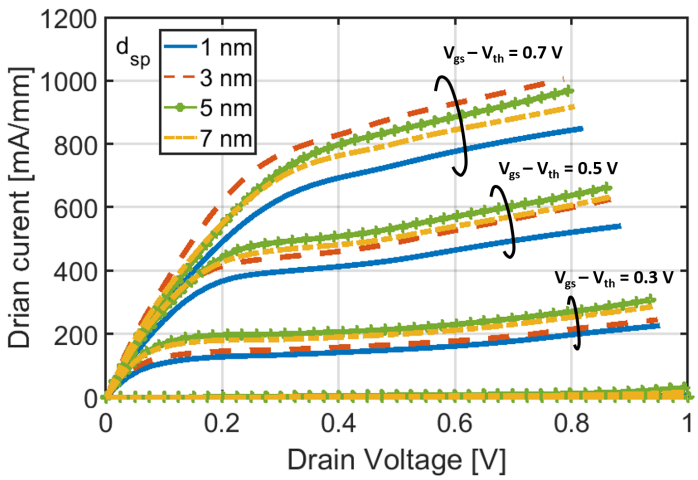

Figure 4.3: Drain current of the InP HEMTs with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. [From Paper B]

The g_m of the InP HEMTs with different d_{sp} in Fig. 4.4 illustrates that the InP HEMT with $d_{sp} = 3$ nm possesses the highest peak g_m at 5 K. This is consistent with its higher current driving capability at elevated drain and gate bias as shown in Fig. 4.3. The variation in V_{th} can be seen in Fig. 4.4. V_{th} is known to depend both on the barrier thickness x_d and δ-doping concentration n_D [3]:

$$V_{th} \approx \phi_{Bn} - \frac{qn_D x_b}{\varepsilon_s} - \frac{\Delta E_c}{q}, \tag{4.1}$$

ε_s is the dielectric permittivity for InAlAs, ϕ_{Bn} is the Schottky barrier height. The decrease of the barrier shifts the V_{th} positively, whereas the increase of the δ-doping concentration shifts the V_{th} negatively [72]. As a result, V_{th} as a function of d_{sp}, plotted in Fig. 4.5, experiences a maximum of around 0.1 V at 5 nm. This makes the cryogenic InP HEMT an enhancement mode (normally off) FET with $d_{sp} = 5$ nm.

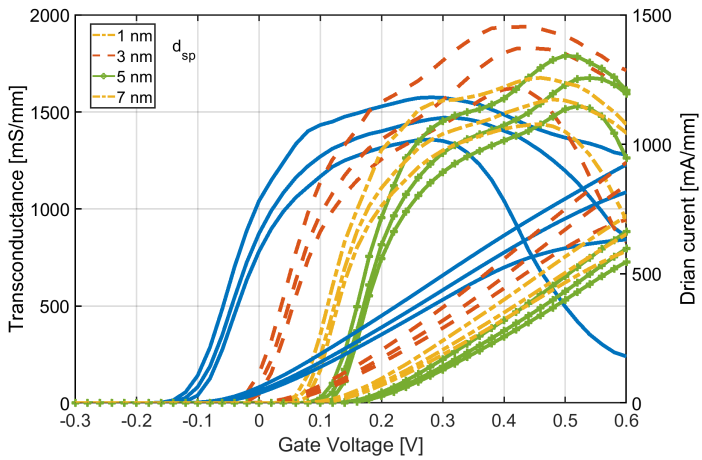

Figure 4.4: The transconductance (left) and drain current (right) of the InP HEMT with $d_{sp} = 1$ (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. $V_{ds} = 0.4$ - 0.8 V with step of 0.2 V.

Elevated I_g in the InP HEMT will increase the noise level and obscure the intrinsic channel fluctuations, in particular when using a 4-8 GHz LNA design. The I_g plotted in Fig. 4.6 indicates that the I_g for all the InP HEMTs was

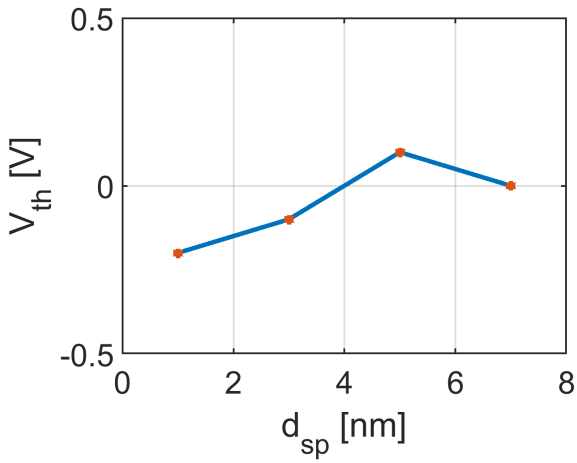

Figure 4.5: Threshold voltage V_{th} as a function of d_{sp} at 5 K.

below 0.1 μA/mm at the expected gate voltage for the lowest noise [59]. Such a low I_g level confirmed the successful development of the low-noise cryogenic InP HEMT given in Chapter 3. Hence, the I_g of the devices is not expected to present problems in the noise extraction procedures described in the next section.

The comparison of S-parameters up to 50 GHz for the InP HEMTs with different d_{sp} is demonstrated in Figures 4.7 and 4.8. The S-parameters are measured at 5 K at a bias of I_d=5 mA and V_{ds}=0.475 V which is the estimated optimum noise bias using the indicator $\sqrt{I_d}/g_m$ [53]. The input and output reflection coefficients S_{11} and S_{22} are very similar for all devices. The gain S_{21} of InP HEMTs with d_{sp} = 5 and 7 nm is slightly higher than d_{sp} = 1 and 3 nm due to their higher intrinsic g_m. Overall, the rf measurements indicated that all InP HEMTs did not show signs of any oscillation behavior at their optimum noise bias points.

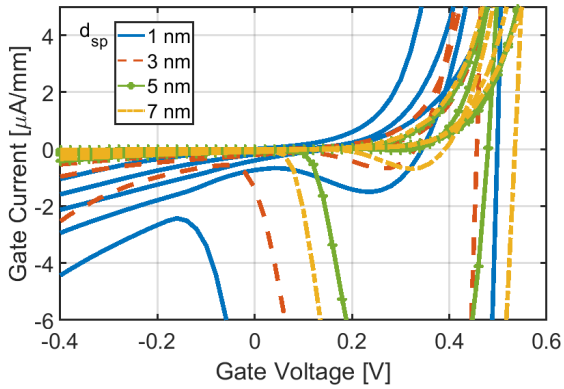

Figure 4.6: Gate current of the InP HEMTs with spacer thickness of 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K. V_{ds} = 0 – 1 V in steps of 0.25 V.

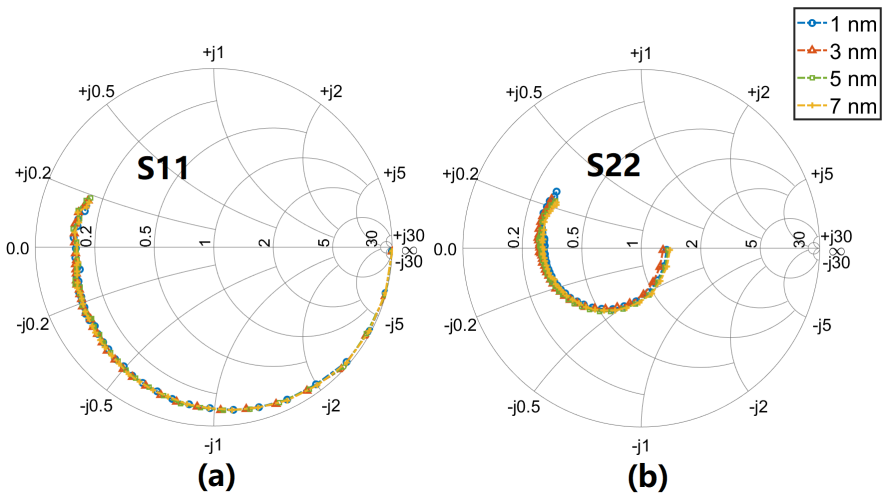

Figure 4.7: The (a) S_{11} and (b) S_{22} measurements at 5 K of the InP HEMTs with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) all at the bias points of I_d = 5 mA and V_{ds} = 0.475 V.

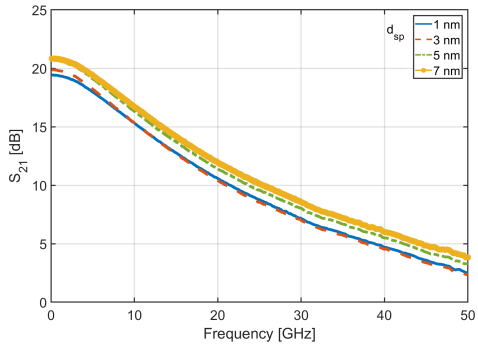

Figure 4.8: The S_{21} measurements at 5 K of the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) all at the bias points of I_d = 5 mA and V_{ds} = 0.475 V.

4.4 Noise characterization of 4-8 GHz cryogenic LNAs

The indirect method for the noise measurement (described in Chapter 2.2.2) was used for a high-accuracy noise comparison between InP HEMTs at cryogenic temperatures. To find the optimum bias conditions for lowest $T_{e,avg}$, the noise temperature was measured by sweeping the LNA drain current I_D. The optimum noise biases V_{DS} and I_D for the LNA and the corresponding biases (V_{ds}, I_d) for the InP HEMT are stated in Table 4.2 for various d_{sp}. Here the dc power consumption P_{LNA} for the LNA is also given. In Fig. 4.9, the minimum noise regions are indicated by the boxes.

The noise and gain of the LNAs based on InP HEMTs with varying d_{sp} at their optimum noise biases are plotted in Fig. 4.10. The $T_{e,avg}$ and average gain G_{avg} of the LNAs are listed in Table 4.3. All LNAs reveal a similar gain of around 40 dB which is indicative of the accuracy in the noise measurements. The $T_{e,avg}$ shows a minimum of 1.4 K for d_{sp} = 5 nm. This is 36% lower than the $T_{e,avg}$ of the InP HEMT with d_{sp} = 1 nm. In comparison with d_{sp} = 3 nm, which previously reported the lowest noise in this frequency range [23], the InP HEMT cryogenic LNA with d_{sp} = 5 nm exhibits a 20% lower noise level.

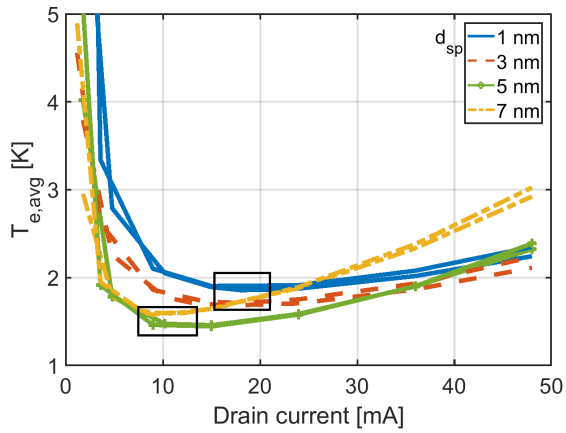

Figure 4.9: The $T_{e,avg}$ for InP HEMT LNAs with $d_{sp} = 1$ (blue), 3 (red), 5 (green) and 7 nm (yellow) versus I_D at 5 K and the drain biases of V_{ds}=0.325 V and 0.475 V. Black boxes indicate the minimum noise regions [From Paper A].

Table 4.2: The optimum noise bias and power consumption for the 4-8 GHz cryogenic LNAs based on InP HEMTs with different spacer thicknesses at 5 K.

d_{sp} (nm)	V_{DS} (V)	I_D (mA)	V_{ds} (V)	I_d (mA/ mm)	P_{LNA} (mW)
1	0.75	18.0	0.475	30	13.5
3	0.73	16.8	0.475	28	12.3
5	0.51	12.0	0.325	20	6.1
7	0.61	9.0	0.475	15	5.5

Table 4.3: The average noise temperature and gain for the 4-8 GHz LNAs based on InP HEMTs with different spacer thicknesses at 5 K.

d_{sp} (nm)	1	3	5	7
$T_{e,avg}$ (k)	1.9	1.7	1.4	1.6
G_{avg} (dB)	40	40	41	41

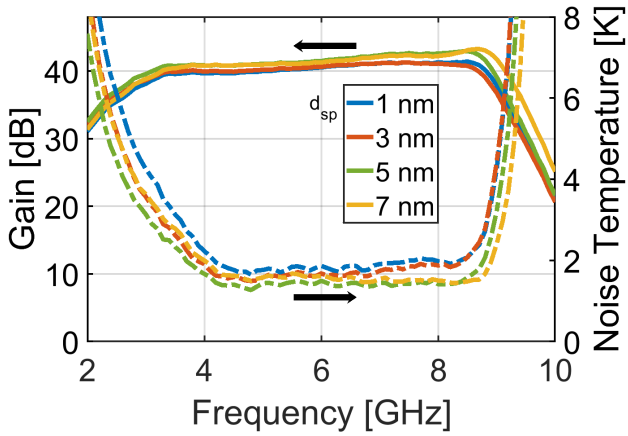

Figure 4.10: The measured gain (solid) and noise (dashed) temperature of three-stage 4-8 GHz hybrid LNAs integrated with the InP HEMT with d_{sp} = 1 (blue), 3 (red), 5 (green) and 7 nm (yellow) at 5 K using optimum noise bias for each LNA [From Paper B].

In addition to being superior in noise performance, InP HEMTs cryogenic LNAs with $d_{sp} = 5$ and 7 nm dissipate around 50% P_{LNA} less than the LNAs with $d_{sp} = 1$ and 3 nm; See Table 4.2. In summary, Tables 4.2 and 4.3 present convincing evidence that the d_{sp} is an essential parameter in noise and dc power reduction for the InP HEMT cryogenic LNA, here investigated for 4-8 GHz.

4.5 InP HEMT noise temperature

T_d for the InP HEMTs was extracted from the SSNM described in Chapter 2.2.3. The intrinsic small-signal parameters for the investigated InP HEMTs are presented in Table 4.4. The values are similar for all devices which is reasonable since they have identical geometries. The relatively low R_i and gate-source capacitance C_{gs} indicate a promising low-noise performance for all devices [56], [59]. The T_d of the InP HEMTs extracted at their optimum noise bias are plotted in Fig. 4.11. The error bars in T_d are estimated from the noise simulations covering the frequency band 4-8 GHz. In Fig. 4.11, the

Table 4.4: Intrinsic small-signal modeling parameters at the optimum noise bias for the InP HEMTs at 5 K.

d_{sp} (nm)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	G_{ds} (mS)	g_m (mS)	R_j (Ω)	R_i (Ω)
1	115	44	60	19	210	21	1
3	119	47	56	19	213	22	1.2
5	114	47	56	18	199	21	1.3
7	112	39	52	13	174	22	1.2

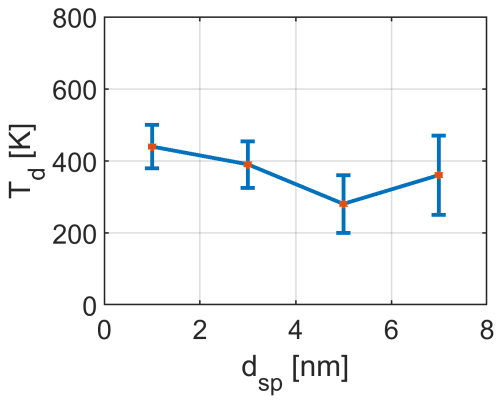

Figure 4.11: The T_d of the InP HEMT as a function of spacer thickness extracted at optimal noise bias at 5 K. [From paper B]

T_d exhibits a clear variation with d_{sp} for the InP HEMT at 5 K. It is observed that the T_d shows a minimum for $d_{sp} = 5$ nm.

Normally, a high μ for the channel material in the InP HEMT is targeted for low-noise applications according to the well-known semi-empirical noise expressions such as Fukui's equation [73]. Dopants serve as an efficient scattering for electrons at d_{sp} below 5 nm, as seen in the reduction of μ. While the scattering mechanism of the 2DEG can be of several physical origins, the impurity scattering is supposed to be significant at cryogenic temperature [74], which is consistent with the measured μ. However, the channel electrons in the investigated InP HEMTs are expected to move at saturated velocity [75]. The μ reflects the average transport of the 2DEG at a low electrical field and

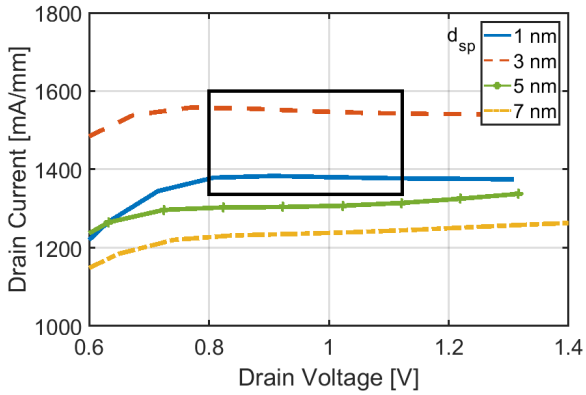

Figure 4.12: The drain current of the InP HEMT with d_{sp} = 1 (blue solid), 3 (red dashed), 5 (green solid-circle) and 7 nm (yellow dash-dot) at 5 K, V_{gs} = 1.14 V. The box in the diagram shows the NDR region [From Paper B].

thus gives limited information on the expected noise level in the intrinsic InP HEMT at low temperatures.

The d_{sp} variation does not affect impact ionization in the channel and ΔE_c. As discussed in Chapter 2, the RST in the InP HEMTs can be important for microwave drain noise [43]. The RST can be experimentally confirmed by the occurrence of negative differential resistance (NDR) in the $I-V$ output curves at elevated gate voltage [40], [76]. It has been proven that prior to the valley transfer, hot electrons experience RST via channel carrier emission into the barrier in the III-V heterostructure of a HEMT [77]. In Fig. 4.12, drain current versus drain voltage at 5 K is plotted beyond V_{gs} = 1 V. It is observed that the NDR is weak, yet observable for InP HEMTs with d_{sp} = 1 and 3 nm at $V_{gs} > 1$ V. The absence of NDR in Fig. 4.12 for d_{sp} = 5 and 7 nm is probably due to the more positive V_{th} of the InP HEMTs, which means they would have required a higher V_{gs} for the RST to be detectable. However, this voltage is far beyond the optimum noise bias range listed in Table 4.2. Nevertheless, RST noise in the InP HEMT may occur before it is detectable by NDR in $I-V$ measurements. It is therefore plausible that even a small fraction of channel electrons suffering from RST may lead to reduced confinement of the 2DEG, resulting in increased T_d for the transistor [43].

If the RST is responsible for noise in the HEMTs, keeping ΔE_c the same for all the epitaxial structures, the noise must be minimized for the lowest V_{ov} at optimum noise bias. This is confirmed in Fig. 4.13 where the V_{ov} shows a clear minimum for $d_{sp} = 5$ nm. V_{ov} illustrates a better correlation with T_d (Fig. 4.11) compared with μ as a function of d_{sp}. Therefore, it is suggested that the observed difference in the channel noise probed by T_d is due to RST in the intrinsic InP HEMT at low temperatures.

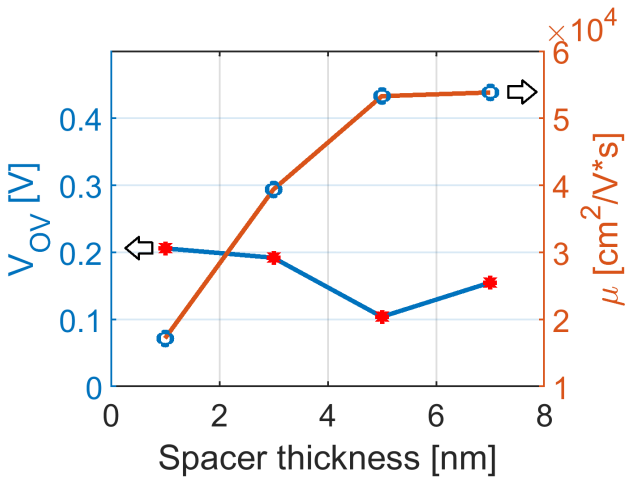

Figure 4.13: The V_{OV} at optimum noise gate bias and μ for the InP HEMT versus d_{sp} at 5 K.

In conclusion, this chapter presented convincing evidence that the d_{sp} is an essential parameter in noise and dc power reduction for the InP HEMT cryogenic LNA. The InP HEMT cryogenic LNA with $d_{sp} = 5$ nm is more suitable for qubit readout than the previous state-of-the-art InP HEMT using $d_{sp} = 3$ nm, offering both lower noise temperature and lower dc power. The variation in the channel noise with d_{sp} was proposed to be caused by RST between the channel and barrier.

CHAPTER 5

Investigation of Channel Indium Content

To further investigate the impact of HEMT epitaxial designs on the noise performance of cryogenic LNAs used in qubit readout, this chapter examines the role of the channel indium content. It has been reported that the $In_xGa_{1-x}As$ channel in the InP HEMT is crucial in determining the noise properties of cryogenic HEMT LNAs [26], [27]. The indium content in the channel influences the electron effective mass and the shape of the quantum well, both of which are important for noise performance. According to Fukui's equation [73], higher g_m correlates with a lower noise figure. Since g_m is directly related to the carrier velocity [3], the increasing μ in the channel should theoretically reduce noise in the HEMTs. The μ in the $In_xGa_{1-x}As$ channel is well-known to increase with a higher indium content [78].

However, recent studies indicate that a higher channel indium content in the InP HEMT does not always result in lower noise. For instance, [30] found that a composite InGaAs channel in an InP HEMT with a 5 nm InAs inset exhibited higher noise than one with a 2 nm InAs inset channel at room temperature. Similarly, [27] reported that an LNA with 80% indium channel InP HEMT showed nearly twice the noise temperature at 4 K compared to one with 65% indium [27]. These results point to a more complex relationship

Table 5.1: The channel indium content and thickness of the investigated structures in Fig. 3.1.

Indium (%)	*Thickness* (nm)
53	15
60	20
70	10

between μ and the resulting noise in the InP HEMT LNA, in particular at cryogenic temperature. This chapter is devoted to optimizing the indium content x in the $In_xGa_{1-x}As$ channel with respect to noise in the HEMT LNA for qubit readout.

5.1 Epitaxial design

The study is based on the noise in a 100-nm gate-length InP HEMT, utilizing the recess-last process and PECVD Si_xN_y passivation as detailed in Chapter 3. The barrier design was chosen based on the result in Chapter 4. Three different indium concentrations (x = 0.53, 0.60 and 0.70) in the active $In_xGa_{1-x}As$ channel of the InP HEMT were investigated. To compensate for the the varying strain levels, the channel thicknesses were varied as in Table. 5.1. The 53% indium content corresponds to a lattice-matched channel with no misfit. For the strained channels with 60% and 70% indium contents, the channel thickness was selected as half of the estimated critical thickness [3]. Since the δ-doping layer is positioned above the channel, the 2DEG will form in the quantum well just beneath the barrier-channel interface. This is shown by Schrödinger-Poisson simulations at 300 K in Fig 5.1 [79]. The confined 2DEG (close to the barrier) is not much affected by the channel thickness. At cryogenic temperatures, the Monte-Carlo simulation shows that the 2DEG confinement will even be stronger at 77 K than 300 K [80]. Given that the transistors were operated at a low drain current for low noise performance, the variations in channel thickness were not expected to impact the noise results for the InP HEMTs studied here. Apart from the channel variations, the epitaxial structures of the three InP HEMTs were identical.

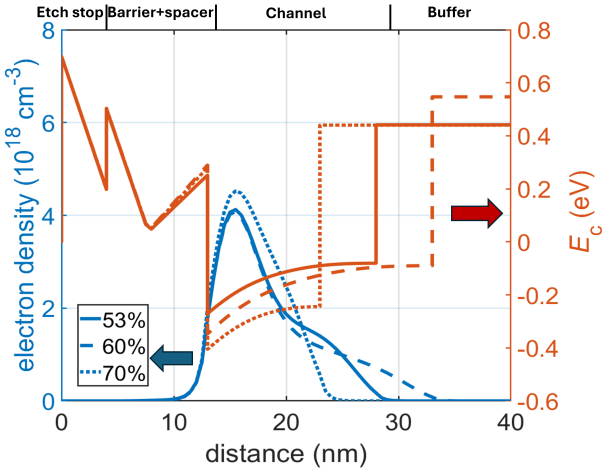

Figure 5.1: Schrödinger-Poisson simulated electron concentration (blue) and band structure (red) profile under the gate along the Y-direction for the three channels at 300 K.

5.2 Hall measurements

To evaluate the properties of the epitaxial structures, the same measurements were done as described in Section 4.2. The μ, R_{sh}, and n_s are presented in Fig. 5.2. As shown in Fig. 5.2(a), μ in the channel increased with both decreasing temperature and higher indium content. The increase in μ with indium concentration was more pronounced at lower temperatures. Below 50 K, the increase in mobility flattened out. At approximately 5 K, the μ reached 28,000, 48,000 and 89,000 cm^2/Vs for channels with 53, 60 and 70% indium content, respectively. This variation in mobility is reflected in the behavior of R_{sh} with temperature, as depicted in Fig. 5.2(b). Fig. 5.2(c) shows that n_s remained consistent at 2.2×10^{12} cm^{-2} for all channels, with less than 10% variation and no significant temperature dependence. According to Fukui's noise model [73], the noise characteristics of HEMTs are of more relevance to mobility-related parameters. The dependence on μ for InP HEMTs has been reported to be weakly dependent on the channel thickness with a similar n_s [81]. In this work, it was therefore assumed that the variation in channel thickness would not influence the noise results.

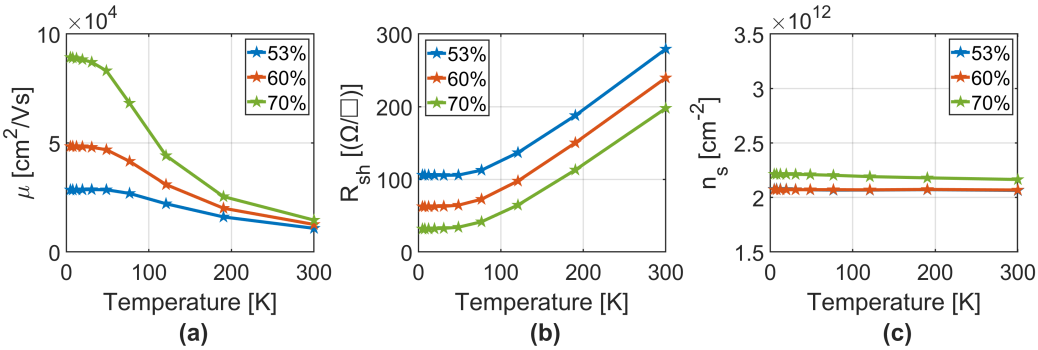

Figure 5.2: The (a) μ, (b) R_{sh} and (c) n_s of the epitaxial structures with 53% (blue), 60% (red) and 70% (green) indium channel.

5.3 DC and RF characterization

The dc and rf properties of the InP HEMTs, with a gate length of 100 nm and a gate width of 4×50 μm, were characterized on-wafer at 5 K. Fig. 5.3 illustrates the dc output characteristics at 5 K for InP HEMTs with 53%, 60% and 70% indium content in the channel. The kink effect observed for 70% is due to the surface traps created by the plasma cleaning before the passivation described in Section 3.3. However, this will not affect the lowest-noise bias region, highlighted with an open rectangle in Fig. 5.4, corresponding to a drain current $I_d \sim 15$ mA/mm and a drain voltage $V_{ds} \sim 0.5$ V [27]. To maintain the same I_d across different devices, the gate voltage V_{gs} must be adjusted.

Fig. 5.5 presents I_d and g_m as a function of V_{gs} at 5 K. The V_{th} are 0.10 V, 0.14 V and 0.16 V for 53%, 60% and 70% indium channels, respectively. Notably, the g_m curve for the 70% indium channel is the highest and narrowest, indicating the highest gain and f_t among the three devices [3], [30]. Compared to the 53% and 60% channels, the 70% indium channel shows the steepest increase in g_m versus V_{gs}, resulting in the smallest $\sqrt{I_d}/g_m$ value at the optimum low-noise bias (with 0.20, 0.21 and 0.16 $\sqrt{V \cdot mm/S}$ for 53%, 60% and 70% indium channel, respectively). According to [53], this suggests that 70% channel indium InP HEMT would have the lowest noise among the three devices in Fig. 5.5. However, as will be shown below, this conclusion is incorrect.

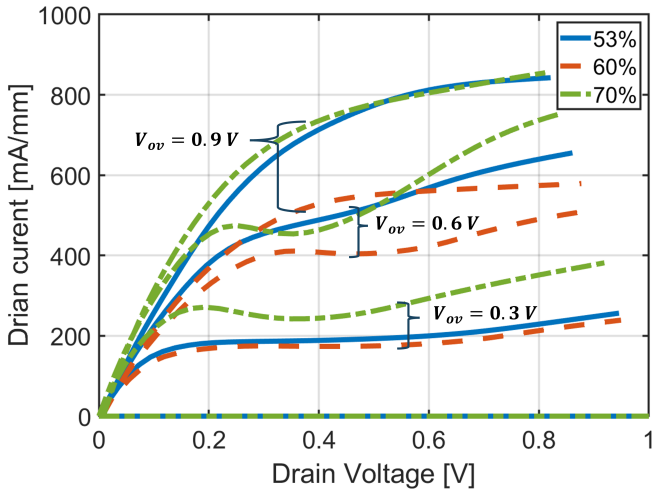

Figure 5.3: The I_d-V_{ds} characteristics of the 100 nm gate length InP HEMT using 4×50 μm gate-width layout with channel indium content of 53% (blue solid), 60% (red dashed) and 70% (green dash-dot) at 5 K. V_{gs}= 0.3, 0.6 and 0.9 V.

Fig. 5.6 presents experimental evidence for a low I_g (< 1 μA/mm) at 5 K in the gate bias range between 0 and 0.2 V. The amount of gate leakage is not expected to degrade the noise temperature of the InP HEMTs. However, the 'bell' shape of the 70% indium channel InP HEMT is more obvious than the other two devices, indicating a higher impact ionization for the 70% indium channel [82].

The S-parameters up to 50 GHz for InP HEMTs with different channel indium contents are compared in Figs. 5.7 and 5.8. Measurements were taken at 5 K with the optimum noise bias of I_d=5 mA and V_{ds}=0.475 V. The S_{11} are similar across all the devices, indicating a comparable matching condition. Differences in S_{22} are attributed to variations in output conductance. The gain S_{21} of the 70% indium content InP HEMT is higher due to its higher intrinsic g_m. Overall, the rf measurements showed that none of the InP HEMTs exhibited oscillation behavior at their optimum noise bias points.

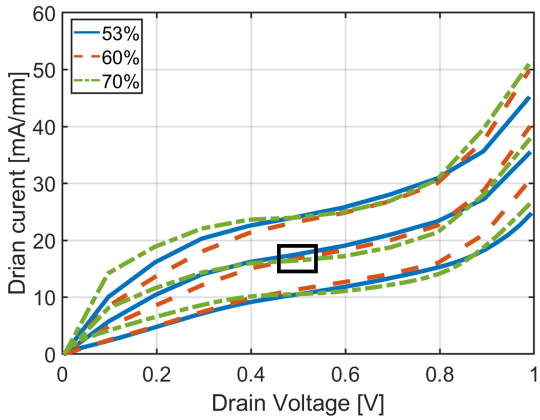

Figure 5.4: The I_d-V_{ds} characteristics of the InP HEMT with channel indium content of 53% (blue solid), 60% (red dashed) and 70% (green dash-dot) at 5 K. The open rectangle around V_{ds}=0.5 V highlights the low-noise bias region used for the HEMTs. For 53%, V_{gs}= 0.20, 0.21 and 0.22 V. For 60% and 70%, V_{gs}=0.24, 0.25 and 0.26 V [From Paper C].

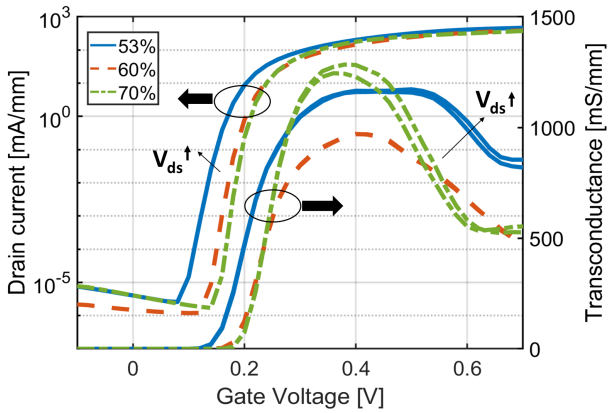

Figure 5.5: The I_d-V_{gs} and g_m of the 100 nm gate length InP HEMT using 4 × 50 μm gate-width layout with channel indium of 53% (blue solid), 60% (red dashed) and 70% (green dash-dot) at 5 K. V_{ds}=0.4, 0.5 and 0.55 V [From Paper C].

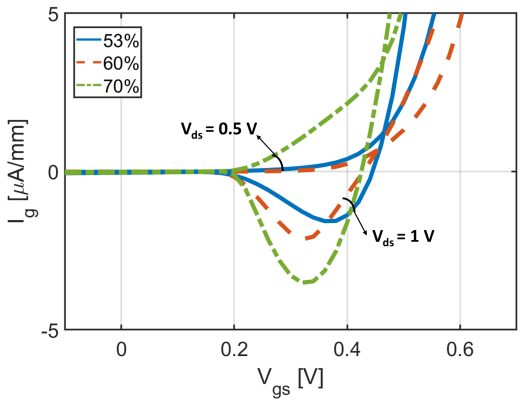

Figure 5.6: The I_g -V_{gs} of the 100 nm gate length InP HEMT using 4 × 50 μm gate-width at 5 K. V_{ds} = 0.5, 1 V. InP HEMTs with channel indium content of 53% (blue solid), 60% (red dashed) and 70% (green dash-dot).

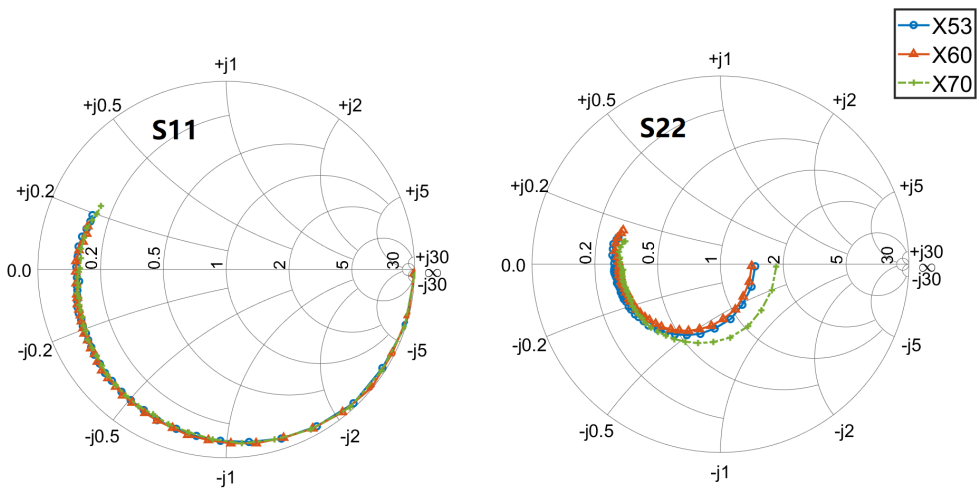

Figure 5.7: The S_{11} and S_{22} measurements at 5 K of the InP HEMTs with channel indium content of 53% (blue), 60% (red), and 70%(green) all at the bias points of I_d = 5 mA and V_{ds} = 0.475 V.

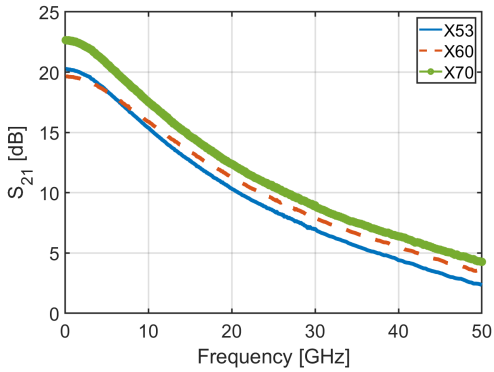

Figure 5.8: The S_{21} measurements at 5 K of the InP HEMTs with channel indium content of 53% (blue), 60% (red), and 70%(green) all at the bias points of $I_d = 5$ mA and $V_{ds} = 0.475$ V.

5.4 Noise characterization of 4-8 GHz cryogenic LNAs

A valid noise comparison between InP HEMTs at cryogenic temperature relies on high accuracy in the noise measurement. An indirect method, as described in Chapter 2.2.2, was used here[51], [83].

Fig. 5.9 shows the gain and noise temperature of the three LNAs at 5 K, equipped with InP HEMTs with 53%, 60% and 70% indium channels. All LNAs were noise-optimized at $V_{DS} = 0.7$ V and $I_D = 11$ mA. The LNA with 70% indium channel exhibited the highest gain of 45 dB whereas the LNAs with 53% and 60% channels showed gains of 41 dB. The measured $T_{e,avg}$ was 1.4 K for the LNA with 53% indium channel InP HEMTs and 1.2 K for both the 60% and 70% indium channel LNAs. Despite its higher gain, the LNA with the 70% indium channel did not exhibit a reduced $T_{e,avg}$ compared to the LNA with the 60% indium channel, indicating higher noise power for the 70% indium channel InP HEMTs.

The noise measurement procedure described in [83] allowed extraction of the noise temperature of the first-stage InP HEMT in the LNA. Fig. 5.10 shows that the first-stage noise temperature of 70% indium channel is slightly higher than that of the 60% (0.02 K). These small differences in noise can

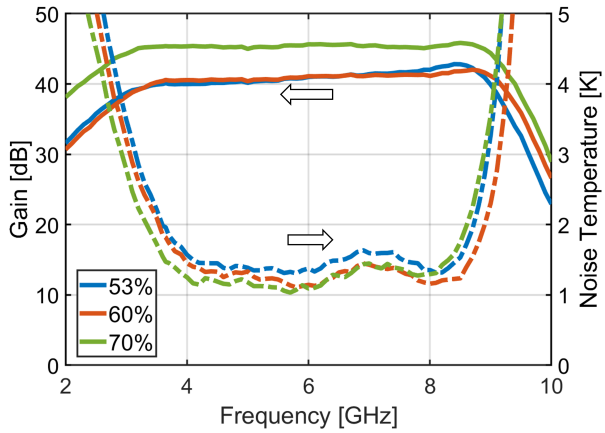

Figure 5.9: The measured gain (solid) and noise temperature (dashed) of three-stage 4-8 GHz hybrid LNAs integrated with the 100 nm InP HEMT with channel indium content of 53% (blue), 60% (red), and 70%(green) at an ambient temperature of 5 K. The optimum noise bias for all LNAs was V_{DS} = 0.7 V and I_D= 11 mA [From Paper C].

be further analyzed by plotting $T_{e,avg}$ and average gain G_{avg} versus the LNA DC power P_{LNA}; See Fig. 5.11 and 5.12. To ensure $T_{e,avg}$ remained minimal for all P_{LNA}, the V_{gs} bias was kept nearly constant at 0.2 V, 0.25 V, and 0.25 V for 53%, 60% and 70% indium channel, respectively. In Fig. 5.11, the $T_{e,avg}$ of the 60% indium channel is lower than that of the 70% for reduced P_{LNA} values, confirming the first-stage noise temperature observation in Fig. 5.10. This corresponds with a reduced gain difference between 60% and 70% indium channels at P_{LNA} values lower than 1 mW (Fig. 5.12). The LNA with 53% showed lower gain and higher noise compared to the LNAs with 60% and 70% indium channel in Fig. 5.11 and 5.12. Compared to the 4-8 GHz LNA result at 300 μW reported in [71], the best $T_{e,avg}$ in Fig. 5.11 was 0.9 K lower with the same G_{avg} = 23 dB. The LNA equipped with the 60% indium channel demonstrated a $T_{e,avg}$ = 3.3 K and G_{avg} = 21 dB at a P_{LNA} of 108 μW, representing a new state-of-the-art noise and gain for a C-band LNA operating below 1 mW.

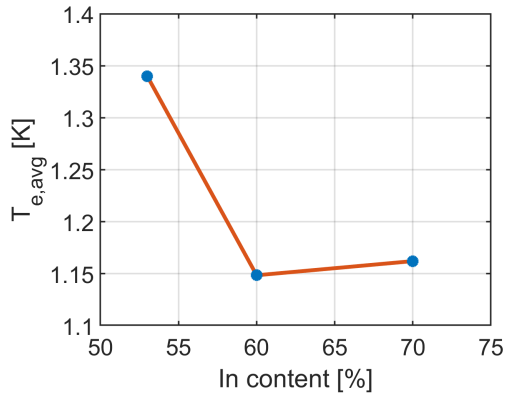

Figure 5.10: The first-stage noise temperature extracted from the three-stage InP HEMT LNAs as a function of channel indium content at an ambient temperature of 5 K [From Paper C].

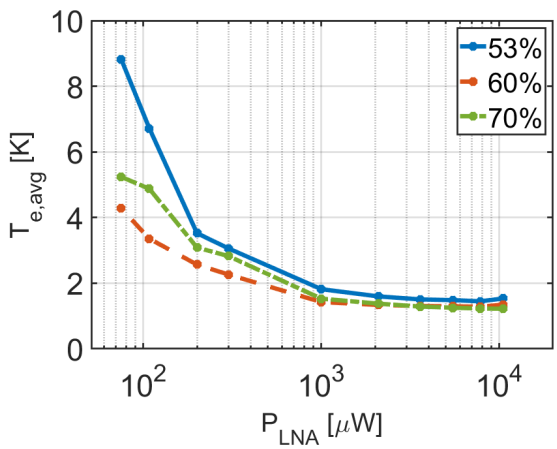

Figure 5.11: The average noise temperature as a function of dc power dissipation P_{LNA} for InP HEMT LNAs with 53% (blue), 60% (red), and 70%(green) indium channel at 5 K [From Paper C].

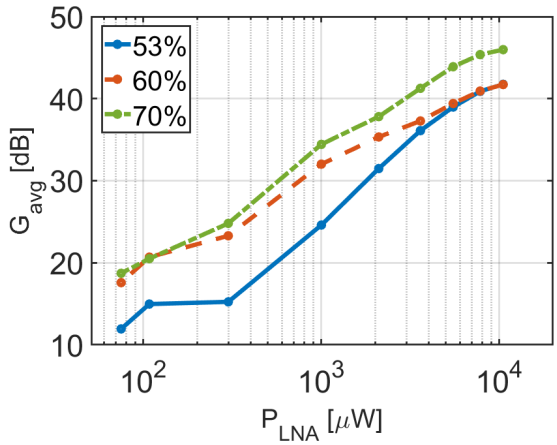

Figure 5.12: The average gain as a function of dc power dissipation P_{LNA} for InP HEMT LNAs with 53% (blue), 60% (red), and 70%(green) indium channel at 5 K [From Paper C].

5.5 InP HEMT noise temperature

The T_d of the InP HEMT, derived from the LNA noise measurement in Fig. 5.9 using the SSNM as described in Section 2.2.3, is depicted in Fig. 5.13. This figure shows the extracted T_d at the lowest noise bias for the InP HEMT alongside the μ versus channel indium content at 5 K. Despite the extraction of T_d normally having an inaccuracy of up to $\pm$ 100 K, Fig. 5.13 indicates a minimum T_d versus channel indium content, whereas μ shows an almost linear increase. At the optimum noise bias, the 70% indium channel exhibits a 20% higher T_d than the 60% channel. Thus, the lowest T_d appears to be associated with an optimum channel indium content, which does not correspond to the highest electron mobility.

With knowledge of the three-stage amplifier circuit configuration, the V_{ds} and I_d of the InP HEMT can be calculated from the LNA's V_{DS} and I_D. Fig. 5.14 shows T_d plotted versus V_{ds} for InP HEMTs with 53%, 60% and 70% indium channel. As expected, T_d increases with V_{ds} for all devices [22]. The 60% indium channel consistently shows a lower T_d than 53% and 70% indium channels across the entire V_{ds} range. Additionally, the 70% indium channel

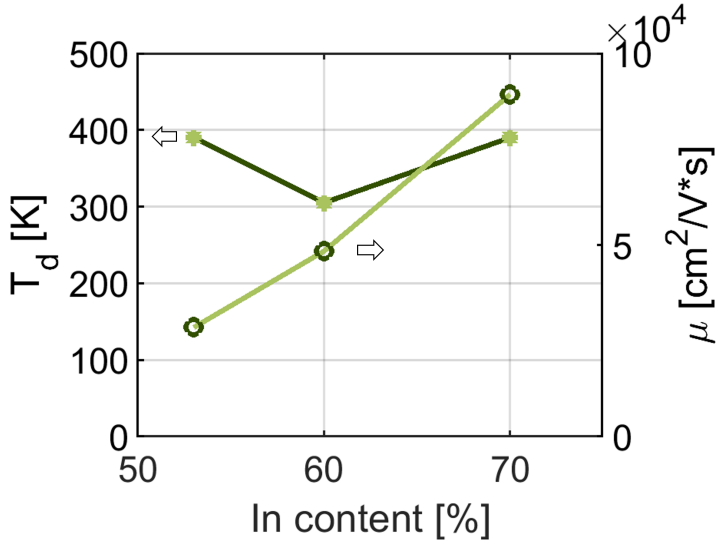

Figure 5.13: The drain noise temperature T_d (dark green line to the left axis) extracted at optimum noise bias of V_{DS} = 0.7 V and I_D = 11 mA and Hall electron mobility μ (light green line to the right axis) of the InP HEMT as a function of channel indium content at 5 K [From Paper C].

exhibits drain noise similar to the 53% channel at high V_{ds}. At the lowest V_{ds}, the T_d of the 70% indium channel is even larger than that for the 53% channel.

To analyze the noise contributions in the LNA, a circuit simulator based on the SSNM was employed, as described in Section 2.2.3. Simulations were performed for InP HEMTs with varying channel indium content. Fig. 5.15 displays the relative contributions of each noise source at the optimum noise bias in the HEMT LNA at 6 GHz and 5 K. As expected, Fig. 5.15 reveals that g_{ds} stands out as the primary factor for the total LNA noise temperature for all the InP HEMTs. The 70% indium content channel produces relatively high gate shot noise in the LNA due to higher I_g [84]. However, I_g contribution is not dominant for any of the investigated devices.

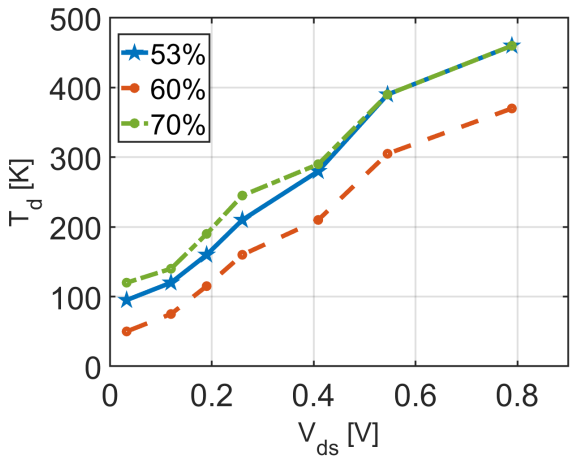

Figure 5.14: T_d as a function of V_{ds} for InP HEMT with 53% (blue), 60% (red), and 70%(green) indium channel at 5 K [From Paper C].

5.6 Temperature dependence of the InP HEMT noise

To understand the impact of the channel indium content on the channel noise of the InP HEMT, noise measurements as a function of temperature for these InP HEMTs with different $In_xGa_{1-x}As$ channels can provide valuable input for identifying the physical origin of the channel noise.

Depending on T_a, two different methods were employed for estimating the InP HEMT noise in the full temperature range of 4-300 K, as described in Chapter 2. At $T_a < 40$ K, an indirect method was applied and at $T_a \geq 40$ K, a direct method was used. In this way, high accuracy in noise measurement could be achieved both at low and high temperatures. For each indium channel content, five different InP HEMTs were measured. Additionally, three independent noise measurements were carried out at each temperature for each device.

In all noise measurements, the individual InP HEMTs were biased at a drain voltage $V_{ds} = 0.5$ V and drain current $I_d = 5$ mA. This corresponded to the lowest noise at 4 K and provided sufficient gain also at 300 K [30]. While the

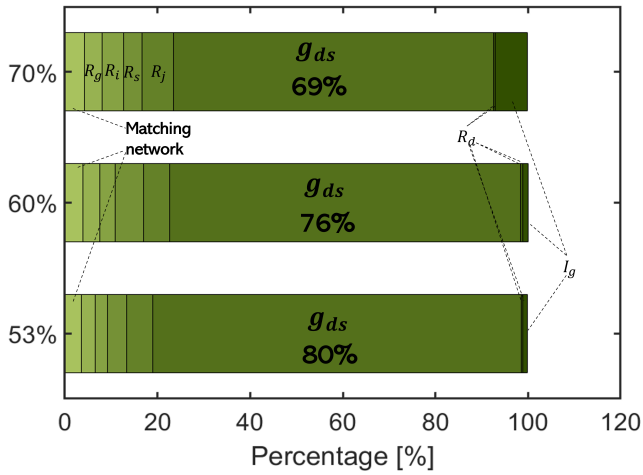

Figure 5.15: Simulated contribution for each noise source at the optimum noise bias in the three-stage InP HEMT LNA at 6 GHz. The InP HEMTs were of 53%, 60% and 70% indium channel. All simulations were carried out at 5 K [From Paper C].

InP HEMTs measured indirectly (using the LNA) had gate widths of 4×50 μm, the InP HEMTs probed on-wafer were 2×100 μm in size. The resulting difference in gate resistance between the layouts had a small effect on the gate thermal noise. However, that does not significantly affect the analysis carried out here for the channel noise [27]. For the indirect noise measurement at 4 K, the LNA had an average gain of 46 dB for the 70% channel and 42 dB for the 53% and 60% channel InP HEMT. For the direct noise method, the average gain of the InP HEMT from 80-300 K was between 15 and 17.5 dB, with the 70% channel exhibiting about 1.5 dB higher gain than the 53% and 60% channel InP HEMTs. The gain numbers were comparable to previously reported values used for high accuracy in noise estimation [30].

Fig. 5.16 illustrates the extracted T_d from 4 to 300 K for the InP HEMTs with channel indium content of 53%, 60% and 70%. The two different noise methods display the same trend in T_d versus T_a with an overlap for the 53% and 60% indium channel InP HEMTs below 100 K. The temperature dependence in T_d seen in Fig. 5.16 agrees with earlier observations in [50], [85],

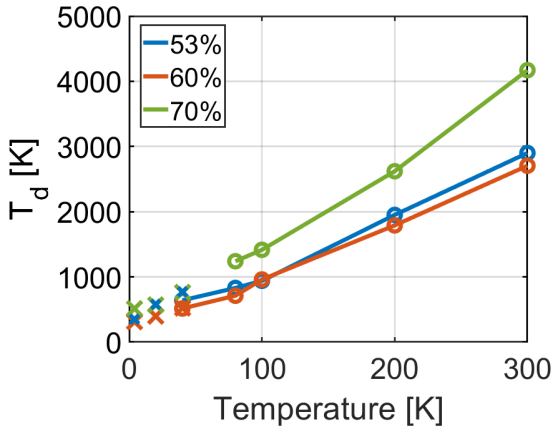

Figure 5.16: Drain noise temperature T_d versus temperature of the InP HEMTs with indium channel contents of 53%, 60%, and 70%. Circles represent noise data measured on-wafer and crosses using an LNA. The absence of on-wafer data below 80 K for 70% InP HEMT was due to oscillations occurring during probing [From Paper D].

[86]. Moreover, the data in Fig. 5.16 indicates that among the InP HEMTs, T_d is lowest for the 60% indium channel in the whole temperature range. The dependence on T_d with indium channel content at 4 K reported in Section 5.5 is thus confirmed.

The channel noise PSD S_{id} can be extracted as described in Eq. 2.10. A well-known observation when cooling the InP HEMT LNA is that noise reduction levels off at around 40 K [87], [88]. This is also true for the channel noise [50], [87], [89]. The S_{id} from on-wafer measurements is plotted in Fig. 5.17. S_{id} was modeled as a function of temperature by a linear decrease from 300 K to 40 K and extrapolated as a plateau between 4 K and 40 K. The S_{id} at 4 K from this model is plotted versus the indium channel content in Fig. 5.18. In the same figure, the calculated S_{id} is given from the indirect noise method at 4 K. The two noise measurements display the same trend versus indium channel content. The difference in absolute number between the direct and indirect methods can be attributed to different calibration procedures and the selection of T_a where the noise levels off.

Since thermal noise alone can not describe the channel noise [37] in cryo-

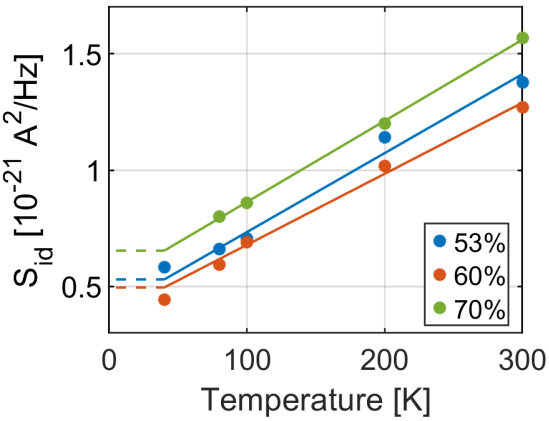

Figure 5.17: Measured (dot) and modeled (line) S_{id} versus temperature of the InP HEMTs measured on wafer. The solid line is a linear fitting from 300 to 40 K and the dashed line is the plateau below 40 K from the empirical model [From Paper D].

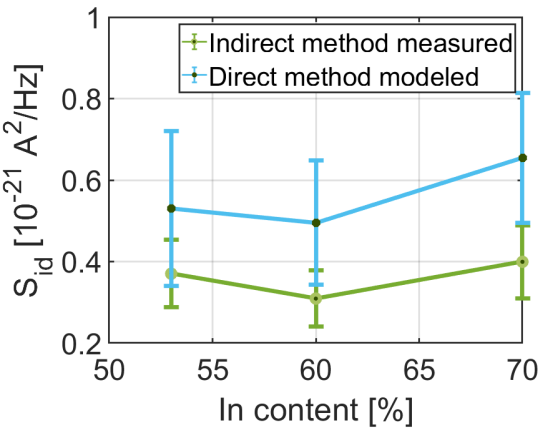

Figure 5.18: S_{id} at 4 K for 53%, 60%, and 70% indium channel InP HEMTs measured by an LNA (green) and extracted from the modeled on-wafer measurement (blue). Error bars were estimated from measurement uncertainties and fitting errors [From Paper D].

genic FETs, alternative noise sources have been proposed for the InP HEMT, e.g. suppressed shot noise [36], RST noise [43], or a combination of thermal noise and RST noise [90]. In a recently proposed model, the channel noise in the InP HEMT is treated as the sum of thermal noise and excess noise contributions [90]. The thermal noise is associated with thermal fluctuations of the carriers in the HEMT channel [91]. The thermal noise current PSD $S_{id,th}$ was calculated using Eq. 2.2 [33]. Fig. 5.19 illustrates $S_{id,th}$ as a function of temperature. Although this may slightly underestimate the thermal noise due to short-channel effects [33], Fig. 5.19 still demonstrates the trend in thermal noise related to the total channel noise for the various InP HEMTs. $S_{id,th}$ increases almost linearly from 4 to 300 K and contributes to the majority of channel noise at 300 K. The excess noise $S_{id,ex} = S_{id}$ - $S_{id,th}$ originates from non-equilibrium processes in hot electrons traveling under velocity saturation in the channel [92]. The $S_{id,ex}$ is plotted versus temperature in Fig. 5.20. For all indium channels, $S_{id,ex}$ remains relatively independent of temperature. Hence the excess noise dominates the total channel noise at 4 K.

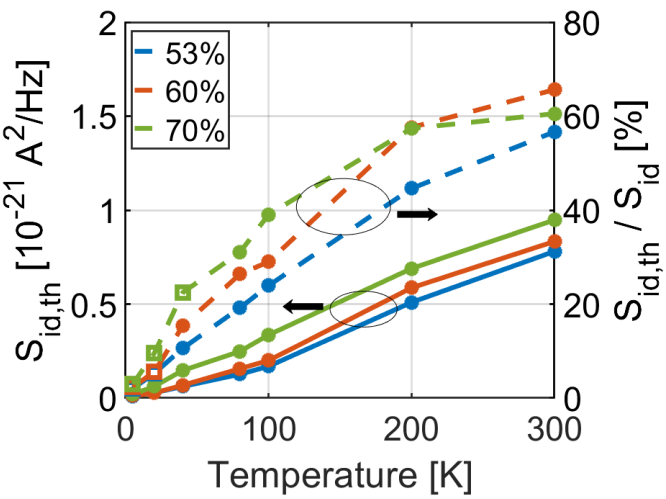

Figure 5.19: Thermal noise $S_{id,th}$ (left axis) and its contribution to the total channel noise (right axis) versus temperature in the InP HEMTs. Solid dots calculated from measured data, open squares from model extrapolation [From Paper D].

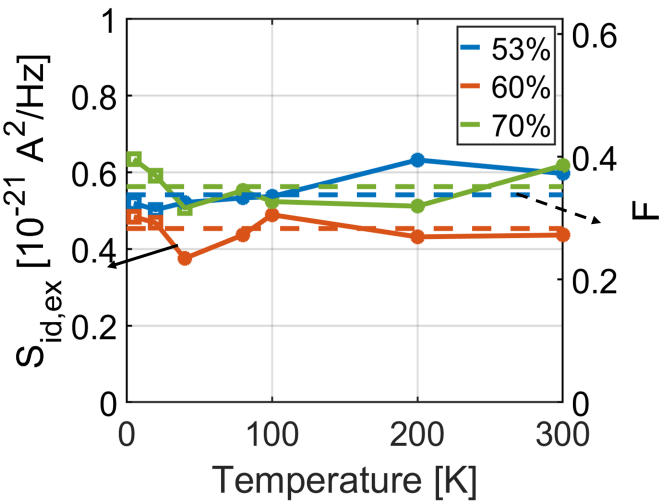

Figure 5.20: Excess noise $S_{id,ex}$ (solid lines, left axis) and average shot noise suppression factor F (dashed lines, right axis) versus temperature for the InP HEMTs. Solid dots calculated from measured data, open squares from model extrapolation [From Paper D].

The average shot noise suppression factor $F = \frac{\overline{S_{id,ex}}}{2qI_d}$ is plotted in Fig. 5.20. It is seen that the 60% indium channel exhibited the lowest $S_{id,ex}$ with a 25% lower F than the other two channels.

It is clear from Fig. 5.20 that the excess noise, being temperature independent, limits the reduction of noise with temperature in our InP HEMTs. The observation of a varying F for the same gate length among different indium channel InP HEMTs suggests that the excess noise involves hot-electron noise generation beyond suppressed shot noise [36]. Hot electrons can create noise by RST, as discussed in Chapters 2 and 4. This mechanism depends on the ΔE_c and V_{ov}. As depicted in Fig. 5.21, V_{ov} does not depend strongly on indium channel composition rather V_{ov} exhibits an almost linear increase with temperature similar for all InP HEMTs (the fluctuation seen in V_{ov} below 40 K comes from V_{th} saturation [13]). The RST is related to ΔE_c which is much smaller for 53% (0.52 eV) than for 60% (0.64 eV) and 70% (0.68 eV) indium channel InP HEMT as shown in Fig.5.22 [93]. Hence, a higher degree of RST noise is expected for the former device.

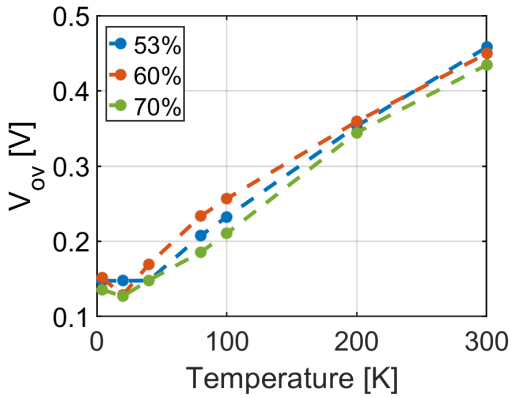

Figure 5.21: V_{ov} versus temperature of the InP HEMTs with indium channel contents of 53%, 60%, and 70% at 4 K.

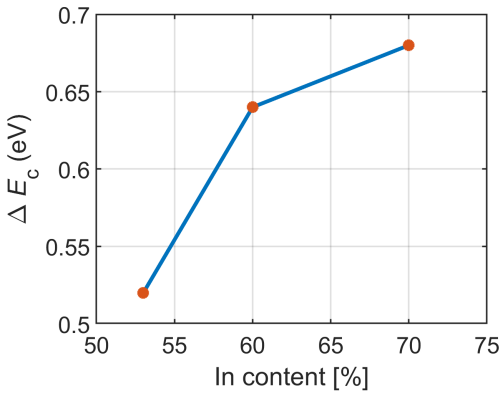

Figure 5.22: The conduction band offset as a function of the channel indium content.

Another potential source of hot-electron noise in the channel arises from impact ionization, typically accompanied by a significant increase in HEMT gate current I_g and I_d [82], [84]. In this study, I_g shown in Fig. 5.6 was measured to 5, 3 and 80 nA at 4 K at the low-noise bias (V_{ds} = 0.5 V, V_{gs} between 0.22 and 0.26 V for I_d = 5 mA), increasing to 10, 30, and 110 nA at

300 K, for 53%, 60%, and 70% indium channel InP HEMTs, respectively. The gate shot noise PSD $2qI_g$ was in the order of $10^{-26}\text{A}^2/\text{Hz}$ which is negligible in relation to $S_{id,ex}$ in Fig. 5.20. The 70% indium channel InP HEMT showed one order of magnitude higher I_g than the other two devices and is more prone to impact ionization related noise than the lower indium channel InP HEMTs. With an ionization coefficient exceeding 10^4 cm^{-1} at 300 K, which increases as temperature decreases [46], channel noise can be affected by impact ionization. Fig. 5.23 displays the g_{ds} at 4 K. The 'bell' shape of g_{ds} with $V_{gs} = 0.7$ V, $V_{ds} > 0.4$ V can be related to the traps on recess surface [82]. At $V_{gs} = 0.25$ V, $V_{ds} > 0.5$ V, the increase in g_{ds} accompanied by a 'bell' shape in I_g which indicates higher impact ionization for the 70% indium channel [82] than for the 53% and 60% indium channel InP HEMTs. Although g_{ds} and I_g do not exhibit a strong response at the low-noise bias, it has been shown that the impact ionization is more easily detected using noise than I_g [94]. Monte Carlo simulations have demonstrated that the increase of S_{id} due to impact ionization is much more pronounced than the increase in output I_d [95].

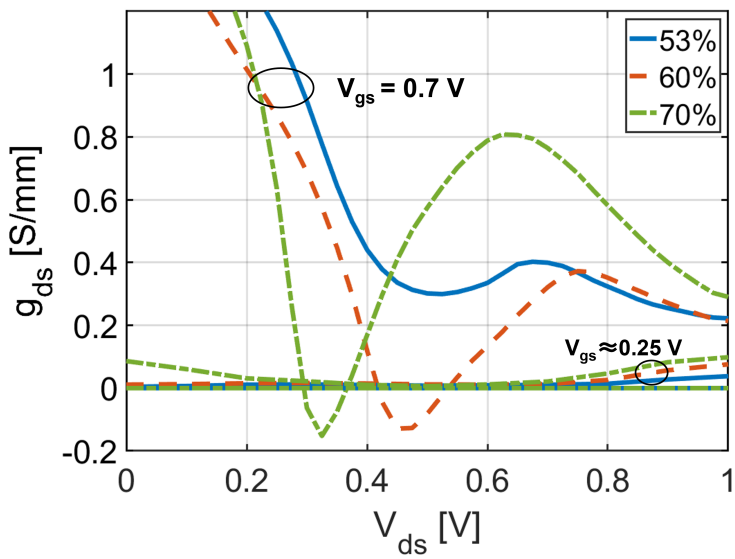

Figure 5.23: g_{ds} for low and high V_{gs} of the InP HEMTs with indium channel contents of 53%, 60%, and 70% at 4 K.

This is also supported by the report on impact ionization at similar bias conditions for InP HEMTs with InAs inset in a composite InGaAs channel at 300 K [96].

In conclusion, it was found that the 60% indium channel InP HEMT LNA showed lower noise temperature than the 53% and 70% indium channel between 4-8 GHz with a reduced P_{LNA} at 4 K, which makes it the best for qubit readout. The noise analysis of the InP HEMT revealed that the excess noise dominated the channel noise for all devices at 4 K and was independent of temperature. Excess noise was found to vary with the indium content in the $In_xGa_{1-x}As$ channel, despite identical gate length and drain current, indicating that excess noise in the channel cannot be attributed solely to suppressed shot noise. Additional noise generation in the channel for the InP HEMT is proposed to originate from RST and impact ionization. The optimization of the channel indium content resulted in a new state of the art for sub-mW C-band LNAs with $T_{e,avg} = 3.3$ K and $G_{avg} = 21$ dB at a total dc power of 108 μW.

CHAPTER 6

Conclusions and Future Work

6.1 Conclusions

This thesis presents achievements in the fabrication, epitaxial design, and analysis of low-noise InP HEMTs for cryogenic LNAs used in qubit readout circuits for superconducting QC.

First, the device technology, based on a 100-nm gate length InP HEMT process, was developed. The gate recess-last method (with respect to metallization) was found to suffer from electrochemical etching making the traditional HEMT fabrication unstable. This was solved by modifying the process to a recess-first variant yielding stable InP HEMTs regardless of the epitaxial structure. Following dielectric deposition, a plasma cleaning procedure prior to passivation was added to solve the problem of enhanced gate leakage at 300 K. Furthermore, no significant difference in noise and gain performance of the InP HEMT at 4 K was discovered for ALD and PECVD passivated devices. The HEMT process development made it possible to fabricate InP HEMTs with the high uniformity and yield required for the noise characterization in hybrid 4-8 GHz LNAs.

Second, a correlation between $T_{e,avg}$ and SS of the InP HEMT, both mea-

sured at 4 K, was observed and related to the traditional dc noise indicator $\sqrt{I_d}/g_m$. It is proposed that the SS for the InP HEMT measured at 4 K may serve as a rapid dc indicator for the device noise in a cryogenic HEMT LNA.

Third, two epitaxial design parameters in the InP HEMT structure were investigated: spacer thickness (1 to 7 nm) and channel indium content (53% to 70%). The channel noise estimated by T_d for the cryogenic InP HEMTs was determined from noise measurements of the HEMT LNA at 4 K. Electron mobility in the channel was found to be a poor noise indicator for the InP HEMT at low temperature. T_d exhibited a clear minimum with $d_{sp} = 5$ nm and 60% indium channel. The state-of-the-art for sub-mW C-band LNAs is presented with $T_{e,avg} = 3.3$ K and $G_{avg} = 21$ dB at a total dc power of 108 μW.

Fourth, a full temperature range noise measurement (4 - 300 K) was conducted for InP HEMTs with 53%, 60% and 70% indium content using both indirect and direct methods. Channel noise was interpreted as a combination of thermal noise and excess noise. It was concluded that the excess noise dominated at 4 K and remained essentially constant with temperature. Excess noise varied with indium content in the $In_xGa_{1-x}As$ channel, indicating the noise source cannot be solely attributed to suppressed shot noise. RST and impact ionization in the channel were proposed as additional contributors to excess noise. RST was confirmed by the correlation between T_d and V_{ov} at the optimum noise bias with d_{sp}, suggesting that the limiting factor for noise reduction in cryogenic HEMTs involves the injection of hot electrons from channel to barrier.

This study showed the significance of epitaxial optimization in InP HEMTs for cryogenic HEMT LNAs targeted for qubit readout. This has led to a better understanding of the noise mechanisms in the InP HEMTs, pointing out the further reduction of noise temperature in cryogenic C-band LNAs by mitigating hot-electron noise sources. The noise reduction in the InP HEMT LNA with sufficient gain will allow reduced power consumption, which is necessary for future large-scale QC.

6.2 Future work

As the SS showed a clear correlation with noise at cryogenic temperature, it would be valuable to explore the relationship between channel noise and SS

across varying ambient temperatures. The correlation will provide a further understanding of the physical origin of the high-frequency channel noise in InP HEMTs.

Additionally, another way to test the RST theory is to change the Al content in the barrier [43]. This will modify the ΔE_c without changing the channel material and control the hot electron fraction emitted from the channel into the barrier. If the theory is correct [43], a higher Al content barrier should result in reduced RST noise. In practice, however, a higher Al content in the barrier risks introducing more defects in the heterostructure.

This thesis has only focused on the influence of channel indium content and spacer thickness on noise in the InP HEMTs. Evidently, numerous material parameters in the epitaxial structure can affect the 2DEG in the InP HEMT. Thus, a study directly on the 2DEG modulation in relation to the noise of the InP HEMT will be important. Correlating the channel transport properties, such as saturation velocity with channel noise, could be one way to understand the HEMT even further [97].

A comparison between InP HEMTs and GaAs mHEMTs was conducted about ten years ago, revealing that InP HEMTs exhibited significantly better noise performance at cryogenic temperatures [98]. However, recent reports indicate substantial improvements in the cryogenic noise performance of GaAs mHEMTs [26]. Despite these advancements, cryogenic C-band LNAs utilizing InP HEMTs still demonstrate half the noise temperature compared to those with GaAs mHEMTs [11]. Therefore, further investigation into the differences in noise source contributions between InP HEMTs and GaAs mHEMTs would be highly desirable.

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Gothenburg, Sweden, September 2024

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