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All-2D CVD-grown semiconductor field-effect transistors with van der Waals graphene contacts

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Two-dimensional (2D) semiconductors and van der Waals (vdW) heterostructures with graphene have generated enormous interest for future electronic, optoelectronic, and energy-harvesting applications. The electronic transport properties and correlations of such hybrid devices strongly depend on the quality of the materials via chemical vapor deposition (CVD) process, their interfaces and contact properties. However, detailed electronic transport and correlation properties of the 2D semiconductor field-effect transistor (FET) with vdW graphene contacts for understanding mobility limiting factors and metal-insulator transition properties are not explored. Here, we investigate electronic transport in scalable all-2D CVD-grown molybdenum disulfide (MoS_2) FET with graphene contacts. The Fermi level of graphene can be readily tuned by a gate voltage to enable a nearly perfect band alignment and, hence, a reduced and tunable Schottky barrier at the contact with good field-effect channel mobility. Detailed temperature-dependent transport measurements show dominant phonon/impurity scattering as a mobility limiting mechanisms and a gate-and bias-induced metal-insulator transition in different temperature ranges, which is explained in light of the variable-range hopping transport. These studies in such scalable all-2D semiconductor heterostructure FETs will be useful for future electronic and optoelectronic devices for a broad range of applications.

Increasing demand for sustainable and energy-efficient electronics requires novel semiconductor materials on the smallest scales, with an objective to achieve enhanced control over their electronic, chemical and optical properties[1–3]. Presently, conventional silicon technology dominates the semiconductor industry, however, it faces challenges for ultrathin, self-powered, flexible, wearable and implantable integrated electronics[3–7]. This brings enormous interest in two-dimensional (2D) semiconducting transition metal dichalcogenides (TMDs) such as MoS_2 for a wide range of potential applications[2–11]. In addition to direct bandgap semiconductors[12], near-ideal band alignment, self-passivated dangling-bond-free surfaces, atomically thin bodies and ultrahigh optical absorption coefficients make them potential candidates for ultrathin field-effect transistors (FETs)[13], tunnel transistors[14], rectifiers[15], light-emitting diodes[16] and solar energy-harvesting devices[17,18]. Furthermore, realizing such 2D devices will create unprecedented opportunities in a broad range of industries, from consumer electronics to aerospace[19–21].

Despite these promising prospects, several challenges must be circumvented for their versatile applications. It remained challenging to form low-resistance contacts with 2D semiconductors[22,23], develop appropriate gate dielectrics and gate-electrodes[21,24], enhance channel mobility, grow large-area materials, develop scalable encapsulation processes[25] and discover reliable doping schemes[26] for atomically thin materials. The advantage of their layered structures enables van der Waals (vdW) heterostructures[27] without the constraint of lattice matching, offering numerous options for

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novel device design[4]. Graphene is a promising monolayer material for 2D semiconductor-based all-2D FETs, demonstrating novel electronic[28] and optoelectronic[29] functionalities. This includes the use of graphene with 2D semiconductors to demonstrate sub-nm gate length[30,31], gate-tunable Schottky barrier[32], mitigating Fermi-level pinning for electronics[33,34] and solar cells[17], highly sensitive photodetection[35] and light-matter interactions[36]. Usually, exfoliated materials[33,34,37,38] were used for preliminary investigation, but they are not favorable for industrial implementation. On the other hand, large-area 2D materials via chemical vapor deposition (CVD) process are inevitable for industry-compatible batch fabrication processes and integrated circuits[25,39–41]. However, all-2D CVD-grown 2D semiconductor FETs with graphene contacts are still in their infancy and detailed electronic transport and electron correlation properties of the devices for understanding mobility limiting factors and metal-insulator transition (MIT) properties with temperature are not explored[34,42].

Here, we combine CVD-grown 2D semiconductor MoS_2 and graphene in vdW heterostructure that offers the possibility to create devices with various functionalities. We demonstrate all-2D MoS_2 FET with graphene contacts, which shows low and tunable Schottky barrier and contact resistances, high ON current and good channel mobility. Temperature-dependent transport properties of the all-2D FETs are investigated to understand the evolution of scattering mechanisms for mobility limiting factors and the electronic correlations to explain gate- and bias-induced MIT. These studies on all-2D transistors are useful to optimize the performances for utilization in a broad range of applications at various temperatures.

Device fabrication and material characterization of all-CVD-grown MoS_2 FET with graphene contacts

To fabricate MoS_2/graphene vdW heterostructure devices, first CVD graphene (grown on Cu foil) is transferred to SiO_2/Si substrate. Next, graphene was patterned into stripes by electron-beam lithography (EBL) and O_2 plasma etching. Later, the wet transfer technique[43] was used to transfer CVD-grown[44,45] monolayer MoS_2 onto the graphene stripes. Subsequently, e-beam lithography was performed to make metallic contacts on the materials for studying transport properties in the devices (see the Methods for details). Figure 1a, b shows the schematic and fabricated device picture consisting of CVD-grown graphene and MoS_2 vdW heterostructure device on SiO_2/Si substrate, which is used to apply back gate (V_g). The corresponding band structures of graphene and MoS_2 are depicted in Fig. 1c, where graphene possesses semimetallic Dirac band and MoS_2 is an n-type semiconductor. In this device geometry, the gate voltage can tune the Fermi level (E_F) in both materials and influence the transport properties. Such tuning of E_F allows to reduce Schottky barriers that are inevitable for high-performance (opto-) electronic devices. First, we perform a Raman spectroscopy analysis of graphene and MoS_2 to investigate the atomic structure after the EBL and wet transfer technique. Figure 1d demonstrates the Raman spectra of bare graphene (bottom panel) and MoS_2 (top panel). The higher intensity of the 2D-peak compared to the G-peak with a very small D-peak in the Raman spectrum of graphene indicates the good quality of single-layer graphene[46]. As expected, the characteristic peaks (E_{2g} and A_{1g}) for single-layer MoS_2 are also observed in Raman spectrum analysis[47,48].

We performed electrical characterization of the individual materials to inspect the transport properties after going through the fabrication processes. Figure 1e presents the gate-dependent resistivity of the graphene channels in graphene-MoS_2 heterostructure and pristine regions. The Dirac points of graphene in the graphene-MoS_2 heterostructure and pristine regions are 8 V and 15 V, respectively. We estimated the maximum field-effect mobility[33] ($\mu = \frac{Lg_m}{WC_g V_{ds}}$) of graphene channels is about 1260 $cm^2 V^{-1} s^{-1}$ in the graphene-MoS_2 heterostructure region and 900 $cm^2 V^{-1} s^{-1}$ in the pristine

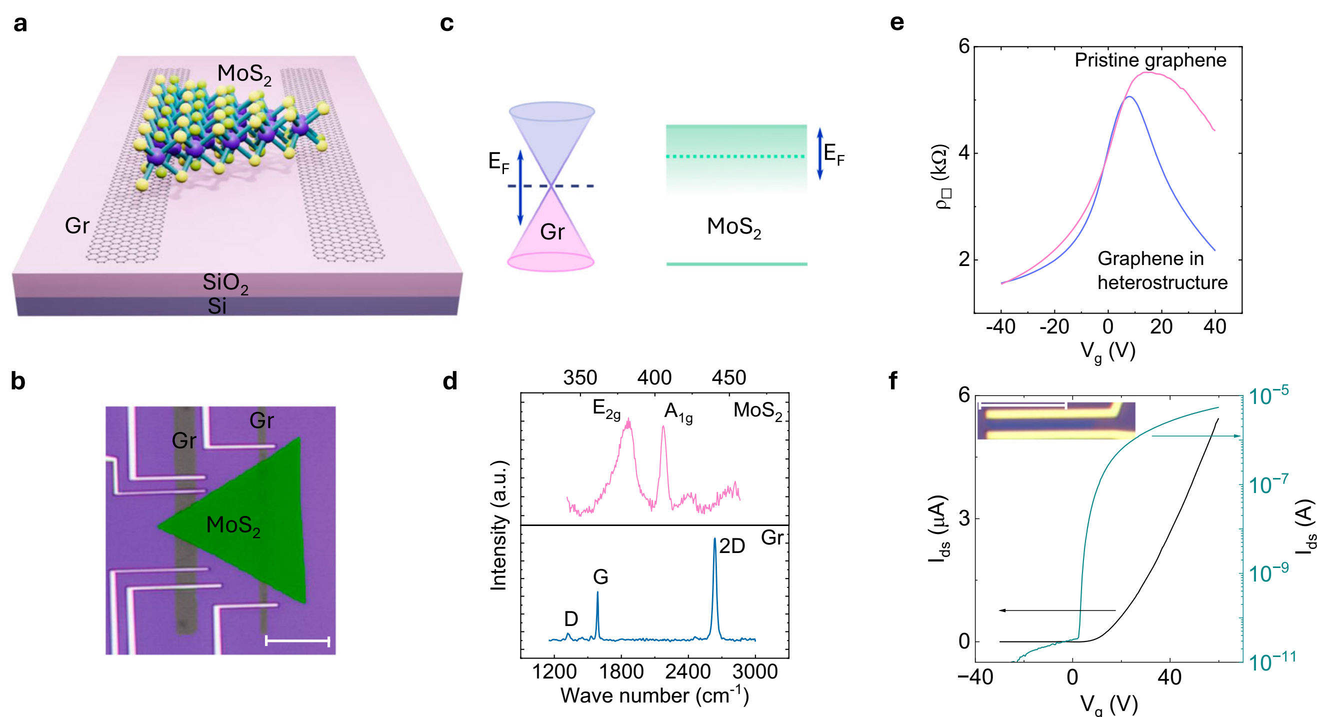

Fig. 1 | Device structure of all-CVD MoS_2 field-effect transistors with graphene contacts. **a** Schematic of the MoS_2 FET with van der Waals graphene contacts on SiO_2/Si substrate. **b** Optical image of the fabricated heterostructure device of CVD monolayer MoS_2 (colored-green triangle) transferred on the CVD graphene stripes. The metallic contacts on graphene are deposited for external electronic connections for electrical measurements. The scale bar is 10 μm, and the average channel width and length are 10.75 μm and 11 μm, respectively. **c** Band diagram of graphene and n-type MoS_2 along with associated Fermi levels (E_F) in these materials that are tunable via gate voltage (V_g). **d** Raman spectra of single-layer CVD graphene and MoS_2 using 638 nm LASER. **e** Gate-dependent resistivity of graphene channels in heterostructure and pristine regions, probed with four-terminal measurement geometry. **f** MoS_2 FET characterization with conventional metallic contacts showing I_{ds} vs. V_g at V_{ds} = 1 V in linear and logarithmic scale. All the measurements are conducted at room temperature. The device micrograph is in the inset, and the scale bar is 10 μm. The channel length and width are 1.4 μm and 12 μm.

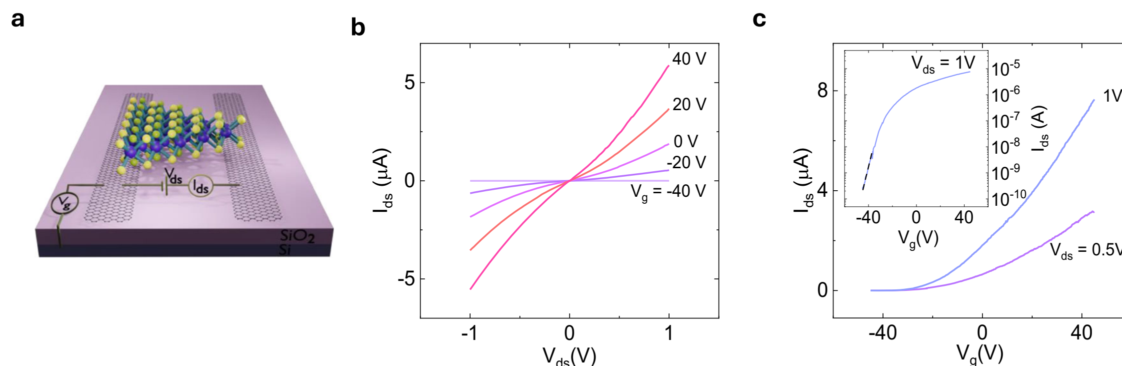

Fig. 2 | Transport properties of all-CVD MoS_2 FET with graphene contacts. **a** Schematic representation of the MoS_2 FET with graphene contacts. **b** I_{ds} vs. V_{ds} at various V_g of the MoS_2 FET with graphene contacts. **c** I_{ds} *vs.* V_g at different V_{ds} (0.5 V to 1 V) of the MoS_2 FET with graphene contacts. The inset shows the transfer properties in the MoS_2 FET with graphene contacts at V_{ds} = 1 V in logarithmic scale along with a linear fitting to estimate subthreshold swing.

region. Here, L, W, C_g, and g_m are channel length, width, gate capacitance per area (1.15 × 10-8 Fcm^{-2}) and transconductance, respectively. Higher μ of the graphene channel in the heterostructure region with respect to the pristine region can be due to the protection of the graphene channel from residues with top MoS_2 during the fabrication processes. Next, the source-drain current (I_{ds}) *vs.* gate voltage (V_g) of MoS_2 with metallic contacts at V_{ds} = 1 V in linear and logarithmic scale are depicted in Fig. 1f. Here, the I_{ds} increases with applying V_g towards positive value due to an upsurge of electron concentration in the channel, agreeing to the n-type transport mechanism in our CVD-grown MoS_2 material. The estimated μ = 1.9 $cm^2\ V^{-1}s^{-1}$, on-off ratio in this FET is about 10^6, threshold voltage (V_{th}) = 5.5 V and subthreshold swing (SS) = 1.42 V/dec. These preliminary electrical properties of the graphene channels and MoS_2 crystal imply hitherto the good quality of heterostructure devices, and the adapted wet transfer technique does not erode the phenomenal electrical transport properties of the materials.

Room temperature transport properties of all-CVD MoS_2 FET with vdW graphene contacts

The detailed transport properties of all-2D CVD MoS_2 transistors with graphene contacts are measured. Figure 2a shows the schematic of the fabricated MoS_2 FET with graphene contacts on the Si/SiO_2 substrate along with the measurement geometry. Current-voltage (I–V) properties at various V_g are presented in Fig. 2b. Channel current (I_{ds}) increases with increasing V_g due to an increase of carrier concentration in the MoS_2 channel and the I-V is slightly non-linear at higher V_g, which can be due to the long channel length (~ 11 μm) of MoS_2 and the vdW gap in the contact region[42]. Transfer properties (I_{ds} *vs.* V_g) at different V_{ds} are shown in Fig. 2c and the inset of Fig. 2c shows the I_{ds} as a function of V_g with V_{ds} = 1 V in a logarithmic scale. We find the V_{th} = -35 V, the on-off ratio is ~10^5, subthreshold swing, SS = 5.88 V/dec and mobility, μ = 14.5 $cm^2\ V^{-1}\ s^{-1}$ in this all-2D FET.

It can be noticed that the MoS_2 FET characteristic did not reach the off-saturation limit while decreasing gate voltage ($-V_g$), as shown in the inset of Fig. 2c. This could affect the calculation of on-off ratio and SS. It is to be mentioned that we took into account the non-uniform shape of the MoS_2 for mobility extraction. We approximated the channel width by averaging the channel width at the source and drain electrodes and considered the distance between the two electrodes as the channel length. Overall, we observed higher I_{ds} and μ, and lower V_{th} in the MoS_2 FET with graphene electrodes (Fig. 2c) with respect to the one with evaporated metallic electrodes (Fig. 1f). The performance enhancement of the MoS_2 FET with graphene electrodes could be due to the absence of Fermi-level pinning in the interface between the MoS_2 channel and graphene contacts[49].

Gate-tunable Schottky barrier and mobility in the all-2D CVD MoS_2-graphene heterostructure FET

Temperature-dependent transport properties of MoS_2 FET with graphene contacts (shown schematically in Fig. 3a) are investigated to understand device performance. The transport characteristic curves (I_{ds} *vs.* V_g) are shown in Fig. 3b from 70 K to 300 K at V_{ds} = 1 V. At this temperature (T) range with this applied V_{ds}, the transfer properties show insulating behavior, where I_{ds} decreases with decreasing temperature. The thermionic emission model is used to estimate the Schottky barrier (SB) height in this heterostructure junction, and the Arrhenius plots of $\ln(I_{ds}/T^{3/2})$ vs. 1000/T at different V_g are shown in Fig. 3c[22,50–53]. Figure 3d depicts the estimated SB at different V_g at V_{ds} = 1 V. The flat-band SB is found to be 52 meV at around V_g = 13 V. The SB decrease with increasing V_g, and at $V_g \geq 30$ V the calculation deviates from the thermionic emission model, limiting further estimation of SB.

Here, the applied V_g modulates the Fermi level (E_F) of graphene and MoS_2 simultaneously. Figure 3e shows the illustration of the band alignment of MoS_2-graphene FET to explain the gate modulation of SB. When V_g is lower (≤7 V), graphene electrodes are p-doped and the MoS_2 channel is in the off state, giving rise to a higher SB height. However, with increasing V_g, E_F in graphene electrodes moves toward the conduction band (CB), and in MoS_2, it moves towards E_c. At V_g = 13 V, the flat-band condition is reached (Fig. 3e, middle panel). Increasing V_g further moves the E_F in graphene into the CB and in MoS_2, E_F moves nearer to E_c. At $V_g > 13$ V, inversion in MoS_2 takes place and graphene shows accumulation contact properties[37,54].

To understand the mobility limiting factors in the all-2D CVD MoS_2 FET with graphene contacts, we estimated the mobility (μ) at different temperatures (T). The extracted μ at different T are shown in Fig. 3f along with a power law ($\mu \propto T^{\gamma}$) fitting (solid line)[55,56]. In this device at the lower T range (T ≤ 230 K), a slight change of μ with T is observed ($\gamma \approx 0.1$) due to impurity scattering. At the higher T range (T ≥ 230) K, μ decreases drastically with T ($\gamma \approx -1$) due to dominant phonon scattering[55,56].

Gate- and bias-induced metal-to-insulator transition in all-CVD MoS_2 FET with graphene contacts

To examine the responsible transport mechanisms, we further investigated the temperature-dependent transport properties of the all-CVD MoS_2 FET with graphene contacts at various applied biases (V_{ds}). The transport properties and corresponding color contour plots at different temperatures for various V_{ds} are depicted in Fig. 4a, b, respectively. The transport properties show insulating behavior at V_{ds} = 1 V in this temperature range at all V_g. In the insulating regime, I_{ds} increases with increasing T, and it can be observed in Fig. 4b (top panel) that the highest I_{ds} is observed at higher T = 300 K. Interestingly, at the higher V_{ds} (5 and 10 V), temperature-dependent transport shows similar characteristics. At the higher V_g (>60 V) and high T range (200–300 K), it shows metallic properties (I_{ds} decreases with increasing T), as shown in the bottom two panels in Fig. 4a, b. However, it shows insulating properties at lower V_g (<60 V) and lower T range (70–200 K). This kind of partial metal-to-insulator transition (MIT) at the higher V_g and V_{ds} in the all-CVD MoS_2 FET with graphene contacts is interesting because usually, MIT is observed in the MoS_2 FET with metallic contacts at the higher V_g and V_{ds} in a broad temperature spectrum[57].

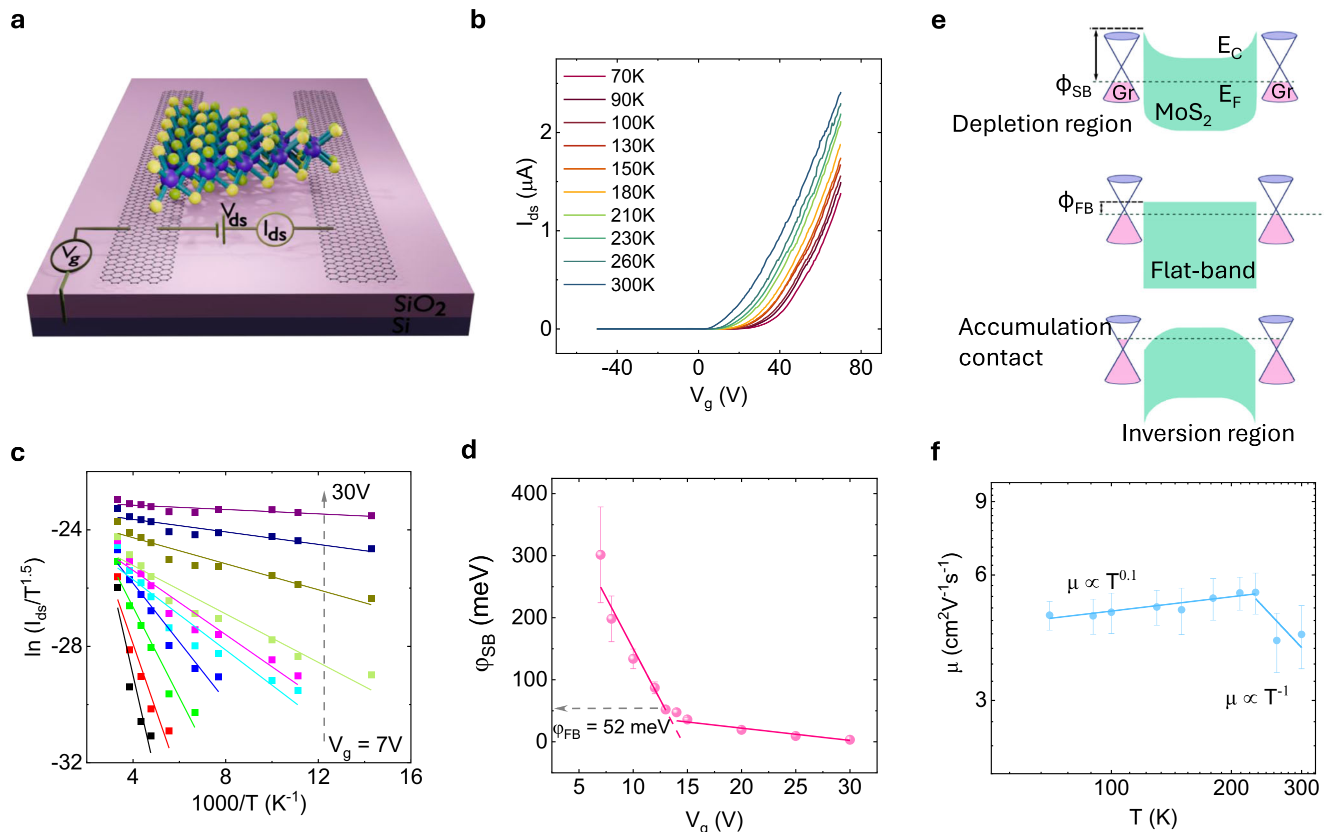

Fig. 3 | Temperature-dependent transport and Schottky barrier height in all-CVD MoS_2-graphene field-effect transistor (FET). **a** Schematic of all-CVD-grown MoS_2-graphene vdW heterostructure FET device and measurement geometry. **b** I_{ds} vs. V_g plots at V_{ds} = 1 V of the CVD MoS_2 FET with vdW graphene contacts. **b** I_{ds} *vs.* V_g at different temperatures with V_{ds} = 1 V. **c** Arrhenius plots of $\ln(I_{ds}/T^{3/2})$ vs. 1000/T at different V_g. **d** Estimated Schottky barrier at different V_g. **e** A pictorial illustration of band alignment to explain the reduction of the Schottky barrier at different V_g. In this measurement geometry, V_g changes the Fermi-level in graphene and MoS_2 simultaneously and modulates band structure accordingly from depletion to inversion region through the flat-band condition. **f** Estimated mobility (μ) at different temperatures with power law ($\mu \propto T^{\gamma}$) fitting (solid lines) in the all-CVD MoS_2 FET with graphene contacts.

Next, we correlated the gate- and bias-induced partial-MIT transport phenomena of the all-CVD MoS_2 FET with graphene contacts to a 2D variable-range hopping (VRH) model. This model accounts for transport carriers hopping through the trap states in the channel, such as defects in the MoS_2 crystal structure and trap sites at the MoS_2/SiO_2 and MoS_2/graphene interfaces. According to the VRH model[58,59], the conductance (σ) can be written as

$$\sigma = AT^m e^{-\left(\frac{T_0}{T}\right)^{\gamma}} \quad (1)$$

where A is constant, T_0 is a hopping parameter related to characteristics temperature, γ = 1/3 for charge transport that takes place in a wide (>>k_bT) band of localized states and m is between −1 and −0.8. The Arrhenius plots of ln $\sigma T^{0.8}$ vs. $T^{-1/3}$ in the all-CVD MoS_2 FET with vdW graphene contacts are shown in Supplementary Fig. S1 for various V_{ds} to estimate T_0. Previous reports on 2D materials showed 2D VRH transport and gate- and bias-induced MIT phenomena, where the localization length ($\xi^2 \propto 1/T_0$, see the equation 1 in the Supplementary Information) increases due to an efficient screening of the potential of trap states at higher carrier density[57–60]. The estimated ξ at different gate voltages with V_{ds} = 1 V, 5 V, and 10 V are depicted in Fig. 4c. It is conspicuous that ξ increases linearly to 25 nm with V_g at V_{ds} = 1 V, but at higher V_{ds} = 5 V and 10 V, ξ increases upto 50 nm and partial-MIT emerges.

Overall, high ξ values at the higher T range (>200 K) indicate unlocalized transport in the MoS_2 channel, where the carriers hop through unlocalized states, resulting in metallic transport within this T range. On the other hand, in the insulating regime, the carriers hop through localized potential barriers, as illustrated in Fig. 4d. At the elevated bias and high carrier concentration (V_g), the effective potential barrier of the trap states reduces, giving rise to the screening of potential trap sites that results in metallic transport with temperature in the all-CVD FET. However, the exact origin and mechanism of bias- and gate-induced MIT in 2D materials are yet to be well understood. Recently, the percolation-mediated 2D VRH model has been used to explain MIT in 2D semiconductors[57]. Furthermore, conductivity and temperature scaling behavior are also used to illustrate MIT due to the quantum-phase transition[61,62]. However, the demonstration of such scaling behavior does not unequivocally certify the corresponding effect for MIT observation because of the presence of other factors like weak localization, trap sites, and heating effects along with intermediate carrier density that can influence the transport mechanism[58]. Further theoretical insights, along with this experimental observation, can unveil the exact origin of the gate- and bias-induced MIT in such 2D semiconductors.

Summary and outlook

We demonstrated all-2D CVD-grown 2D FETs by combining scalable semiconductor MoS_2 channel with graphene contacts. We confirmed that the CVD-grown 2D materials can endure complex fabrication processes and exhibit good charge transport properties. We observed the ease of Fermi-level tunability of graphene contacts to MoS_2 *via* gate voltage, achieving appropriate band alignment, tunable Schottky barrier and improved channel mobility. Our comprehensive temperature-dependent transport measurements have shed light on the impurity and phonon mediated mobility limiting factors. Additionally, we observed gate- and bias-induced partial metal-insulator transitions due to the variable-range hopping mechanism in the all-2D CVD-grown FET. Utilizing graphene contacts overcomes Fermi-level pinning and enhances the transport

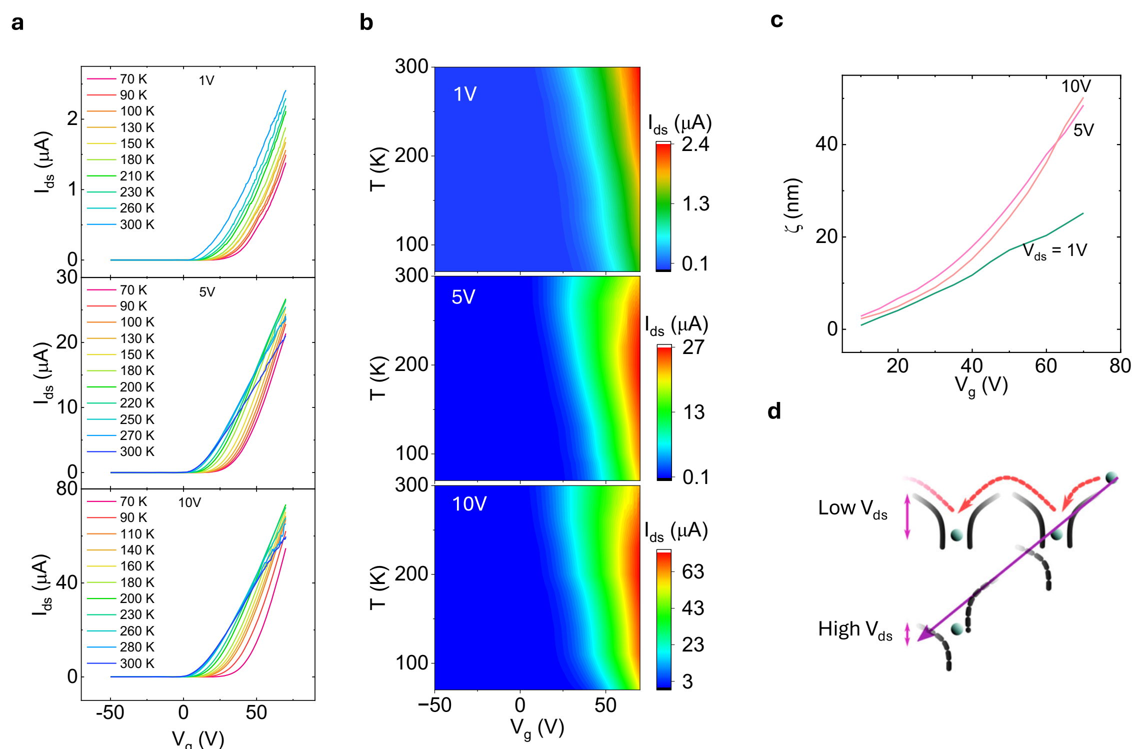

Fig. 4 | Gate- and bias-induced metal-to-insulator transition in the all-CVD MoS_2 FET with graphene contacts. a, b Measured temperature-dependent transfer characteristics and corresponding color contour plots of the all-CVD MoS_2 FET with vdW graphene contacts at V_{ds} = 1 V, 5 V, and 10 V, respectively. **c** Estimated hopping parameter, ξ, as a function of V_g for the MoS_2 FET with vdW graphene contacts at various V_{ds}. **d** Deformation of hopping potential barrier of the MoS_2 channel at low and high biases.

properties of MoS_2 FET with promising implications for sustainable electronics, optoelectronics and energy-harvesting devices. Further development of such high-performance scalable CVD-grown 2D FETs can pave the way for ultrathin, flexible, transparent, wearable, implantable and self-powered electronics.

Methods

The all-2D field-effect transistor was fabricated using all-CVD-grown monolayer graphene (from Graphenea) and MoS_2 heterostructures. The four-inch wafer-scale CVD graphene grown on Cu foil is transferred onto a highly doped SiO_2/Si (thermally grown 285 nm thick) substrate. First, graphene contacts were patterned by electron-beam lithography and oxygen plasma etching and cleaned afterwards by acetone and IPA. The CVD-grown monolayer MoS_2 layers of triangular shape with a typical size of about 50–100 μm were grown by the CVD process as described in George, A. et al.[44,45]. on a SiO_2 (300 nm)/Si substrate. A wet-transferred technique was employed to transfer CVD MoS_2 on top of CVD graphene contacts[43]. An appropriate heterostructure region was identified by an optical microscope for device fabrication. We used EBL to define the contacts and e-beam evaporation for depositing 1 nm TiO_2/80 nm Co, followed by the lift-off process in warm acetone at 65 °C. The use of such contacts is motivated by the observation of the lower Schottky barrier at the MoS_2-metal interface[50,51] and for spin transport studies[63]. The tunnel contacts are used to characterize only MoS_2 materials and the all-2D CVD MoS_2 is studied with graphene contacts. It is to be noted that no annealing was performed in the devices presented in this manuscript, but we believe that proper annealing, passivation and encapsulation can further improve the transport properties of the devices[64,65]. The highly doped SiO_2/Si is used as a back gate. We used Keithley 2612B dual channel source meter to apply bias and back gate voltages and to measure channel current. The transport measurements were conducted in a vacuum cryostat.

Data availability

The data that support the findings of this study are available from the corresponding authors on a reasonable request.

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Competing interests

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