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Word length dependent sensitivity penalty in high speed VCSEL based optical interconnects

M.Bilal Aziz, Stavros Giannakopoulos, *Member, IEEE,*, Alexander Grabowski, *Member, IEEE*, Peter Andrekson, *Fellow, IEEE, Fellow, Optica,*

***Abstract*—The use of long pseudo-random bit sequences to emulate random data in optical transmission links often gives rise to degradation of the receiver sensitivity for a given target bit error rate resulting in a power budget penalty. This is a well know fact and conventionally attributed to the non-ideal response of the system at very low frequencies. Here, we investigate this in the context of directly-modulated vertical-cavity surface emitting laser (VCSEL) based optical interconnects. We observe, both in simulations and in experiments, a substantial increase in the penalty with long sequences especially at symbol rates exceeding the VCSEL bandwidth. Our results show that this is related to the high frequency dynamic behavior of the VCSEL itself and we identify a few certain short bit sequences that cause the large penalty observed. We also show that the penalty can be significantly reduced by a simple modification of the sequences.**

***Index Terms*—Vertical-cavity surface emitting lasers, Optical interconnects, High speed data transmission, 850 nm, IM/DD, Pseudo-random bit sequence (PRBS), Fiber-optical communication.**

I. Introduction

In the world of high performance computing, from high performance signal processing units to cutting-edge data centers, optical interconnects (OIs) are essential for efficient and high speed performance. These interconnects are designed to provide seamless data flow between storage, switch, and computation units as well as among the integrated circuits residing within these units [1]–[4].

A vertical-cavity surface-emitting laser (VCSEL) combined with an intensity modulation and direct detection (IM/DD) scheme is preferred for short-reach optical interconnects. This preference is due to its cost efficiency, simple design, and ease of implementation [5]. Generating a test signal that emulates the random nature and continuous power spectrum distribution of a real signal is important for experimental purposes. Real signals can be approximated using pseudo-random bit sequences (PRBS) generated by a feedback shift register, offering bit streams of different lengths. These sequences, though deterministic, exhibit random behavior, making them suitable for testing the efficiency and performance of the system [6]. The length of the transmitted data sequence (word length) plays a crucial role. The longer the pattern, the closer it will be to a random pattern. This is important for mimicking real patterns and assessing system performance [7].

Previous work [8] has suggested the possibility that the presence of long sequences of identical bits may cause issues in the low-frequency region, which contributes to a penalty or an error floor in long patterns. Other studies [9], [10] have indicated that these long sequences of identical bits could induce a local temperature change in the VCSEL. Such work has been conducted with bit rates up to 40 Gbps, with some research using long word lengths extending to 50 Gbps in [11] (error floor of 10^{-4} using $2^{31}-1$ word length) and 56 Gbps in [12] (error floors of 10^{-7} and 10^{-3} using $2^{31}-1$ word length at 50 and 56 Gbps, respectively). To enhance data transmission in OIs with VCSELs as sources, a key objective is to minimize pattern dependency. Specifically, the goal is to bring the data transmission quality in long patterns closer to that of short patterns. However, the penalty in longer patterns, compared to short ones, cannot be entirely eliminated due to residual system penalties, where each component contributes a minor penalty.

Addressing these challenges, we investigate the relationship between word lengths and VCSEL performance, particularly highlighting the adverse effects of using longer word lengths at high bit rates and under extreme temperatures. Initially, we address the issue of residual system penalties. We demonstrate error-free data transmission (10^{-12}) at 50 Gbps using a $2^{31}-1$ sequence without any pre-emphasis or equalization, employing a non-return-to-zero (NRZ) on-off keying (OOK) modulation scheme. Next, we use the Cadence Spectre simulator with a comprehensive large-signal VCSEL model, as presented in the subsequent section. This methodology allows us to dissect the root causes of word length dependence in VCSELs, responding to previous assumptions and research. Contrary to earlier beliefs about longer word lengths, our study identifies significant underlying causes not related to low-frequency content and proposes a potential solution, corroborated through both simulation and experimental validations.

II. VCSEL equivalent model

Analytical approaches offer insights into certain aspects of VCSEL operation through exact mathematical solutions. However, capturing the full complexity of their behavior often necessitates numerical simulations. These simulations can approximate responses in more realistic and varied conditions, especially in the large signal domain. For our simulations, we used a physics based circuit-level large signal VCSEL model, designed for datacom applications [13], [14]. It is implemented in Verilog-A and uses subcircuits to model rate equations,

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The authors are with the Photonics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Gothenburg 412 58, Sweden (e-mail: bilalaz@chalmers.se; stagia@chalmers.se; alegra@chalmers.se; peter.andrekson@chalmers.se).

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input impedance, thermal impedance, and carrier transport and capture effects. Each sub-circuit tracks rates of various carrier and photon phenomena using current sources, and uses a voltage node to track the number of carriers in the separate-confinement-heterostructure (SCH) and quantum wells (QW), the number of photons in the resonator, temperature and input impedance, as well as noise sources specified in [14].

The sub-circuits are highly interdependent, as many parameters are temperature dependent, but also because several physical effects that increases a voltage in one sub-circuit will decrease it in another, such as carriers being captured from the SCH to the QWs. The model provides an output voltage proportional to the power of the light emitted from the VCSEL. Considering this and that the model is circuit based, we are able to perform simulations of our full experimental setup. A more thorough description of this model can be found in [13], [14]. The parameters used to perform the simulations are the same as specified in those papers, as the VCSELs used in our experiments is of the same design.

III. Experimental Setup

The experimental setup is shown in Fig. 1(a). The BERT generates 2^7-1, $2^{15}-1$ and $2^{31}-1$ patterns, which are then fed to a 6 µm aperture size VCSEL. Fig. 1(b) shows the VCSEL's frequency response. The VCSEL is placed in a closed capsule probe station where the temperature can be varied from -60 °C to +300 °C [15].

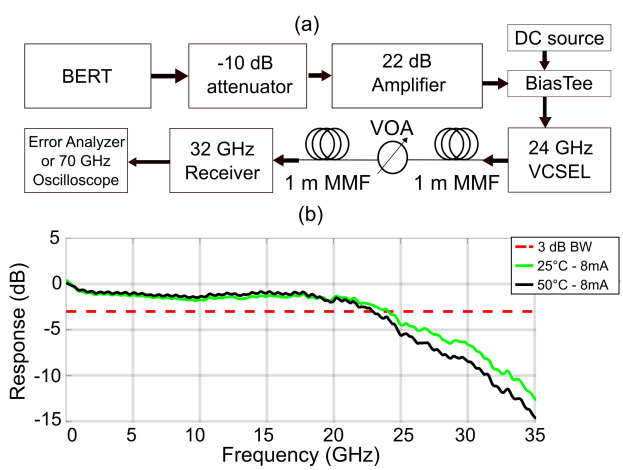

Fig. 1: (a) Experimental setup (b) Frequency response of the VCSEL.

IV. Results

A. Experimental Results

The system's word length dependent penalty was mitigated by systematic optimization, leading to an improved performance compared with [11], [12], with results shown in Fig 2. Operating at room temperature with $2^{31}-1$, we successfully achieved, for the first time 50 Gbps error-free transmission (10^{-12}) at an average received power of $\approx$ 5 dBm, not previously reported even with the application of differential signals, as discussed in [12]. Furthermore, we observed a word length dependent penalty (2^7-1 to $2^{31}-1$) of ≈ 1.5 dB at 40 Gbps and ≈ 9 dB at 50 Gbps. The system optimization also

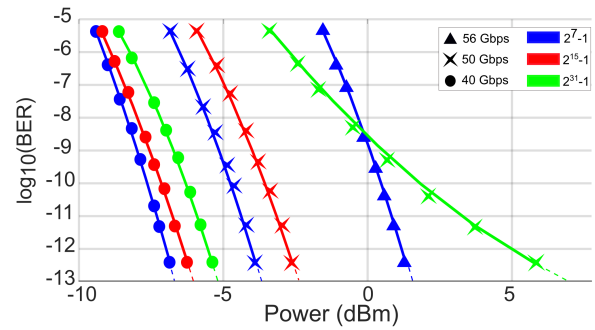

Fig. 2: Bit error rate vs received optical power using different word lengths and bit rates at room temperature.

reduced the power required for error-free transmission at 50 Gbps using $2^{15}-1$ to -2.7 dBm. Following the reduction of the system's residual penalty, the penalty is mainly attributed to the VCSEL and is subsequently investigated and addressed in section IV-C.

B. Simulation

The simulations were conducted using the Cadence Spectre simulator to investigate the additional penalties primarily associated with the VCSEL in the case of long patterns. In the initial phase, the setup described in [13], [14] was employed to capture the current values (representing binary 1s and 0s) entering the VCSEL. Subsequently, this setup underwent modifications to regenerate these recorded current values using a single, noise-free current source. This adaptation effectively substitutes all components preceding the VCSEL, thereby focusing solely on the influence of word length on VCSEL performance. Apart from a 1 TΩ shunt resistor, incorporated solely for convergence purposes, no additional components were present, ensuring that the VCSEL received an ideal input signal. The current source was set to generate ideal signals using different word lengths, and custom patterns, operating at temperatures of 25°C and 75°C. The high and low voltage levels correspond to the voltage levels of the signal driving VCSEL in full system. This was done to solely investigate the added penalties caused by the VCSEL for longer patterns.

C. Discussion

In this section, the penalties attributable to the long sequences were investigated. Previous research [8]–[10] suggested that the penalty in long patterns can be attributed to the small thickness of the epitaxial layers adjacent to the gain region, achieving local thermal time constant in the ns range. Fig. 3 shows simulation results that demonstrate, despite the presence of a large local thermal time constant, the thermal effects on the VCSEL remain minimal. In Contrast, our study demonstrates that these longer sequences are not the primary cause of the penalty.

Utilizing Cadence Virtuoso and the VCSEL model in [13], [14], we identified certain bit sequences, specifically variants of '000101' and '111101', as culprits for additional penalties in longer patterns. This issue arises when a low frequency component '000' or '111' is followed by a high frequency component '101', leading to the VCSEL's inadequate transition between low and high levels, and thus failing to generate

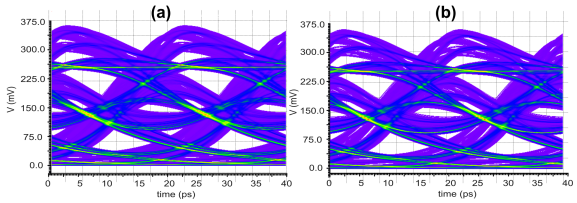

Fig. 3: Simulated received eye diagrams using $2^{15}-1$ at 50 Gb/s transmission with different thermal time constants. (a) 100 ns. (b) 10 µs.

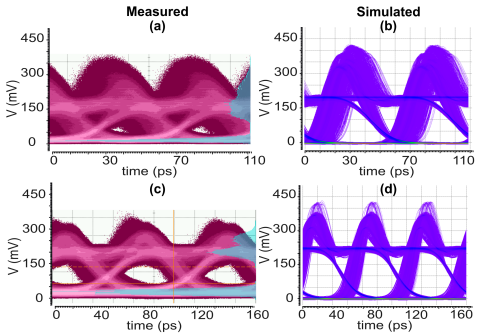

Fig. 4: Eye diagrams received at 25 Gbps and 100°C: (a) measured with standard $2^{11}-1$ sequence, (b) simulated with standard $2^{11}-1$ sequence for the full system, (c) measured with modified $2^{11}-1$ sequence, and (d) simulated with modified $2^{11}-1$ sequence for the full system.

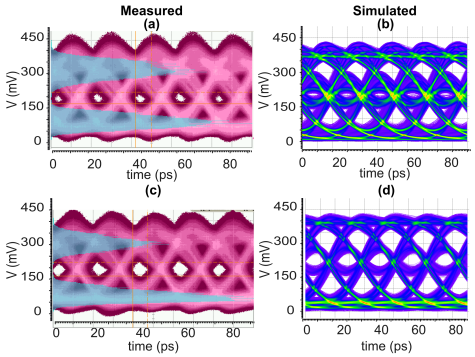

Fig. 5: Eye diagrams received at 50 Gbps and 50°C: (a) measured with standard $2^{15}-1$ sequence, (b) simulated with standard $2^{15}-1$ sequence for the full system, (c) measured with modified $2^{15}-1$ sequence, and (d) simulated with modified $2^{15}-1$ sequence for the full system.

sufficient amplitudes for high frequency bit sequences. The reduced instantaneous bandwidth of the VCSEL, which is explained later in this letter, is responsible for the additional penalties. We modified the problematic sequences 000101 to 000000 and 111101 to 111111, thereby creating sequences that mitigate the penalties associated with long patterns. Fig. 4 and Fig. 5 compare the eye diagrams of standard and modified sequences, incorporating both measurements and simulations. The simulations show good agreement with the measured diagrams, demonstrating improved eye openings with the modified sequences. This also evaluates the impact of extended identical bit sequences, as the modified sequence features even longer sequences of identical bits and achieves a more pronounced eye opening compared to the standard $2^{15}-1$ sequence.

Fig. 6 shows BER curves of the measurement setup using standard words (black) and modified words (blue). Error-free transmission at room temperature with standard PRBS sequences was achieved at 40 Gbps with a received power level of -4.0 dBm using $2^{15}-1$. Increasing the bit rate to 50 Gbps allows for error-free transmission at room temperature with a received power of -3.2 dBm using $2^{7}-1$ sequence. However, significant degradation is observed, evidenced by an error floor 10^{-10}, with a penalty of about $\approx$ 7.25 dB at BER = 10^{-7} when moving to a longer word length (i.e., $2^{15}-1$). Further increasing the temperature leads to a severe deterioration in the signal, indicated by an error floor 10^{-6} with a penalty of ≈ 3.1 dB at 10^{-6} at 50°C using $2^{15}-1$, and a penalty of ≈ 3.8 dB at 10^{-6} at 100°C using $2^{11}-1$. Fig. 6 illustrates the improvements in transmission achieved with the modified sequences compared to standard PRBS patterns. At room temperature, using $2^{15}-1$ sequence at 50 Gbps, the error floor was improved to allow error-free transmission with an average received power of 0.5 dBm. Under more severe conditions, significant error floors are eliminated using the modified sequences. Fig. 6 shows that the higher the temperature and/or bit rate, the more pronounced is the improvement in the penalty. This is because higher temperatures and/or bit rates stress the high-frequency dynamic behavior of the VCSEL more. As seen in simulations, sequences that are variants of ...000101... (which contain a jump from the low-frequency component ...000... to the high-frequency component 101) undergo greater distortion compared to other sequences. This is evident when comparing the 50 Gbps curves with the 40 Gbps curves, where the improvement in penalty is ≈ 1.2 dB. However, this reduction introduces a trade-off between the penalties and the loss of information as seen in Fig. 7. With the current penalty reduction strategy, a loss of $\approx 5-6\%$ in information was calculated using eq. 1.

$$\text{Information Loss} = \left(\frac{\text{Instances of '000101'} \times \text{Number of Bits Modified}}{\text{Total Number of Bits in PRBS Sequence}}\right) \quad (1)$$

Fig. 7 depicts the relationship between vertical eye opening and the information loss, derived from simulation data. The initial data points, marked in black and red, represent the eye diagrams for the standard $2^{15}-1$ and $2^{7}-1$ sequences without modifications respectively. Subsequently, we modified the default sequence, marked in blue, by selectively omitting (inserting zeros) certain segments of problematic patterns, i.e. '000101' and '111101'. The extent of deletion varied from 1 to 7 bits, with a single-bit deletion corresponding to an information loss of 1.72% when '000101' was altered to '000100', and 2.08% when modified to '000001'. The trend demonstrates that the vertical eye opening increases almost linearly with the incremental removal of information bits. This maximum loss occurs when all bits are deleted, converting '000101' and '111101' to '000000', signifying a cumulative deletion of 7 bits from the two sequences (2 bits from '000101' and 5 bits from '111101').

Fig. 7 illustrates that, based on simulation data, merely modifying the '000101' sequence (1.72% reduction of information loss) is sufficient to eliminate the additional penalties in long sequences, as exemplified by $2^{15}-1$ sequence. However,

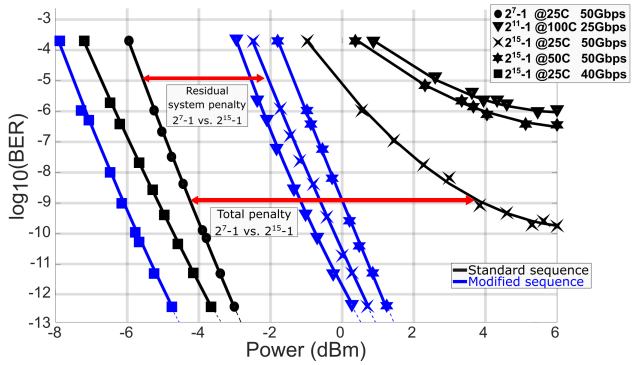

Fig. 6: BER vs received power for standard and modified sequences.

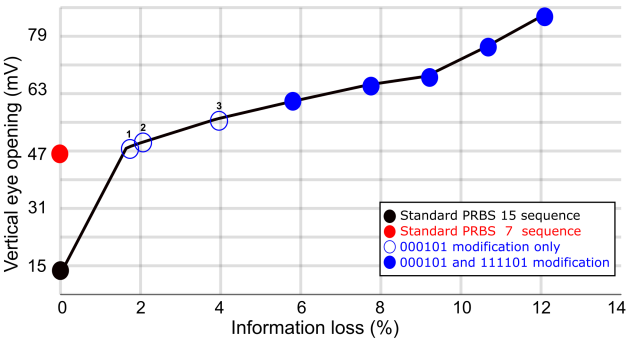

Fig. 7: Eye diagram opening as a function of Information loss in $2^{15}-1$ sequence. The empty blue circles show modifications from the sequence 000101 to 000100^1, 000001^2 or 000000^3, aimed at eliminating high frequency components.

in practical measurements, altering the '111101' sequence is also necessary to reduce the additional penalty associated with extended sequences (5-6% reduction of information loss). This requirement arises because, in an actual system, components preceding the VCSEL contribute to the word length penalty. Therefore, the signal received by the VCSEL is already influenced by this penalty, making the '000101' sequence a primary focus due to its direct impact on the VCSEL's performance. Upon close examination of the '000101' sequence, a consistent pattern emerges: long sequences exhibit a higher incidence of consecutive zeros preceding the problematic sequence than short sequences do. These zero sequences are implicated in shifting the VCSEL's operating point downwards on the IP curve—a shift that is less pronounced with shorter sequences such as 2^7-1 sequence. The resulting downward shift in the bias operating point, in turn, constrains the VCSEL's instantaneous bandwidth. This limited bandwidth precipitates a performance decline when the '101' sequence follows.

V. Conclusion

We presented high data rate transmission using NRZ OOK direct modulation of 850 nm VCSELs, achieving data rates up to 56 Gbps with PRBS sequences of varying lengths. This work demonstrates error-free transmission of long bit streams at high bit rates and elevated temperatures—an achievement not previously realized without equalization. Our findings suggest that the cause of this issue lies in the VCSEL's high frequency dynamic characteristics, pinpointing a limited number of specific short bit sequences as the culprits behind the substantial penalties noted. Furthermore, we demonstrate that a sequence modification can considerably reduce these penalties.

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