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Detection of Very Fast Interface Traps at 4H-SiC/AlN and 4H-SiC/Al_2O_3 Interfaces

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Abstract. Modest channel carrier mobility in SiC-MOSFETs with NO annealed gate oxides has been the main factor hampering development of low power devices (300 – 650 V). A very fast interface trap, noted as NI, has been suggested to be the main culprit for poor inversion channel carrier mobility. The origin of the NI trap is unknown, but it is likely a property of the SiO_2 and it is enhanced during post nitridation. In this study we show that the NI trap is also detected in 4H-SiC/AlN and 4H-SiC/Al_2O_3 MIS-capacitors. Observations are done using conductance spectroscopy and capacitance voltage measurements at cryogenic temperatures. This strongly suggests that the NI trap is a property of the SiC surface and not the dielectric used to form the SiC/dielectric interface. Furthermore, a scanning transmission electron microscopy (STEM) was performed to confirm that there are no SiO_2 layers or islands present at the 4H-SiC/AlN and 4H-SiC/Al_2O_3 interfaces.

Introduction

High voltage SiC metal oxide semiconductor field effect transistors (MOSFETs) with nitrided gate oxides have been commercially available for several years. However, SiC-MOFETs have struggled to enter the low voltage market. This is attributed to poor channel carrier mobility that results in high channel resistance and poor efficiency. A very fast interface trap, noted as NI, has been speculated to be the main cause of this poor performance hampering the development and manufacturing of low voltage SiC devices. Previous studies have shown the presence of the NI trap in dry thermal SiO_2 oxides, and that post annealing in NO ambient enhances the NI signal [1,2]. These NI traps cannot be observed at room temperature without using very high frequency measurements due to their very fast response time. By utilizing low-temperature capacitance-voltage measurements and conductance

spectroscopy we are able to observe the NI traps as a frequency dispersion in capacitance voltage spectra and as a peak in conductance spectroscopy at low temperatures. As these NI traps have been speculated to be a property of the SiO_2 oxide, other dielectrics have been investigated as an alternative to the SiO_2 gate dielectric. Dielectrics such as aluminium nitride (AlN) and aluminium oxide (Al_2O_3) are of great interest since they are high-k dielectrics. 2H-AlN is of special interest since it has well matching lattice structure to the 4H-SiC, both being hexagonal structures, and only having about 1.2% mismatch between the *a* lattice parameter [3]. AlN is used as a buffer layer on 4H-SiC before growing GaN on top of the AlN. Therefore, the growth method of AlN on SiC is well established. We made AlN/SiC and Al_2O_3/SiC MIS capacitors and applied capacitance-voltage and conductance spectroscopy methods at cryogenic temperatures. We observe that the NI traps are in fact present at the interfaces of these MIS capacitors. Furthermore, the interface is studied using scanning transmission electron spectroscopy (STEM) and electron energy loss spectroscopy (EELS) to investigate the possible presence of SiO_2 layers or islands at the SiC/dielectric interface. Our results strongly suggest that the NI trap is a property of the SiC surface and not the dielectric used to form the SiC/dielectric interface.

Experimental Details

Samples are grown on 4° off axis n-epitaxial 4H-SiC layer with net doping of 1 - 2×10^{16} cm^{-3}. The NO reference sample was made by dry oxidation at 1250˚C for 60 min, followed by annealing at 1250˚C for 60 min in pure NO. The AlN dielectric was grown using hot wall metal-organic chemical-vapour-deposition (MOCVD) at 1100°C resulting in a 30 nm thick 2H-AlN film. The growth method is detailed in [4]. The Al_2O_3 was grown using e-beam evaporation by depositing 1–2 nm of Al, followed by oxidation of Al on a hot plate at 200°C for 5 minutes in air. This cycle was repeated 12 times, resulting in a 15 nm amorphous Al_2O_3 thick film [5].
Quasi-static CV measurements were performed using Keithley 6517B electrometer. High-frequency CV measurements and conductance analysis were done using Agilent 4980A LCR meter by sweeping the gate DC voltage that is coupled with AC test signal with 10 mV amplitude at frequencies between 1 kHz and 1 MHz at fixed temperatures between 75 K and 300 K.
In the conductance spectroscopy analysis, the samples were cooled to 50 K without bias. At 50 K, a fixed DC voltage was applied, coupled with a 10 mV AC test signal with frequencies between 1 kHz and 1 MHz. The sample is then heated to 300 K with a fixed ramp of 5 K/min and the conductance is monitored.

Results and Discussion

Figure 1 shows the conductance spectra of both samples for differently applied voltages using 100 kHz test signal. The peak labelled as N(c) in both graphs is due to nitrogen doping ions located at cubic sites in the SiC epilayer. The peak that appears in both samples between 140 – 160 K and increases and shifts to lower temperatures as higher gate voltage is applied, is the NI signal observed in NO annealed and dry oxides [2, 6]. The broad signal at higher temperatures, above 250 K, is labelled as OX and is due to slow interface traps [2].

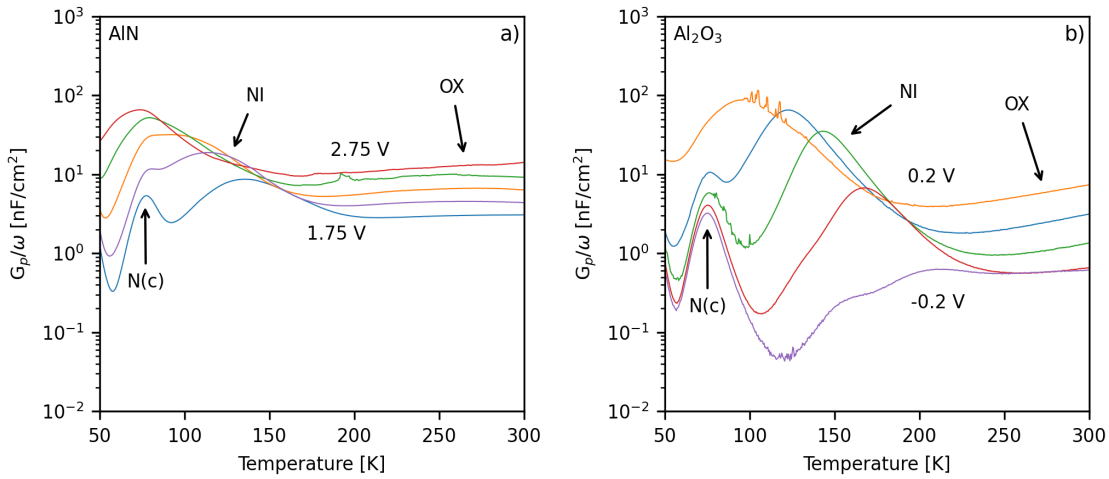

Fig. 1. Conductance spectroscopy spectra of a) AlN and b) Al_2O_3 samples for differently applied gate voltages at 100 kHz.

Figure 2 shows capacitance–voltage spectra of both samples at 300 K and 75 K. At 300 K both samples exhibit insignificant frequency dispersion between the high frequency measurements, but some dispersion is observed between the quasi-static and the 1 kHz curve. This is due to slow traps and corresponds to the OX signal in the conductance spectroscopy measurements. At 75 K, a large frequency dispersion appears in the higher frequency measurements revealing a presence of high density of very fast traps with energy close to the SiC conduction band edge. This dispersion is attributed to the NI trap [6]. Note that in Fig. 2 c) and d) the quasi-static measurements of the Al_2O_3 fit poorly to the higher frequency measurements. This is due to the sensitivity of the Al_2O_3 film, which is very sensitive to charge injection and leakage.

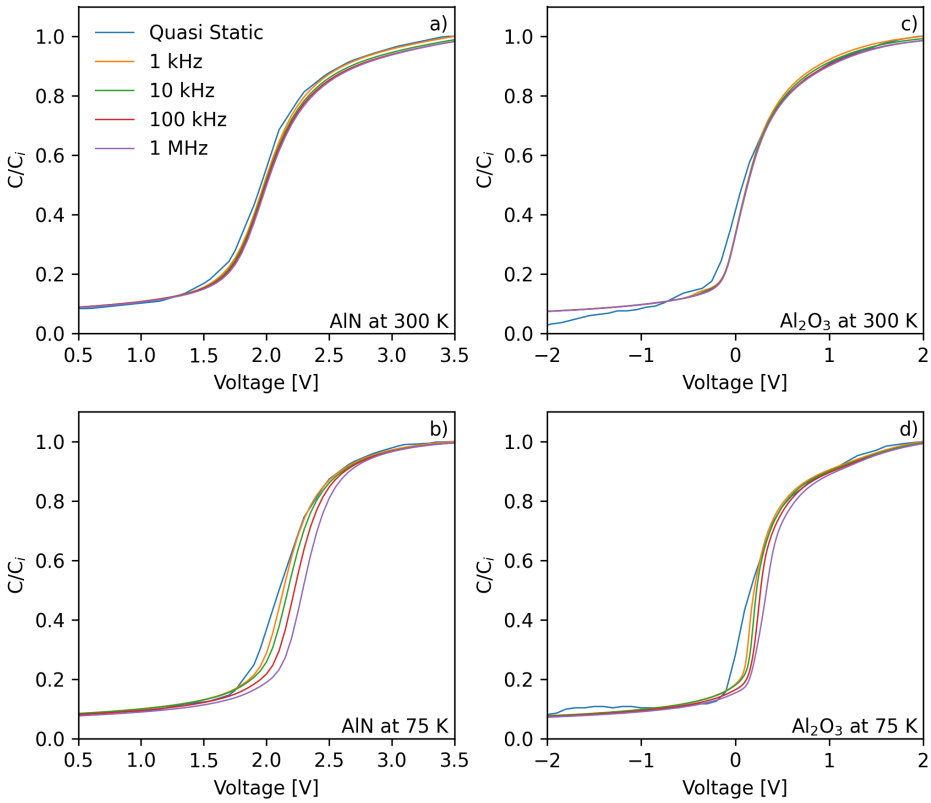

Fig. 2. Capacitance–voltage spectra of the AlN and Al_2O_3 samples at 75 K and 300 K using quasi-static and high frequencies between 1 kHz and 1 MHz.

Figure 3 shows the density of interface traps (D_{it}) extracted from capacitance–voltage measurements at 300, 200, 125, and 75 K using the high–low method together with the D_{it} of NO annealed dry oxide reference sample. The Al_2O_3 shows the highest D_{it} at 300 K while AlN has the lowest D_{it}. There is poor fit between the quasi-static and higher frequency measurements of the Al_2O_3 sample. This might result in an overestimate of the D_{it} for this sample. The D_{it} of the NO annealed sample at 300 K lands between the AlN and Al_2O_3. Cooling down to cryogenic temperatures allows for extraction of D_{it} of traps with energies closer to the SiC conduction band edge. At 75 K, the NO annealed oxide has the highest D_{it} while the AlN and Al_2O_3 have similar D_{it}. The NO annealed sample shows the highest increase in D_{it} from 300 K to 75 K but the trend of increasing D_{it} when approaching the SiC conduction band edge is clear for the Al_2O_3 and the AlN samples. The NI trap was initially thought to be a property of the SiO_2 dielectric and was modelled as a near-interface trap with energy level close to the SiC conduction band edge and located inside the SiO_2 [7]. Since the NI trap was observed in the AlN and Al_2O_3 samples, STEM and EELS was performed to search for SiO_2 layers or islands that might be the cause of the NI signal in the AlN and Al_2O_3 samples as displayed in Figs. 4 and 5. No SiO_2 was detected at the SiC/dielectric interfaces. The STEM and EELS studies hence suggest that thin SiO_2 layers or islands are not the source of the NI trap. EELS cannot detect any accumulation of chemical elements such as nitrogen and carbon at the interface so such elements cannot be excluded as the source of NI. However, it is concluded that the NI trap is most likely a property of the SiC surface and not the specific dielectric used to form the MIS-capacitor interface.

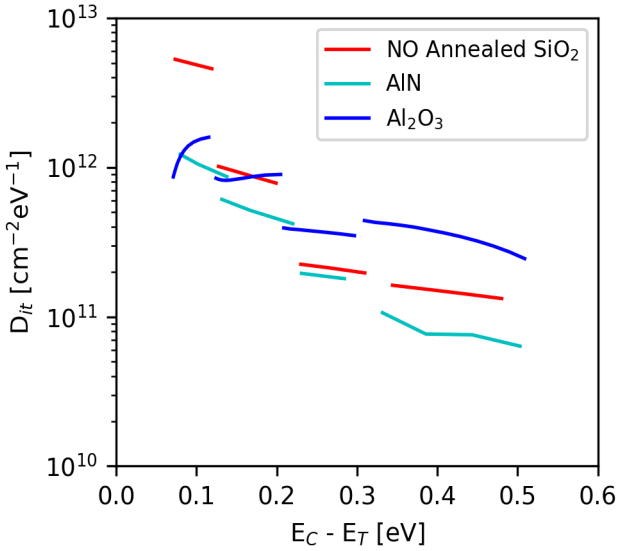

Fig. 3. Density of interface traps as a function of energy below the SiC conduction band edge, extracted from capacitance-voltage measurements at 300, 200, 125 and 75 K.

Summary

The NI traps have been suggested to be the main factor hampering channel carrier mobility in SiC-MOSFETs causing development of low voltage devices to be very difficult. It has been suggested that the NI traps are inherently a property of the SiO_2 gate oxide and their density is enhanced with post NO annealing. However, the observations of the NI traps in SiC/AlN and SiC/Al_2O_3 MIS capacitors, using capacitance-voltage and conductance spectroscopy, coupled with detailed chemical analysis of the interface using STEM and EELS analysis strongly suggests that the NI traps are not a property of the dielectric used to form the MISFET gate but are rather a property of the SiC surface.

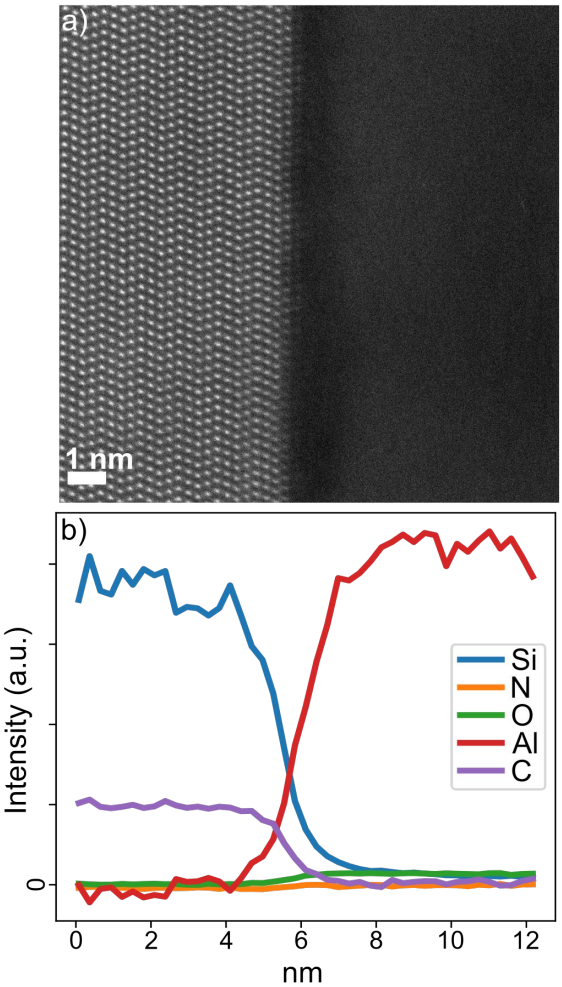

Fig. 4. a) STEM image of the SiC/Al_2O_3 interface, b) EELS plot showing the intensity of the Si, N, O, Al, and C signals.

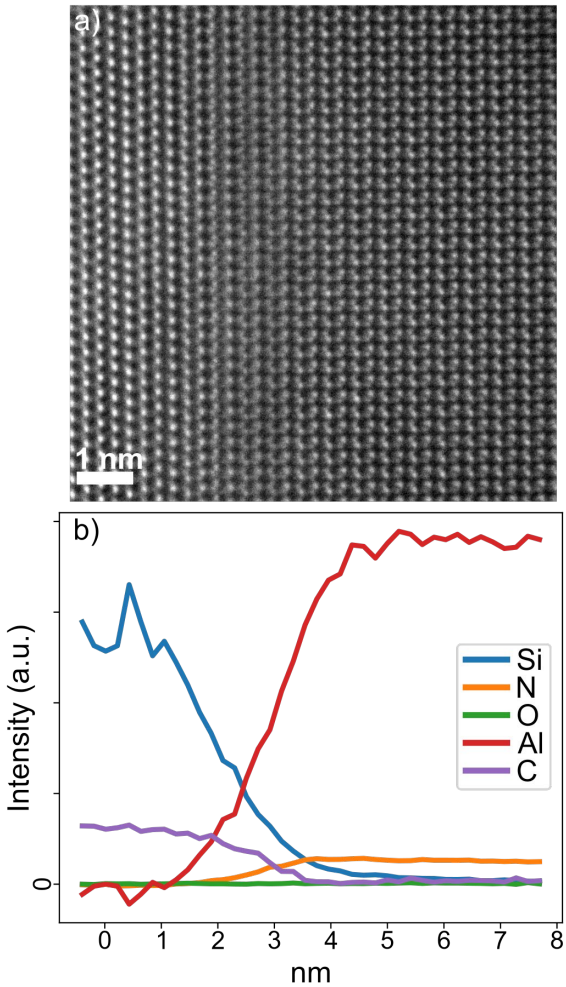

Fig. 5. a) STEM image of the SiC/AlN interface, b) EELS plot showing the intensity of the Si, N, O, Al, and C signals.

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