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Citation for the original published paper (version of record):
Kristensen, T., Nilsson, T., Divinyi, A. et al (2024). Dynamic Thermal Coupling in GaN MMIC Power Amplifiers. IEEE Transactions on Microwave Theory and Techniques, In Press. http://dx.doi.org/10.1109/TMTT.2024.3458189

Dynamic Thermal Coupling in GaN MMIC Power Amplifiers

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***Abstract*—The influence of dynamic thermal coupling on GaN MMIC power amplifiers is investigated through transient measurements, numerical simulations, and equivalent circuit modeling. The measured thermal coupling exhibits a low pass filtered response, where the magnitude and cut-off frequency decreases with increasing separation from the heat source. The coupling between two neighboring transistor channels shows a fractional order transient response and a pronounced temperature increase after ≈ 1 µs in the measurements. The coupling between transistors on the same MMIC is close to a first-order transient response and shows a pronounced temperature increase after 100 µs to 2.6 ms for the measured structure. It is shown that the thermal coupling causes the transistors in the power amplifier to operate at different temperatures, where the transient response of the PA exhibits five distinct time regions. An equivalent linear network is extracted to model the effect efficiently in a circuit simulator. Here, it is shown that the thermal coupling between neighboring transistors can change the thermal response of the PA considerably below 10 kHz. The outlined results give guidelines for predicting the dynamic self-heating in GaN PAs.**

***Index Terms*— Electro-thermal device modeling, Dispersive effects, Gallium nitride, Power amplifiers, Time-varying systems.**

I. Introduction

THE gallium nitride (GaN) high electron mobility transistor (HEMT) can reliably deliver high power and excellent high-frequency performance at elevated temperatures. This makes GaN HEMTs an attractive technology for compact power amplifiers (PA) in modern microwave frontends. Here, multiple gain stages, performance enhancement circuitry, and the receive chain can be realized in the same monolithically microwave integrated circuit (MMIC) as the PA. Such high levels of integration are attractive for size constraints, minimized loss, and high-frequency performance. However, adding more functionality into the constrained area of an MMIC complicates the thermal management of the circuit.

Thermal management is important for GaN PAs operating at high power levels as they can experience considerable self-heating that degrades the electrical performance and reliability of the PA [1], [2]. Self-heating is also a source of time-variance that influences the PA's dynamic behavior, where it can affect, e.g., its linearity [3]-[6]. High integration density complicates the system as the heat generated in a single device will influence the other devices integrated on the same MMIC. This thermal coupling will increase the temperature on the MMIC and can cause the devices in the PA to operate at different temperatures. The coupling is also a dynamic effect, where a device can modulate its neighboring devices [7]. The influence of thermal coupling on dynamic self-heating has been studied for single transistors [8]-[10]. However, there is less knowledge on the dynamic influence of thermal coupling between transistors integrated on the same MMIC. It is important to model the outlined effect of thermal coupling to predict a power amplifier's behavior and how the coupling will influence other components on the same MMIC. Further, it is vital to ensure reliable operating temperatures and optimize the MMIC layout, as demonstrated in [11]. Therefore, the impact of thermal coupling should be investigated to enable reliable, highly integrated GaN MMIC frontends with optimum performance.

The dynamic thermal coupling between transistors integrated on the same GaN MMIC PA was investigated in [7] based on transient measurements and Finite Element Method (FEM) simulations. This study provides a more detailed analysis of the results in [7] and provides an equivalent linear model to show how the thermal coupling between neighboring transistors changes the thermal response of a PA. The equivalent linear model is implemented in a circuit simulator for fast thermal simulations and can be used to predict how the thermal response impacts the PA for modulated signals. The outlined results provide valuable guidelines and tools for designers of GaN MMIC PAs.

II. Experimental Setup

The structure shown in Fig. 1 is used to replicate the heat generation in the output stage of a GaN power amplifier [7]. The structure consists of eight heaters designed as ungated HEMTs with eight 3 x 75 µm channels. The heaters are connected in four pairs, H_1-H_4, that can be biased independently, as shown in Fig. 1 (a). Ungated heaters are used

Manuscript received 4 June 2024; Revised 18 August 2024. This work, conducted within the Advanced Digitalization program at the WiTECH Centre's REMU project, has been financed by Vinnova, Chalmers University of Technology, Ericsson AB, Kongsberg AS, Saab AB, and United Monolithic Semiconductor. *(Corresponding author: Tobias Kristensen)*

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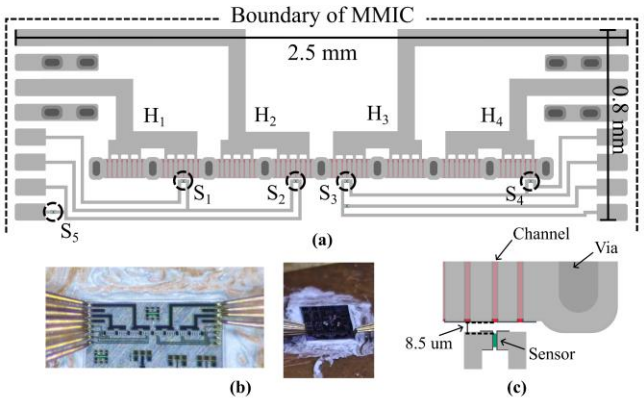

Fig. 1: (a) Test structure. (b) Images of measured MMIC. (c) Enlarged view of ungated transistor and sensor placement. Adapted from [7].

to get a uniform and controllable source of heat dissipation for a more certain characterization of the thermal coupling. This neglects how the heat flux and temperature in the channel change due to the vertical electric fields from the gate [12]. However, the mechanisms that determine the diffusive heat transport away from the channel are equal with or without the gate.

Five temperature sensors are integrated to monitor the temperature, using 2.5 x 10 µm semiconductor resistors [7], [13], [14]. The sensors S_1, S_2, S_3, and S_4 are placed with an 8.5 µm separation between the edge of the sensor channel and the closest transistor channel, as shown in Fig. 1 (c). This separation is comparable to the separation between the transistor channels. In this way, these sensors capture the coupling within a transistor cell. An additional sensor, S_5, is placed at the corner of the structure as a reference. The test structure is manufactured using Win Semiconductors NP15 GaN-on-SiC technology and placed on a copper carrier with Arctic MX-6 thermal paste to improve the thermal interface (Fig. 1 (b)).

The setup shown in Fig. 2 (b) is used for the measurements, where one sensor is measured at a time. The sensor is calibrated by measuring the IV characteristic of the sensor for steady-state temperatures between +40°C and +140°C set by a calibrated thermal chuck. A polynomial model is fitted to find the sensor temperature as a function of the sensor current at 0.75 V (Fig 2 (a)), assuming the sensor temperature equals the temperature of the thermal chuck [14]. The chosen operating point of 0.75 V is a compromise between sensor sensitivity and low electric fields to minimize self-heating and electron trapping in the sensor [13].

Transient measurements are performed by applying a voltage pulse to the ungated transistors with a rise time of approximately 100 ns. The pulse is on for 100 ms and repeated with a 1 s pulse repetition interval (PRI), as shown in Fig. 2 (c). The transient response of the sensor current is measured with an oscilloscope that is triggered at the same time as the voltage pulse. The oscilloscope is set to average over 64 acquisitions to reduce measurement noise. The polynomial model from the sensor calibration is used to extract the temperature transient from the measurement. The voltage and current applied to power the ungated transistors are measured to find the instantaneous dissipated power ($P_{diss} = I_H \cdot V_H$) to be used as stimuli in the simulations.

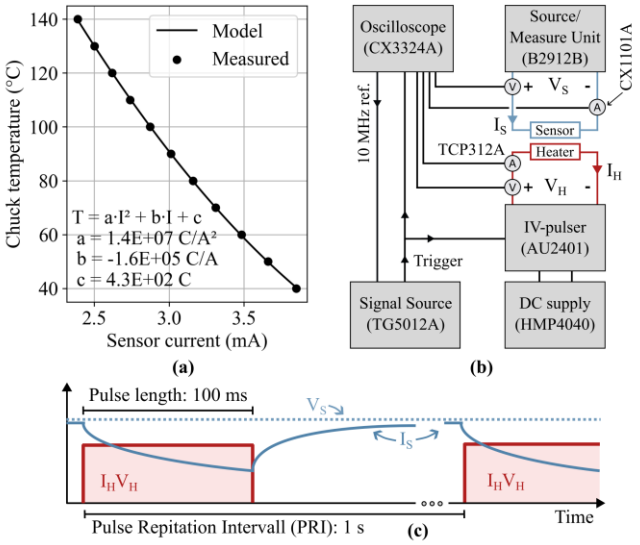

Fig. 2: (a) Example of chuck temperature versus measured sensor current at 0.75 V. (b) Measurement setup (c). Signal applied to the ungated transistors.

III. Numerical Model

The test structure in Fig. 1 is implemented in COMSOL Multiphysics 3D FEM solver to validate the measurements and as a basis for further analysis. The heat transport is modeled by solving Fourier's Heat Equation,

$$\rho(\boldsymbol{r})C_p(\boldsymbol{r},T)\frac{\delta T(\boldsymbol{r},t)}{\delta t} + \nabla\cdot(\kappa(\boldsymbol{r},T)\nabla T(\boldsymbol{r},t)) = Q(\boldsymbol{r},t) \quad (1)$$

where $\mathbf{r}$ = [x, y, z] is the position, T is temperature, ρ, C_p, and κ are material parameters, and Q is the heat generation. While Fourier's Heat Equation underestimates the initial heat-spreading around the gate in a transistor, it is shown to agree with more complex Monte-Carlo phonon analysis at the length scales concerning coupling effects (> 5 µm) [15].

The FEM model considers the conductive heat path from the transistor channel to the thermal chuck, as shown by the stack-up in Fig. 3. The heat transport upwards through the passivation layer and metallization is assumed to be neglectable compared with the high thermal conductivity in the SiC substrate. A single GaN layer is used to capture the heat

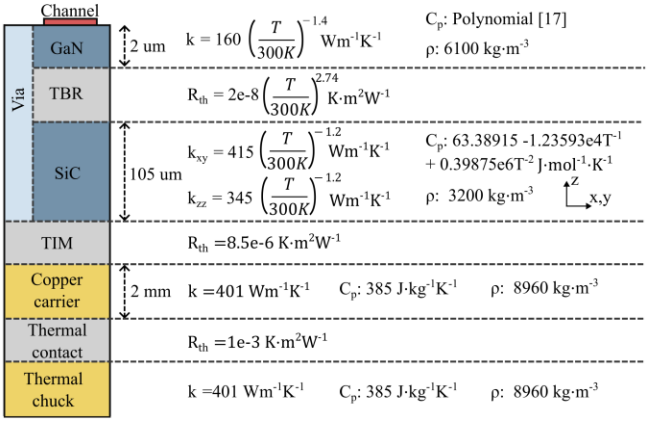

Fig. 3: Stack-up of test structure and material parameters used in the numerical model [16]-[20]. Figure not to scale. Adapted from [7].

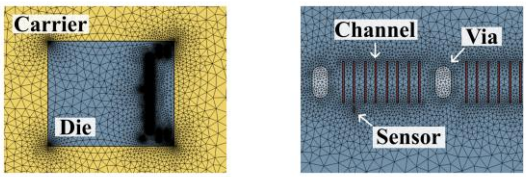

Fig. 4. Geometry of numerical model. Black lines show mesh.

spreading in the epitaxial layer. The thermal resistance due to the nucleation layer between the GaN layer and SiC substrate is modeled with a thermal barrier resistance (TBR) [16]. The density (ρ), specific heat capacity (C_p), and thermal conductivity (κ) are provided for each layer in Fig. 3 [16]-[20]. Temperature dependency is added for all semiconductor materials. Anisotropic heat spreading is considered for the SiC substrate by differencing the in-plane (κ_{xy}) and out-plane (κ_{zz}) thermal conductivity. The thickness and thermal contact resistances associated with the thermal interface material (TIM) between the MMIC and copper carrier are unknown. To overcome this, the TIM layer is implemented as a single thermal resistance fitted to the measured results to reduce the number of fitting parameters. The thermal contact resistance between the copper carrier and the thermal chuck is implemented in the same way.

The heat generation is modeled as a uniform heat source at the 2DEG of the channels in the ungated transistors. A linear interpolation of the measured P_{diss} is used to account for the slew rate and decreasing dissipated power due to self-heating in the measurement. A simplification is done by assuming that P_{diss} is equal for all transistors. The sensor temperature is extracted as the average temperature at the 2DEG of the sensor channel. The full size of the diced MMIC is considered in the model to ensure that the influence of the boundary conditions is captured. The thermal chuck is implemented as an ideal heat sink with T_A = 40°C. The effect of convection and radiation is neglected for remaining boundaries using an adiabatic boundary condition. There is uncertainty related to how well heat is transported through the via holes in the test structures, as it depends on how much of the via is filled by metal and on the interface between the substrate and the metal. As a simplification, it is assumed that heat transport through a via hole is low compared to the high thermal conductivity of the SiC substrate, and the via is implemented as a void to reduce the number of fitting parameters. The mesh in the FEM solver is refined until further refinements give no significant change in the result, and the used mesh is shown in Fig. 4.

IV. Experimental Results

This section presents an experimental characterization of the test structure in Fig. 1 to investigate the dynamic behavior of thermal coupling between transistors integrated on the same MMIC. The FEM model from section III. is calibrated based on these experiments.

A. Thermal Coupling Between Neighboring Transistors

The measurement in Fig. 5 shows the step response for the temperature increase in S_1-S_5 when a voltage pulse is applied to H_1. The measurement of S_1 suffers from an electrical ringing

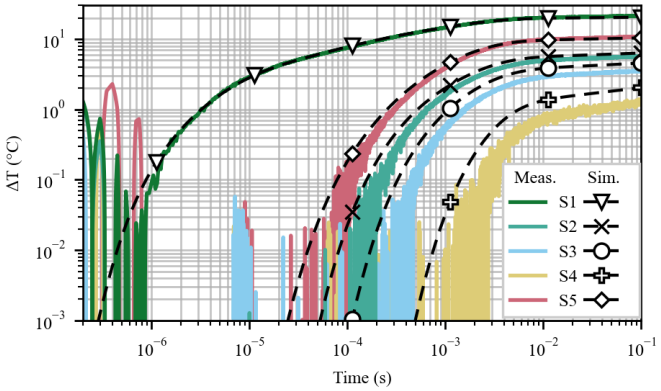

Fig. 5: Measured transient response when a voltage pulse is applied to the H_1 transistor pair. The simulated result is shown with black dashed lines. 2.3 W power dissipated at steady state. Data from [7].

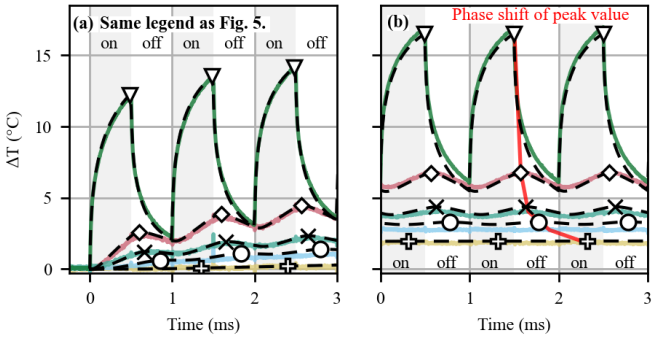

Fig. 6: Measured temperature increases when a voltage pulse is applied to the H_1 transistor with 500 µs pulse length and 1 ms PRI. (a) shows three first pulses and (b) shows response at steady state. The simulated result is shown with black dashed lines. Same legend as Fig. 5. Data from [7].

effect before 1 µs due to parasitic effects in the measurement setup. Besides this, the response of S_1 is comparable to the response added to a transistor channel from neighboring channels, and the response is consistent with previous investigations on the dynamic thermal coupling between channels [8]-[10]. The step response is a lowpass response of the applied pulse of dissipated power. Further, it follows a fractional order response, as expected from the Fourier Heat Equation close to the heat source.

As the separation from the heat source increases, does the solution of the Fourier heat equation go towards a first-order response. This is seen for the remaining sensors, S_2-S_5, that show how the heat generation in H_1 influences other transistors integrated on the MMIC. The amplitude of S_2-S_5 decreases with increasing separation from H_1. Further, the time needed for S_2-S_5 to reach the same ΔT increases with separation from H_1. For reference, is S_5 placed 250 µm from the closest channel in H_1, and it takes 103 µs for it to reach a ΔT = 0.1 °C. S_4 is placed on the opposite side of the MMIC than H_1 with a separation of 1330 µm, and it takes 2.6 ms for it to reach ΔT = 0.1 °C. This ratio is 220 µs : 389 µm for S_2 and 490 µs : 594 µm for S_3. The increase in time for S_2-S_5 to reach ΔT = 0.1°C follows a trend proportional to r^2/t as expected for a first-order response, where r is separation. S_1 deviates from this trend, with 1.1 µs : 8.5 µm, due to its fractional order response.

A voltage pulse with 1 ms PRI and 50% duty cycle is applied to H_1 to illustrate how the lowpass filtered response will look for a time-varying signal. S_1 placed next to H_1 increases

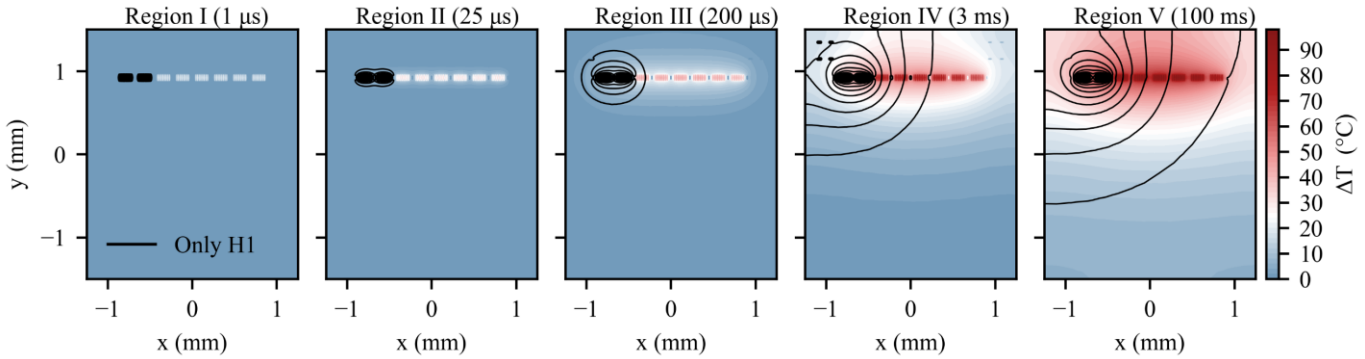

Fig. 7: Simulated temperature distribution in MMIC at surface of GaN layer for the end of region I, II, III IV and V. Heat map shows simulation with heat dissipated in all heaters. Black contour shows simulation with heat dissipated only in the H_1 transistor pair. The equidistance is 2°C.

quickly when the pulse is turned on in Fig. 6 (a). However, 500 µs is insufficient for the system to cool down to its initial steady state. Hence, the temperature increases for each pulse until a steady state is reached, as shown in Fig. 6 (b). The sensors S_2 and S_5 also capture the temperature increase within 500 µs when the pulse is on. The dynamic temperature change is low for S_3, as S_3 needs close to 500 µs to reach a notable temperature increase in Fig. 5. Further, S_4 is shown to need 2.6 ms to couple in Fig. 5. Consequently, only a slow, gradual temperature increase is measured on S_4 in Fig. 6. These results show that the dynamic thermal coupling can be minimized by increasing the separation between two heat sources, so the time needed for the propagating heat wave to reach a neighboring transistor is longer than the period of the time-varying input signal. However, the sensors still reach different temperatures at a steady state due to the thermal resistances in the MMIC and packaging. A second observation in Fig. 6 is that the diffusive heat spreading causes the phase shift between the dissipated power and the temperature increase to increase with separation from the heat source. The phase shift correlates well with the first-order response for S_2-S_5 observed in Fig. 5.

B. *Thermal Coupling in a Power Amplifier Stage*

A voltage pulse is applied to all the transistor pairs H_1-H_4 in Fig. 1 to replicate the heat dissipation in the output stage of a large power amplifier. The different responses seen in Fig. 8 for the sensors S_1-S_4 show that transistors in the amplifier will operate at different temperatures due to thermal coupling across the amplifier. The response can be divided into five distinct time regions that will be investigated in this section. For further analysis, the simulated surface temperature when driving all heaters on the MMIC is shown as a heat map in Fig. 7 for the end of each time region. The black contour lines in Fig. 7 show the surface temperature with only H_1 dissipating heat as a reference.

The self-heating is contained within the transistor channel in region I, and no pronounced temperature increase is seen in the FEM simulation in Fig. 8. The measurements are dominated by parasitic electrical effects in this range. The temperature in S_1-S_4 starts to increase in region II. S_1-S_4 exhibits the same gradual temperature increase, indicating that the coupling is contained within the transistor cell. This is consistent with the simulated surface temperature in Fig. 7, where the contour from H_1 starts to spread outside the transistor cell at the end of region II. S_4 starts to deviate from S_1-S_3 in region III. Fig. 7 shows that

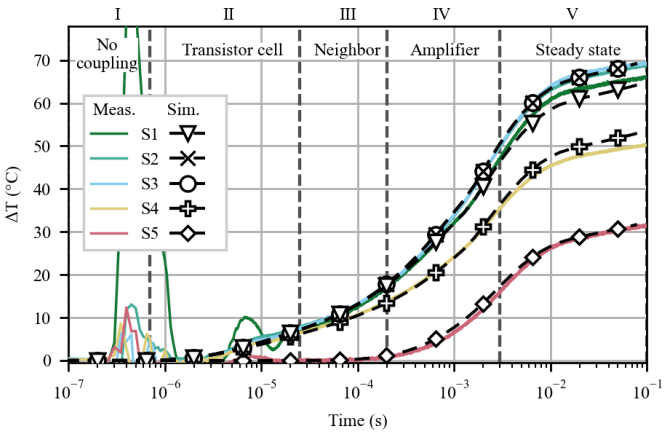

Fig. 8: Measured transient response with voltage pulse applied to all heaters (H1-H4). The simulated result is shown with black dashed lines. 15.2 W power dissipated at steady state. Data from [7].

this is the region where the heat generated in H_1 has diffused to transistors placed next to it. S_4 measures a lower temperature as it is placed next to a transistor with only one neighbor. In region IV, S_1 starts to deviate from S_2 and S_3. This shows that there is coupling over the whole PA, as seen by the temperature distribution in Fig. 7. This is consistent with S_5 increasing in region III and IV. It is observed in Fig. 7 that the heat generated in H_1 starts to interact with the boundary of the die in region IV. The time constant of this interaction fits well with the measurements in [21]. S_2 and S_3 reach the same temperature as they are placed symmetrically around the center of the PA. All the sensors exhibit a similar temperature increase as the temperature reaches a steady state in the last time region.

V. Implications for PA Operation

The result in section IV has shown the dynamics of the thermal coupling between transistors integrated in the same MMIC. This section proposes a model to capture how the thermal coupling impacts the thermal response of the power amplifier structure in Fig. 1 and discusses its implication for the operation of a PA.

A. *Equivalent Circuit Model*

The FEM simulation is shown to replicate thermal coupling well and can be used to find the thermal response for other operating conditions. However, FEM simulations are computationally demanding, especially in the comprehensive

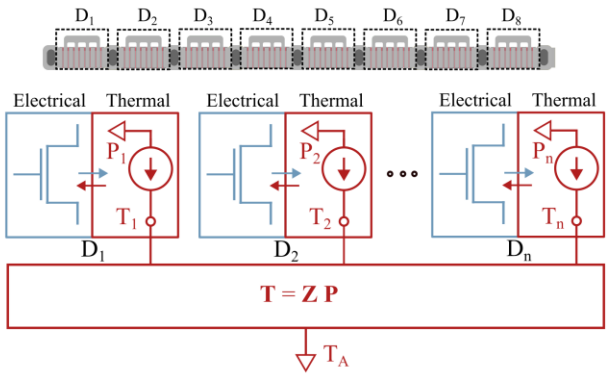

Fig. 9: Illustration of implementation of thermal network.

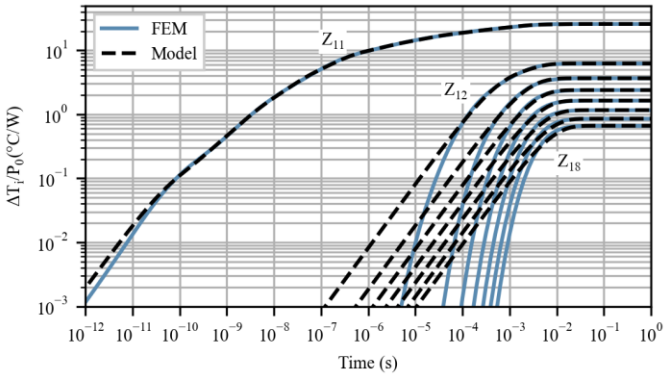

Fig. 10: Step response for P_j=u(t)·P_0 applied to D1.

form they are performed here. This makes the FEM simulation less suited for the thermal analysis of PAs when excited with complex modulated signals. To overcome this, an equivalent model is extracted from the FEM simulations to be used in a circuit simulator. A simple model is proposed to capture the effect of thermal coupling between neighboring transistors. Two simplifications are done in the model; First, the model will be extracted from the FEM simulations in section III to reuse the calibrated model. This model assumes an ungated device. The heat flux in a gated device would spread from a dominant hot spot next to the gate [12] and, therefore, have a different thermal impedance in the quasi-adiabatic region before 100 ns identified in [22]. However, the model with ungated devices should still give a good approximation for the effect of thermal coupling after 100 ns. Secondly, the thermal model will be approximated by a linear model. This assumption is only reasonable for small temperature changes due to the temperature-dependent material parameters in the MMIC. However, the linear model will be usable to capture how the thermal coupling changes the thermal response, and it could be expanded to a nonlinear model in future work.

The temperature, T(ω), in a transistor is modeled by a linear relationship between T(ω) and the instantaneously dissipated power, P(ω),

$$\mathrm{T}(\omega) = \mathrm{Z}(\omega)\mathrm{P}(\omega) + \mathrm{T_A} \tag{2}$$

where Z(ω) is the thermal impedance, and T_A is the ambient temperature. The linear model in (2) can be expanded to a thermal impedance matrix (**Z**) to capture the coupling between several nodes

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_i \end{bmatrix} = \begin{bmatrix} Z_{11}(\omega) & Z_{12}(\omega) & \cdots & Z_{1j}(\omega) \\ Z_{21}(\omega) & Z_{22}(\omega) & \cdots & Z_{2j}(\omega) \\ \vdots & \vdots & \ddots & \vdots \\ Z_{i1}(\omega) & Z_{i2}(\omega) & \cdots & Z_{ij}(\omega) \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_j \end{bmatrix} + T_A \tag{3}$$

where the diagonal terms (i = j) represent the self-heating in the transistors, and the remaining terms (i ≠ j) represent the thermal coupling between the transistors. The thermal impedance matrix in (3) is extracted for the eight heaters in Fig. 1 implemented in the FEM model. The thermal impedance network is designed to be combined with transistor models (denoted D1 to D8), as shown in Fig. 9. Here, P_n is the instantaneous heat dissipated in the transistor, and T_n is the average temperature when integrating over all channels in the transistor. The average temperature is used as it correlates well with the electrical performance of the HEMT.

Each term in the impedance matrix is found by applying dissipated power to each transistor (P_j) individually and extracting the corresponding temperature increase in all transistors ($\Delta T_i = T_i - T_A$) in the PA:

$$Z_{ij}(\omega) = \left.\frac{\Delta T_i(\omega)}{P_j(\omega)}\right|_{P_k=0\ for\ k\neq j} \tag{4}$$

In the following analysis is the dissipated power implemented as $P_j(t)= u(t)\cdot P_0$ for the model extraction, where u(t) is the Heaviside unit step function and P_0 = 1 mW is a scaling factor ensuring a linear temperature response. This would be $P_j(\omega)= P_0/j\omega$ in (4). Analytical solutions of Fourier Heat Equation show that the temperature increase for the Heaviside unit step can be represented by an infinite sum of weighted exponential terms [23]. Hence, the consequent temperature increase in a transistor in the FEM simulations can be modeled by

$$\Delta T_i(t) = Z_{ij}(t) * P_j \approx \sum_{n=0}^{N} R_n\left[1 - e^{-\frac{t}{\tau_n}}\right] \tag{5}$$

where $Z_{ij}(t) = \mathcal{F}^{-1}\{Z_{ij}(\omega)\}$ is the impulse response of the thermal impedance. One time constant per decade is used to get a good fit with the transient response [23], with N = 12 for the self-heating terms (i = j) and N = 2 for the thermal coupling terms (i ≠ j). R_n and τ_n are fitted to the FEM simulations using least squares regression. The model is in good agreement with the FEM simulations, as shown in Fig. 10, when power is dissipated in D1. However, the first-order approximation in (5) overestimates the slope for the coupling terms (i ≠ j) and demands a high number of time constants to fit the slope of the thermal response of $Z_{ij}(\omega)$ for i = j. It should be noted that fractal order models [4] or other behavioral models [5] could be considered for more flexibility in fitting this slope.

The frequency response of the thermal impedance is given as

	1	2	3	4	5	6	7	8
1	25.8	6.2	3.7	2.4	1.6	1.2	0.9	0.7
2	6.2	25.2	5.8	3.4	2.2	1.5	1.1	0.9
3	3.7	5.8	24.9	5.7	3.3	2.2	1.5	1.2
4	2.4	3.4	5.7	24.8	5.6	3.3	2.2	1.6
5	1.6	2.2	3.3	5.6	24.8	5.7	3.4	2.4
6	1.2	1.5	2.2	3.3	5.7	24.9	5.8	3.7
7	0.9	1.1	1.5	2.2	3.4	5.8	25.2	6.2
8	0.7	0.9	1.2	1.6	2.4	3.7	6.2	25.8

Fig. 11: Sum of thermal resistance, $\sum_n R_n$, for each term in the thermal impedance matrix.

the Fourier transform of the system's impulse response, which is the time derivative of (5). This gives

$$Z_{ij}(\omega) = \mathcal{F}\left\{\frac{\delta}{\delta t} Z_{ij}(t) * u(t)\right\} = \sum_{n=0}^{N=K} \frac{R_n}{(1 + j\omega\tau_n)} \qquad (6)$$

Hence, fitting the model in (5) to the FEM simulations can be used to find the parameters needed for the frequency response in the thermal impedance matrix. Fig. 11 shows the sum of thermal resistance, $\sum_n R_n$, for each term in the thermal impedance matrix. As expected from the experimental results, does $\sum_n R_n$ decay as the separation from the diagonal (i = j) increases. In the diagonal, does $\sum_n R_n$ vary depending on the proximity to the die boundary. Further, it can be observed that the matrix is symmetric around the diagonal and the center row due to the symmetry in the considered amplifier layout. This could be used to reduce the number of simulations needed in this case. The extracted impedance matrix is implemented in a nonlinear circuit simulator for further analysis (Keysight, ADS).

B. *Frequency Response*

The frequency response of the network is investigated by applying a sinusoidal stimulus to the transistor nodes of the thermal network. The magnitude and phase of the excitation signals are equal for all nodes. The real part of the thermal impedance ($\Re\{\Delta T_n/P_n\}$) is shown in Fig. 12 (a). Here, the real part of the thermal impedance is equal for all devices above 10 kHz. The response > 10 kHz overlaps with a simulation where the coupling terms ($i \neq j$) are set to zero in the impedance matrix. The thermal coupling significantly increases the thermal impedance below 10 kHz. Here, different responses are seen for the transistors in the amplifier, as expected from section IV.B.

The phase shift between the applied dissipated power and the temperature increase is shown in Fig. 12 (b). The addition of thermal coupling causes a local minimum around 0.1 to 1 kHz in the phase shift. Taking D_4 as an example, this minimum can be explained by looking at the sum of coupling responses affecting D_4, $\sum T_{c4}$, in Fig. 12 (b). The slope of the local phase minimum begins at the same frequency as $\angle \sum T_{c4}$ begins to transition. $\sum T_{c4}$ has a cut-off frequency of 151 Hz, found at $\angle \sum T_{c4} = -45°$. This corresponds well with the point where D_4

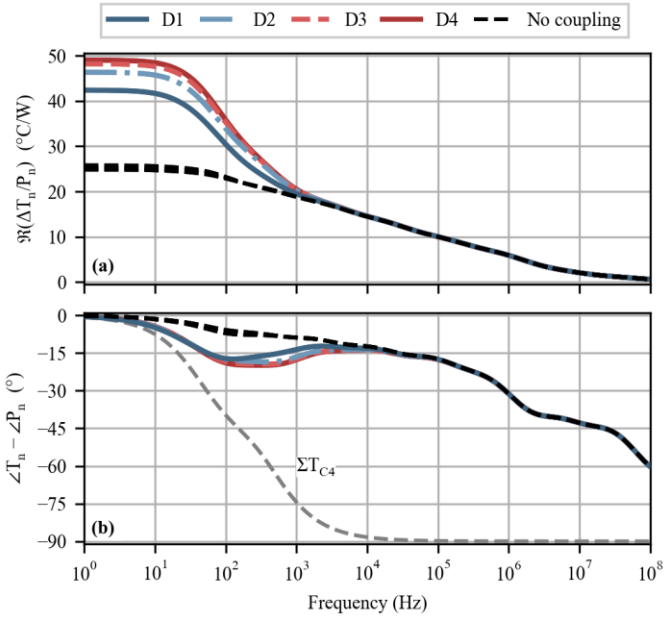

Fig. 12: AC simulation of thermal network with equal power dissipated in all devices in Fig. 9. (a) Real part of thermal impedance. (b) Phase shift between dissipated power and temperature increase. Black line shows simulation when coupling terms ($i \neq j$) is set zero in (3). Grey line in (b) shows sum of coupling terms impacting D_4.

transitions back to the phase response without thermal coupling. The phase response of D_4 follows the case where the coupling terms ($i \neq j$) are set to zero when $\sum T_{c4}$ go towards zero. Besides the phase minimum, does the phase shift vary slightly between devices due to the thermal coupling, where the center devices have a more distinct change than the edge devices.

The simulation without thermal coupling also differs between 1 Hz and 1 kHz due to the interaction with the boundary conditions observed in section IV.B. This is captured in the model as the thermal impedance is extracted for each transistor, considering its placement on the die. The proposed model captures the full spectrum of time constants in the dynamic self-heating, from the heat generation in the transistor to thermal coupling and interaction with the package of the MMIC. The addition of a gate should be considered for valuable predictions beyond 100 MHz.

C. *Implications for PA Operation*

The thermal coupling changes the dynamic thermal response between 1 Hz and 10 kHz for the technology and layout analyzed in this study. While this range is outside the RF frequency of most amplifiers, the low-frequency response of the thermal network could influence an amplifier's intermodulation distortion due to the electro-thermal feedback, as reported in [3]- [6]. In this case, the thermal coupling would influence the amplifier for frequency separations lower than 10 kHz. Beyond this, it will be important to account for the increased thermal impedance at DC and the different operational temperatures caused by the thermal coupling. From section IV.A, the magnitude and cut-off frequency of the coupling terms can be reduced by increasing the separation from the heat source. Hence, the layout could be optimized to reduce the thermal coupling. Further, the magnitude of the thermal response is

found to depend on the material stack in the FEM simulations. For instance, could a reduction of the thermal resistance in the TIM reduce the magnitude of the thermal coupling.

VI. Conclusion

This study has investigated the role of thermal coupling in the dynamic self-heating of GaN MMIC power amplifiers. The thermal coupling exhibits a low pass filtered response, where the magnitude and cut-off frequency decrease with increasing separation from the heat source. The results show that the dynamic coupling can be minimized by ensuring sufficient separation between the transistors. The thermal coupling causes the transistors in an amplifier to operate at different temperatures, where five distinct regions are identified in the transient response. It is demonstrated that a FEM model can replicate this result. The FEM simulations are suitable for investigating alternative layouts of MMIC PAs for optimum thermal management of the PA. The FEM model is used to extract a thermal impedance matrix that can be used in circuit simulators to model the thermal transient and capture the influence of thermal coupling for modulated signals. Here, it is shown that thermal coupling must be considered to predict the thermal response below 10 kHz. This can be a valuable tool for accurate prediction of the dynamic behavior of a PA and its influence on other components on the MMIC. This study has provided guidelines and tools for modeling the dynamic self-heating of GaN MMIC PAs. Future work should expand the model to consider gated transistors and a complete nonlinear thermal impedance matrix for increased accuracy.

Acknowledgment

The authors would like to express their gratitude to WIN Semiconductor corp. for providing access to their NP15 technology and manufacturing the test chips as a part of WIN's university multiproject wafer program.

References

[1] S. Nuttinck *et al.*, "Thermal analysis of AlGaN-GaN power HFETs," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 12, pp. 2445–2452, 2003, doi: 10.1109/TMTT.2003.819192.

[2] J. A. Del Alamo and E. S. Lee, "Stability and Reliability of Lateral GaN Power Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4578–4590, 2019, doi: 10.1109/TED.2019.2931718.

[3] S. David, W. Batty, A. J. Panks, R. G. Johnson, and C. M. Snowden, "Thermal transients in microwave active devices and their influence on intermodulation distortion," *IEEE MTT-S Int. Microw. Symp. Digest*, vol. 3, pp. 431–434, 2001, doi: 10.1109/mwsym.2001.966923.

[4] A. E. Parker and J. G. Rathmell, "Broad-band characterization of FET self-heating," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 7, pp. 2424–2429, 2005, doi: 10.1109/TMTT.2005.850399.

[5] V. Camarchia, F. Cappelluti, M. Pirola, S. D. Guerrieri, and G. Ghione, "Self-Consistent Electrothermal Modeling of Class A, AB, and B Power GaN HEMTs Under Modulated RF Excitation," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 9, pp. 1824–1831, 2007, doi: 10.1109/TMTT.2007.903839.

[6] J. H. K. Vuolevi, T. Rahkonen, and J. P. A. Manninen, "Measurement technique for characterizing memory effects in RF power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 8, pp. 1383–1389, 2001, doi: 10.1109/22.939917.

[7] T. Kristensen, T. M. J. Nilsson, A. Divinyi, J. Bremer, and M. Thorsell, "Characterization and Modeling of Dynamic Thermal Coupling in GaN MMIC Power Amplifiers," in *2024 IEEE/MTT-S Int. Microw. Symp. - IMS 2024*, Washington, DC, 2024.

[8] A. Manoi *et al.*, "Time-dependent thermal crosstalk in multifinger AlGaN/GaN HEMTs and implications on their electrical performance," *Solid State Electron*, vol. 57, no. 1, pp. 14–18, 2011, doi: 10.1016/j.sse.2010.11.002.

[9] A. Cutivet *et al.*, "Scalable Modeling of Transient Self-Heating of GaN High-Electron-Mobility Transistors Based on Experimental Measurements," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2139–2145, 2019, doi: 10.1109/TED.2019.2906943.

[10] B. K. Schwitter, A. E. Parker, S. J. Mahon, and M. C. Heimlich, "Characterisation of GaAs pHEMT Transient Thermal Response," *EuMIC 2018 - 2018 13th Eur. Microw. Integrated Circuits Conf.*, pp. 218–221, 2018, doi: 10.23919/EuMIC.2018.8539961.

[11] H. Park, H. Nam, K. Choi, J. Kim, and Y. Kwon, "A 6-18-GHz GaN Reactively Matched Distributed Power Amplifier Using Simplified Bias Network and Reduced Thermal Coupling," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 6, pp. 2638–2648, 2018, doi: 10.1109/TMTT.2018.2817521.

[12] S. Rajasingam *et al.*, "Micro-Raman temperature measurements for electric field assessment in active AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 456–458, 2004, doi: 10.1109/LED.2004.830267.

[13] J. Bremer *et al.*, "Analysis of Lateral Thermal Coupling for GaN MMIC Technologies," *IEEE Trans. Microw. Theory Tech.*., vol. 66, no. 10, pp. 4430–4438, 2018, doi: 10.1109/TMTT.2018.2848932.

[14] A. Divinyi *et al.*, "On-Chip Sensors for Temperature Monitoring of Packaged GaN MMICs," *IEEE Trans. Compon. Packaging Manuf. Technol.*, vol. PP, p. 1, 2024, doi: 10.1109/TCPMT.2024.3387736.

[15] Y. Shen, X. S. Chen, Y. C. Hua, H. L. Li, L. Wei, and B. Y. Cao, "Bias Dependence of Non-Fourier Heat Spreading in GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 409–417, 2023, doi: 10.1109/TED.2022.3227894.

[16] A. Sarua *et al.*, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3152–3158, 2007, doi: 10.1109/TED.2007.908874.

[17] S. Lee, S. Y. Kwon, and H. J. Ham, "Specific heat capacity of gallium nitride," *Jpn J Appl Phys*, vol. 50, no. 11 PART 2, pp. 8–11, 2011, doi: 10.1143/JJAP.50.11RG02.

[18] Q. Zheng, C. Li, A. Rai, J. H. Leach, D. A. Broido, and D. G. Cahill, "Thermal conductivity of GaN, GaN 71, and SiC from 150 K to 850 K," *Phys. Rev. Mater.*, vol. 3, no. 1, pp. 1–14, 2019, doi: 10.1103/PhysRevMaterials.3.014601.

[19] F. Cardarelli, *Materials Handbook : A Concise Desktop Reference.*, 3rd ed. 20. Springer International Publishing, 2018.

[20] L. Hitova, R. Yakimova, E. P. Trifonova, A. Lenchev, and E. Janzen, "Heat Capacity of 4H-SiC Determined by Differential Scanning Calorimetry," *J Electrochem Soc*, vol. 147, no. 9, p. 3546, 2000, doi: 10.1149/1.1393935.

[21] T. Kristensen, A. Divinyi, J. Bremer, T. M. J. Nilsson, and M. Thorsell, "Thermal Transient Measurements of GaN HEMT Structures by Electrical Measurements," *Proc. of the 18th Europ. Microw. Integrated Circuits Conf.*, pp. 293–296, 2023, doi: 10.23919/eumic58042.2023.10288814.

[22] G. J. Riedel *et al.*, "Nanosecond timescale thermal dynamics of AlGaN/GaN electronic devices," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 416–418, 2008, doi: 10.1109/LED.2008.919779.

[23] K. R. Bagnall and E. N. Wang, "Theory of Thermal Time Constants in GaN High-Electron-Mobility Transistors," *IEEE Trans. Compon. Packaging Manuf. Technol.*, vol. 8, no. 4, pp. 606–620, Apr. 2018, doi: 10.1109/TCPMT.2017.2773065.