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A Ku-Band GaN MMIC Push-Pull Power Amplifier with Coupled-Line Balun and Capacitive Neutralization for 6G Applications

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***Abstract*— This paper demonstrates a $11.0 - 17.5$ GHz GaN on SiC MMIC push-pull power amplifier (PA) for emerging 6G FR3 centimeter-wave (cmWave) applications, featuring an innovative input balun for impedance matching, an output balun to counteract transistor parasitics for enhanced bandwidth and compactness, and cross-coupled neutralization networks with interdigitated and metal-insulator-metal (MIM) capacitors to boost stability and gain. To validate the proposed design, a prototype GaN MMIC push-pull PA was fabricated. Experimental results exhibit a peak power added efficiency (PAE) of $18\% - 34\%$ with an output power of $34.0 - 36.5$ dBm within the design frequencies.**

***Keywords*— Balun, coupler, GaN, interdigitated capacitors, MMIC, push-pull, power amplifier, neutralization, wideband.**

I. Introduction

In the advancement towards the sixth generation (6G) mobile wireless communications, the FR3 centimeter-wave (cmWave) frequency band ($7 - 24$ GHz) is crucial for its balanced transmission capacity and coverage area. Spectra within the FR3 band, such as $10.7 - 13.25$ GHz and $14 - 15.35$ GHz, are identified by the International Mobile Telecommunications (IMT) consortium as vital for future developments [1]. This evolution, accompanied by the transition from single-antenna configurations to active antenna array systems, increases transmitter design complexities, necessitating wideband, efficient, and compact power amplifiers (PA). Moreover, PAs intended for handsets, access points, and base stations are expected to deliver power within $30 - 35$ dBm [2], aligning with the anticipated increase in cell size in 6G arrays. In this context, gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) PAs stand out for their high power density, efficiency, and wide bandwidth.

The GaN MMIC push-pull PA architecture is widely adopted for its wideband and highly efficient performance. The conventional GaN push-pull PA, as shown in Fig 1(a), employs input and output baluns with a characteristic impedance of 50 Ω, and additional input (IMN) and output (OMN) matching networks to match between the balun and transistors' optimal source and load impedance. However, from a system design point of view, it is highly desired that baluns from push-pull PA have impedance matching [3], [4] and device parasitic compensating [5], [6], [7] functionality to reduce the overall circuit size and loss. Furthermore, the push-pull PA is particularly suitable for broadband operations by enabling cross-coupled capacitor neutralization, which naturally leads to enhanced stability, gain, and reverse isolation over a broad bandwidth [8]. This technique is, however, rarely employed in compound semiconductors compared to silicon-integrated circuits, with a notable exception being the first GaN MMIC push-pull neutralized PA for improved linearity [9].

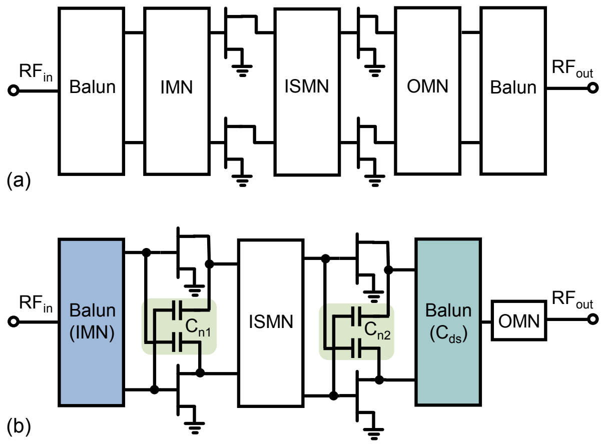

Fig. 1. GaN MMIC push-pull PAs with (a) conventional topology, and (b) proposed topology employing distributed balun and cross-coupled capacitors.

This paper demonstrates the theory and design approach of a $11.0 - 17.5$ GHz GaN MMIC push-pull PA, featuring a novel input balun with impedance matching capability and an output balun with transistor parasitic compensation, as shown in Fig 1(b). Furthermore, cross-coupled interdigitated and metal-insulator-metal (MIM) capacitors are employed for neutralization networks. Fabricated in a 150 nm GaN on SiC process, this PA is tailored for potential 6G FR3 cmWave applications. The subsequent sections present the proposed push-pull PA's theory, design, and characterization.

II. Theory and Design

A. Coupled-Line Baluns

In this section, we explore the use of coupled-line-based baluns for GaN MMIC push-pull PAs. To analyze the three-port baluns, it is possible to add an extra fourth port to form symmetrical four-port networks, which can be decomposed into even- and odd-mode circuits for analysis. It is worth noting that a balun can be formed if the four-port

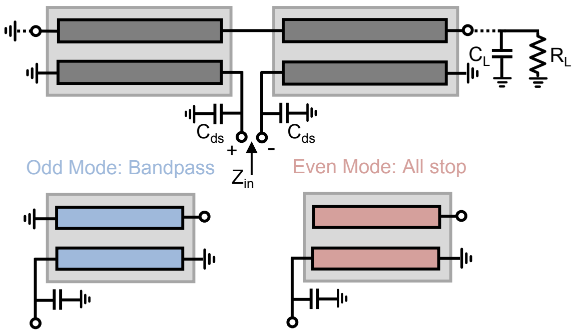

Fig. 2. (a) The output coupled-line balun and (b) its equivalent even- and odd-mode circuits, used for the GaN MMIC push-pull PA.

symmetrical network behaves as a transmission-stop network in the even-mode excitation and as a transmission-pass network in the odd-mode excitation [4].

1) Output Baluns

The output of a GaN transistor can be modeled as an optimum resistive load in parallel with the parasitic capacitor C_{ds} [10]. It is therefore crucial for the output balun to properly compensate C_{ds} while presenting low insertion loss. The modified Marchand-type balun, initially proposed in [6], stands out as an excellent candidate and has been successfully implemented for silicon differential PAs with broadside coupled lines [7]. We employed the same balun structure with coupled microstrip lines for the output of GaN MMIC push-pull PAs, as illustrated in Fig 2, which avoids area-consuming and lossy OMNs between the transistor output and baluns. The input admittance seen from the transistor current source plane can be derived as [7]

$$Y_{\text{in}} = \frac{\frac{1}{2}Y_m^2 \csc^2\theta}{1/R_L + j\omega C_{\text{L}} - jY_p \cot 2\theta} + j\omega C_{\text{ds}} - jY_p \cot\theta \quad (1)$$

Equating Y_{in} to the PA optimal admittance results in the following solutions

$$\begin{cases} Y_{0o} = Y_p + Y_m \\ Y_{0e} = Y_p - Y_m \end{cases} \quad (2)$$

where

$$Y_p = \omega \left(C_{\text{ds}} - \frac{C_L R_L}{R_{\text{opt}}} \right) \left(\cot\theta - \frac{R_L \cot 2\theta}{R_{\text{opt}}} \right)^{-1} \quad (3)$$

$$Y_m = \sin\theta \sqrt{\frac{2R_L}{R_{\text{opt}}} \left(\frac{1}{R_L^2} + \left(Y_p \cot 2\theta - \omega C_L \right)^2 \right)}. \quad (4)$$

The solutions for the coupled-line parameters Y_{0o} and Y_{0e} can therefore be determined in terms of transistor parameters R_{opt} and C_{ds}, which are derived from load-pull simulations. The variables, R_L, C_L, and θ remain as the primary design variables that offer flexibility during the design process. In practical design procedures, an idea current source with a shunt C_{ds} is utilized. This setup enables plotting the impedance seen at the current source plane across a range of design

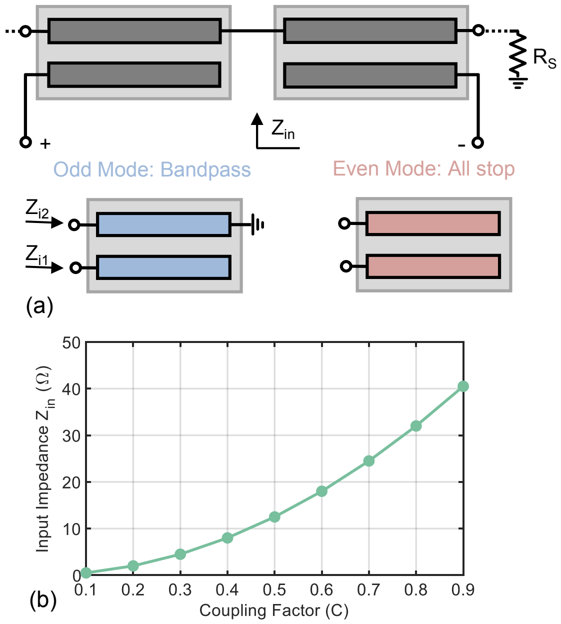

Fig. 3. (a) The input coupled-line balun, and its equivalent even- and odd-mode circuits used for the GaN MMIC push-pull PA. (b) The input impedance versus the balun coupling factor when $R_S = 50\ \Omega$.

frequencies, while iteratively adjusting the values of C_L, R_L, and θ to optimize the design outcomes.

2) Input Baluns

We employed the balun structure proposed in [4], [11] for the input of our design. As shown in Fig. 3(a), the input impedance at two ports of the coupled-line structures, when operating in the odd mode, can be expressed as [12]

$$Z_{i1} = \frac{\sqrt{Z_{0e}Z_{0o}}\sqrt{\left(Z_{0e} - Z_{0o}\right)^2 - \left(Z_{0e} + Z_{0o}\right)^2 \cos\theta^2}}{\left(Z_{0e} + Z_{0o}\right)\sin\theta} \quad (5)$$

$$Z_{i2} = \frac{Z_{0e}Z_{0o}}{Z_{i1}}. \quad (6)$$

Based on equations (5) and (6), it is evident that the input balun we employed inherently possesses the impedance-matching capability, as further illustrated in Fig. 3. This feature is particularly beneficial as it allows us to omit the need for additional PA IMNs, thereby saving costly MMIC areas and further reducing loss.

B. Cross-Coupled Neutralization Capacitors

It is crucial to emphasize that the capacitive neutralization network plays a significant role in enhancing PA stability and gain performance. This is primarily due to the substantial contribution of the transistor's gate-to-drain capacitance (C_{gd}) to the deterioration of reverse isolation. The stability factor for the small signal equivalent circuit of push-pull PAs, incorporating capacitive neutralization as shown in Fig. 4(a) can be expressed as [13]

$$K = \frac{2 + \omega^2 \left(C_{gd} - C_n\right)^2 R_g R_d}{\omega |C_{gd} - C_n| R_g R_d \sqrt{\omega^2 \left(C_{gd} - C_n\right)^2 + g_m^2}}. \quad (7)$$

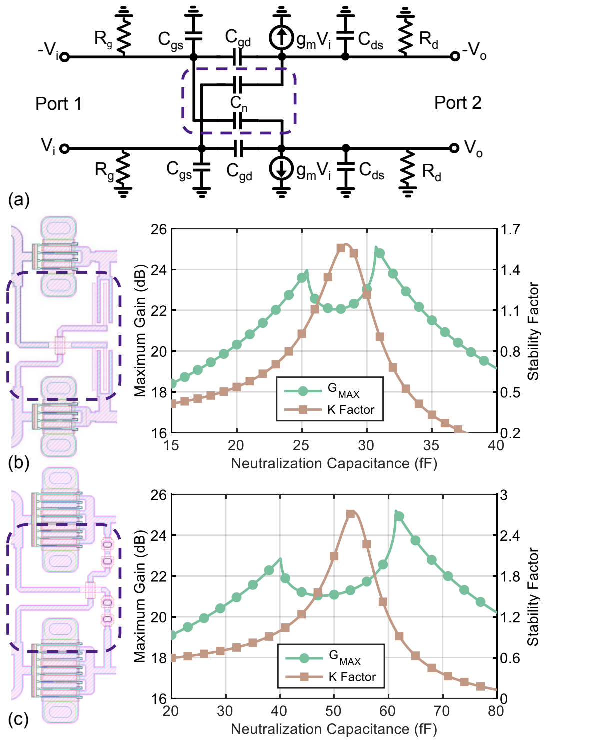

Fig. 4. (a) Small signal equivalent circuit of idea push-pull PA with capacitive neutralization network. Simulated stability factor and maximum available gain of (b) 4×80 μm and (c) 8×100 μm GaN transistors.

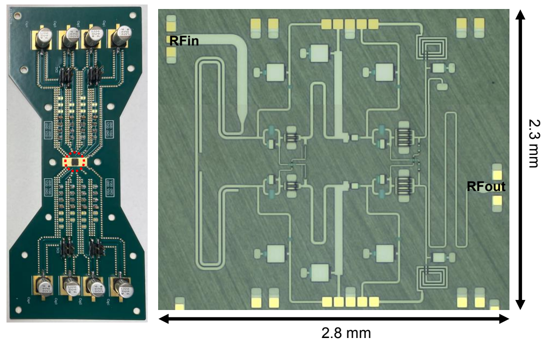

Fig. 5. (a) The test PCB board and (b) chip photograph of the fabricated prototype (Total chip area: 2.8 mm $\times$ 2.3 mm including DC and RF pads).

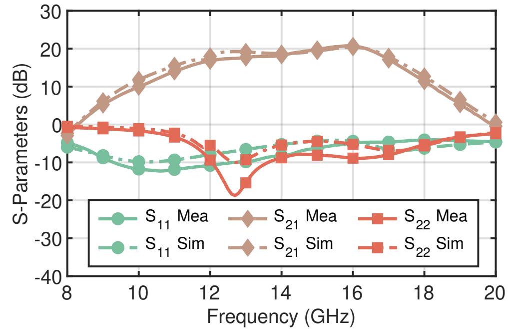

Fig. 6. Measured (solid line) and simulated (dashed line) small-signal results of the fabricated prototype Doherty PA circuit.

Hence, when $C_n = C_{gd}$, the stability factor reaches its maximum value, indicating an optimal state for stability within the PA. We conducted a sweep of the neutralization capacitance for both the driver stage (4×80 μm) and power stage (8×100 μm) GaN transistors. As expected, Fig. 4(b) and (c) demonstrate that both stability and gain improve when the appropriate neutralization capacitance is selected. We, therefore, chose a neutralization capacitance of 28 fF and 54 fF for the driver stage and power stage amplifiers, respectively. Due to the GaN MMIC process's limitations on directly implementing small capacitance values, interdigitated capacitors were employed in the driver stage amplifiers for enhanced accuracy and stability [14]. For the power stage, two series MIM capacitors were used to meet the required capacitance within the constrained space.

III. Prototype Circuit

The proposed push-pull PA is fabricated using a 150 nm GaN on SiC MMIC process by WIN Semiconductors (NP15-00) and adopts a two-stage design. Aimed at achieving a peak output power over 34 dBm, the design includes the use of 8×100 μm devices for the power stage and 4×80 μm devices for the driver stages. These amplifiers operate in Class-AB mode, with a 20V drain supply voltage. The stability of the circuit is a paramount concern, addressed through extensive simulations that incorporate Winslow Stability (WS) probes at every gate and drain terminal. To thoroughly evaluate the PA's stability, a combination of loop gain and driving point admittance methods was applied. In addition to neutralization networks, parallel RC networks were placed at the gate terminals of both driver and power stages to counter potential instabilities effectively [15].

IV. Measurement Results

A photograph of the fabricated push-pull PA prototype is shown in Fig. 5, which occupies a compact chip area of 2.8 mm $\times$ 2.3 mm including the DC and RF pads. This chip was subsequently installed on a custom-designed printed circuit board (PCB), where the PA's DC pads were connected to decoupling capacitors via wire bonds. The small signal performance was assessed using a vector network analyzer, with the calibration reference plane extended to the GSG pads. For the large signal tests, a signal generator and driver amplifier was utilized to generate sufficient static signals, and the output power was measured with a power meter. In Fig. 6, the measured small-signal results of the prototype are presented and compared with simulated data. This comparison reveals a close match between the measured and simulated outcomes, noting only slight discrepancies at the edge frequencies. Fig. 7 illustrates the prototype's measured power added efficiency (PAE) versus its output power at 13 GHz and 16 GHz, demonstrating a smooth compression behavior without any signs of parametric oscillations. Both static measured and simulated results regarding peak power and PAE across design frequencies are presented in Fig. 8. Here, a peak output power of $34.0 - 36.5$ dBm was recorded across the

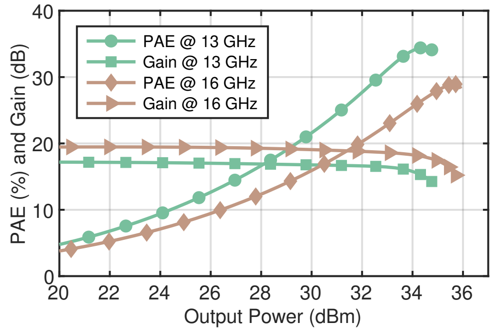

Fig. 7. Measured PAE and gain of the prototype versus output power.

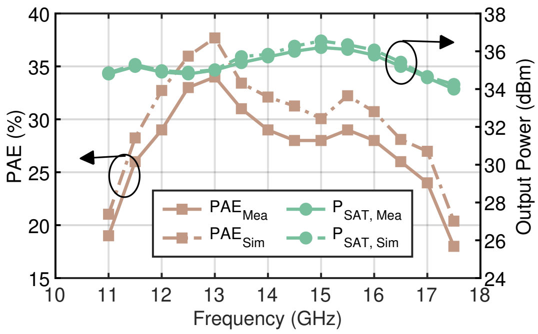

Fig. 8. Measured and simulated saturated power at P5dB (5-dB saturation) and peak PAE at P3dB (3-dB saturation) of the prototype versus frequency.

entire frequency band of $11.0 - 17.5$ GHz. Meanwhile, the measured peak PAE was between 18% and 34%, showcasing an excellent concordance between the measured and simulated large-signal performances. The performance of the fabricated PA is subsequently evaluated and benchmarked against the state-of-the-art MMIC PAs in Table I. This comparison shows that our prototype delivers competitive PAE across a broad frequency range and maintains a compact size.

V. Conclusion

This work explores the theory and practical design aspects of a compact $11.0 - 17.5$ GHz GaN MMIC push-pull PA, employing an input balun for effective impedance matching and an output balun for compensating transistor parasitics. Furthermore, it integrates cross-coupled interdigitated and MIM capacitors to enhance stability and gain. Demonstrating the feasibility of this approach, we present a two-stage, GaN on SiC, capacitive neutralized push-pull PA, achieving an output power range of $34 - 36.5$ dBm and a peak PAE of $18\% - 34\%$ across 11–17.5 GHz. The design demonstrates significant promise for application in future 6G cmWave applications.

Acknowledgment

This work has been carried out in the WiTECH center. We acknowledge WIN Semiconductors for chip fabrication.

Table 1. Summary of Efficient and Wideband MMIC PAs.

Ref.	Frequency (GHz)	L_{Gate} (μm)	PAE (%)	Chip Area (mm^2)	P_{SAT} (dBm)
[16]	17.0 – 20.0	0.25	8 – 32	15.8	36.0 – 40.0
[17]	16.3 – 20.3	0.10	23 – 31	30.0	36.6 – 37.7
[18]	6.0 – 12.0	0.15	16 – 30	10.4	32.5 – 37.2
[19]	10.0 – 14.0	0.15	28 – 38	10.6	34.0 – 35.8
T.W.	**11.0 – 17.5**	**0.15**	**18 – 34**	**6.4**	**34.0 – 36.2**

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