THESIS FOR THE DEGREE OF LICENTIATE OF ENGINEERING

Characterisation of Dynamic Effects in Compact GaN Microwave Front Ends

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Göteborg, Sweden, 2024

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Abstract

GaN HEMT technology exhibits dynamic behaviour due to thermal and electrical memory effects, which reduce the performance of GaN MMICs used in compact microwave front ends. Addressing these challenges requires careful characterisation under realistic operating conditions to identify, mitigate, or compensate for these effects. This thesis investigates the thermal and electrical effects in two main ways.

The characterisation of thermal effects focuses on accurately monitoring on-chip hotspots caused by high-power operations. The surrounding thermal environment, including packaging and thermal management components, complicates this task. The proposed solution involves the use of on-chip sensors integrated into both dedicated test structures and actual circuits, enabling real-time, package-independent, and electrical measurements for thermal characterisation of device operation.

The trapping-induced effects risk unpredictable performance degradation, especially in GaN HEMT switch devices, where drift conditions are not yet fully characterised. The second part of this thesis aims to develop a method for determining the impact of trapping on the recovery time of GaN HEMT switches used in front-end applications. This method quantifies the effects of recovery, allowing for comparing different devices and technologies.

Keywords: GaN MMIC, Thermal, Transient, HEMT, Dynamic effects, Trapping

List of Publications

Appended Publications

This thesis is based on work contained in the following papers:

[A] **A. Divinyi**, T.M.J. Nilsson, N. Rorsman, T. Kristensen, H. Hultin, S.E. Gunnarsson and M. Thorsell, "On-Chip Sensors for Temperature Monitoring of Packaged GaN MMICs", *IEEE Transaction on Components Packaging and Manufacturing Technology*, 2024

[B] **A. Divinyi**, N. Rorsman, N. Billström and M. Thorsell, "Transition Time of GaN HEMT Switches and its Dependence on Device Geometry", *IEEE European Microwave Integrated Circuits Conference,* Sept. 2023

[C] **A. Divinyi**, N. Rorsman, N. Billström and M. Thorsell, "Short Term Drift in the Recovery Time of GaN HEMT Switches", *IEEE European Microwave Integrated Circuits Conference*, Sept. 2024

Other Publications

The content of the following publications partially overlaps with the appended papers or is out of the scope of this thesis

[a] T. Kristensen, **A. Divinyi**, J. Bremer, Torbjörn M.J Nilsson, M. Thorsell, "Thermal Transient Measurements of GaN HEMT Structures by Electrical Measurements", *IEEE European Microwave Integrated Circuits Conference, 2023*

[b] T. Kristensen, T.M.J. Nilsson, **A. Divinyi**, J. Bremer, M. Thorsell, "Characterization and Modeling of Dynamic Thermal Coupling in GaN MMIC Power Amplifiers", 2024 *IEEE/MTT-S International Microwave Symposium – IMS 2024*, Washington DC, USA, 2024

[c] T. Kristensen, T.M.J. Nilsson, **A. Divinyi**, J. Bremer, M. Thorsell, "Dynamic Thermal Coupling in GaN MMIC Power Amplifiers", Accepted 2024 T-MTT

[d] T. Kristensen, T.M.J. Nilsson, **A. Divinyi**, J. Bremer, M. Thorsell, "Numerical Modeling of Dynamic Thermal Coupling in GaN HEMTs Calibrated by Transient Measurements", T-ED

Contents

Chapter 1

Introduction

Radar technology is vital in an insecure world where its role in defence systems for object detection is pivotal [1]. There has been a clear trend towards the adoption of digital technology in radar systems, in part replacing highly specialised analogue components with more versatile off-the-shelf solutions such as Field Programmable Gate Arrays (FPGAs) and CPUs for signal processing [1]. This added processing power offers advantages, such as increased versatility in designing microwave systems. This has led to further developing microwave systems such as active electronically scanned arrays (AESA), which relies on multiple compact microwave front ends or transmitter and receiver modules (TRMs). These have been enabled using solid state components (SSD) such as gallium nitride (GaN) high electron mobility transistors (HEMTs) due to their ability to provide high output powers at microwave frequencies.

GaN HEMT is a commercially available technology but remains a vibrant research area with numerous challenges and possible improvements. Firstly, with demonstrated power densities in GaN HEMT devices up to 24.4 W/mm [2] at X-band has been accomplished with additional effort dedicated to further increasing the breakdown voltage [3]. Secondly, through scaling the size of the device dimensions, such as the gate length reaching 40 nm [4] and even 20 nm [5], thus improving the cut-off frequency $f_{T,}$ which has enabled GaN HEMTs to be operated at frequencies up to 200 GHz [3]. Furthermore, as part of a continuous desire to reduce size and weight, as seen in the integration of GaN HEMTs with new or existing technologies, either through heterogeneous integration [3], [6] or the development of GaN on Si [7], [8].

However, increasing the level of integration and power density causes challenges with thermal effects and trapping contributing to dynamic behaviour, which degrade device performance [9] and reliability [10]. Similarly, a well-known challenge with GaN technology is the presence of time-dependent memory effects caused by electron trapping. This causes the device to be partly dependent on previous bias and operating conditions [11]. The fundamental principles of memory effects are well understood in terms of, e.g., trapping where electron states in the semiconductor are charged and discharged. However, the current transistor models do not always capture the gradual time-dependent behaviour associated with both trapping and thermal effects, which constitutes a considerable challenge [12]. This has been

demonstrated to degrade both amplifier operation [5] and switch operation [13], [14] which all contribute to decreasing system performance.

These are, therefore, significant challenges in the context of multifunctional GaN microwave front ends. Consequently, it is essential to have methods for characterising dynamic effects caused by thermal and trapping in GaN HEMTs. Chapter 3 discusses on-chip sensors compatible with packaged devices for temperature monitoring and thermal characterisation of GaN HEMTs during operation. This is approached by using sensors based on GaN resistor, which can be readily integrated into MMIC circuits, and which is compatible with most processes. The sensors concept is demonstrated using a thermal test structure which reflects the use of the sensor by dissipating power thus causing an increase in temperature captured using the sensor. Furthermore, the impact of trapping on device performance is investigated in Chapter 4, focusing on GaN HEMT switch devices intended for front-end operation, a topic often neglected in favour of the more common amplifier-relevant use cases. Investigating the impact of device geometry and technology choices for the switch time degradation caused by recovery. By characterising these effects could help designer decreasing the sensitivity to dynamic effects as well as to better predict the behaviour of compact GaN MMIC transceivers.

Chapter 2

GaN in Radar Systems

Increasing the level of integration using GaN poses some challenges with dynamic effects but has considerable advantages. Depending on the specific application and platform limitations, numerous considerations are required for implementing the microwave front end. For example, size, weight and power (SWaP) requirements pose exceptionally high demands for compact designs. These demands have been met by replacing older magnetron and travelling wave tubes (TWT) with SSDs, which are significantly smaller and lightweight [1]. The reduced size has been one enabling factor for the success of AESA, systems which rely on multiple TRMs. Using multiple TRMs, signal processing allows for electrical beam steering by introducing different phase delays φ in the systems. Instead of physically aiming the antenna in the direction to transmit and receive signals from, in an AESA. The TRMs can be configured to achieve this through clever use of additive and negative interference from the different elements, the combined signal that is radiated, i.e. the sum of all the radiated energy from the antenna [1], will act as an antenna directed in a particular direction (Figure 1).

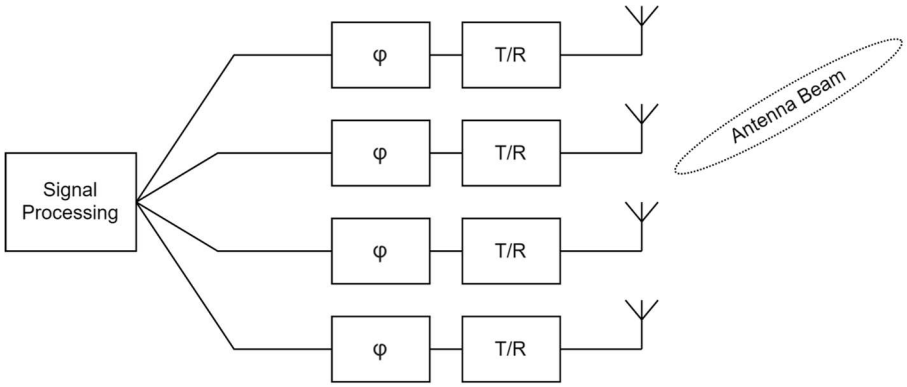


Figure 1 Illustration of AESA, different elements each containing an antenna, transmit/receive module and phase shifter function. Resulting signals are summed and processed.

Additional advantages of this include increased resilience to system breakdown. Previously, if just one transmitter breaks, the whole system goes down. Instead, with tens to thousands of TRMs, it is possible to achieve a graceful degradation, with each broken TRM having a limited impact on system performance. This decreases the urgency of system repair and ensures that some functionality remains instead of a critical failure occurring. Previously, AESAs relied on analogue equipment to introduce the necessary phase delays. Still, with the increasing performance and capabilities of FPGAs, it is possible to digitise the different channels, which enables a greater degree of freedom in both design and operation. Thus, opening up for new high-performance radar systems with the potential of realising new exciting applications with even smaller form factors while simultaneously making use of the increased processing power using technologies such as artificial intelligence (AI) and machine learning (ML).

Modern microwave systems (Figure 2) can, therefore, be described as consisting of a digital core, including the digital signal processor (DSP), which processes sensor data. Starting from a digital waveform, the radar signal can be converted to and from an analogue signal using a digital-to-analogue converter (DAC) and analogue-to-digital converter (ADC) [1]. Currently, it is still necessary for the signal to require up conversion from an intermediate frequency (IF) to the desired microwave frequency using an up converter and a down conversation back to be processed by the digital core. However, the frequency at which DACs/ADCs operate steadily increases, and devices operating for lower GHz signals are readily available.

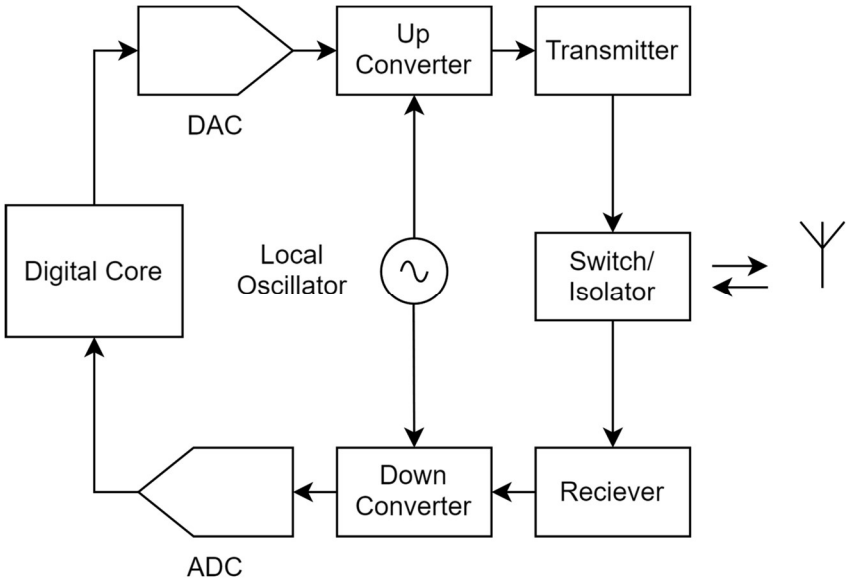


Figure 2 Example Microwave System containing parts necessary to go from digital to analog signals and to both transmit and receive these.

Similarly, one system critical component is the front end, which enables the transmission and reception of microwave signals and typically includes two amplifiers. Firstly, the High-Power Amplifier (HPA) for amplifying the signal for transmission, especially important in radar applications is to maximise the available output power in order to increase range and increasing the signal to noise ratio (SNR). Secondly a Low-Noise Amplifier (LNA) to amplify and maintain the integrity of the received signal by minimising the noise in order to extract useful information. These two functions are frequently consolidated into a single TRM that uses one antenna, with a switch or circulator to select between sending and receiving modes, as illustrated in Figure 3.

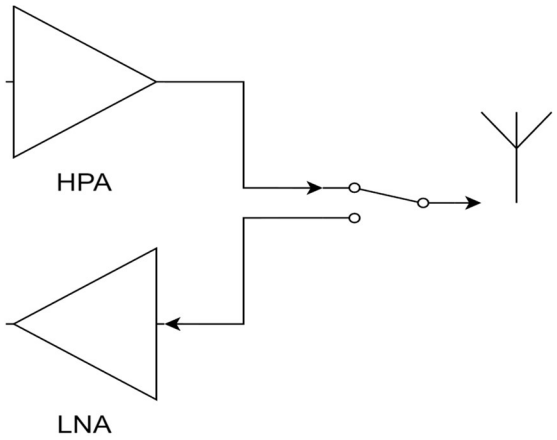


Figure 3. An example transceiver consists of LNA, HPA and a switch before the antenna to select between the two for outgoing or incoming signals.

2.1 Monolithic Microwave Integrated Circuits (MMICs)

Therefore, the choice of technology is critical to fulfilling all the requirements from performance to size. GaN HEMT technology is currently the primary alternative for high-power applications at microwave frequencies. The key technical advantage of using SSD for compact and lightweight transceiver design is realised through a monolithic microwave integrated circuit (MMIC) with the components manufactured directly from a substrate using photolithography [15]. Thus, MMIC enables a designer to realise entire circuits and functions on a single chip, such as a GaN transceiver. However, the design of a GaN MMIC transceiver requires appropriate MMIC processes with high overall performance. The viability of this approach was demonstrated with Saab and Raytheon winning the Aviation Week Laureate Innovation Award in 2015 for their work with GaN in a defence setting and pioneering the use of the technology in products [16] and emerged from a series of works demonstrating a process aimed at transceiver functionality [17]. The demonstration of individual building blocks [17] and the subsequent demonstration

of a GaN MMIC front end has since further demonstrated the validity of the concept [18], [19].

Further advancements in GaN MMIC have improved performance [20] and the state-of-the-art GaN on SiC MMIC chipsets for transceiver design for military applications, including scaled-down devices and increased power densities [21]. GaN transceivers have been implemented for a wide array of applications such as 5G [25], synthetic aperture radar (SAR) [26] and use for satellites [22]. Other trends includes, for example, the DARPA DREaM program investigating novel epitaxial structures [23].

A limitation that needs consideration is the design of the LNA and front-end switch in GaN MMIC technology. For example, the noise figure in GaN LNAs has historically been considerably higher than alternatives such as gallium arsenide (GaAs) [24]. However, the use of GaN in LNAs also presents some attractive advantages, such as utilising the material's robustness, which allows the LNA to survive higher input powers and maintain linearity at comparably higher input powers [25]. This is highly relevant since the receiver can be subject to unintentional and intentional jamming. Previously, this was only possible by including protective circuitry such as limiters, which is commonplace to protect technologies that are more sensitive than GaN but at the cost complexity and, in some instances, also size.

2.2 Integration of GaN MMIC

Since, size is an essential consideration as miniaturisation is in demand, and continuous efforts are being made to increase the integration of components, including the GaN microwave front end. One approach to this is GaN-on-Si MMIC processes that could provide the potential for further integration with Si technology at the cost of thermal performance, e.g., at the risk of decreasing output power [26]. A similar level of integration could also be achieved through the heterogeneous integration of GaN and Si for example attaching two different wafers to each other [27].

Circuits utilising both Si and GaN transistors have yet to be widely adopted. This could be partly due to difficulties achieving high performance using this approach and the added complexity of additional manufacturing steps. An alternative to this could be improvements and advancements in technologies similar to or further developments of multi-chip modules (MCM) or chiplets, which are compact multichip packages consisting of an interposer or similar to host the different chips with the potential of including GaN [6] [28].

Furthermore, as GaN HEMT transceivers are increasingly adopted in more sophisticated applications, the need to properly characterise individual aspects of the GaN front end from the impact of epitaxial structure, device processing, circuit design and packaging increases. Part of this is the careful characterisation of the dynamic effects in a relevant context for GaN transceiver operation to fully capture the different use cases.

Chapter 3

Thermal Characterisation of GaN MMIC

Self-heating is present in all microwave devices to a certain extent and is an inherent consequence that efficiency can never reach 100%. Consequently, some energy is inevitably converted to heat. Despite being able to withstand higher temperatures than the alternatives, thermal effects are still a concern for GaN HEMT devices [9], [10]. Even though GaN HEMTs comprise only a fraction of the MMIC chip surface, they comprise most of the dissipated power (Figure 4). In the HEMTs, most of the heat is generated right next to the gate on the drain side, where the electric field becomes strong in a common source configuration [29]. These localised heat sources pose challenges for characterisation and risk reducing long-term reliability [9], [10].

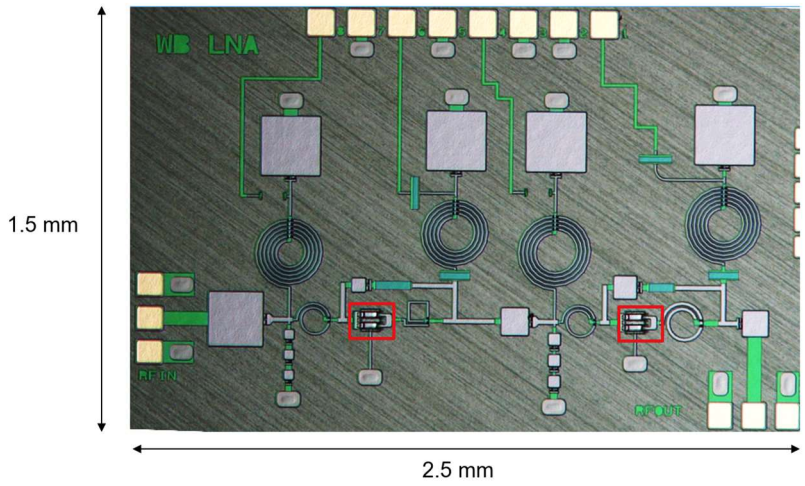


Figure 4. Example of a GaN MMIC, HEMTs marked in red.

Conduction is the dominant process of heat transfer closest to the active device, with heat spreading laterally and vertically into the rest of the epitaxial structure and the surrounding package. The device performance is correlated with temperature, the

amount of power dissipated during operation, and the capacity of the surrounding chip and packaging to transfer the heat away from the device are essential [30]. Additionally, thermal behaviour is an essential input for the device model since it considerably impacts device performance and contributes to memory effects. It is, therefore, imperative to gain insight into the impact of device operating conditions on temperature and evaluate the effectiveness of thermal management [30]. To account for the temperature of e.g., a pulsed HPA requires a method that capture the dynamic behaviour which is non-trivial but essential to predict performance. This chapter explores the challenges and solutions associated determining device temperature, focusing on GaN MMIC.

3.1 Temperature in Packaged GaN MMIC

Packaging of microelectronics protects chip physically and also acts as the thermal environment. It is also especially important to consider for high power semiconductors such as GaN since an estimated 30% of the temperature increase during operation can be attributed to packaging [31]. This is essential since thermal management and packaging are usually application-specific. It is therefore of interest to evaluate circuit performance and be able to monitor temperature in a relevant setting such as the specified packaging environment, one possible packaging could be copper coin/heatsink, such as in Figure 5.

Figure 5. GaN chip mounted on copper carrier using a silver epoxy TIM [Paper A]

The temperature is especially problematic for highly integrated systems since high-power components such as the power amplifier are close to the temperature-sensitive low-noise amplifier, making proper thermal environment evaluation crucial. Further complicating the temperature estimation by limiting direct access to the device e.g., be fully encapsulated using polymers or equivalent (Figure 6). This, combined with the desire to limit the size and weight, restricts available cooling solutions and results in a thermal environment caused by the chip and its surrounding environment, increasing the risk of overheating.

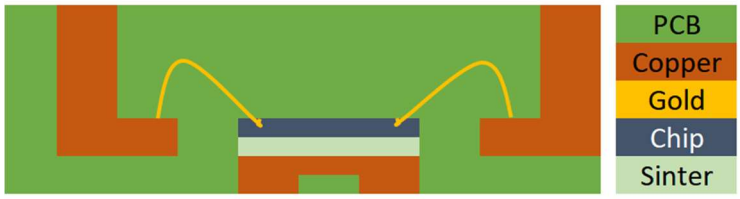


Figure 6. Chip encapsulated in PCB [Paper A] with gold bond wires connecting the chip to PCB.

3.2 Temperature Measurements

One way to address the risk of overheating is to purposefully operate the device at lower power to decrease the temperature but at the cost of reduced performance. This is not ideal, since it might introduce unnecessary reduction in performance instead it would be more beneficial to monitor the chip temperature and make decisions from information about temperature. There are several approaches to temperature measurements, which all have their advantages and disadvantages depending on the use case. The temperature should ideally be accurately predicted to the degree necessary for the intended application to avoid unacceptable degradation in performance and reliability.

3.2.1 Optical Measurement Techniques

Different properties of light can be used to determine temperature, such as registering infrared radiation, which is a common method of determining temperature using an IR camera [32]. These measurements require a certain amount of a priori information about the devices for increased accuracy since they cannot be assumed to be perfect blackbodies. A material-dependent coefficient is required to compensate for this [33]. The technique can map surface temperature but with lesser spatial resolution than other optical methods [32]. In part due to the size of the wavelength of around 3 µm, which is a considerable dimension in GaN HEMTs with gate lengths for many commercial processes in the range of 0.1 µm to 0.25 µm.

An alternative is to study the temperature-dependent optical properties of the materials used. In thermal reflectance imaging, the change in reflected light from a surface characterises the temperature. In Raman spectroscopy, the changes in scattered incident light by the crystal structure of a semiconductor material are sufficient to determine the temperature [33]. The advantages of using optical methods are that they enable good spatial resolution, which makes them helpful in characterising local hotspots. The disadvantage is that they require dedicated, complex, and expensive equipment that requires optical access to the device, so the possibility of using these methods for packaged devices is reduced. For example, devices packaged similarly to Figure 6 would be ill-suited for these methods.

3.2.2 Electrical Sensors

Another approach is to measure temperature-dependent electrical properties of the GaN HEMT itself, which could be an attractive option since it has several metrics that vary with temperature, e.g., properties of the gate diode or gain [32]. However, when integrated into a circuit, this is not always practical since, for example, the difficulties of correlating gain and temperature in a multi-stage amplifier. Similarly, using the drain current or R_{on} can be used to monitor temperature, state, but the dynamic behaviour will be filtered through the device bias network and therefore more suitable for steady state temperature measurements.

Instead, dedicated sensors consisting as diodes or resistors could be used to monitor temperature since these can be biased independently. One key advantage of using electrical sensors is that they do not require physical access to the device which makes them interesting for packaged circuits. Generally, there are several parameters to consider when implementing a temperature sensor, such as availability, size and sensitivity. Ideally, the sensor should be as sensitive as possible to temperature changes, enabling a relevant measurement resolution. It should also dissipate as little power as possible to minimise sensor self-heating and the impact of temperature chip temperature. Another metric usually used to describe a sensor is how linear this response is concerning temperature, as this could be useful to simplify characterisation and, in some instances, use the sensor response to compensate for thermal effects.

The diode-based temperature sensor monitors the shift in threshold voltage by having well-defined voltage and current measurements. In the context of GaN MMIC, Schottky barrier diodes (SBD) have primarily been used since they are commonly available components in most processes. The use of diodes for measuring temperature has been previously explored and demonstrated [34], [35]. Other possible implementations of diodes have been demonstrated mainly in experimental MMIC processes, which indicate high performance and appear very suitable for temperature sensing [36]. Another approach is GaN mesa resistors, where the 2DEG's mobility significantly varies with temperature, with the potential use as temperature sensors previously investigated [37] and are widely available. Depending on application the sensor size could also be of significance since a large sensor placed at a distance from the active regions registers more of an average chip temperature compared to a small one.

The benefit of this is that it is possible to place the sensors considerably closer to the active areas. A comparison in Table 1, illustrates that the metrics vary between sensor implementations but remain comparable overall.

Table 1 Sensor Characteristics

Sensor	Sensitivity /K	Linearity	Size μm²	Ref
Circuit	0.35 mV	0.993	250x200	[38]
Circuit	31.28 mV	0.995	-	[39]
Integrated Resistor	0.36 Ω	0.9997	Small	[40]
Integrated Resistor	10 Ω	-	Small	[41]
Resistor	0.4 Ω	-	-	[42]
PIN Diode	19.7 mV	0.938	50 diameter	[36]
SBD Diode	1.61 mV	-	20x100	[34]
SBD Diode	2.54 mV	0.992	90 diameter	[35]
GaN Resistor	2.17 mV Or 3.3 Ω	0.9785	10x4	[Paper A]

Still, the main advantage of the approach is that resistor require few manufacturing steps and are readily available in all processes. The sensor size is also an advantage with an active sensor area of 40 μm^2, magnitudes smaller than most other proposed sensors. This is limited to how small different MMIC processes can reliably manufacture resistors. The small sensor size, therefore, not only reduces the required chip area but also to a larger extent resembles a point like measurement of the chip compared to other sensors [37]. The small form factor of this sensor also enables a higher degree of flexibility.

3.2.3 Thermal Test Structures

The validity of GaN resistor-based temperature sensors is demonstrated in [Paper A] using a thermal test structure. The idea with a thermal test structure is relatively straightforward: an active part that dissipates heat and another active part that registers the change in temperature using a temperature sensor. Thermal test structures have previously been demonstrated [43] an iteration of a previously suggested thermal test structure is included in [Paper A]. With even closer distance to the active heater, as seen in Figure 7. The sensor has been integrated as if it were the middle finger in a nine-finger GaN HEMT. Furthermore, the structure also includes additional sensors, such as a top sensor that can be seen at a distance of 200 μm away from the active area.

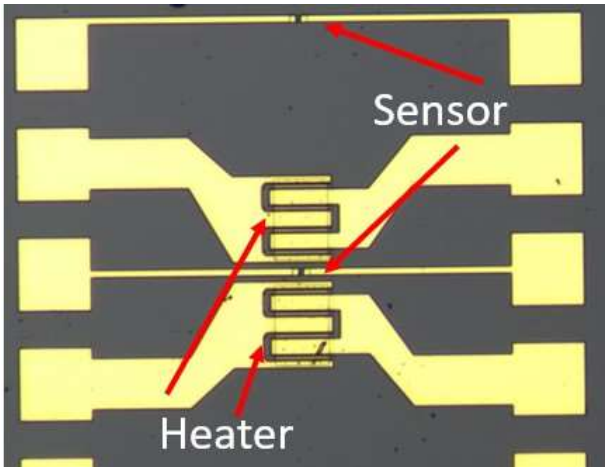


Figure 7. Thermal test structure, including a heater consisting of two parts as well as two sensors. One sensor embedded into the heater and one place further away.

The idea of using two sensors is to correlate the temperature recorded using both the sensors in the middle of the device and with the temperature sensor further away. The results for a test structure mounted on copper (Figure 8) can be seen in Figure 9, for different power dissipations using both the middle and top sensors. The sensor temperature is captured during 200 ms with a complementary measurement after 1 s from the applied voltage step. Firstly, what can be noticed is that the two sensors differ in both recorded temperatures and characteristics. The top sensor registers, as expected, a low pass filtered dynamic temperature compared to the middle sensor, which is further explored in [Paper A].

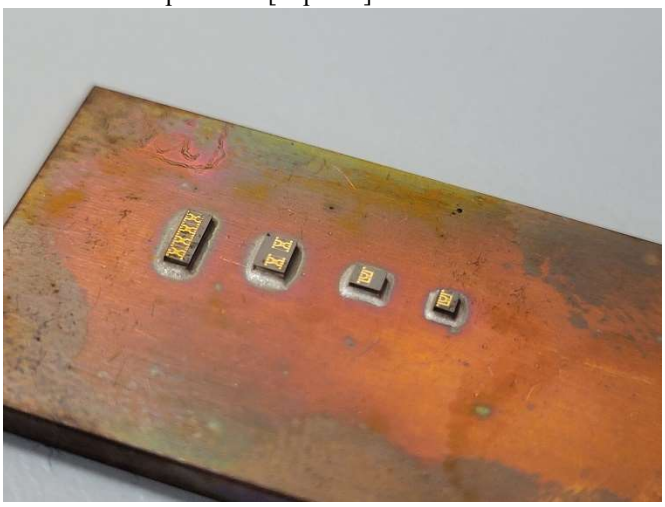


Figure 8. Differently sized thermal test structures mounted on a copper carrier using silver epoxy.

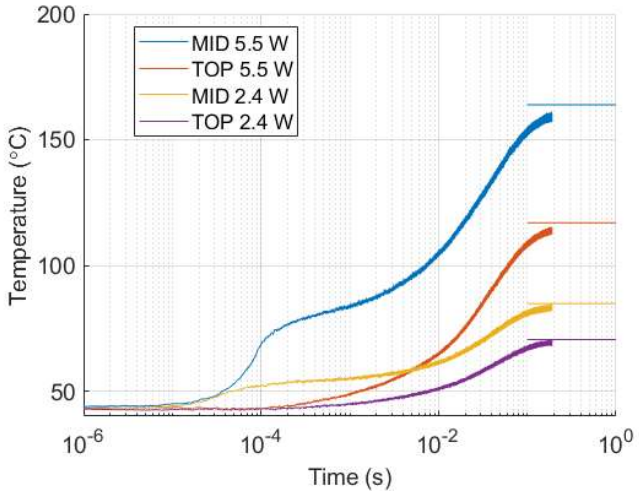


Figure 9. Dynamic temperature response registered at the top and middle sensor in test structure during different power dissipations.

3.3 Thermal Modeling

The proposed test structure and measurement method [37], [44], [45], [46], [47] used in [Paper A] has enabled the thorough characterisation of the thermal coupling between transistors in HPA and can be used as input for formulating models. It can also be used to predict the gradual temperature increase during continuous pulsed operation corresponding to realistic PA operation. [43]. There are different approaches to modelling the effects of self-heating in GaN HEMT devices

One approach which is highly suitable for compact device modelling is to use an electro-thermal RC network [48]. While consistent with the physical behaviour, this allows for a more empirical approach to modelling self-heating effects, which do not require detailed knowledge of the epitaxial structure. This also enables the temperature to be modelled using circuit design tools such as ADS. The thermal circuits are constructed using thermal resistor R_{th} to describe the resistor of the heat flow through materials, while the dynamic and time-dependent part is described using thermal capacitances C_{th} (Figure 10), which is used to describe the time delay contribution of the different layers [48].

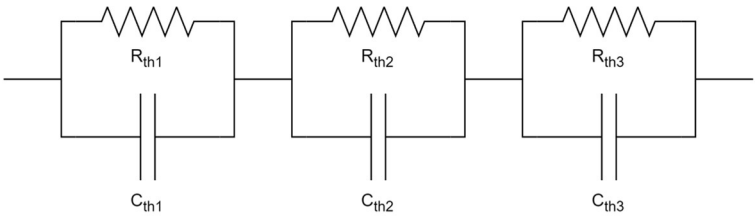


Figure 10. Example of Thermal lowpass RC network in series for modelling the thermal response of the device. The resistor describes the ability to conduct heat with the time dependent properties described using the capacitance.

A thermal network can be used to describe how heat flows in a GaN HEMT, and the temperature of different locations of a GaN MMIC, as demonstrated in [Paper A]. The power dissipation level in the heaters describes a current source, and the ambient temperature is applied as a constant DC source to set the circuit's ambient temperature. The equivalent temperature at the different nodes is then synonyms with the circuit voltage and can, as such, be easily extracted as seen in in Figure 11.

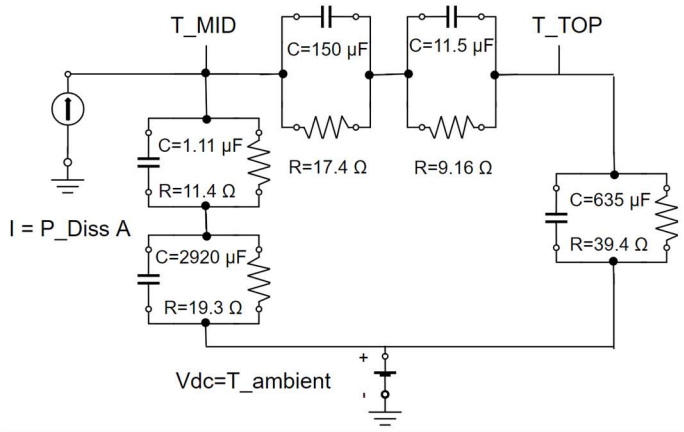


Figure 11. Extracted thermal network for test structure and package. T_MID and T_TOP corresponds with middle and top sensor locations. P_Diss is the dissipated power in the heater and T_ambient the starting temperature.

The middle sensors, is placed close enough to the heat source which enables a more accurate temperature reading and registration of the dynamic behaviour. The values for the corresponding components in the thermal low pass filters are experimentally derived to match the derived temperatures and correspond with the recorded power dissipations using an ideal power step. During actual operation, the step is non-ideal, and the heater elements themselves display a nonlinear temperature dependence, which impacts the dissipated power, which would be required to be considered if a more precise analysis is to be performed. However, using the acquired model, it is still possible to estimate the temperature for an arbitrary power dissipation, as seen in Figure 12. Except for the initial high-frequency temperature increase, the model faithfully replicates the measured temperature for both the top and middle sensors.

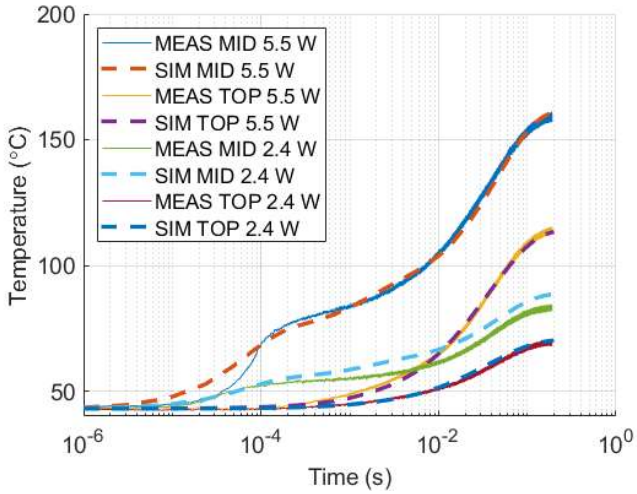


Figure 12. Transient thermal behaviour, agreement between simulation using proposed thermal network and measured temperature as registered by the sensors in thermal test structure.

This is highly advantageous since the test structure can, therefore, be used to formulate a model for how the temperature in the middle of the device behaves. This knowledge of how the two sensors are corelated can then be transferred to a real-life application where a temperature sensor is placed at a distance can be used to estimate the temperature in the transistor.

Another approach is to create physical models of the device and package and perform numerical simulations, for example, by solving the Fourier equations of thermal conduction describing thermal propagation through the physical properties of a GaN HEMT model using the finite element method (FEM). The configuration of these simulations requires detailed insight into the structure of the device and package being simulated and the effort to set it up. In return, the physical description provides significant insight and valuable information for thoroughly analysing the behaviour.

While FEM simulations can be used to replicate the registered thermal response of the sensor, the actual temperature of the GaN HEMT channel is more challenging describing thermal processes at the micro to nanoscale. [49]. One challenge when simulating semiconductor devices is the difficulty of determining the temperature of the active part constituting the hot spot at the gate or channel temperature [50]. Using a Fourier analysis significantly underestimates the device peak temperature as it is not valid at the small dimensions at the scale of µm and nm that constitute the channel hotspot [50]. This is caused by the limitations in accurately capturing the impact of phonons using Fourier equations [49],

Instead, Monte Carlo Method can be used, which has been shown to provide more realistic values of the channel temperature. However, at the cost of computational complexity, it is possible to improve this by compartmentalising the simulation into one part using the Monte Carlo method closest to the active device to describe heat generation and Fourier analysis to determine the impact of the surrounding geometry [50]. This approach can therefore help with identifying the contributions of individual layers in the epitaxial structure and the cooling solution, such as the thermal interface between the chip and substrate or mounting. Since the heat spreads vertically into the epitaxial structure, the interaction with the underlying TIM below the chip and underlying structures is also significant [48].

Chapter 4

Memory Effects in GaN

Different mechanisms can cause memory effects in GaN, such as thermal, as discussed in Chapter 3, which impacts device operation. Memory effects can also be caused by electron trapping and manifest as the build-up of electric charge, which has been thoroughly researched and increasingly well understood. The traps originate from within the device's epitaxial structure and can be caused by intentional and unintentional doping or other defects. These traps result in undesired energy states in the semiconductor bandgap, which become occupied when a high electric field is applied. Causing electrons to collect at different locations in the device, such as at the surface [51], [52], in the AlGaN barrier [52] and the GaN buffer [53], [54]. The presence of trapped electrons causes a negative charge, which can act as a virtual gate. This virtual gate interferes with the effect of the applied gate voltage, as the effective device threshold voltage becomes unstable. The prevalence of traps and the associated time scales could differ since the manufacturing process, materials, and epitaxial structure vary between the foundries, resulting in different characteristics [55], [56]. Still, dynamic non-ideal behaviour degrades device performance as the electric field changes, introducing time constants ranging from ns to ms and in some instances, trapping effects can impact the device over several hours or even longer.

Processing improvements in the manufacturing of GaN HEMTs have diminished electric field-induced surface trap charging partly by introducing surface passivation as well as a GaN cap layer along with buffer engineering [57]. Additionally, improvements in device geometry such as the use of field plates has also reduced the impact of trapping, but the phenomenon remains as an issue [57].

Therefore, the impact of memory effects in GaN HEMT must be characterised and modelled. For example, similar thermal effects, trapping can also be described using RC networks [58]. Alternatively, a more physics-oriented approach, such as the Shockley-Read-Hall model [59], has been implemented and demonstrated to predict trapping-related effects accurately These approaches are included in the compact models used by circuit designers [60]. Currently, the two most prominent approaches to device modelling are empirical and physical-based devices, exemplified by the Angelov model [61], [62] and the ASM-HEMT model [63], [64], respectively, which both have certain approximations of these effects but are often simplified. Improving these models would enable circuit designers to evaluate the

impact of memory effects during circuit design. It could be used to compensate for the dynamic effects, such as biasing of the circuit to compensate for decreases in performance [65]. Some methods also include the necessary components for describing gradual effects, such as varying inter-pulse stability in HPAs [66] or increasing memory effects in switches, as investigated in [Paper C], but it remains a nontrivial challenge to address [67]. This is important, especially when adapting GaN technology to high-power and high-performance applications and how memory effects affect circuit operation. This is nontrivial to predict in the design stage and sometimes only becomes apparent when subjecting the circuit to actual operating conditions.

4.2 Amplifiers

For radar applications, HPAs are driven in deep compression to maximise output power. These operating conditions result in high electric fields and significant power dissipation. The power consumption and heat generation associated with continuously operating power amplifiers would be considerable. Instead, the device is often operated in a pulsed mode where the gate voltage is switched from below the threshold voltage to the active operating point to decrease average power dissipation. While this significantly reduces the heat generation, it can also cause issues with trapping in terms of gate lag, which reduces the output power and, in turn, reduces system performance [57], [68]. Furthermore, pulse-to-pulse instabilities can be caused by both gradual heating of the device and gradually increasing or varying trapping effects [66]. This means that the properties of the initial pulses will differ over time, which could introduce uncertainties when performing the final analysis. Another effect to consider for multifunctional systems is how selecting between different waveforms, such as pulses with varying amplitude and duration, affects operation since this has been demonstrated to cause memory effects [69]. The result of this distorts the shape of the original waveform or signal with in-pulse trapping and thermal effects [69].

On the other hand, LNAs have different conditions since the use case and design differ from HPAs. Instead of pulsed operation, they are usually continuous on during operation to enable the detection of incoming signals. They are also typically biased with lower drain voltages and drain currents to reduce heat generation caused by continuous operation, and compared to HPA, the device is not intended to be subject to varying high fields, which could cause complex memory effects. However, since the LNAs are designed to amplify weak signals requiring high sensitivity, they make them vulnerable to intentional and unintentional jamming. While the robustness of GaN reduces the risk of permanent damage, high input signals can disrupt signal reception during jamming [70]. More probable, it could cause the LNA to experience temporary gain collapse [71] and degrade signal detection during recovery as charged trap states are discharged.

4.3 Front End Switches

The front-end switch is another component whose operation condition differs from amplifiers since the dedicated switch transistor is not biased to provide gain and is often integrated into circuits using a common gate configuration. Additionally in a transceiver, the switch should affect the signal as little as possible. Especially, in terms of electron trapping since this would result in unwanted dynamic behaviour in both the send and receive signal. Therefore, it is highly relevant to characterise this effect to evaluate the impact on circuit performance in front-end switch devices and to determine the technology's stability over time.

There are significant trade-offs and challenges to consider since significant trapping has been demonstrated when the switch is operated with highly negative voltages [14] [13]. One trade-off in the biasing of the switch with highly negative off voltages is to increase isolation in off-state and prevent self-biasing if the device is subjected to high input powers. However, the high electric fields cause trap states to be charged. When the switch is turned on, the turn-on time is ideally only limited by the technology cut-off frequency f_T, in the order of ns for GaN HEMTs. Instead, the behaviour will initially display a quick rise time, which then transitions to a transient with a time constant of 100 ms or more. The results can be seen in Figure 13, which illustrates the recovery of the S_{21} of a GaN HEMT switch transistor as the device is switched from off to on state for increasingly negative off voltages ($V_{G,OFF}$) seen in [13], [14].

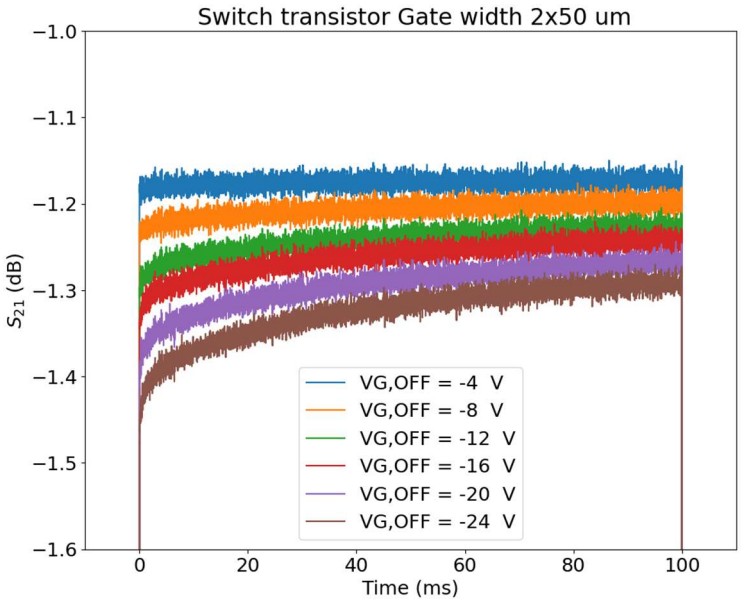


Figure 13. Increasing recovery time with increased off-voltage for GaN HEMT switch devices [Paper B].

Therefore, it is of interest to evaluate this recovery for transceiver operation, which is performed in [Paper B] and [Paper C]. This is achieved by approximating realistic operating conditions where the device is continuously pulsed from off to on, a measurement setup (Figure 14) is proposed to characterise this effect.

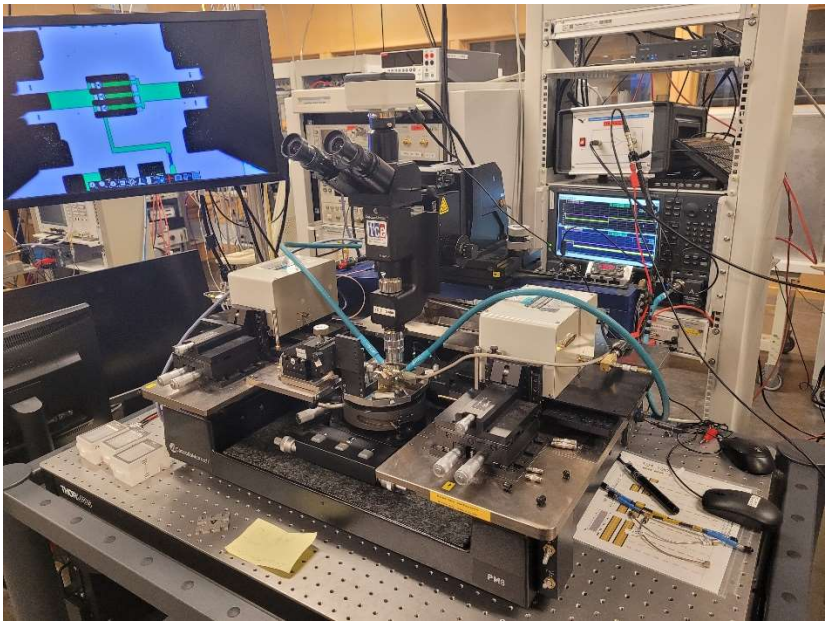
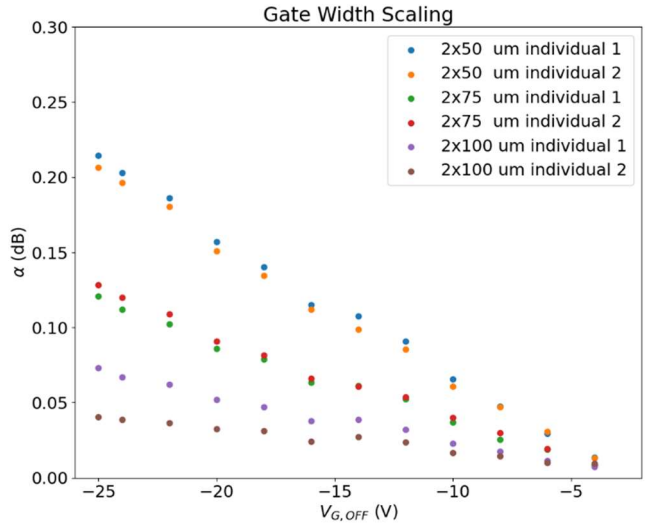


Figure 14. Switch characterisation lab setup.

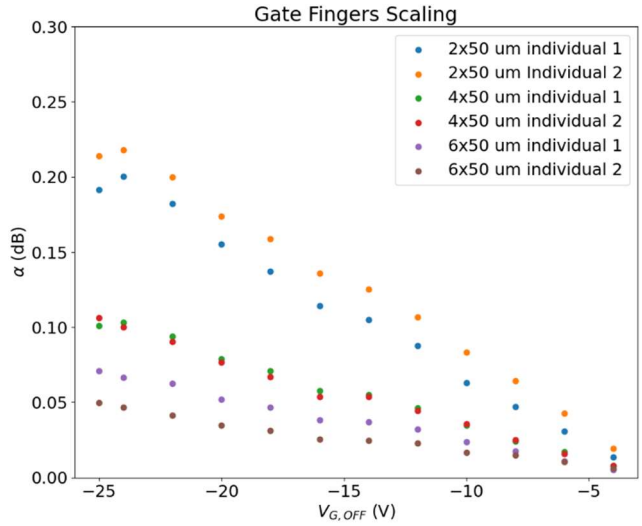
Furthermore, a method to quantify the transient recovery of the IL is used to estimate the impact of recovery, outlined in [Paper B] and relies on a simplified approach to describe the impact of trapping for amplifier operation by studying the transient response in the drain current. Since the switch devices do not have a drain current that can be used to model this behaviour, the IL is used instead, as can be seen in (1). The transient recovery is described using an exponential part where the term α is useful for demonstrating the dependence of the $V_{G,OFF}$.

$$IL = IL_0 - \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}} \quad (1)$$

This approach is used in [Paper B] to study how the total gate width and the gate width distribution amongst different gate fingers impact the amount of trapping. As expected, the amount of trapping increased with decreased $V_{G,OFF}$ as indicated with higher values of α, with the smaller devices displaying a higher impact of trapping (Figure 15a). Additionally, the distribution of the gate width can also be shown to impact the amount of experienced trapping (Figure 15b). Interestingly, two devices with the same total gate width, such as 2x100 µm and 4x50 µm, showed differences in recovery, indicating the importance of carefully selecting device geometries during circuit design.



a)



b)

Figure 15. Differences in recovery depending on device geometry illustrated by using amplitude α against off voltage $V_{G,OFF}$. With a) variations in gate width and b) variations in number of gate fingers.

Another aspect to consider is the stability of recovery during continuous operation. Therefore, the switch setup [Paper B] was complemented to allow for an investigation of the stability of the recovery over time in combination with a gradual decrease of $V_{G,OFF}$. The topic is of interest since the amount of trapping can potentially increase over time as illustrated in Figure 16. In [Paper C] the same model as in [Paper B] is used for quantifying the recovery using three different technologies which are studied over time. The drift in memory effects can be observed during continuous operation, illustrated in Figure 17, especially for one particular technology denoted "A", as outlined in [Paper C]. For all technologies studied the

recovery increase with varying sensitivity to decreased off voltage but for “A” there is also a drift over time as outlined in [Paper C]. The potential instability in recovery could, therefore, be a relevant aspect to consider for circuit designers depending on the requirements of consistency for example the pulse-to-pulse stability.

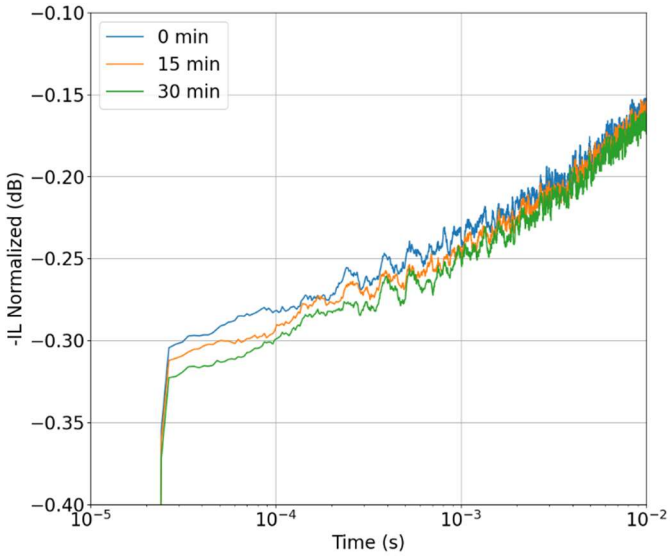


Figure 16. Drift in recovery of GaN HEMT Switch due to dynamic memory effects for continuous operation during 30 minutes.

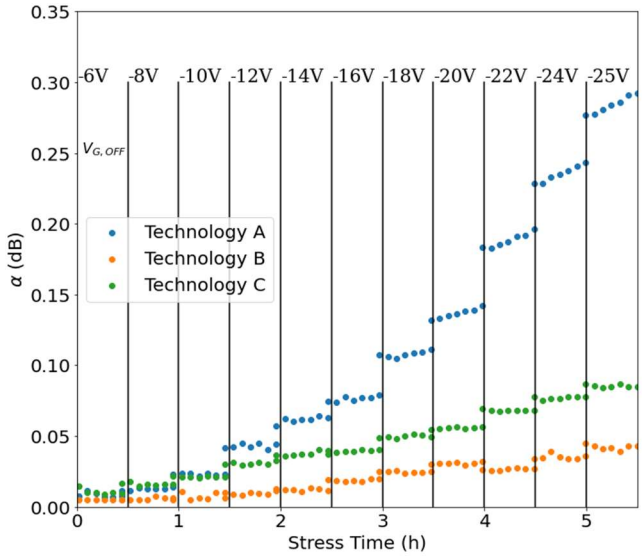


Figure 17. Increased impact and drift of switch recovery over time for continuous operation indicated with increasing α vs $V_{G,OFF}$ for different technologies.

4.4 Compensating for the Impact of Memory Effects

Thanks to extensive research into characterising memory effects, different strategies have been formulated to mitigate their impact on performance. Improving the compact models to accurately predict the effect of trapping techniques such as digital pre-distortion (DPD) can decrease the impact of memory effects further (Figure 18). For example, taking the effects studied in [Paper B], [Paper C] into consideration could contribute to the work on DPD already during the design phase of the GaN HEMT front end instead of characterising already manufactured transceivers. These methods rely on being able to predict the behaviour of the trapping to compensate for, e.g., an increase or decrease in output power in pulsed operation to achieve the desired waveform [72] [73]. Alternatively, DPD has also been shown to be possible by formulating behaviour models based on measurement data of a circuit, which can be used to predict or adapt to memory effects [66]. The effectiveness of this has also been demonstrated to significantly decrease inter-pulse instabilities and improve the output signal when selecting between different waveforms, e.g. amplitudes and pulse lengths.

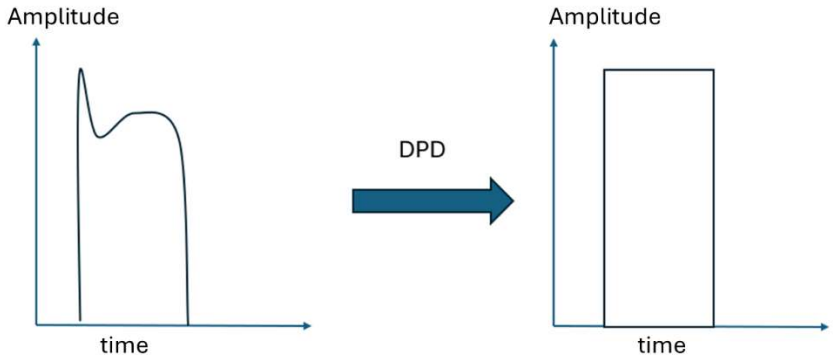


Figure 18. Example of a waveform (pulse) distorted by nonlinear effects (left) and the desired waveform after DPD (right).

Chapter 5

Conclusions

The continuous adaptation of GaN HEMTs as the primary technology for high-power applications at microwave frequencies is unlikely to stop in the foreseeable future. Increasing demands for higher performance drive the improvement of the technology itself and the models used to realise circuit functionality, package, and integration.

As part of this effort, this thesis has briefly outlined the challenges with the dynamic properties of GaN in terms of electrical and thermal effects and the issue of heat generation because of high-power operation. In this regard, the temperature sensors with complementing measurement techniques detailed in [Paper A] constitute a valuable contribution to monitoring temperature in packaged devices with the potential to contribute to evaluating the effectiveness of thermal management as well as measurement data to be used to calibrate physical simulations, especially on circuit and package levels.

The importance of estimating the impact of electron trapping on the circuit level for the continuous operation of front-end switches in multifunctional GaN MMICs is investigated. For example, it is essential to consider bias conditions, device geometries and technologies for the front-end switches to reduce the impact of the off voltage on switch recovery as demonstrated in [Paper B], [Paper C].

Both of these aspects contribute to a deeper understanding of the operating conditions of GaN MMIC front ends. Improving the description of the thermal and trapping effects could, by extension, also improve the conditions for using methods such as DPD.

Future Work

There are many interesting further studies within the context of the nonlinear effects and the use of GaN technology for compact systems. Below are a few topics that could constitute the work's relevant and exciting continuation.

- Investigate temperature-insensitive power amplifiers using the proposed method to extract the thermal RC network and apply it to an actual packaged GaN HEMT. Included thermal sensors will extract temperature and use this information to bias the device dynamically

- Including the thermal test structures in packages to evaluate the impact of different thermal management techniques, such as TIMs, heat spreaders, and active cooling solutions, could be interesting as it would help clarify which applications require active cooling and which can suffice using passive cooling.

- Further investigating the impact on continuous operation using switch devices by including a medium to high input to study the impact of jamming on the switch device performance.

Investigate, if any, or to what degree the switch device performance permanently degrades during high-off voltages and the possibility of restoring the switch time performance by trying to decrease the electron charge by, for example, placing the device at an elevated temperature to reduce the emission time.

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Paper A

On-Chip Sensors for Temperature Monitoring of Packaged GaN MMICs

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On-Chip Sensors for Temperature Monitoring of Packaged GaN MMICs

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***Abstract*—A novel approach to on-chip temperature sensors for non-invasive thermal characterization and monitoring of packaged GaN MMICs is presented. The proposed sensor is fully compatible with commercial GaN foundry processes and enables improved reliability estimation of highly integrated systems. A dedicated test structure is developed to demonstrate the capabilities of the sensor, and an accurate calibration method of its temperature response is proposed. This combination allows for continuous temperature monitoring during operation with electrical acquisition of temperature transients. The method also enables the thermal characterization of the device and package.**

***Index Terms*—Electro-thermal effects, GaN, MMIC, Semiconductor device packaging, Thermal sensors**

I. Introduction

THE primary semiconductor technology for high-performing radar and communication systems is gallium nitride (GaN) high electron mobility transistors (HEMT) due to its high cutoff frequency and power density. Until recently, the demonstrated output power densities for gate lengths between 0.10 and 0.15 µm have typically been around 4 W/mm at frequencies of 30 GHz [1]. However, as the technology is continuously evolving, even higher power densities of 10 W/mm at both 30 GHz and 94 GHz is targeted in, e.g., the DARPA DREaM program [1]. Furthermore, the use of AlN substrates has recently enabled power densities up to 24.4 W/mm for gate lengths of 0.25 µm at X-band [2].

This technological development results in smaller transistors with higher levels of dissipated power. Higher power densities will increase the operating temperature of the HEMT, which impair its long-term reliability and performance, especially in a package [3]. This may impose system designs with a backed-off performance to ensure reliable operation.

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Several methods can be used to measure the temperature of GaN HEMTs, e.g. optical techniques, temperature-dependent device parameters or dedicated on-chip sensors. Optical methods like Infrared thermography (IR), Raman spectroscopy, and thermoreflectance [4] can be accurately calibrated to measure the device temperature provided optical access and dedicated equipment, which is not feasible for real-time monitoring of packaged components. The use of temperature-dependent device properties such as on-resistance (R_{on}) [5] is not always practical for real-time monitoring since the operating conditions of the HEMT could vary depending on the application. Dedicated on-chip temperature sensors can be realized by, e.g., HEMTs with integrated special temperature-dependent thin film resistances [6], AlGaN/GaN Schottky barrier diodes (SBD) [7], or GaN resistors [8]. A key advantage is that dedicated sensors do not require optical access and can be operated independently of the monitored GaN MMIC. Furthermore, on-chip circuits for temperature readout have been successfully demonstrated, but at the cost of more area and the need for enhancement mode HEMTs [9] [10]. However, not all integrated temperature sensors are compatible with commercially available GaN MMIC foundries.

This paper proposes using an on-chip temperature sensor placed close to the device while not impairing device performance [8][11]. This sensor is based on a GaN resistor, which does not require additional manufacturing steps and is fully compatible with commercial GaN MMIC foundries. Furthermore, it is demonstrated to be compatible with bare-die as well as encapsulated MMICs, as no optical access is required. This facilitates improved reliability estimations of encapsulated devices through the capability of continuous temperature monitoring and, e.g., adaptation of operational conditions.

II. Fabrication and Packaging

Dedicated GaN on silicon carbide (SiC) test dies is fabricated to demonstrate the operating principle of the proposed sensor. The fabrication is done using the Chalmers University of Technology in-house GaN technology [12]. The GaN HEMT structure consists of an $Al_{0.25}Ga_{0.75}N$ barrier with a thickness of 25 nm followed by a Fe-doped GaN buffer and a 500 µm thick SiC substrate. The fabricated sample of 16 x 16 mm^2 is diced into smaller dies of around 1 x 2 mm^2 that each contain a single test structure. The backside of the substrate is metalized with Ti/Au to enable the use of an adhesive for the packaging.

A. Bare Die Mounting

The individual test chip is mounted on a copper carrier using a silver epoxy adhesive (ABLEBOND 84-1LMINB1) to examine the feasibility of the thermal test structures and the proposed method for real time temperature monitoring. The copper carrier simplifies handling and, combined with the silver epoxy improves the interface of the chip backside. The silver epoxy is manually dispensed, and the thickness of the interface is calculated by measuring the distance between the top of the chip and the copper carrier *h*, as seen in Fig. 1. The thermal properties and dimensions of bare-die mounting is summarized in Table 1.

B. Embedded Die Mounting

The method is evaluated for packaged devices by encapsulating the test chip in PCB, as illustrated in Fig. 2. Connection to the chip is accomplished by gold bond wires and connectors on the top of the PCB. The chip is attached to the ground plane by use of a pressureless silver sinter paste (Heraeus DA295A, Table 1) and copper-filled thermal vias through a 254 µm thick PCB layer.

III. Thermal Test Structure

The purpose of the thermal test structure is to replicate the power dissipation of a GaN HEMT and to monitor the device temperature. In this case, an 8 x 75 µm^2 HEMT is approximated with 8 parallel 3 x 75 µm^2 GaN resistors used as heaters. The fabrication of the test structure did not include air bridges, and hence, the heater is split into two equal parts with four fingers in each, as seen in Fig. 3 a).

The temperature monitoring is achieved by the placement of a GaN resistor at the center point of the heating structure. This sensor is ideally as small as possible [8] while complying with process design rules, resulting in the dimensions 10 x 4 µm^2, as seen in Fig. 3 b).

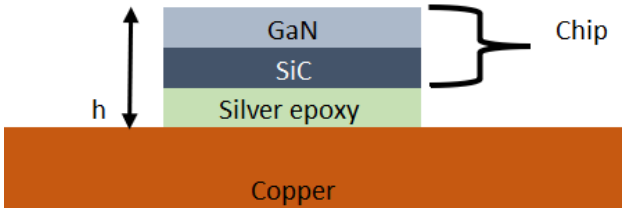


Fig. 1. Cross section of bare die on copper, not to scale.

TABLE I
Thermal Properties and Device Geometry

Layer	Area	Thickness	Thermal conductivity W/m K
GaN	875 x 1975 µm^2	1.6 µm	160 [13]
SiC	875 x 1975 µm^2	500 µm	400 [13]
Ag Epoxy	Similar to chip	25 µm	3.9 [14]
Ag Sinter	Similar to chip	-	150 [15]
PCB	25 x 25 mm^2	254 µm	-
Copper	25 x 20 mm^2	2 mm	387.6

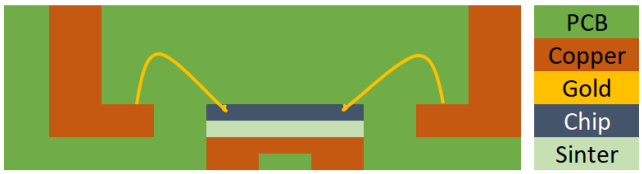


Fig. 2. Cross section of embedded die, not to scale.

The sensor placements must also obey the design rules to avoid short circuits between metal layers. This resulted in a minimum separation of 25 µm from the sensor's center to the closest active area in the heater (Fig. 3.c). A second sensor is placed 200 µm from the nearest active area. The purpose of the top sensor is to monitor the temperature at a non-invasive distance to not risk interfering with the electromagnetic environment of the HEMT and hence degrade its high-frequency performance. Furthermore, the Chalmers GaN technology uses mesa isolation to define the GaN resistors, but the concept would work equally well with other temperature sensitive resistances such as thin films or GaN resistors defined by implantation.

A. Sensor Characterization and Modeling

The operating principle of the sensor is to apply a constant voltage across it and monitor its temperature-dependent conductance. The conductance of each sensor is, therefore, first characterized versus temperature to obtain individual models. The characterization is carried out by placing the test structure on a temperature-controlled chuck, and thermal equilibrium is ensured by a fixed settling time before measurements. The used temperature range is from 40 °C to 200 °C in 20 °C steps. The voltage is swept from -0.7 V to 0.7 V (Fig. 4) to achieve a linear I-V characteristic with minimal effect of self-heating [8] while providing a current that can be accurately monitored.

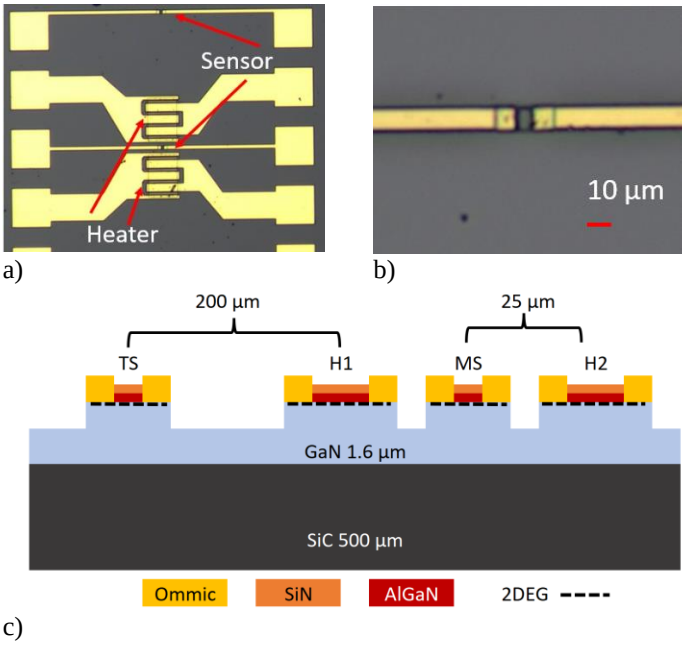


Fig. 3. Photograph of the integrated thermal test structure (a), a zoom in on the small sensor (b), and the device cross section (c) where TS, MS, H1, and H2 stands for top sensor, middle sensor and heater elements respectively.

The conductance of the sensor is determined by a linear fit of current versus voltage for each operating temperature. The temperature dependence of the conductance at a fixed voltage is thereafter modeled using a second-degree polynomial, as given by:

$$T = c_2 G_s^2 + c_1 G_s + c_0 \quad (1)$$

where T is the sensor temperature in °C, G_s is the sensor conductance in mS, and the fitting parameters c_o, c_1, and c_2. The model provides a good fit for the used temperature range, as seen in Fig. 5, and the conductance is, as expected, decreasing with increasing temperature.

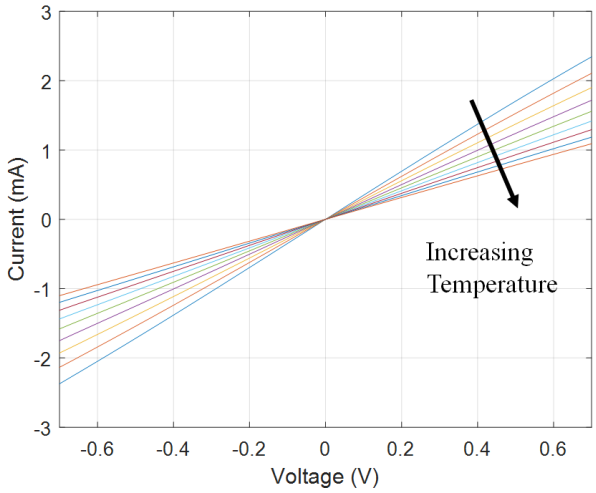


Fig. 4. I-V characteristics of different sensor operating points for temperature range from 40 °C to 200 °C in 20 °C steps.

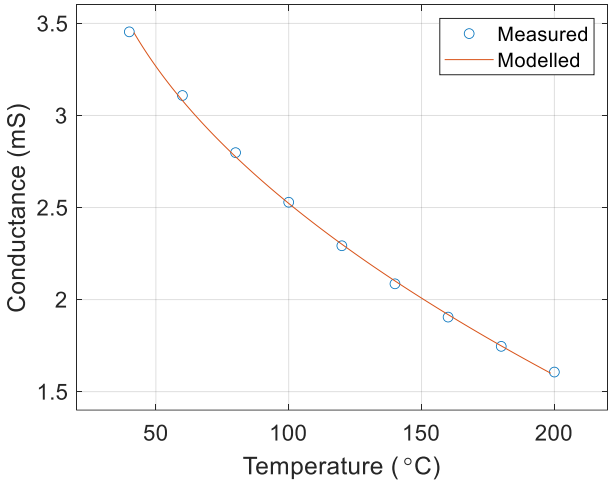


Fig. 5. The measured and modeled sensor conductance versus ambient temperature for a representative sensor

The reproducibility of the sensors is assessed by characterizing eight individuals. Their conductance versus temperature is measured, and a least square fit using (1) is used to extract an average representation. The variation in temperature with respect to the average is ± 7.9 °C (2σ), as shown in Fig. 6. Part of this variation is due to the uncertainty of the used temperature chuck, which has a temperature specification of ± 2 °C.

B. State of the Art Comparison

The most common metrics when comparing temperature sensors are their linearity and sensitivity. Furthermore, size and manufacturability are important when considering the implementation and use of the sensor for packaged MMICs. The proposed sensor based on a GaN resistor is compared to other state of the art on-chip sensors in Table 2.

The required sensitivity depends on how the sensors, in the end, are integrated in the intended system, and the proposed GaN resistor performs comparable to other published sensors.

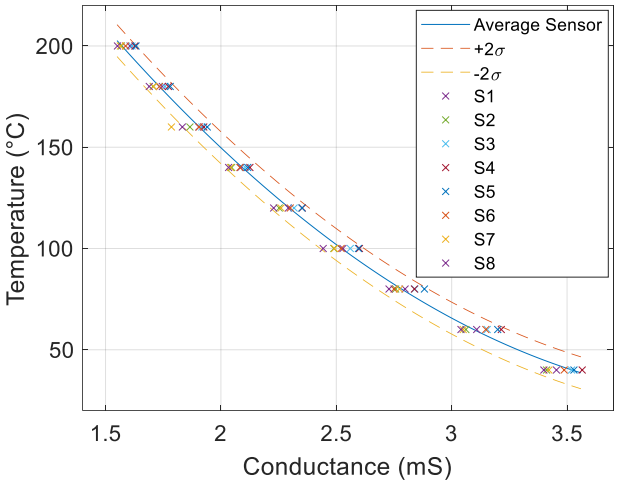


Fig. 6. Reproducibility by comparing the variance in conductance of eight individual sensors.

TABLE II
COMPARISON BETWEEN ON-CHIP TEMPERATURE SENSORS

Sensor Type	Sensitivity /K	Linearity	Size µm²	Reference
Integrated TFR	0.36 Ω	0.9997	-	[6]
Integrated TFR	10 Ω	-	-	[16]
TFR	0.32 Ω	-	-	[17]
GaN Resistor	31.28 mV	0.995	400	[9]
GaN Resistor	2.17 mV at 1 mA Or 3.3 Ω at 0.7 V	0.9785	40	This work
PIN Diode	19.7 mV	0.938	1950	[18]
SBD Diode	1.61 mV	-	2000	[19]
SBD Diode	0.35 mV	0.993	50000	[10]
SBD Diode	2.54 mV	0.992	6400	[7]

The linearity depends on the operating conditions and could be improved at the cost of reduced sensitivity. The GaN resistor shows comparable linearity and by using a nonlinear model description (1), satisfactory performance is achieved. Furthermore, the proposed GaN resistors and SBDs are the only components available in commercial foundry processes. Finally, the size of the GaN resistor is significantly smaller compared to the SBD, and it is, therefore, a good candidate for low cost integration of temperature sensors in GaN MMICs.

IV. Dynamic Response Characterization

The sensor can be used both for steady state temperature monitoring as well as measuring the thermal transient for a fast transition, such as the turn-on of a GaN HEMT. However, the distance between the sensor and heater will limit the sensitivity to very fast temperature variations, and this limitation is characterized by comparing readings of the middle sensor with the top sensor located further away.

The dynamic response is measured by the setup in Fig. 7 that consists of a current waveform analyzer (Keysight CX3324A) to capture the current and voltage waveforms, as well as a source measure unit (Keysight B2912B) to apply a voltage step function. However, the applied voltage step is not instantaneous due to the limited slew rate of the source measure unit (SMU), and it takes 50 µs to reach the desired voltage level of the heater. The sensor is kept at a constant bias of 0.7 V, and the current through it is measured between -10 ms and 190 ms relative to the measurement trigger, with a complementary steady state measurement after 1 s. The ambient temperature is controlled by a thermal chuck set to 40 °C. The temperature of the sensor is then calculated using the empirical conductance model described in (1).

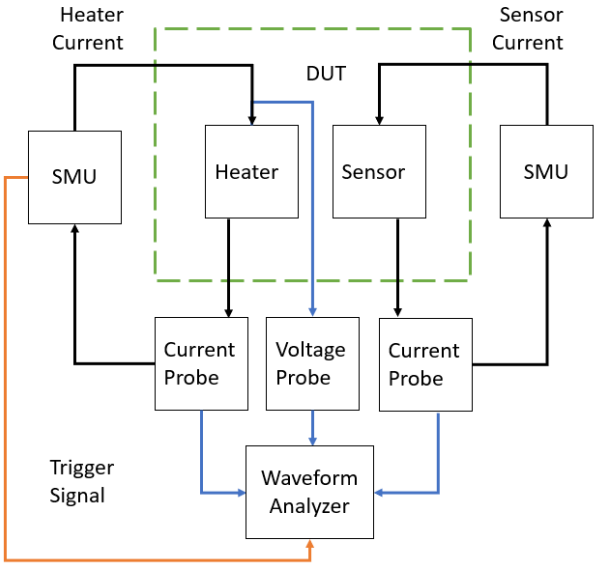


Fig. 7. Measurement setup for thermal characterization. Black lines indicate current path for heater and sensor. Blue lines voltage and current probes. Trigger signal is orange and green dashed line indicates device under test (DUT)

A. Power Dissipation in Test Structure

The GaN resistors used as heaters have a nonlinear I-V characteristic and a strong temperature dependence, as seen in Fig. 8, where the current decreases with time as the heater dissipates power. The heaters display a transient in dissipated power up to 60 ms before converging. For simplified modeling, the steady state value of dissipated is sufficient. However, the dynamic power characteristics could be of interest in a more detailed analysis of the temperature impact on the device,

B. Sensor Placement

The purpose of the two sensors is to have one (top) representing a realistic placement and the other (middle) to capture the temperature in the center of the HEMT and correlate this with the top sensor. Measuring the temperature at a certain distance away will have some implications on what level of detail can be obtained, such as limitations in capturing fast modulations. If the difference in temperature between the two readings is stable, a prediction of the peak temperature can be made based on the readings of the top sensor by developing an equivalent thermal impedance model of the device.

C. Measured Thermal Response

The temperature response for the top and middle sensors is recorded for a voltage pulse applied to the heater. To exemplify this, two different dissipated power levels (2.4 W and 5.5 W) are used. The results in Fig. 9, clearly indicate that the top sensor is a low pass filtered version of the middle sensor, as the initial fast transient before 1 ms is missing.

To fully utilize the top sensor, it needs to be correlated with the middle sensor. The temperature difference between the two placements versus time is therefore calculated, as seen in Fig. 10. The close proximity of the middle sensor causes it to heat up first, and an increase in temperature difference is observed after 10 µs. The continued temperature increase between top and middle sensor is correlated until 10 ms when another sharp

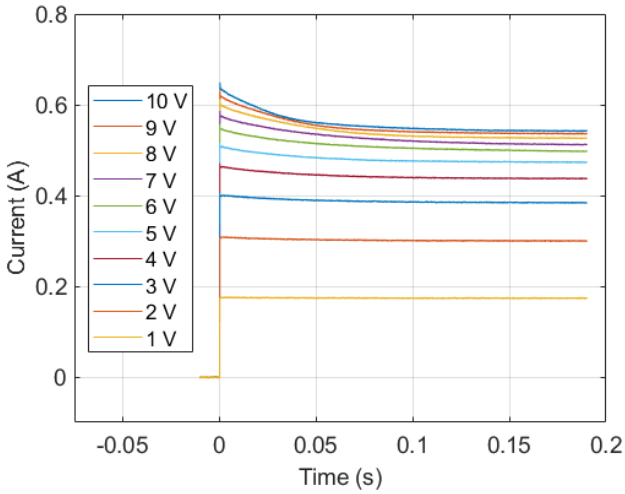


Fig. 8. Measured current through heater elements for different applied voltages.

increase in temperature is observed for the middle sensor. At around 20 ms, the temperature difference between the two sensors starts to converge to a stable final value. This indicates that the proposed test structure can be used to accurately predict the operating temperature of the heater for signal modulations slower than 20 ms.

D. Equivalent Thermal Impedance Model

An electro-thermal model of the thermal test structure, including the two sensors, is derived and implemented in a microwave CAD software. The purpose of the model is to estimate the temperature and the dynamic thermal response of the middle sensor based on the reading of the top sensor. The thermal properties of the test structure are modeled by multiple RC networks [20], as illustrated in Fig. 11, where the temperature is extracted at the two nodes T_MID and T_TOP, representing the middle sensor and top sensor, respectively. The model parameters are extracted by fitting the simulation to the measured response (Fig. 9). It should be noted that the model is extracted only for the maximum steady state dissipated power of 5.5 W.

An accurate model description will thus allow calculating the peak temperature in the middle of the device by measurements on a sensor positioned a significant distance apart, as demonstrated in IV.C. To illustrate this, simulations with different dissipated power levels are carried out on the model. The simulation result is compared with the measurements of both sensors in Fig. 12, and good agreement is achieved even though only one power level was used for the model parameter extraction.

E. Embedded Die Temperature Monitoring

The influence of packaging upon sensor performance is evaluated by encapsulating the test structure using the embedded die packaging technology in Fig. 2. The measured temperatures for the top and middle sensors of the device are seen in Fig. 13 a), and similar characteristics as for the bare die test structures mounted on copper is observed. Importantly, the temperature difference for the top and middle sensor, as seen in Fig. 13 b), converges to a stable value as for the on-copper test structure. This indicates that the proposed technique is applicable for real time monitoring of packaged MMICs.

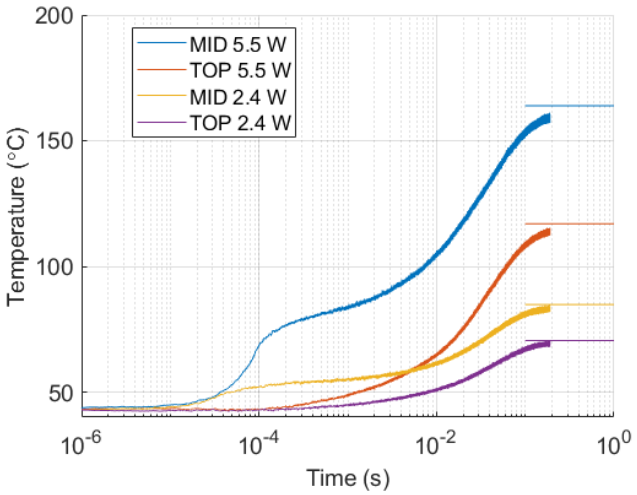


Fig. 9. Measured temperature responses for bare die on copper, using top and middle sensors.

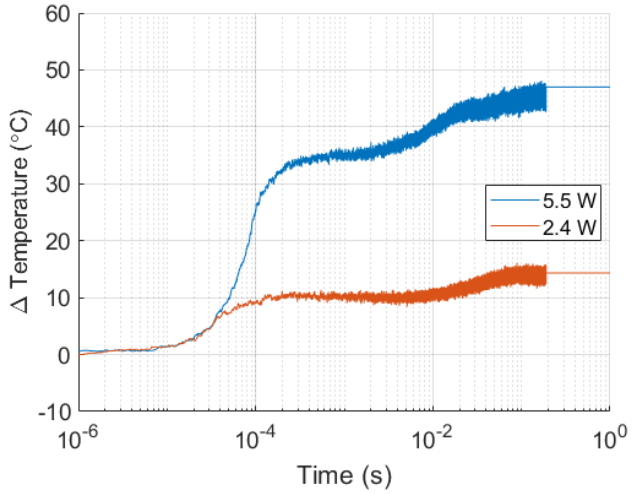


Fig. 10. Bare die on copper temperature difference between top and middle sensor.

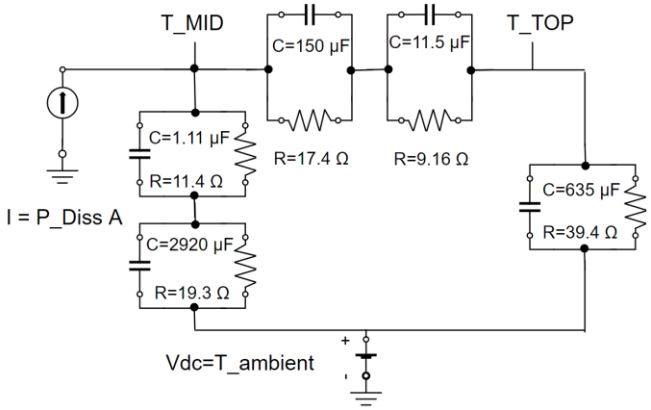


Fig. 11. Electro-thermal model representation used in a microwave CAD software.

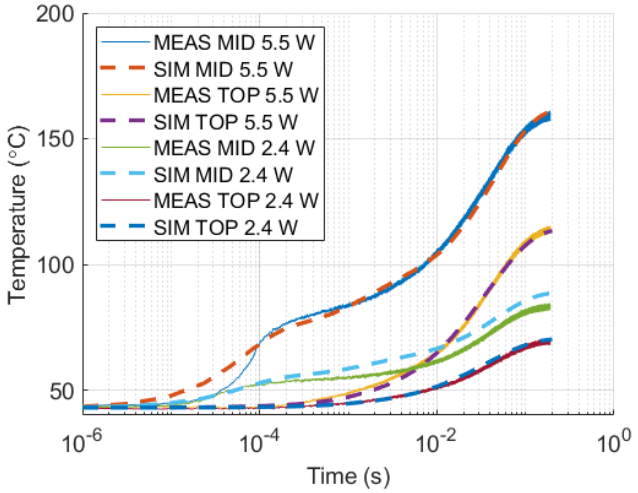
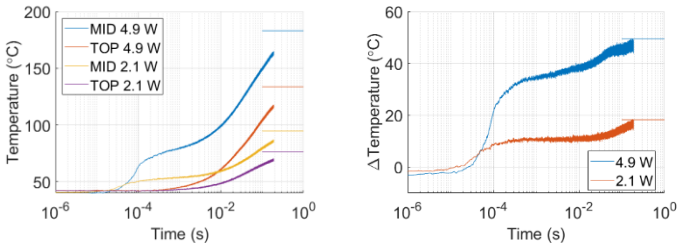


Fig. 12. Electro-thermal model comparison with measurements.



a) b)

Fig. 13. Logarithmic representation of measured temperature responses and sensor difference for embedded die.

The reproducibility of the packaged temperature sensors is evaluated by characterizing six embedded sensors similar to the bare-die evaluation in section III.A. The variation for packaged sensors is ± 9.5 °C (compared with 7.9 °C in III.A), which indicates that the packaging has little or no influence on sensor operation.

V. Conclusion

We have developed a novel method for temperature monitoring of GaN HEMT devices, independent of packaging technology. This was achieved by the use of small and non-invasive sensors, which are easily implemented using commercially available foundry processes and technologies. It is demonstrated that a sensor placed at a distance of 200 µm can be used to accurately characterize the impact on temperature caused by signal modulation of 20 ms or slower for bare-die as well as packaged GaN MMICs. This is enabled by the integration of two sensors into a thermal test structure consisting of heater elements that dissipate power similar to that of a GaN HEMT. As such, thermal characterization during the operation of GaN HEMT technology is no longer limited to optical access and is thus more easily implemented on a system level.

Acknowledgment

This work was performed within the Competence Center for III-Nitride Technology C3Nit-Janzén and has received financial support from the Swedish Governmental Agency for Innovation Systems (VINNOVA) via grant No. 2016-05190, Linköping University, Chalmers University, Lund University, Epiluvac, Ericsson, FMV, Gotmic, Hexagem, Hitachi Energy, Saab, SweGaN, United Monolithic Semiconductors (UMS), and Volvo Cars.

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Paper B

Transition Time of GaN HEMT Switches and its Dependence on Device Geometry

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Transition Time of GaN HEMT Switches and its Dependence on Device Geometry

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***Abstract* — This paper presents the impact on the slow transition time of GaN HEMT switch transistor due to size and geometry. Measurements in the time domain are used to characterize the transition time of the switch from off to on. This is done for several switch transistors with variations on total gate width and number of fingers. In order to enable the comparison of transition times a figure of merit is established. This is achieved by using a commonly used model for trapping effects to quantify the amplitude of the slow transient with respect to the gate voltage. The resulting analysis indicates that transition time is sensitive to transistor size and dependent on the geometry of the device as increasing the width of the gate fingers is more advantageous compared to increasing the number of fingers.**

***Keywords* — Gallium nitride (GaN), hemt, switch, MMIC.**

I. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMT) for microwave applications is an active research field. The wide band gap of the semiconductor makes it attractive for various applications, such as transceiver (TR) modules which are operated as both transmitter and receiver. GaN HEMT based front-end switches are suitable for this application as they are resilient to high input and output powers. Furthermore, by using GaN it is possible to integrate the transceiver using MMIC, enabling more compact system designs.

There are well-known challenges with GaN devices, such as electron trapping due to energy states in the band gap. This is caused by e.g. intentionally doping the buffer and unintentional defects in the epitaxial structure [1]. The charging of these electron traps results in memory effects in the device as performance depends on previous operating conditions. This is a problem in a system that e.g. switch between sending or receiving regularly. Extensive work has been performed in characterizing trapping, memory effects, and recovery time in GaN HEMTS, primarily aimed at amplifier design [1], [2].

In the case of switch transistors, trapping has been determined to affect the transition time for switching [3]. Ideally, the switch has a swift off to on characteristics close to the switching speed of the device Fmax which should be in the order of 50 GHz for this technology [4]. Trapping however, causes an additional slow transient behaviour which will be referred to as transition time. Both measurement methods and models have been developed [3], [5] to characterize this, but the effect of transistor layout on transition time has yet to be investigated. This is of interest to an MMIC designer as switch transistors are often designed using other layout considerations and operating conditions compared to ordinary RF transistors. The insertion loss (IL) in the on state and isolation in the off state are important device properties that depend on transistor size, but the transition time impacts this performance. This is especially relevant to consider for front-end switches which benefit from low off bias conditions to increase isolation [3].

This paper compares a selection of switch transistors to investigate how transition time is affected by transistor geometry in terms of total gate width and the number of fingers. These parameters are typically available to a designer using a commercial foundry process. Characterization is done through pulse profile S-parameter measurements in the time domain [3]. To compare the results, a model is used to quantify the impact on transition time.

II. GaN HEMT Switch Transistors

The layout of a GaN HEMT switch transistor differs from an ordinary RF transistor as the drain and source connections are used as input and output, respectively as seen in Fig. 1. The gate is used to turn the switch on or off by applying a DC bias VG between gate and source/drain. While the drain and source are set to the same potential to maintain the transistor in a passive state.

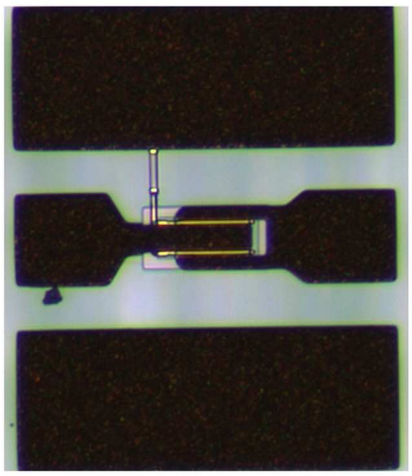

Fig. 1. Switch transistor layout.

The switch transistors are manufactured using the Chalmers in-house GaN on SiC process [4]. The study includes six switch transistors with the same general layout parameters described in Table 1. This include Lg which is the gate length while Lgds and Lgds represent the distance between the gate and the source/drain connection. The integrated gate field plate is the length of which the gate extends over the 2DEG towards the drain.

Table 1. Layout parameters of the used switch transistors

Layout parameters	Values (µm)
Gate Length (Lg)	0.25
Gate source separation (Lgds)	1
Gate drain separation (Lgd)	1
Field plate	0.25

The total gate width can be varied in two ways to investigate the size scaling effects of switch geometry. This is done by, firstly, increasing the gate width for a fixed number of fingers and, secondly, by increasing the number of gate fingers. As a result, the total gate width for the transistors varies from 100 to 300 µm, as described in Table 2.

Table 2. Geometry variations of the switch transistors

Switch transistor	Nr of gate fingers	Gate width (µm)	Total gate width (µm)
1	2	50	100
2	4	50	200
3	6	50	300
4	2	50	100
5	2	75	150
6	2	100	200

III. Transition Time Measurement

The switch is operated by changing the VG from below Vth (off) to above Vth (on). Ideally, the switch on behavior should be the same regardless of the previous VG. In practice, the device displays a transition time due to previous bias conditions. When turned on, the switch is initially fast with a measured rise time of less than 50 ns, but instead of quickly reaching a steady state value, it has a prolonged transition time [3], [5]. Depending on the bias condition and transistor layout, this affects the switch for tens to hundreds of milliseconds [3].

The transition time is characterized by a pulse profile S-parameter measurement [3] at 6 GHz with an input power of -15 dBm. The gate voltage is pulsed from varying off-state conditions to a fixed on-state VG of 0 V. The pulse frequency is 5 Hz with a 50 % duty cycle, which enables the capture of the slow transient behavior after the switching instance.

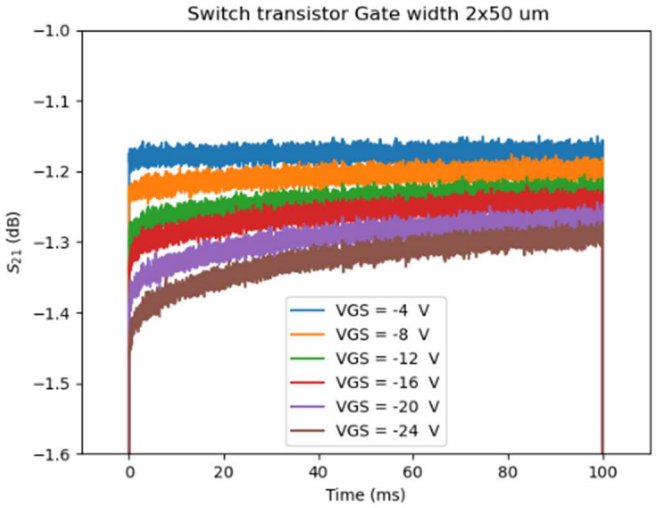

Fig. 2. Insertion loss time transition measurement for a 2x50 µm switch transistor for different VG.

Measurements on a 2x50 µm switch, as seen in Fig. 2, show that for lower VG the device displays an increasing amplitude of the transient response. The time constant of the transient is estimated to be around 30 ms. In addition, the insertion loss increases with lower, previously applied VG, even though the on voltage remains the same. This indicates the impact of memory effects on transition time due to previous VG.

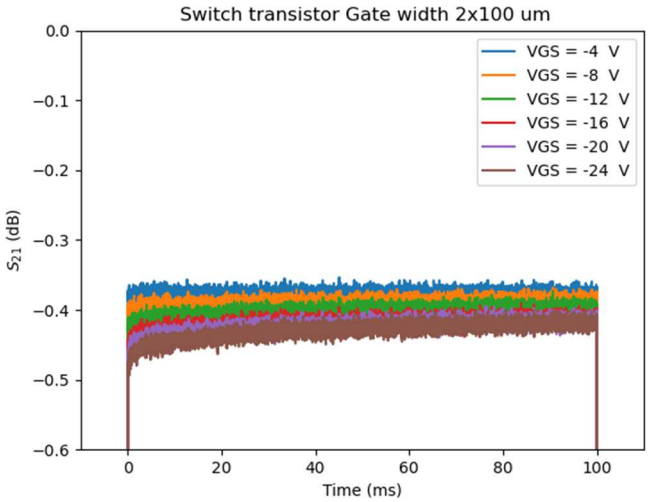

Fig. 3 Insertion loss transient recovery measurement for a 2x100 µm switch transistor

Interestingly, the impact on transition time is not as significant when performing the identical measurement on a 2x100 µm transistor, as seen in Fig. 3. This is important as it suggests a relationship between transistor size and the amplitude of the transition time due to memory effects. The difference between the two devices can be ascertained from comparison with Fig. 2. But confirming the effect and establishing a trend requires more gate width variations. Preferably with several specimens to avoid uncertainties due to device spread. Furthermore, as the number of measurements

increases, the method of visually inspecting each time transient becomes insufficient. Therefore, characterizing the dependence requires a qualitatively comparison of the transition time differences between devices in terms of a figure of merit.

IV. Transition Time Modeling

In order to quantify the transition time, a model is used to extract parameters that can be used as a figure of merit. Previous work has used the transient characteristic of the drain current to model the effects of trapping in terms of a sum of exponentials [6]. This does not directly apply to how a switch is used as it does not have a DC drain current, but the same approach can be applied to the IL, as given in (1). Assuming one dominant trapping contribution, the model will have an exponential term describing the transient behaviour of the transition time compared to the steady state value, denoted $S_{21,0}$.

$$S_{21} = S_{21,0} - \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}} \quad (1)$$

The exponential time dependence is described using the time constant τ. The β parameter is used to describes the character of trap states. The value of β can vary between 1 and 0.5 to describe a continuum of trap states [6]. A least square fitting is used to extract the model parameters. This reveals that the τ varies slightly around the initially estimated 30 ms. The β consistently remains close to 0.5 indicating a continuum of trap states, rather than a single state. The amplitude of the transient is modeled by α and is most affected by the gate voltage. The α parameter increases as a function of VG. Thus, the larger α is, the more significant the effect on transition time. Therefore, the amplitude of the transient helps characterize the impact of trapping in switches.

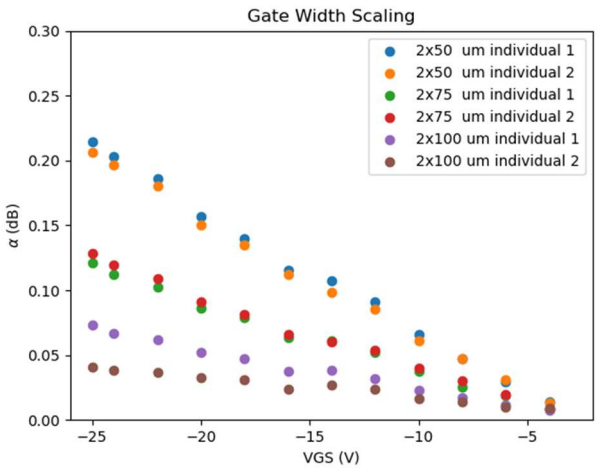

Fig. 4 The α for switch transistors with gate width scaling for 2 gate fingers.

How α varies with respect to VG for different switch transistors can be seen in Fig. 4. Increasing the gate width for a switch transistor with two gate fingers from 50 to 100 µm with two individuals of each, shows that α decreases with the total gate width. Thus, the previously observed dependence on size for the transition time is further confirmed by the general trend of smaller transistors displaying higher α for the same VG.

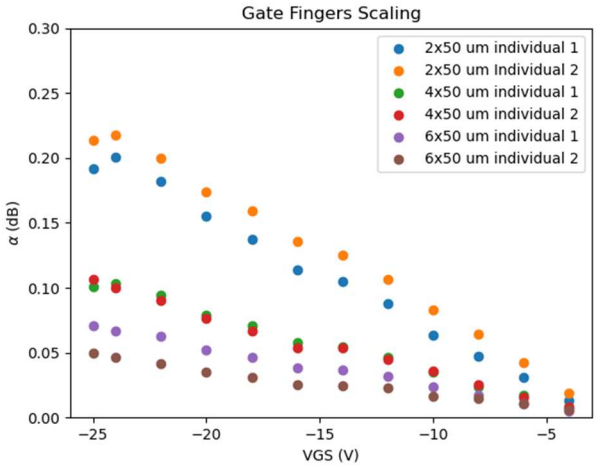

Fig. 5. The α for switch transistors with different number of gate fingers with a gate width 50 µm.

Increased α for smaller switch transistors in terms of VG can also be observed when increasing the number of fingers for a fixed finger width of 50 µm, as seen in Fig. 5. Interestingly, the 2x100 µm from Fig. 4 and the 6x50 µm have similar values of α even though the total gate width is 200 µm and 300 µm respectively.

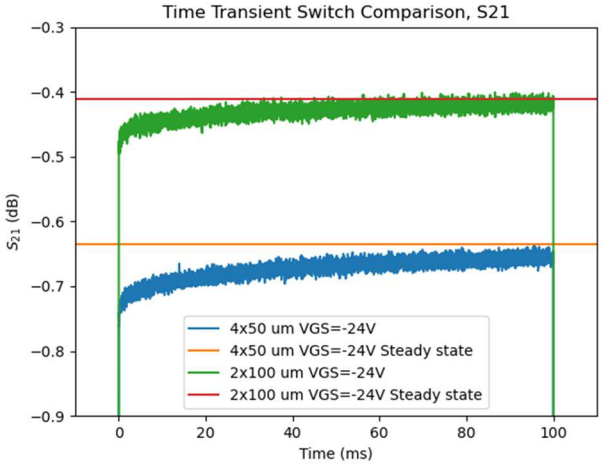

Fig. 6. Comparison of 4x50 µm and 2x100 µm switch transistors.

Furthermore, comparing the 2x100 µm and 4x50 µm transistors reveals they have different α. This is important as both devices have the same total gate width but different geometries. As seen in Fig. 6 the amplitude is higher for the 4x50 µm transistor. However, to determine that these effects are, in fact, intrinsic properties caused by difference in geometry and not an effect of a difference in series resistance compared to the system impedance. This is of interest as series resistance determines the IL as the voltage is divided over the switch series resistance and the 50 Ω system impedance. Assuming a π-network [3] equivalent small-signal model, the

series resistance of the switch transistors is calculated from the S-parameters as

$$Z_{switch} = Z_0 \frac{(1+S_{11})(1+S_{22})-S_{21}S_{12}}{-2S_{21}}. \quad (2)$$

The switch series resistance between the two devices is comparable at 7.25 and 7 Ω, as seen in Fig. 7. Therefore, the voltage division should be approximately the same and the difference in IL is not explainable through a difference in series resistance. Furthermore, they display similar tendencies as the IL in Fig. 6, with a more significant transient response for the 4x50 µm switch transistor at lower VG. The 4x50 µm switch series resistance is also significantly more affected by low VG. This means that the difference in transition time between the devices will not be possible to improve by changing the system impedance.

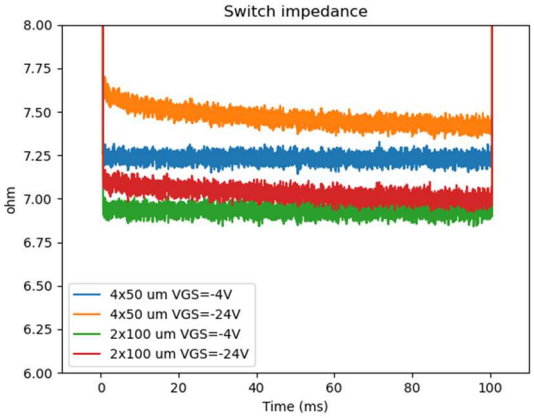

Fig. 7. The switch resistance for 4x50 µm and 2x100 µm.

V. Conclusion

Characterization of the transition time of switch transistors with respect to size and geometry has been performed. The results show that the transient response is dependent on transistor size. It is shown that the amplitude of the transient response scales inversely with total gate width. Furthermore, it was demonstrated that two switch transistors with the same total gate width, but different geometries display different transition times. A switch with few long gate fingers displays less impact of transition time compared to a switch with more and shorter gate fingers. In combination with that the series resistance of a switch with long gate fingers or more gate fingers did not deviate considerable due to layout. We can conclude that the impact on transition time is not due to voltage division between the series resistance and the system impedance. Instead, this indicates that this is an intrinsic property of the devices due to a difference in geometry.

The reason for the slow transition time is due to trapping, and the difference due to geometry still needs to be fully understood by further studies. However, as there is a significant impact on transition time depending on the switch layout, this result is highly relevant for MMIC designers. The amplitude of slow transient was modeled by using the α parameter. Thus, this paper proposes the α parameter as a figure of merit to indicate the impact on time transition for switch transistors. The results can assist designers in the process of making qualitative and informed decisions regarding their designs in order to improve performance.

Acknowledgment

This work was performed within the Competence Center for III-Nitride Technology C3Nit-Janzén and has received financial support from the Swedish Governmental Agency for Innovation Systems (VINNOVA) via grant No. 2016-05190, Linköping University, Chalmers University, Lund University, Epiluvac, Ericsson, FMV, Gotmic, Hexagem, Hitachi Energy, Saab, SweGaN, United Monolithic Semiconductors (UMS), and Volvo Cars.

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Paper C

Short Term Drift in the Recovery Time of GaN HEMT Switches

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Short Term Drift in the Recovery Time of GaN HEMT Switches

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***Abstract*—A step stress characterization method is proposed to enable the study of the gradual degradation of memory effect-induced recovery in GaN HEMT switches. This is achieved by characterizing the transition from off- to on-state over time and tracking short-term degradation in the recovery of the insertion loss for decreasing off-state voltages. The method is demonstrated on three different technologies. The results show that the degradation varies between foundry processes, illustrating the merit of the method for evaluating the impact of memory effects in GaN HEMT switch operation.**

***Keywords* — Gallium nitride (GaN), HEMT, switch, MMIC.**

I. Introduction

Gallium nitride (GaN) high electron mobility transistor (HEMT) technology has been proven suitable for high-power applications at microwave frequencies and is increasingly applicable for low-noise applications. This makes it attractive for highly integrated transmit and receive modules (TRMs) since both transmit and receive functionality can be integrated into a single microwave monolithically integrated circuit (MMIC). This is relevant when realizing compact and lightweight radar and communication systems for airborne platforms. The TRM requires switching between transmission and reception, which can be realized using an integrated front-end switch.

The switching between modes of operation (i.e. changing terminal voltages) will result in the charging and discharging of trap states originating from defects as well as intentional and unintentional doping of the epitaxial structure [1], [2]. The impact of memory effects due to the traps can be studied by recovery measurements, which have shown performance degradation on both amplifiers [2] and switches [3], [4]. In a time-multiplexed system, the front-end switch will operate continuously, and the traps will hence be in a non-equilibrium condition. Therefore, the evolution of the trap dynamics during the short-term stress of a front-end switch is of large interest.

A step stress characterization method is proposed to capture the short-term drift of trapping-induced recovery effects in GaN HEMT switches. The method is further applied to different GaN MMIC technologies to demonstrate generality and acquire insight into device operation.

II. Step-Stress Characterization

A dedicated switch transistor from a commercially available GaN on SiC foundry process (denoted technology A) with a gate length of 0.15 µm and a gate width of 5x75 µm is used to demonstrate the method. The switch devices are operated in common gate configuration with the source and drain potentials set equal. This provides low insertion loss (IL) in on state and high isolation in the off-state. The off-state voltage ($V_{G,\,OFF}$) should be low to achieve high isolation and prevent self-biasing at high-power operation. The recovery of the device is characterized by measuring the insertion loss when changing from an isolating to a conducting state [5]. The operating condition is to continuously switch between $V_{G,\,OFF}$ and $V_{G,\,ON}$ (0 V) with a 200 ms period and a 50% duty cycle. The results in Fig. 1 illustrate the recovery of the insertion loss for the device normalized to a steady state measurement and the isolation versus $V_{G,\,OFF}$ in the inset. It is observed that the amplitude of the recovery of the insertion loss increases with lower $V_{G,\,OFF}$ which is in line with previous studies [3], [4].

Memory effects are dynamic, and it is likely that more traps will be charged if the device is operated for a longer time at a high electric field. This effect is illustrated by operating the device at $V_{G,\,OFF}$ = -25 V for 30 minutes while measuring the recovery in the On-state. The selected $V_{G,\,OFF}$ is a typical bias conditions for GaN front-end switches [5]. The results in Fig. 2 indicate that the amplitude of the transient increases with operating time.

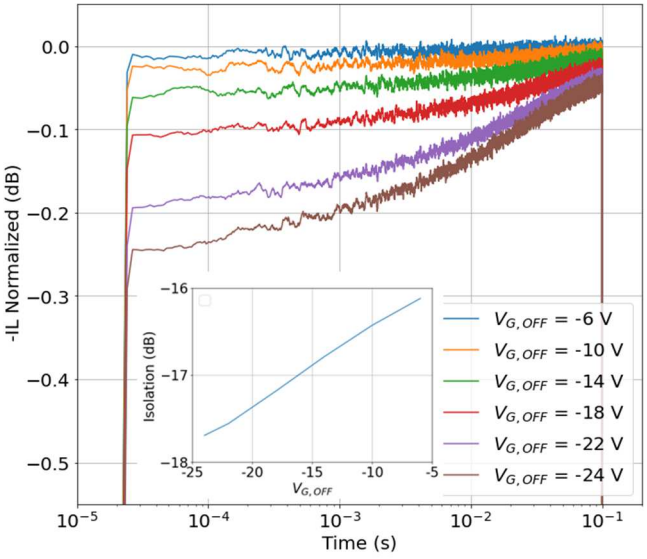

Fig. 1. Recovery of the insertion loss for different Off-state voltages for technology A. Inset: Isolation versus $V_{G,\,OFF}$.

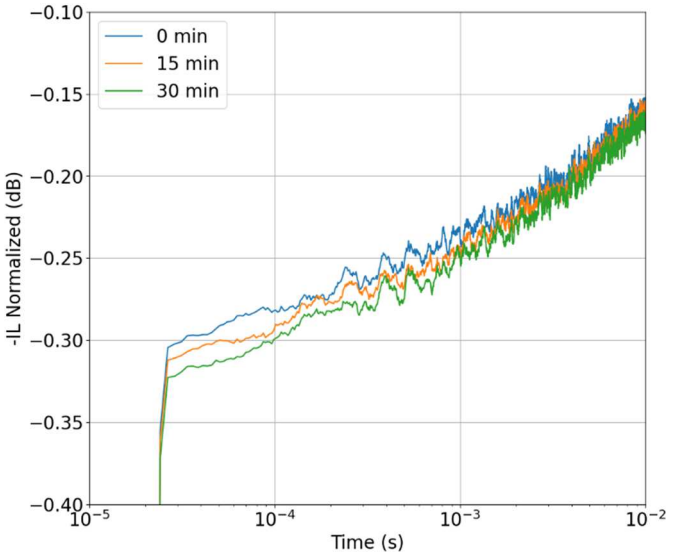

Fig. 2. Recovery of the insertion loss for 0, 15, and 30 min operating time with $V_{G,\,OFF}$ = -25 V for Technology A.

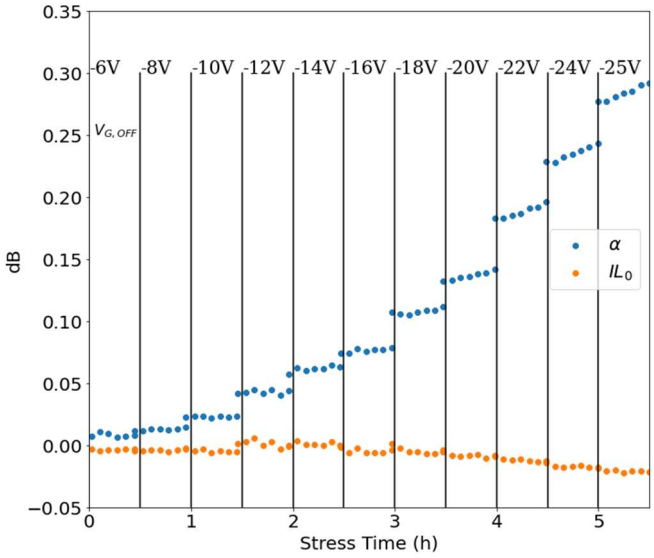

Fig. 3. Evolution of α and IL_0 during the step stress.

These measurements are complemented with a step-stress characterization, in which $V_{G,\,OFF}$ is gradually decreased vs. time, and the recovery characteristics of the switch is monitored. $V_{G,\,OFF}$ is kept constant for 30 minutes while the recovery characteristic is measured every 5 minutes. $V_{G,\,OFF}$ is decreased from -6 V to -24 V in steps of 2 V, with an additional measurement at -25 V.

The change in the recovery characteristics is quantified by fitting the time domain measurement to the exponential model

$$IL = IL_0 - \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}}, \qquad (1)$$

where IL_0 is the steady state insertion loss value, α is the amplitude of the exponential, τ is the time constant, and β is a fitting term to account for the distributed energy levels of the traps [6]. Changes in the fitted model parameters provide insight into, e.g., variation in the number of charged traps (α) or change in energy level (β).

The resulting α parameter is shown in Fig. 3, and two observations can be made. Firstly, the α parameter is increasing with decreasing $V_{G,\,OFF}$, which aligns with previous observations [3], [4], [7]. Secondly, there is a clear drift in the α parameter at each stress voltage during the 30 minutes of operation. This indicates that with operating time, more trap states will be charged until they reach a steady state condition. The IL_0 parameter is initially constant, but a small deviation is observed for lower $V_{G,\,OFF}$ values. This is likely due to that the measurements do not capture the full transient, and the parameter fitting therefore has a large uncertainty. The same uncertainty impacts the extraction of τ (Fig. 4). Furthermore, as observed in Fig. 1, a flat response is obtained for $V_{G,\,OFF}$ values down to -14 V, and hence no reliable τ can be extracted in this region.

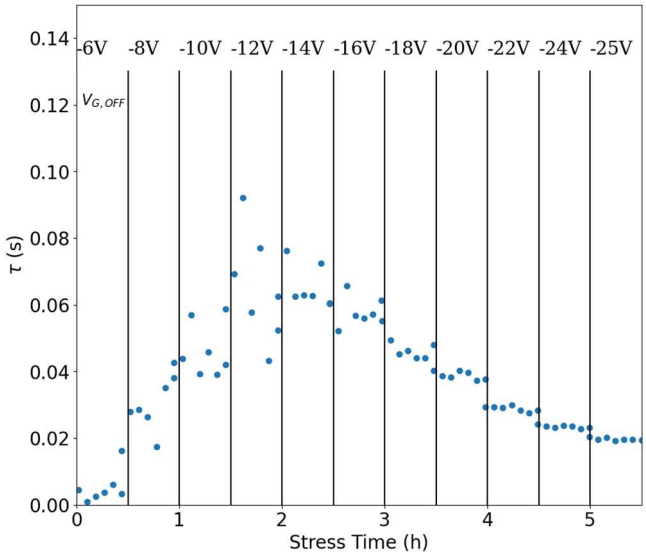

Fig. 4. Evolution of τ during the step stress.

III. Technology Evaluation

The method is further demonstrated with the inclusion of two additional technologies B (Commercial 0.1 µm MMIC), and C (Chalmers technology, 0.25 µm) [8]. The gate lengths of the three technologies differ, which could have an impact on the recovery characteristics as previously observed for different transistor geometries [7]. The Chalmers technology (C) includes multiple gate lengths on the same wafer, and hence enables an investigation of the impact of gate length upon the recovery of the insertion loss.

A. Gate Length Evaluation

The impact of gate length on the recovery time is characterized for technology C (L_g 0.1, 0.2, and 0.5 µm) with a gate width of 2x50 µm. The results in Fig. 5 show an expected

increase in insertion loss with decreasing $V_{G,\,OFF}$. The variation in the recovery of the insertion loss between the three samples show a significant variation and no clear trend versus gate length can be observed.

B. Technology Comparison

The three technologies are compared by characterizing HEMTs with similar geometries (Table 1). The results in

Fig. 6 indicate that the insertion loss increases with $V_{G,\,OFF}$ for all technologies. They all show comparable recovery characteristics for the -6 V measurement but significant variations in their dependence on more negative off-state voltages. Technology B and C show almost no impact, while, as previously observed, technology A is severely degraded when operated at lower off-state voltages.

The observed drift could be due to other effects than an increase in electron trapping. A common failure mechanism in GaN HEMTs is an increase in the leakage current of the gate diode, which could impact the trap dynamics [9]. Therefore, the gate diode characteristics are measured before and after the step stress test (Fig. 7). Instead, it can be observed that the leakage current in the gate diode is reduced after the step stress. Hence, no noticeable Schottky contact degradation has occurred, suggesting that the degradation on recovery illustrated in Fig. 6 is mainly caused by increased electron trapping. This increase in electron trapping could be due to an increase in the capture cross-section for the traps, as observed in [10] after HTRB stress. However, the HTRB stress is an accelerated test at elevated temperatures and the relatively early degradation observed in Fig. 6 indicate a potentially worse reliability for technology A.

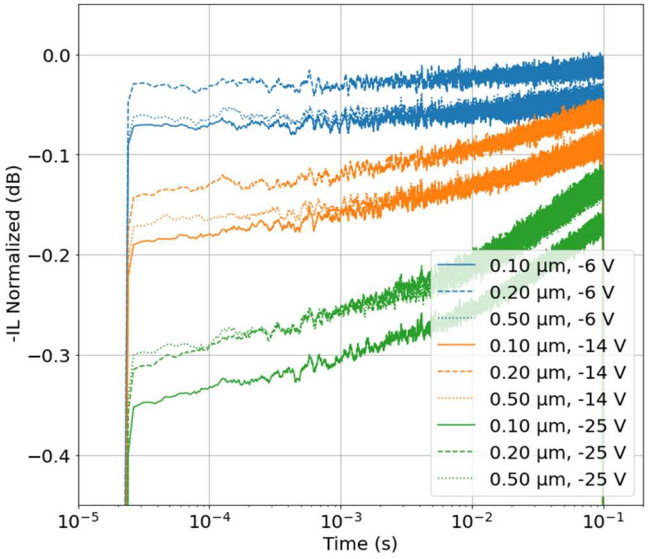

Fig. 5. Recovery of the insertion loss with decreasing $V_{G,\,OFF}$ for different gate lengths

Table 1. Transistor Geometries

Technology	Gate width µm	Number of fingers	Total gate width µm	Gate length µm
A	75	5	375	0.15
B	60	6	360	0.10
C	50	6	300	0.25

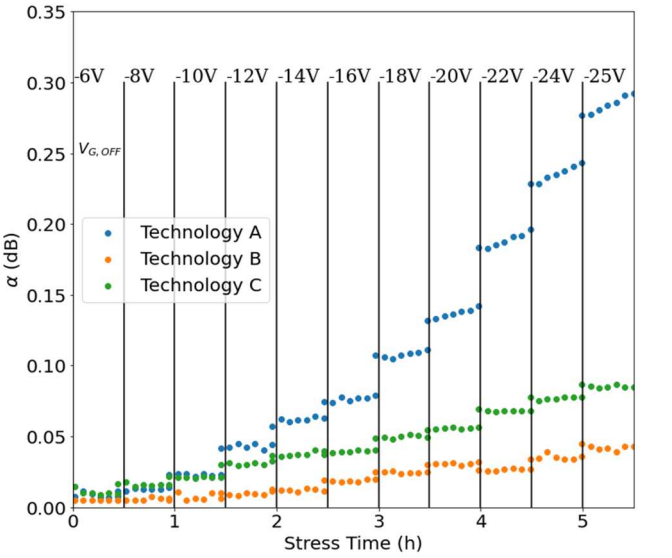

Fig. 6. Evolution of the α parameter versus stress voltage and operating time for Technologies A, B, and C.

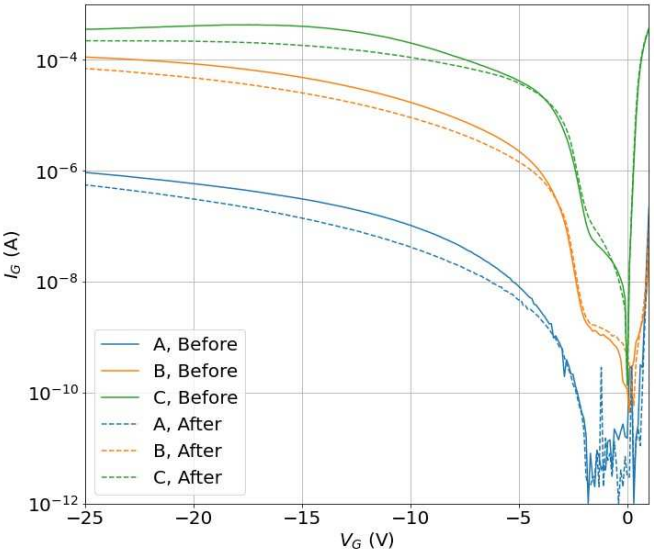

Fig. 7. The gate diode current I_G for technologies A, B, and C before and after the step stress

IV. Conclusion

The proposed method enables characterization of the recovery in GaN switches during short term stress. The gate leakage analysis revealed no degradation of the Schottky contact, suggesting that the observed drift is due to electron trapping effects. The method is demonstrated by evaluating three different GaN HEMT technologies, and the results

demonstrate different gradual degradation of the recovery of the insertion loss. The slow recovery in the GaN switches need to be accounted for when used as a front-end switch to not impair the system performance in terms of e.g. linearity for transmission, and signal-to-noise ratio for reception. The drift observed in this study poses challenges to compensation methods due to the uncertainty in the states of the traps.

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