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Dielectric Breakdown Mechanisms in High-κ Antimony Trioxide (Sb_2O_3)

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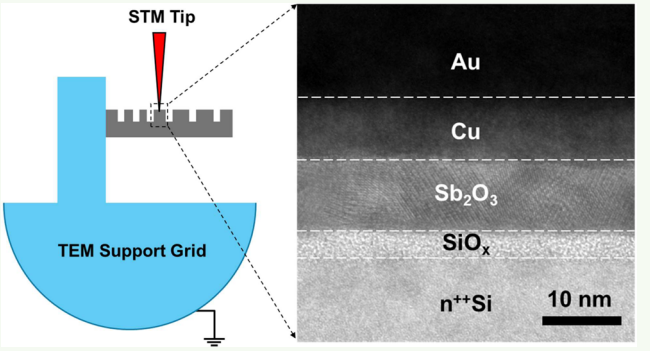
ABSTRACT: High-κ gate dielectrics compatible with two-dimensional (2D) materials are crucial for advanced electronics, and Sb_2O_3 (antimony trioxide) shows significant potential. Here, we show that the soft breakdown induces oxygen vacancies and migration of copper into Sb_2O_3. Hard breakdown, driven by joule heating, gives rise to a substantial temperature increase, leading to morphological transformations and oxygen redistribution. In situ transmission electron microscopy (in situ TEM) measurements correlated with device performance show the formation of nanoconducting filaments due to the increased concentration of oxygen vacancies and copper migration in connection with the soft breakdown. The hard breakdown is associated with the formation of antimony-enriched nanocrystals. These findings offer critical insights into the suitability of Sb_2O_3 as a high-κ gate dielectric.



KEYWORDS: *in situ TEM, molecular crystal, gate dielectric, 2D materials, high-κ, Sb_2O_3*

INTRODUCTION

Field effect transistors (FETs) play a fundamental role in achieving ultrafast and energy efficient logic and memory devices. Silicon has been the material of choice, and improvement in the FET performance has been traditionally achieved through dimensional scaling. With state-of-the-art FETs now reaching the sub5 nm length scale, further physical scaling is no longer feasible. Therefore, researchers are continuously exploring new materials and device architectures. Utilizing emerging atomically thin van der Waals (vdW) semiconductors (e.g., MoS_2, WS_2, etc.) as channels in FETs holds promise due to its higher intrinsic carrier mobility and enhanced material performance.[1] Since the transport of charge carriers is confined within the atomically thin layers, short channel effects could also be effectively mitigated in the *ultrascaled* FETs.

An atomically sharp and defect-free two-dimensional (2D) semiconductor film and dielectric interface are critical requirements for transistor applications.[2] Previous studies have shown that conventional gate dielectrics (e.g., SiO_2, HfO_2, etc.) are incompatible because they create defective vdW semiconductor and three-dimensional (3D) dielectric interfaces. These defective interfaces degrade carrier mobility in the vdW semiconductor and can lead to long-term reliability issues such as bias temperature instability (BTI) in FETs.[3] A viable solution is to use a vdW dielectric to achieve an atomically sharp and defect-free semiconductor/dielectric interface. Hexagonal boron nitride (h-BN) has been extensively used as a gate dielectric in prototype devices.[4−6] It would be difficult to meet the stringent requirements of the gate dielectric using h-BN as devices are further scaled down. This is because, as FET dimensions are scaled down, the gate dielectric thickness must be appropriately scaled to maintain a constant power density. The use of sub2 nm thin h-BN would significantly increase the standby power consumption in the scaled transistors due to direct tunneling.[2]

The use of a high-κ gate dielectric is advantageous because a relatively thicker dielectric can be used without compromising the electrical performance of the vdW materials. Thicker dielectrics also alleviate the constraints on the growth process, as growing atomically thin dielectrics on a wafer scale with a low defect density is challenging. Physically thicker dielectrics are also beneficial, as they mitigate the undesirable effect of the inherent defects at the gate electrode/dielectric interfaces. This effect could be significant when only a few layers thick gate dielectric is used.

Several high-κ dielectric materials have shown promising results, and they include calcium fluoride (CaF_2),[7] bismuth−selenium oxide (Bi_2SeO_5),[8] and antimony trioxide (Sb_2O_3).[9]

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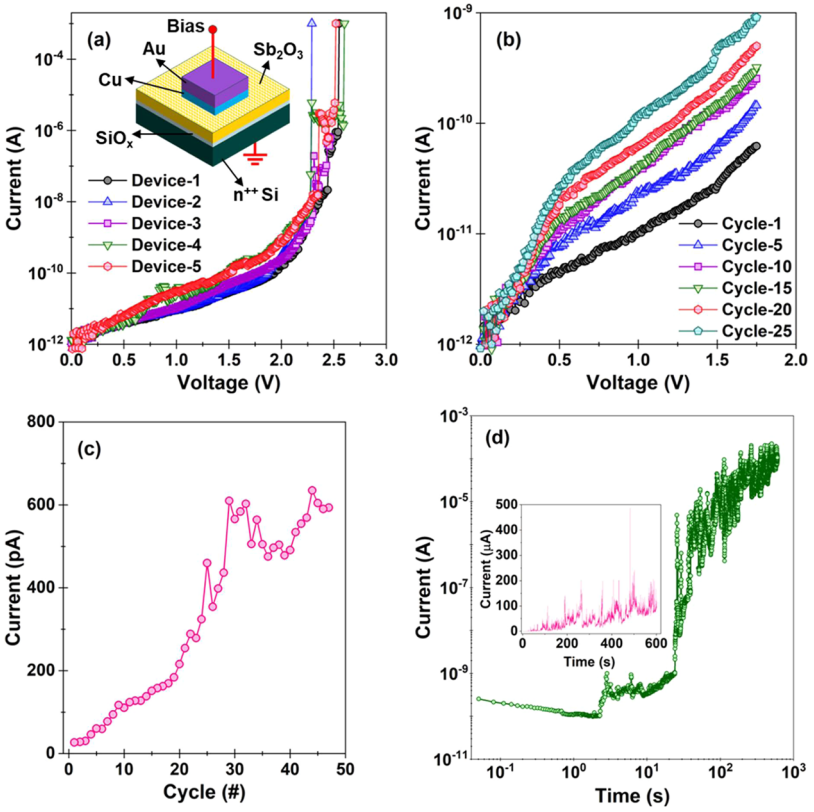

Figure 1. Standard device-level electrical measurements: (a) $I-V$ breakdown characteristics measured on capacitor devices. The inset shows the schematic of a capacitor and electrical connections for the measurements. The area of the capacitor is 100 μm × 100 μm. (b) $I-V$ characteristic showing the progressive increase in tunneling current when subjected to a cycling ramp voltage stress. (c) Plot of the increase in tunnel current with RVS cycles at 1.50 V. (d) Plot of TDDB characteristic of the capacitor at an applied bias of 1.75 V. The inset plots the data on a linear scale to show the noisy behavior observed during later periods of TDDB.

Among the available options, Sb_2O_3 is promising as a high-κ gate dielectric because it can be integrated with various vdW materials, including graphene and MoS_2. The deposition of Sb_2O_3 can be scaled up to a wafer scale, and Sb_2O_3 films can be deposited with nanometer precision in thickness. Prototype FETs with MoS_2 channels and 10 nm Sb_2O_3 gate dielectrics have demonstrated an on/off ratio of ~10^8 and a threshold swing of ~64 mV/decade at room temperature.[9] The choice of gate electrode/contact is crucial for harnessing the full potential of Sb_2O_3, as it affects dielectric performance, including breakdown voltage and leakage current.[10]

Dielectric breakdown is a key reliability challenge for FETs, and addressing it is crucial, especially when considering new materials. Under normal FET operating conditions, defects are gradually generated in the gate dielectric. Upon reaching a critical defect density threshold, a soft dielectric breakdown can be triggered.[11,12] Soft breakdown can be identified with a sudden increase in tunnel current (at least by 1 order of magnitude) in time-dependent dielectric breakdown (TDDB) measurements. The FET remains functional after soft breakdown, albeit with a degraded performance. If the defect generation continues, permanent damage occurs in the dielectric, leading to the complete functional failure of the FET. This is known as hard dielectric breakdown. Currently, there is a limited understanding of the defect generation, degradation, and permanent damage in Sb_2O_3 gate dielectrics. Therefore, it is important to understand the mechanisms of degradation and dielectric breakdown to inhibit them before the material can be used in practical applications.

Transmission electron microscopy (TEM) imaging and spectroscopy techniques are well suited for understanding gate dielectric properties on the nanoscale. TEM techniques have been extensively used in prior works to directly probe the material structure, degradation, and breakdown in gate dielectrics.[13−15] In situ TEM electrical biasing allows for direct observation of defect generation and dielectric breakdown under electrical stress, providing fundamental insights into the mechanisms. In this work, we apply in situ TEM biasing and energy-dispersive X-ray spectroscopy (EDXS) to probe defect generation and dielectric breakdown in Sb_2O_3. We show that the mechanisms governing soft dielectric breakdown and hard dielectric breakdown in Sb_2O_3 are different. Soft dielectric breakdown is due to the generation of new oxygen vacancies and gradual migration of metallic species from contact into Sb_2O_3. In contrast, hard dielectric breakdown is catastrophic, caused by joule heating, leading to a significant temperature increase in Sb_2O_3. This increased temperature causes a complete redistribution of oxygen, leaving the Sb_2O_3 film. This results in the formation of Sb-enriched nanocrystals.

RESULTS AND DISCUSSION

Device-Level Measurements. The capacitor test structures are fabricated to measure the electrical behavior of Sb_2O_3 devices. The test structure consists of Au/Cu/Sb_2O_3/n^{++}Si, as shown in the inset of Figure 1a. The details of the device fabrication are provided in the Experimental Section. The area of the capacitors is 100 μm × 100 μm. First, the I−V breakdown measurements are carried out to determine the

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breakdown voltage of Sb_2O_3. A ramp voltage stress is used for the breakdown measurements, where the voltage is increased until a current compliance of ∼1 mA is reached. The $I-V$ breakdown curves for the five capacitors are plotted in Figure 1a. The current increases with voltage and is followed by a sudden exponential jump in current at the time of the dielectric breakdown in Sb_2O_3. We define the breakdown voltage as the voltage at which the current reaches a compliance current of ∼1 mA. The mean breakdown voltage measured for the five capacitors is ∼2.4 V (Figure 1a).

Understanding the degradation behavior of Sb_2O_3 when the maximum applied voltage is lower than the breakdown voltage is crucial. This voltage region is pertinent to the actual operating conditions of a FET. The degradation in the Sb_2O_3 capacitor is initiated by applying a cyclic ramp voltage stress. During electrical stress, the applied maximum voltage is ∼70% of the breakdown voltage. The trends in the $I-V$ characteristics for a capacitor subjected to electrical stress are shown in Figure 1b. Here, the capacitor was stressed up to a bias of 1.75 V, and the current was measured as a function of applied bias over successive cycles. The trend shows a gradual and progressive increase in the current with the number of stressing cycles. The tunnel current is extracted at 1.5 V for all of the stressing cycles to quantify the changes in the current as a function of the number of stressing cycles. The results are plotted in Figure 1c. A visual inspection of the current in Figure 1c shows that there is a gradual and linear increase in current up to the first #20 cycles. For the subsequent #20 cycles, the increase in current remains linear but with a higher rate. This is evident by an increase in the slope of the plot between stressing cycles 21 and 40 in Figure 1c. From cycle 41, the rate of increase in current further intensifies, and random fluctuations in the current are observed as stress continues.

The ramp voltage stress can be complemented with TDDB measurements, providing insights into the defect generation and the complete degradation behavior of the dielectric over time.[16] The TDDB data for one such capacitor subjected to an electrical bias of 1.75 V are shown in Figure 1d. During TDDB measurements, a constant voltage is applied, and the leakage current is monitored over time. The stressing voltage in TDDB is arbitrary, generally kept at ∼50−70% of the breakdown voltage. We find that the current decreases over the first few seconds of the measurements. This reduction is up to ∼60% of the initial current, characteristic of charge trapping in the Sb_2O_3 films. This drop is often associated with filling charge traps at the pre-existing defects in the dielectric. These defects in Sb_2O_3 are primarily oxygen vacancy defects, as discussed below. Filling charge traps at these vacancy defects increases the local potential, reducing the tunnel current. Following charge trapping, the tunnel current increases over time due to the generation of new defects, referred to as stress induced leakage current (SILC).[17] A sudden rise in current at ∼20 s indicates a soft dielectric breakdown in Sb_2O_3. The current rapidly increases for the remaining duration of the measurements. There is a notable increase in the tunnel current fluctuations following the soft dielectric breakdown. This is evident when the current is plotted on a linear scale as a function of time, as shown in the inset of Figure 1d.

In Situ TEM Biasing Measurements. While device-level measurements are useful for understanding the electrical behavior and extensive reliability characterizations, they do not provide insights into the physical mechanisms governing degradation and breakdown in Sb_2O_3. A challenge in large area devices is finding the breakdown spot, as dielectric breakdown is a stochastic phenomenon extending over a spatial dimension of 10−100 nm. Additionally, the spatial location is randomly distributed within the device. Pinpointing the exact location of the dielectric breakdown in both device and TEM measurements is challenging, especially after a soft breakdown when no obvious structural defects form. The absence of obvious indications makes it extremely difficult to reliably identify the soft dielectric breakdown location in a large area ex situ device test structure. Using a scaled nanocapacitor test structure for both ex situ and in situ TEM biasing measurements is advantageous for the breakdown spots, as the complete device structure remains preserved after dielectric breakdown.[6,18]

We use in situ electrical biasing in TEM to understand the nature of dielectric breakdown in Sb_2O_3. The schematic of the nanocapacitor test structures and the connection for electrical biasing is shown in Figure 2a. The test structure is prepared

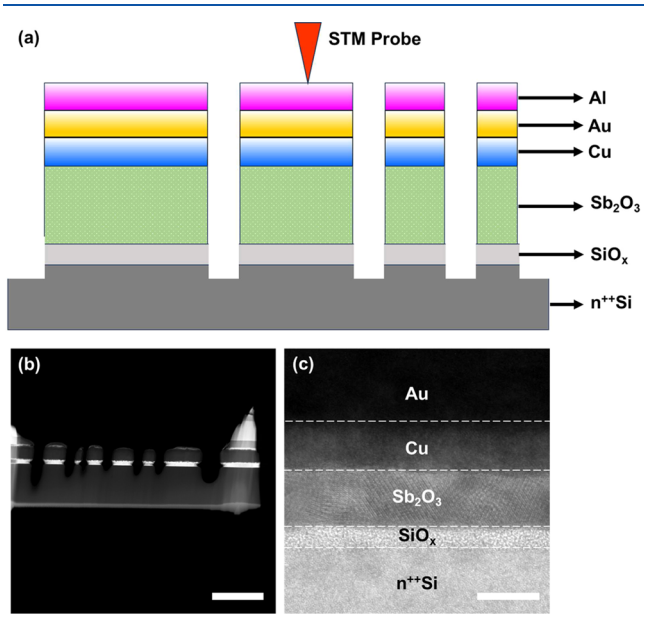

Figure 2. Device for in situ TEM biasing: (a) Schematic showing the cross section of the capacitor test structure used for the in situ TEM biasing to probe dielectric breakdown in Sb_2O_3. Here, each nanopillar is a capacitor and can be individually contacted using a movable and piezo-controlled STM tip inside a TEM. (b) HAADF STEM image showing an overview of the prepared test structure. (c) TEM image showing a cross section of the prepared capacitor. The thickness of Sb_2O_3 varies between 7.5 and 8.0 nm, and the film is polycrystalline. Scale bar in panels (b) and (c) are 2 μm and 10 nm, respectively.

using a focused ion beam scanning electron microscope (FIB-SEM). A high-angle annular dark field (HAADF) scanning TEM (STEM) image of the fabricated device for the in situ TEM biasing measurement is shown in Figure 2b. This test structure allows the preparation of multiple nanocapacitors in a single TEM lamella.[18]

Here, the electrical biasing is performed using a specialized scanning transmission microscope (STM)−TEM holder, which integrates inertial and piezo movement mechanisms for manipulating across a wide dynamic range, from millimeter to Ångström scales, within a TEM.[19] The holder enables individual contact with the nanocapacitors. During measurements, an electrical bias is applied to the top contact via the STM tip. The silicon substrate acts as a global bottom contact

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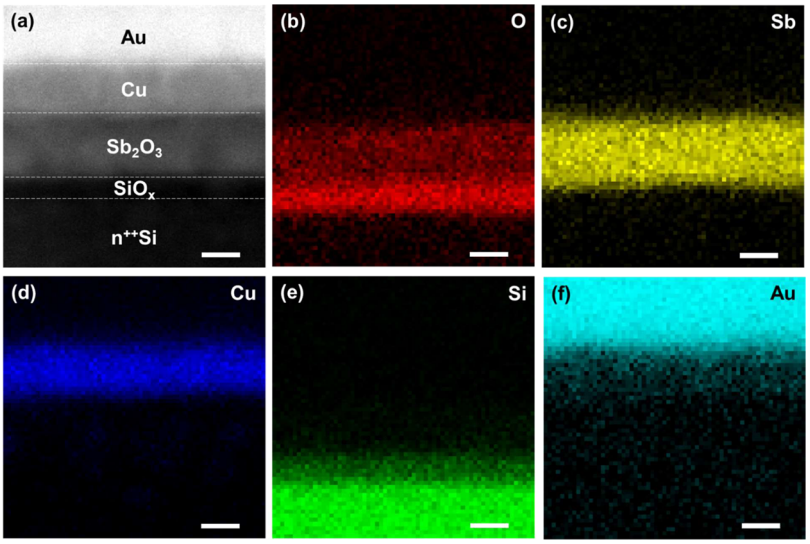

Figure 3. As-prepared device prior to in situ TEM biasing: (a) STEM image showing the cross section of the capacitor where EDXS measurements have been acquired. The capacitor structure consists of thin films of Sb_2O_3 dielectric, Cu as the contact, and Au as the capping layer. EDXS maps of the area in panel (a) showing the spatial distribution of (b) O, (c) Sb, (d) Cu, (e) Si, and (f) Au. Scale bar in panels (a–f) is 5 nm.

and is electrically grounded. The STM tips used in the experiments are prepared in-house through wet-chemical etching and subsequent FIB milling of tungsten wires. Complete details of the sample fabrication, STM tip preparation, and the in situ TEM electrical biasing procedure are provided in the Experimental Section.

As-Prepared Sb_2O_3 Nanocapacitor. Before applying electrical biasing, we acquired a high-resolution TEM image of the device's cross section, as depicted in Figure 2c, to visualize the Sb_2O_3 layer, metal-oxide interfaces, and contacts. The Sb_2O_3 film is continuous and polycrystalline, with a thickness of ~7.5–8.0 nm. An interfacial SiO_x layer of 3.3 nm thickness exists between Sb_2O_3 and the Si substrate. The top Cu contact has a thickness of ~10 nm. To prevent the oxidation of Cu and enhance electrical contact during the in situ TEM biasing, the Cu contact is capped with Au and Al layers.

The high-resolution TEM (HRTEM) images were used to determine the crystal structure of the Sb_2O_3 film, and the details are provided in Note-S1 (Supporting Information) and Figure S4. Although the interplane spacings in different regions of the Sb_2O_3 film match some of the interplane spacings of the cubic and the orthorhombic phases of Sb_2O_3, there are also interplane distances that do not match those in either phase. This is in agreement with the EDXS analysis, which shows that the Sb_2O_3 films are nonstoichiometric, as discussed below.

A comprehensive elemental analysis of the as-prepared in situ devices was conducted using EDXS, as illustrated in Figure 3. Figure 3a displays a STEM image highlighting the Sb_2O_3 layer, contacts, and the Si substrate. The elemental maps for O, Sb, Cu, Si, and Au from the same area of the device, in Figure 3a, are plotted in Figure 3b–f. The elemental distribution across the metal and dielectric layers of the capacitors aligns with the intended device structure. Both TEM imaging in Figure 2c and EDXS analysis in Figure 3 indicate that the Cu contact remains unreactive with the Sb_2O_3. This discovery is significant because the contacts can significantly influence oxygen redistribution in the Sb_2O_3 film.[10] At the nanometer scale, the Sb_2O_3/Cu interfaces appear sharp, with no observable chemical reactions between the Cu contact and the Sb_2O_3 film. The line profile showing the elemental distribution of Si, O, Sb, Cu, and Au is shown in Figure 4.

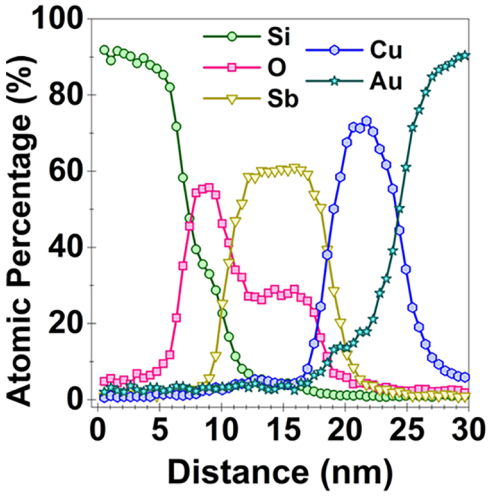

Figure 4. EDXS line profile from Figure 3 showing the elemental distribution of Si, O, Sb, Cu, and Au. The plot is averaged across the complete area along the horizonal to show the representative trends. The elemental ratio between O and Sb is ~0.45. An Au signal can be observed in the Cu layer due to migration of Au through the grain boundaries of the Cu layer.

The line profile has been horizontally averaged. The EDXS analysis shows that the O/Sb ratio in the bulk of the film is ~0.45 (compared to a ratio of 1.5 in an ideal stoichiometric Sb_2O_3 film). This implies that the as-deposited Sb_2O_3 film is nonstoichiometric and oxygen-deficient.

Soft Dielectric Breakdown in Sb_2O_3. In this section, we present the results of the soft dielectric breakdown of Sb_2O_3. A ramp voltage stress is used to initiate the breakdown, and the current compliance is controlled using an external resistor. The resistor restricts the maximum current that can flow at the instant of breakdown. It has a resistance of ~10 MΩ, permitting a maximum current of ~100 nA through the device. The STEM image of the overview of the nanocapacitor

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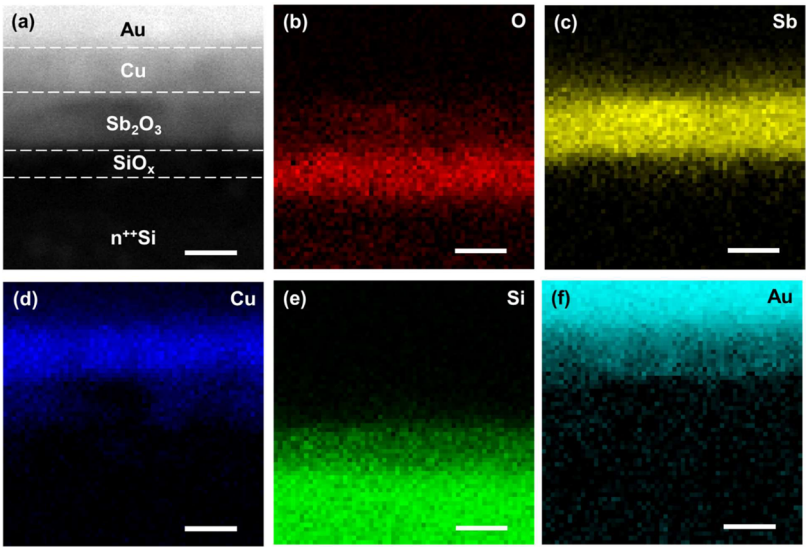

Figure 5. After Soft Breakdown in Sb_2O_3: (a) High-resolution STEM image showing Sb_2O_3, Cu, Au, and n^{+2}Si substrate in the capacitor. (c) EDXS map showing the spatial distribution of (b) O, (c) Sb, (d) Cu, (e) Si, and (f) Au. The migration of Cu into the Sb_2O_3 layer can be observed in the Cu elemental distribution map. The scale bar in panels (a–f) is 5 nm.

subjected to the soft breakdown is shown in Figure S1. The device remains physically intact, showing no structural damage after soft dielectric breakdown.

A high-resolution HAADF STEM image highlighting the Sb_2O_3 and Cu contact is shown in Figure 5a. The EDXS maps showing the elemental distribution of O, Sb, Cu, Si, and Au are plotted in Figure 5b–f. There are two distinct observations. (a) The oxygen signal in the Sb_2O_3 layer is weak (O/Sb ratio is ∼0.24) in Figure 5b, in contrast to as-prepared devices (O/Sb ratio is ∼0.45) in Figure 3b. (b) Cu is present in the Sb_2O_3 bulk after the soft breakdown, as evident in Figure 5d. A line profile showing the atomic percentage distribution of all of the elements in the device after the soft breakdown is plotted in Figure 6. The line profile, averaged across the horizontal area, portrays the representative trends. These findings suggest a generation of additional oxygen vacancies in Sb_2O_3 under electrical stress.

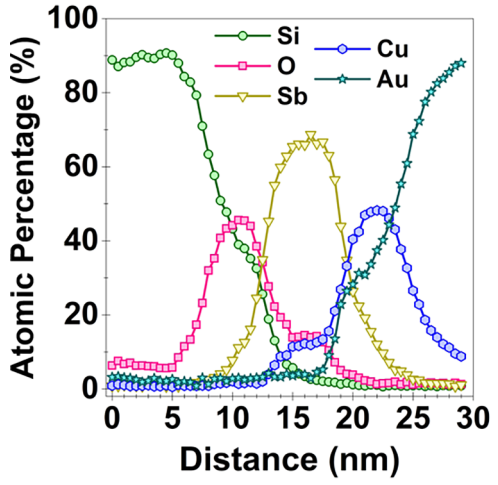

Figure 6. Line profile showing the percentage atomic distribution of different elements after soft dielectric breakdown from the area shown in Figure 5. The data show that 10–12 atom % of Cu is present in the Sb_2O_3 layer.

In addition, migration of Cu in the Sb_2O_3 film is also observed. The EDXS analysis of the Cu map is replotted in Figure S2b, and a line profile showing the distribution of Cu in the Sb_2O_3 layer, the Cu contact, and the Si substrate is plotted in Figure S2c. The line profile showing the distribution of Cu is also plotted in the Si substrate for reference. The analysis indicates the presence of up to ∼20 atom % of Cu within the Sb_2O_3 film after the soft breakdown. The increase in the Cu concentration in Sb_2O_3 is compensated by the corresponding decrease in the concentration of Cu within the contact. The line profile of Cu in Figure S2c shows that the redistribution of Cu in the Sb_2O_3 film is spatially nonuniform. Additionally, a significant diffusion of Au into the Cu layer took place during the soft breakdown (see Figure 5). Au can diffuse into Cu through structural defects such as grain boundaries.[20,21] Furthermore, the electron beam broadening effects can further enhance the Au signal in the Cu layer.[22]

Hard Dielectric Breakdown in Sb_2O_3. In this section, we present the results of hard dielectric breakdown in Sb_2O_3. A ramp voltage stress is used to initiate the breakdown, and the maximum current flow is limited to ∼1 mA using an external resistor of ∼1 kΩ placed in series with the capacitor. A HAADF STEM image providing an overview of the device after the breakdown is shown in Figure 7a. The morphology of the thin film capping layer of Au has changed from a continuous thin film to a polycrystalline one with high surface roughness, as highlighted in Figure 7a. Substantial changes are observed in the morphology of the Sb_2O_3 layer after hard breakdown (see Figure 7b,7c). Analysis reveals a transformation of the Sb_2O_3 film into Sb nanocrystals, indicated by arrows in Figure 7b,7c. These Sb nanocrystals exhibit varying dimensions, with typical lateral dimensions ranging from ∼20 to 50 nm and heights between ∼10 and 15 nm.

The EDXS maps of the device showing the distribution of Au, Al, and Si are plotted in Figure 7d–f. The EDXS maps of Al and Si plotted in Figure 7e,7f show that there is a migration of Al into the silicon substrate located to the right of the capacitor. Additionally, a small amount of Cu is also present, along with Al, in this region of the silicon substrate (not shown here for the sake of brevity). The migration of Al and Cu into

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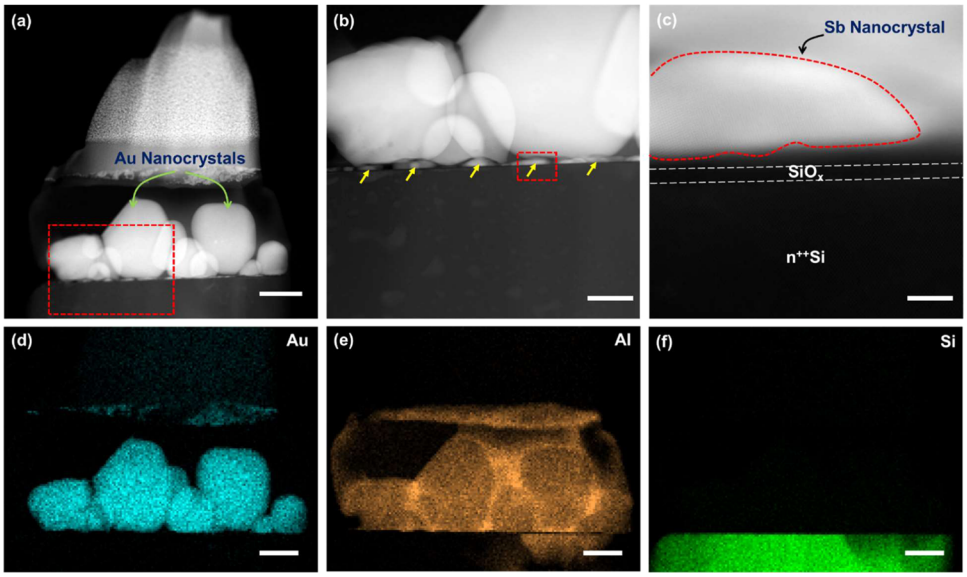

Figure 7. After hard breakdown in Sb_2O_3: (a) STEM image showing the overview of the capacitor after the hard breakdown. The Au layer has melted and created nanocrystals, as marked by arrows. (b) Zoom-in STEM image from the marked region (in red) in panel (a) showing the presence of Sb nanocrystals, marked by arrows. (c) High-resolution STEM image of one of the nanocrystals from the marked region in panel (b) (in red) is shown. (d–f) EDXS maps showing the overall spatial distribution of Au, Al, and Si in the device after the hard breakdown. Scale bars in panels (a–c) are 250, 100, and 5 nm, respectively. Scale bar in panels (d–f) is 200 nm.

the silicon substrate results in a corresponding reduction in Si content in the EDXS map (see Figure 7f).

A representative STEM HAADF image of the resulting Sb nanocrystals formed after the breakdown is shown in Figure 8. The EDXS maps showing the relative distribution of O, Sb, Cu, and Al are plotted in Figure 8b–e, respectively. An analysis showing the percentage atomic distribution of all of the elements is provided in Figure S3. A line profile showing the percentage atomic composition across the nanocrystal marked by the dotted region in Figure 8a is plotted in Figure 9. The

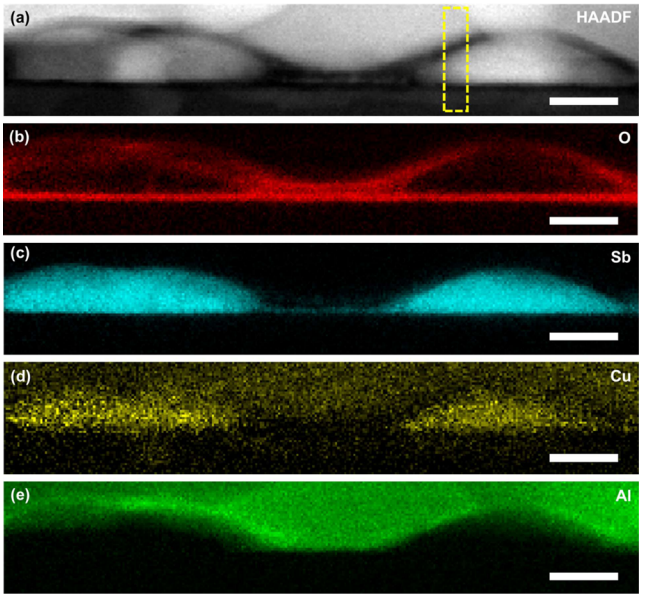

Figure 8. Chemical analysis after the hard breakdown of Sb_2O_3: (a) STEM image showing two of the Sb nanocrystals formed after breakdown. EDXS maps showing the spatial elemental distribution of (b) O, (c) Sb, (d) Cu, and (e) Al. The nanocrystals are metallic. Scale bar in panels (a–e) is 25 nm.

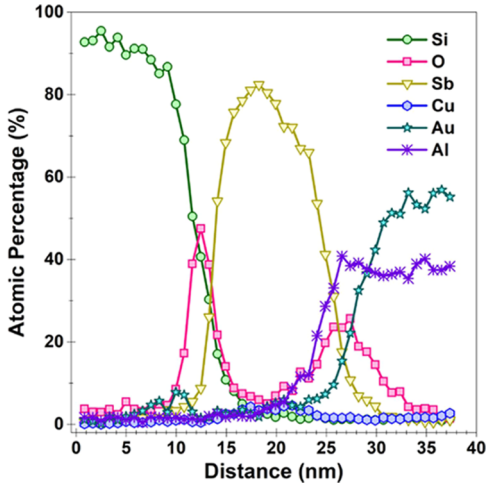

Figure 9. EDXS line profile of the area highlighted by the dashed rectangle in Figure 8a shows the redistribution of different elements after hard breakdown. Sb nanocrystals are formed.

observations indicate that the nanocrystal formed in the Sb_2O_3 layer after the breakdown consists of metallic Sb. A small amount of Cu is also present in these nanocrystals. The oxygen is completely redistributed, and there is no remaining Sb_2O_3. Furthermore, the oxygen has migrated to the upper surface of the nanocrystal, where it has reacted with Al, forming a nonstoichiometric Al_xO_y (with $x/y \sim 0.5$).

DISCUSSION

Performance of the Sb_2O_3 Films as a Gate Dielectric. The TDDB measurements reveal distinct stages of degradation in the Sb_2O_3 dielectric, including charge trapping, soft breakdown, and progressive degradation. These general trends of degradation in Sb_2O_3 are similar to those reported for other high-κ gate dielectrics. The average breakdown voltage measured for an ~8 nm thick Sb_2O_3 film is 2.4 V when Cu

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is used as a contact. The contribution of the interfacial layer to the estimation of the breakdown voltage of Sb_2O_3 is estimated using the total dielectric thickness ($t_{ox} = t_{SiO_2} + t_{Sb_2O_3}$) for the measurement of the breakdown field. The breakdown field (E_{bd}) is obtained by dividing the breakdown voltage (V_{BD}) by the t_{ox}. This represents a worst-case scenario and provides a lower bound on the estimates of the breakdown field of Sb_2O_3 as interfacial oxides are known to be defective.[10] The breakdown field strength measured for Cu is ~2.2 MV/cm compared to ~2.7 MV/cm when Au and InAu are used as contacts.[9] Directly comparing the impact of contact on the breakdown voltage is challenging due to the influence of contact material on the stoichiometry of the Sb_2O_3. Nonetheless, it can be inferred that the decrease in the breakdown field strength of Sb_2O_3 with Cu contacts correlates with a relative increase in the oxygen vacancy concentration.

We note that the breakdown field strength of Sb_2O_3 is about ~4−5 times lower than expected from the thermochemical model of dielectric breakdown.[23] The model predicts that the breakdown field strength should decrease as the dielectric constant increases. It is important to note that the model assumes stoichiometric Sb_2O_3, which is devoid of defects. Given that the dielectric constant of Sb_2O_3 is ~11.5, a breakdown field strength of ~10 MV/cm is projected. The observed oxygen deficiency of the as-grown Sb_2O_3, indicated by an O/Sb ratio of 0.45 by using EDXS, is expected to result in a lower dielectric constant and provides an explanation for a lower breakdown field.

It is speculated that oxygen vacancy defects are primarily incorporated into the Sb_2O_3 film during film deposition. These oxygen vacancy defects cause charge trapping, as evidenced by the TDDB measurements and also lead to random telegraph noise.[10] This highlights the importance of maintaining the stoichiometry of Sb_2O_3 during growth to enhance the breakdown field.

Mechanism of Soft and Hard Dielectric Breakdown in Sb_2O_3. The cyclic stressing of the Sb_2O_3 capacitors reveals a gradual and linear increase in the leakage current (see Figure 1b) over time, eventually leading to soft dielectric breakdown. Insights about the mechanism of the soft breakdown are obtained from the in situ TEM biasing measurements, which indicate the formation of additional oxygen vacancy defects in the Sb_2O_3 film after soft breakdown. The ratio of O/Sb decreases from ~0.45 in the unstressed Sb_2O_3 devices to ~0.24 after the soft breakdown.

In addition, migration of Cu into the Sb_2O_3 film is also observed after soft breakdown. The spatial distribution of Cu in the Sb_2O_3 film is nonuniform, and the EDXS data indicate the formation of Cu-based multiple nanoconduction filaments through the dielectric, as shown in Figure 10a. These conduction filaments extend from the Cu contact to the Si substrate. The width of the Cu conduction filaments, estimated from the EDXS mapping in Figure S2, is around ~5−7 nm. This study and prior works on gate dielectrics have shown that the role of the electrode material is important for the mechanism of dielectric breakdown. In the case of electrodes such as Cu and Ag, it is favorable to form metallic nanoconduction filaments during the soft breakdown.[6,24] In the case of inert electrodes such as Pt and Au, it is possible that the breakdown path could be formed by aggregation of oxygen vacancies.[25] The migration pathways for Cu in the Sb_2O_3 film require further evaluation using *ab initio* calculations. It would also be important to investigate the role of the pre-existing oxygen vacancies in the dielectric breakdown.

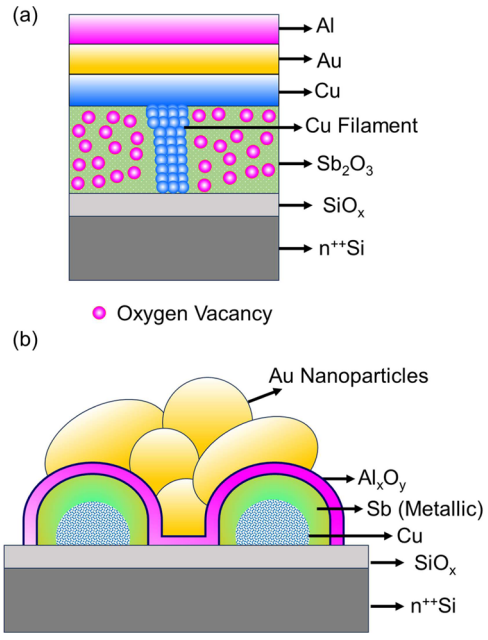

Figure 10. Cartoon showing the mechanisms of dielectric breakdown in Sb_2O_3. (a) Soft breakdown leads to the generation of the additional oxygen vacancies in Sb_2O_3 and the formation of Cu conduction nanofilament. (b) Hard breakdown changes the morphology of the Sb_2O_3 film and the formation of Sb-enriched nanocrystals.

The in situ TEM biasing shows that the hard breakdown in Sb_2O_3 is catastrophic, completely disrupting the device structure. The hard breakdown changes the morphology of the Sb_2O_3 layer, leading to a complete redistribution of oxygen in the film. Sb-enriched metallic nanocrystals are formed (Figure 10b). The results also show that the oxygen in the Sb_2O_3 layer migrates to the top Al contact, forming a continuous ~3−5 nm thick Al_xO_y layer, which acts as a barrier coating on the top of the Sb nanocrystals.

These structural changes due to the hard dielectric breakdown in Sb_2O_3 are completely different from those of the conventional gate dielectrics. The catastrophic damage of the device and the restructuring of the Sb_2O_3 layer suggest that temperature effects are dominant. A high current flowing through the nanoconduction filaments in the device could dissipate a significant amount of heat, and this could increase the temperature in the Sb_2O_3 layer. This increase in temperature leads to a change in the microstructure of the Sb_2O_3 film, resulting in the formation of Sb nanocrystals. This formation of the Sb nanocrystals also provides an indirect estimate of the temperature experienced by the device during the breakdown. The analysis of the phase diagram of Sb_2O_3 suggests that the formation of Sb is favored above a temperature of ~550 °C at which Sb_2O_3 transforms into a solid metallic Sb phase.[26]

CONCLUSIONS

In this work, we study the breakdown mechanisms of antimony trioxide (Sb_2O_3) films, correlating the device properties with the results from in situ electrical biasing measurements in a transmission electron microscope (TEM). Various stages of dielectric degradation, including charge trapping, stress-induced leakage current, and the breakdown, are identifiable

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in the device measurements. We show that the as-grown Sb_2O_3 films are nonstoichiometric and contain a high concentration of pre-existing oxygen vacancies. The in situ TEM measurements show that the soft dielectric breakdown in Sb_2O_3 leads to the generation of additional oxygen vacancies and the migration of Cu from the contact into Sb_2O_3. The hard dielectric breakdown is catastrophic, leading to the complete removal of oxygen from the Sb_2O_3 film and the formation of Sb nanocrystals.

EXPERIMENTAL SECTION

Sb_2O_3 Thin Film Deposition. The Sb_2O_3 deposition is carried out on a 3-inch n^{++} Si wafer (ρ < 0.025 Ωcm). The wafer is precleaned in IPA and acetone. The wafer is dipped in hydrofluoric acid for 30 s to remove native oxide. The Sb_2O_3 film is deposited using standard thermal evaporation in a high vacuum deposition chamber, as described in earlier works. A low deposition rate of ∼6 Å/s is used to obtain smooth films.

Capacitor Fabrication. A small piece of 2 cm × 2 cm is diced from the Sb_2O_3 deposited Si wafer. Photolithography is carried out using a laser writer (Model: MLA 150, Heidelberg Instruments). The pattern development is carried out by dipping the sample in MIBK:IPA for 40 s, followed by a gentle clean in DI water. A bilayer Cu (∼10 nm)/Au (∼30 nm) film was then deposited in sequence using Kurt J. Lesker physical vapor deposition system under high vacuum conditions at room temperature. Liftoff is carried out by soaking the sample overnight in resist remover 1165, followed by a gentle cleaning in acetone, IPA, and DI water.

Electrical Measurements. Electrical measurements are carried out using an Agilent B1400 semiconductor parameter analyzer, which is connected to a probe station. The probe station is equipped with four independent source measurement units, and the base noise measured for the current is ∼1 pA. Bias is applied to the top Cu contact, and the n^{++}Si substrate is electrically grounded during the measurements. All of the measurements are carried out at room temperature. For ramp voltage stress measurements, a ramp rate of ∼0.4 V/s is used, and for TDDB measurements, a sampling rate of ∼500 points/s is used.

Preparation of Device for In Situ Biasing in TEM. A small piece of 1 × 1 cm^2 of sample is diced from the Sb_2O_3 deposited Si wafer, and a bilayer film of Cu and Au is deposited using Kurt J. Lesker physical vapor deposition. An additional ∼700 nm thick Al layer is deposited using sputtering and then coated with ∼50 nm of Au to prevent the oxidation of Al. The nanocapacitor test structure for the in situ TEM electrical biasing is prepared using a FEI Versa 3D FIB-SEM microscope. The microscope is equipped with a Pt gas injection source for site selective metal deposition and an Omniprobe to enable lift-out. During sample preparation, a few micrometers thick Pt layer is first deposited using a Ga ion beam. A lift-out is then carried out to prepare 10 μm long and 2 μm wide lamella and glued to a Molybdenum Omniprobe TEM grid. The sample is thinned down to a thickness of 200 nm by progressively reducing the ion current from 1 nA to 100 pA. Trenches are then milled in the lamella to create the nanocapacitor test structure. The final milling is carried out by progressively reducing acceleration voltage from 30 kV to 500 V to remove any amorphous layer from the surface of the lamella.

Preparation of STM Tips. STM tips were prepared from tungsten wires. The tungsten wires used in the experiments were purchased from Goodfellow. The wires have a purity of about ∼99.95% and are 250 μm thick in diameter. About 15−20 mm long tungsten wires were cut and cleaned in acetone, IPA, and DI water. The setup for electrochemical etching is described elsewhere.[27] Briefly, the tungsten wire to be etched is used as an active electrode, and a ring-shaped Pt wire is used as a counter electrode. A part of the tungsten wire of 5 mm is immersed in KOH solution, and the remaining part of the wire is outside in air. The etching takes place at the KOH-air interface, and the part of the wire outside the KOH solution in the air forms the STM tip after the etching. A positive bias of about 15−25 V was applied to the tungsten wires, and the counter Pt ring was electrically grounded during etching. As the etching proceeds, the current gradually decreases as the tungsten wire gradually etches away. When the tungsten wire has completely etched away, the current suddenly drops to zero, and the power supply is manually switched off. The upper part forming the STM tip is collected and thoroughly cleaned in acetone, IPA, and DI water. The STM tips were finally milled in a FIB to mill away any native oxide from the tip of the material to achieve tips with 10−100 nm apex diameter. The tips were inspected in a TEM instrument prior to the measurements and used immediately for the in situ TEM biasing experiments.

Transmission Electron Microscopy. The scanning TEM (STEM) measurements are carried out at 200 kV on a JEOL Mono NEOARM 200F microscope both before and after the electrical biasing of the sample. The instrument is equipped with a monochromator, an imaging and a probe aberration corrector, a Gatan Imaging Filter Continuum HR electron energy loss spectrometer (EELS), and a double silicon drift detector (SDD) for energy-dispersive X-ray spectroscopy (EDXS). The in situ TEM electrical biasing is carried out in a FEI Titan TEM at 300 kV. A single tilt STM-TEM holder from Nanofactory Instruments AB is used for the in situ biasing of the devices. For electrical biasing, a Keithley source meter is externally connected to the in situ TEM holder. An external series resistor of ∼10 MΩ is connected to precisely control the current compliance at the onset of soft dielectric breakdown. For hard breakdown, a series resistor of ∼1 kΩ is used instead. The elemental maps shown in Figures 3, 5, 7, and 8 are the composition maps. The procedure used for the EDXS quantification is described in our previous work.[10]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.4c01818.

EDXS analysis of the soft and hard breakdown and identification of the crystal structure of the as-deposited Sb_2O_3 film (PDF)

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Notes

The authors declare no competing financial interest.

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