Analysis and Design of RF-Input Doherty-Like Circulator Load Modulated Amplifier

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***Abstract* — This paper introduces the design and analysis of an RF-input circulator load-modulated amplifier (CLMA), with Doherty-like operation and efficiency enhancement. The performance of the proposed architecture has been analyzed thoroughly for varying levels of isolation and loss. A detailed design methodology for the RF-input CLMA prototype is provided. To demonstrate the concept's viability, a prototype CLMA employing GaN HEMT transistors and a commercially available surface mount (SMT) circulator is constructed. Experimental results exhibit a peak and back-off output power drain efficiency of 57% and 53%, respectively, with an output power of 42.3 dBm at 3.4 GHz. When tested with a 20-MHz orthogonal frequency division multiplexing (OFDM) signal, characterized by a peak-to-average power ratio (PAPR) of 7 dB, the prototype circuit exhibits an average efficiency of 51%, with an adjacent channel leakage ratio (ACLR) better than -51.6 dBc after applying digital pre-distortion (DPD). To the best of our knowledge, this is the first RF-input Doherty-like CLMA with a SMT circulator.**

***Keywords* — Circulator, energy efficiency, gallium nitride (GaN), load modulation, non-reciprocal, power amplifier (PA), Doherty operation, wideband.**

I. Introduction

Modern wireless communication systems demand spectrally efficient modulation schemes to achieve elevated data throughput, leading to the emergence of communication signals characterized by substantial peak-to-average power ratio (PAPR) values. To enhance power amplifier (PA) efficiency, particularly when operating at significantly backed-off output power levels, active load-modulated PA architectures have gained popularity. In recent years, several innovative active load-modulated PA architectures have emerged, including the load-modulated balanced amplifier (LMBA) [1], [2], [3], [4], the distributed efficient power amplifier (DEPA) [5], [6], and the circulator load-modulated amplifier (CLMA) [7], [8].

The CLMA architecture leverages two active devices and a non-reciprocal output combiner. In this configuration, the auxiliary amplifier injects power into the output of the main amplifier via the circulator, effectively modulating its load impedance. This modulation ensures the maintenance of high efficiency at both peak and back-off power conditions. In the prior research [7], [8], the CLMA operated on a dual-input topology, requiring an external control signal with phase tuning for optimal performance. This property makes the architecture less attractive than a Doherty approach [9] with its ability to operate directly on a single radio frequency (RF) input, in a typical class B/C configuration [10].

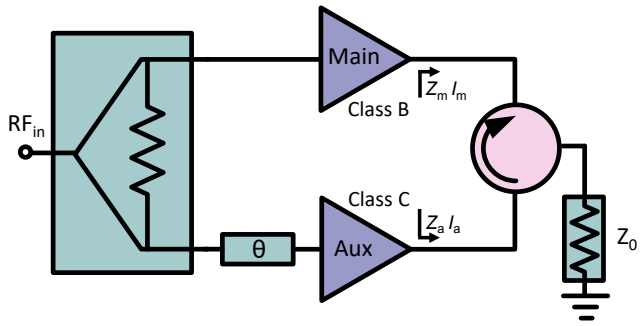

Fig. 1. Block diagram of the RF-input circulator load modulated amplifier.

In this paper, the design and analysis of an RF-input CLMA architecture is demonstrated. We explore the theoretical performance of the CLMA when paired with a circulator, taking into account varying isolation levels and losses. A detailed design methodology for the proposed architecture, incorporating a surface-mount (SMT) circulator, is illustrated. Moreover, experimental results from the fabricated prototype highlight a drain efficiency of 57% at peak and 53% at back-off power levels, operating at 3.4 GHz. The performance of the designed PA underscores the efficacy and potential of our proposed approach.

II. Principle of Operation

Fig. 1 illustrates the RF-input CLMA architecture. Within this setup, the main amplifier operates under a class-B bias. Concurrently, an auxiliary amplifier, biased in class-C mode, is used to inject current into the output of the main amplifier through the circulator-based combiner. This process effectively modulates the load impedance of the main amplifier. Moreover, the phase-adjusting network ensures the necessary phase correlation between the main and auxiliary amplifiers.

As presented in [7], the relationships between voltage and current at the CLMA circulator's three ports can be utilized to determine the load impedance seen by both the main and auxiliary amplifiers as

$$Z_{\mathrm{m}} = Z_0 \left(1 - 2\frac{I_{\mathrm{a}} e^{j\theta}}{I_{\mathrm{m}}}\right) \tag{1}$$

$$Z_{\mathrm{a}} = Z_0. \tag{2}$$

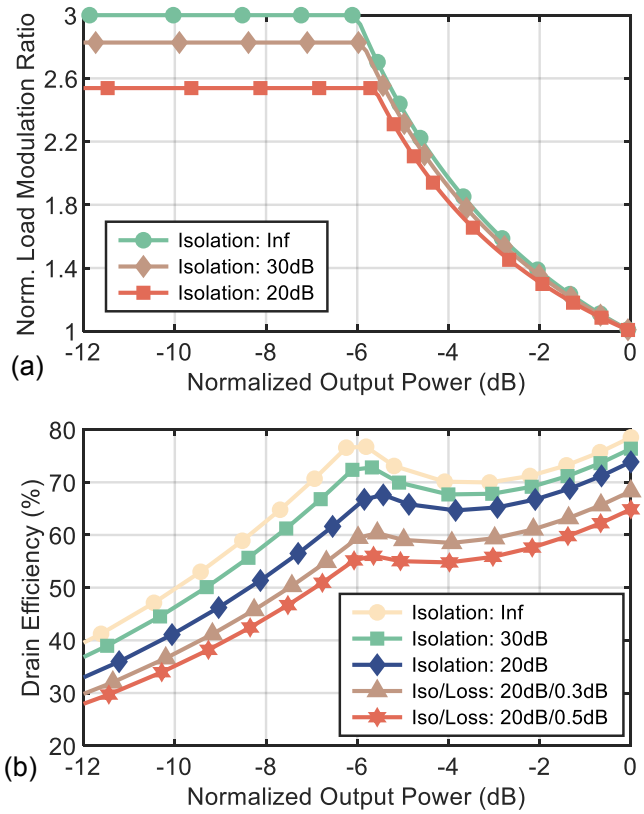

Fig. 2. (a) Normalized main load modulation ratio, and (b) drain efficiency of the RF-input CLMA versus the normalized output power with different circulator isolation and loss.

Equation (1) reveals that by adjusting the magnitude and phase delay of the auxiliary current, the load impedance observed by the main amplifier can be dynamically altered. Considering the inherent non-reciprocal property of the circulator, it ensures that both the powers injected by the main and auxiliary amplifiers are effectively delivered to the load. This observation paves the way for an RF-input CLMA configuration with Doherty-like behavior. Furthermore, for practical implementations, it is beneficial to understand the performance of the RF-input CLMA when deploying non-ideal circulators. In our analysis, the main and auxiliary amplifiers within the CLMA architecture are represented as ideal piece-wise voltage-controlled linear current sources. Their fundamental output currents, I_{m} and I_{a}, are functions of the normalized input drive voltage. It is worth noting that only the fundamental component is factored into the efficiency analysis. All harmonics beyond this are short-circuited, mirroring an ideal class-B operation. Fig. 2(a) illustrates the normalized load modulation ratio of the RF-input CLMA's main amplifier. It is evident that the load modulation process is influenced by the non-ideal isolation of the circulator. This factor compromises the efficiency performance of the RF-input CLMA, as shown in Fig. 2(b). The inherent loss in a practical circulator results in reduced RF power, and further degrades the efficiency. From the five illustrated scenarios, it is clear that when the circulator's isolation level is at 30 dB, the efficiency of the

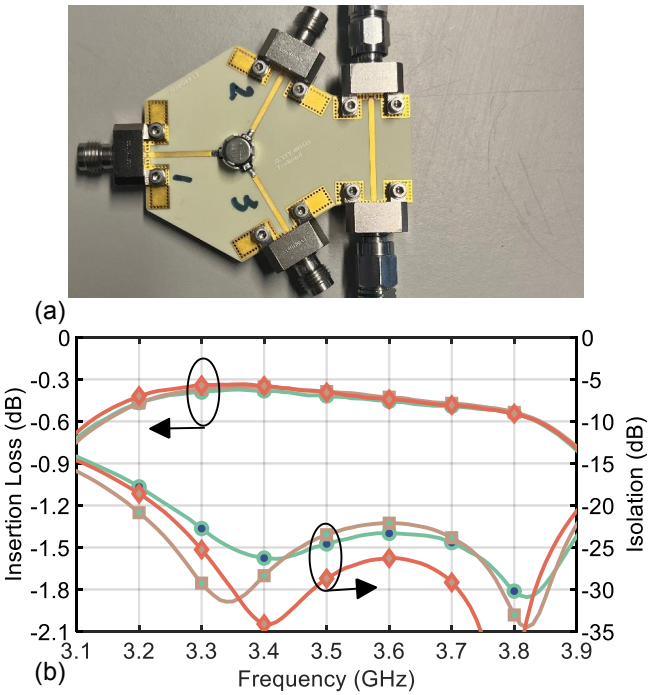

Fig. 3. (a) The fabricated PCB for testing the surface-mount circulator. (b) The measured isolation and insertion loss of the fabricated circulator.

CLMA aligns closely with the peak theoretical efficiency of a class-B operation. However, when this isolation level decreases from 30 dB down to 20 dB, there is an observable drop in efficiency, approximately within the range of 8-10%. Furthermore, this decline in efficiency can escalate to around 20% when the circulator exhibits an isolation of 20 dB coupled with an insertion loss of 0.5 dB.

Building upon the analysis, we can anticipate the influence of circulator isolation and loss on the overall efficiency performance, providing valuable insights before the design phase. In the next section, we will illustrate the design process for an RF-input CLMA prototype with a SMT circulator.

III. Prototype Design

For the construction of the RF-input CLMA prototype, we selected the SMT single-junction circulator from Skyworks (SKYFR-001822) to function as the combiner. To evaluate the circulator's performance, rigorous testing was conducted on a dedicated printed circuit board (PCB), as depicted in Fig. 3(a). After the de-embedding process, which accounted for connector and transmission line effects, we analyzed the insertion loss and isolation characteristics of the circulator, as illustrated in Fig. 3(b). Note that the measurements indicated an insertion loss of 0.3 dB and isolation of 25 dB at 3.4 GHz.

The complete schematic of the RF-input CLMA prototype circuit is depicted in Fig. 4. The designed prototype is implemented on a 20-mil Rogers 4350B substrate. The 10-W packaged gallium nitride (GaN) transistor from Wolfspeed (CGH40010F) was selected to serve as both main and auxiliary amplifiers. The output-matching networks for both amplifiers were designed together with the three-port small-signal

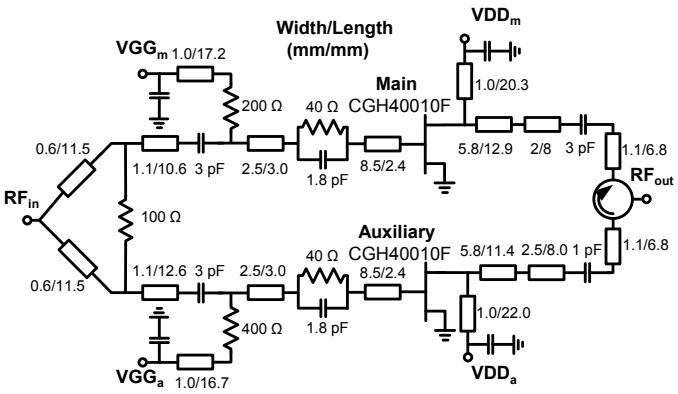

Fig. 4. Circuit schematic of the RF-input CLMA prototype circuit.

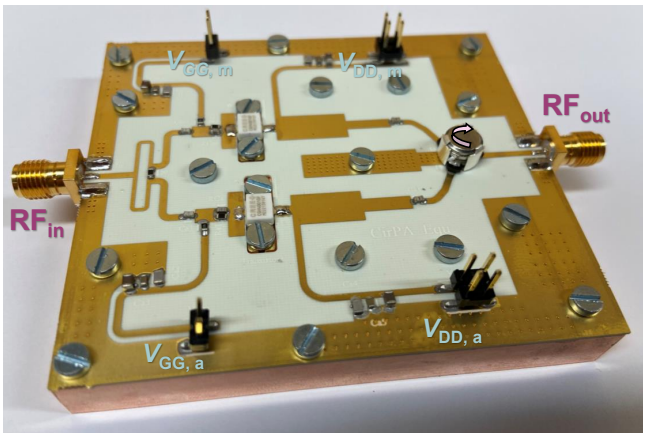

Fig. 5. Photograph of the fabricated RF-input CLMA prototype circuit.

parameters obtained in previous analyses to ensure precise load modulation. To maintain stability and achieve optimal input matching for both amplifiers, a series RC network was employed at the input with a gate bias resistor [11]. We also designed a Wilkinson power divider to supply the required input power and employed a transmission line at the input of the auxiliary amplifier as the phase-adjustment network.

IV. Measurement Results

A photograph of the fabricated RF-input CLMA prototype is shown in Fig. 5. To thoroughly characterize this prototype, we conducted measurements using both continuous-wave (CW) and modulated signal testing approaches. Specifically, the main amplifier had a gate bias of -2.7 V and a quiescent current of 40 mA. The auxiliary amplifier was given a gate bias of -6.5 V. As for the drain bias, the main amplifier was set at 26 V, while the auxiliary amplifier was at 28 V. Throughout the measurements, both CW and modulated signals were generated by a signal generator, and the output power was assessed using a power meter and spectrum analyzer, with the inclusion of a low-pass filter to prevent the entry of harmonics into the power meter.

A. Continuous-Wave Measurement

In Fig. 6, we present the CW measurement results obtained from the prototype circuit. Note that the maximum measured

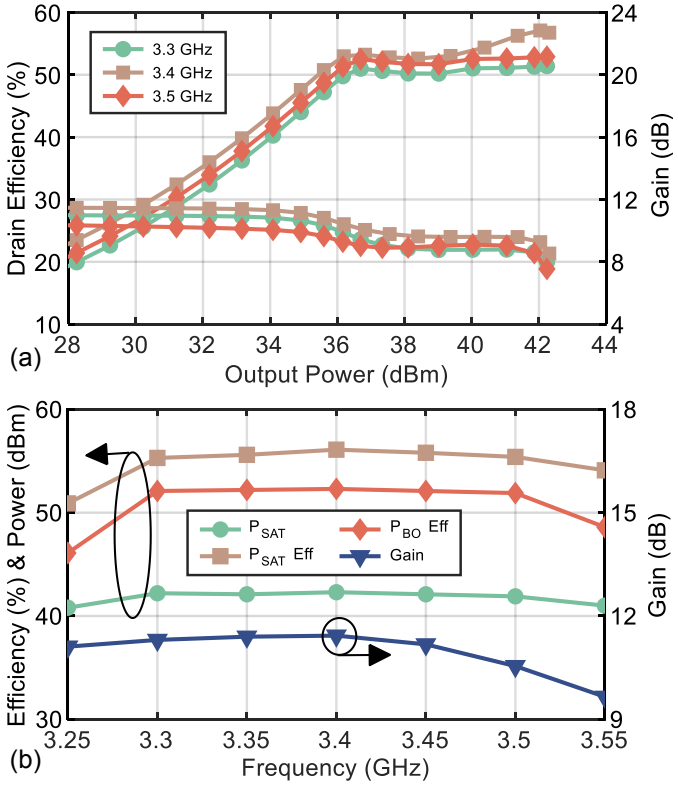

Fig. 6. (a) Measured efficiency and gain of the prototype versus output power. (b) Measured power, efficiency, and gain of the prototype versus frequency.

output power reached 42.3 dBm, with measured drain efficiency and power added efficiency (PAE) values of 53% and 49% at the 6-dB back-off power level, respectively. Fig. 6(a) clearly illustrates the measured efficiency plot versus the output power, showcasing a distinctive Doherty-like behavior. Further insights into the characterization results, encompassing drain efficiency, output power, and gain across various frequencies, are provided in Fig. 6(b). The prototype circuit consistently maintains a drain efficiency and PAE exceeding 47% and 44% at the back-off power levels within the frequency range of 3.25 GHz to 3.55 GHz.

B. Modulated-Signal Measurement

The prototype circuit's performance was also assessed using a 20-MHz orthogonal frequency division multiplexing (OFDM) signal, with a 7 dB peak-to-average power ratio (PAPR). As shown in Fig. 7, we present the measured output spectrum characteristics, contrasting the results with and without the use of digital pre-distortion (DPD) employing the generalized memory polynomial model [12]. The measured average drain efficiency was 51%, accompanied by an average output power of 35.6 dBm. The adjacent channel leakage ratio (ACLR) exhibits substantial improvement, transitioning from -30.8 dBc to -51.6 dBc after applying DPD.

C. Performance Comparison

The performance of the prototype PA is detailed and benchmarked against state-of-the-art load-modulated PAs

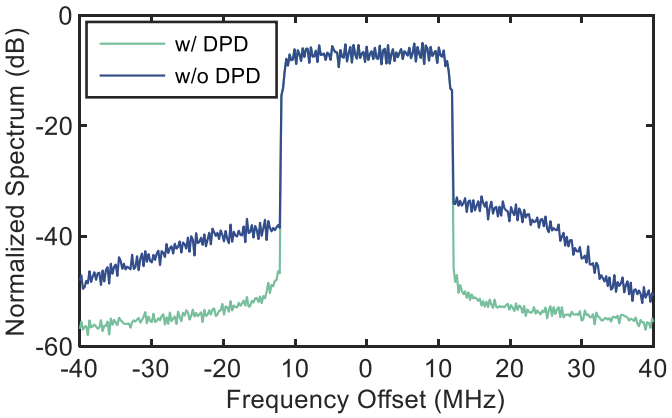

Fig. 7. Normalized power spectral of the prototype circuit when applying a 20-MHz 7-dB PAPR OFDM signal at 3.4 GHz, before and after using DPD.

Table 1. Summary of State-of-the-art Load-modulated PAs.

Ref.	Arch.	f_0 (GHz)	η_{SAT} (%)	$\eta_{BO\text{-}6dB}$ (%)	P_{SAT} (dBm)	ACLR / BW (dBc / MHz)
[13]'22	3-DPA	2.1	69	55	45.3	$-45.7/20$
[14]'22	LMBA	2.4	54	47	44.1	$-48.0/10$
[15]'23	2-DPA	3.2	54	46	43.2	$-49.1/100$
[16]'23	2-DPA	3.6	53	45	45.5	N.A.
T.W.	**CLMA**	**3.4**	**57**	**53**	**42.3**	$\mathbf{-51.6/20}$

η stands for drain efficiency

with back-off efficiency enhancement in Table I. The proposed RF-input CLMA demonstrates excellent efficiency at both saturation and power back-off levels compared to previously published high-efficiency PAs. Moreover, the prototype circuit achieves notable linearity with modulated signals, satisfying the demands of contemporary wireless communication standards.

V. Conclusion

An RF-input Doherty-like CLMA architecture with a SMT circulator has been analyzed and designed. This RF-input CLMA serves as a promising and viable alternative for prospective applications in future wireless infrastructures. A demonstrator circuit has been fabricated, revealing an enhanced 6-dB back-off efficiency of 53% at the frequency of 3.4 GHz. Furthermore, the prototype demonstrates excellent linearity performance with modulated signals after applying DPD, effectively meeting the rigorous demands imposed by modern wireless communication standards.

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