SIS technology development to serve Next Generation receivers for ALMA

GARD
SIS Junction Fabrication Process
to serve
Next Generation Receivers
for ALMA

GARD standard SIS fabrication process status before ALMA Wideband Sensitivity Upgrade

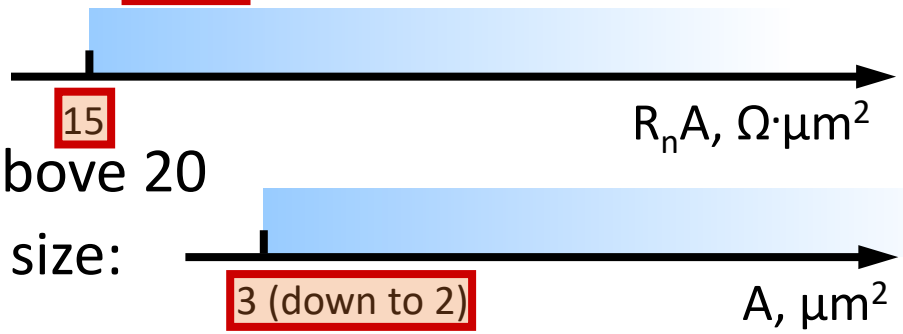
- **Mature process with high yield** (typically above 90%)
- **In-house microfabrication facility** with dedicated Nb-SIS deposition system

- **Track record:**
  - ALMA Band 5 full production
  - APEX SHeFI Band 1, 2, 3 (=ALMA Band 6, 7, 8)
  - APEX SEPIA Band 5
  - Novel Nb-SIS frequency multiplier

GARD SIS fabrication process: limitations and motivation for the upgrade

- **The ALMA 2030 Roadmap:** up to **4x bandwidth** compared to today's receivers
- Demand for stable fabricating process of SIS junctions with:
  - **lower specific capacitance** and **specific resistance**
  - **smaller size**

- **Junctions:** Nb/Al-AlOx/Nb
  - R_nA:
  - R_j/R_n – above 20
  - junction size:



- **Resistors:**

- **Nb tuning circuitry:**
  - stripe width:

GARD SIS process upgrades

- ✓ **AlN-barrier SIS junctions process**
  lower specific capacitance and lower specific resistivity
  supported by ESO study 2017 – 2020

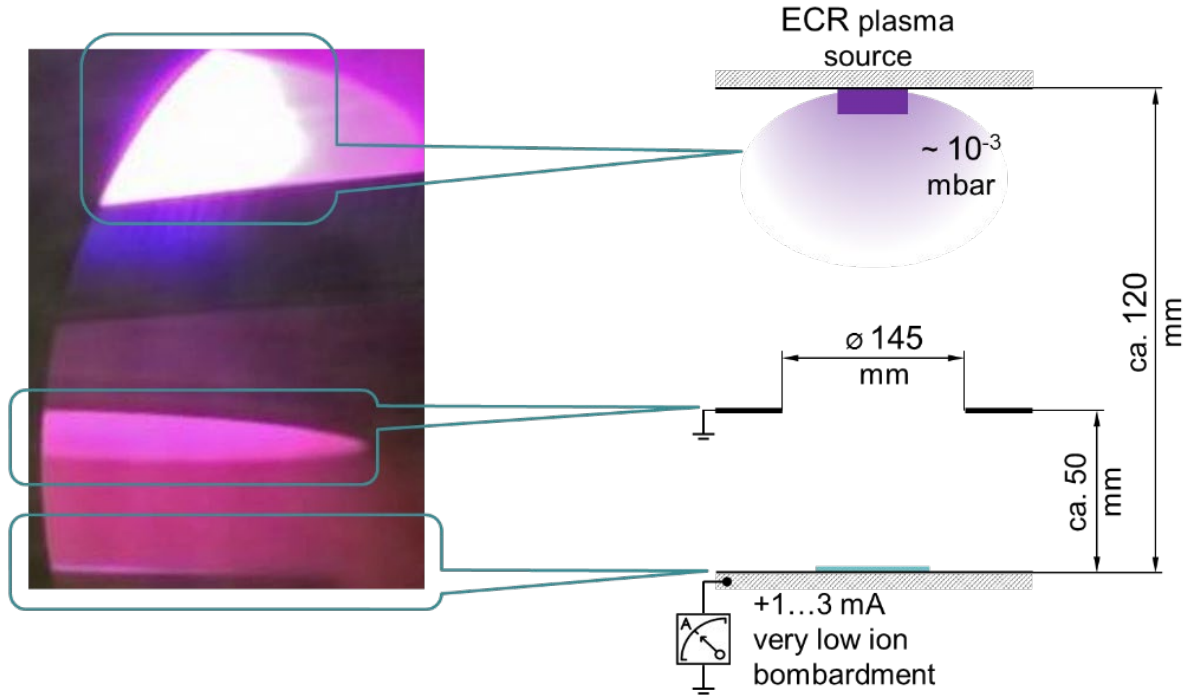
- ✓ **Smaller SIS junctions process**
  ≤ 1 μm^2
  supported by ESO study 2021 – 2024

Strategy:

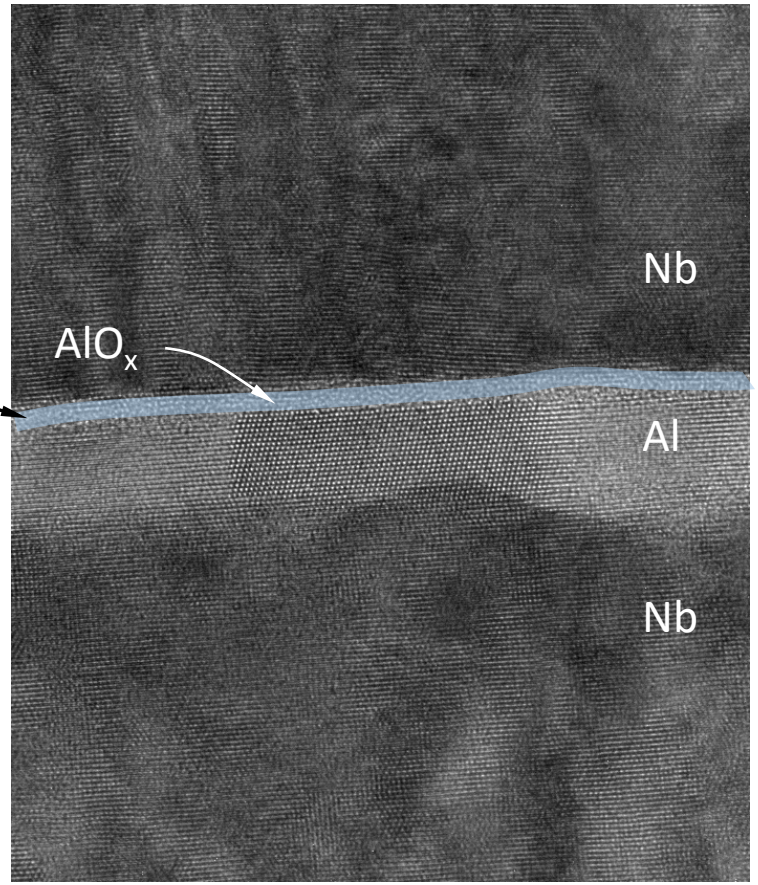
- **Do not change overall process integration** to preserve reliability of the process and its high yield
- **Modify only one key step at a time**:
  - Tunnel barrier plasma nitridation instead of thermal oxidation
  - Direct laser writing instead of contact photo lithography

AlN-tunnel barrier SIS-junctions process

- Standard Nb-SIS process, but with a **plasma nitridation** instead of thermal oxidation

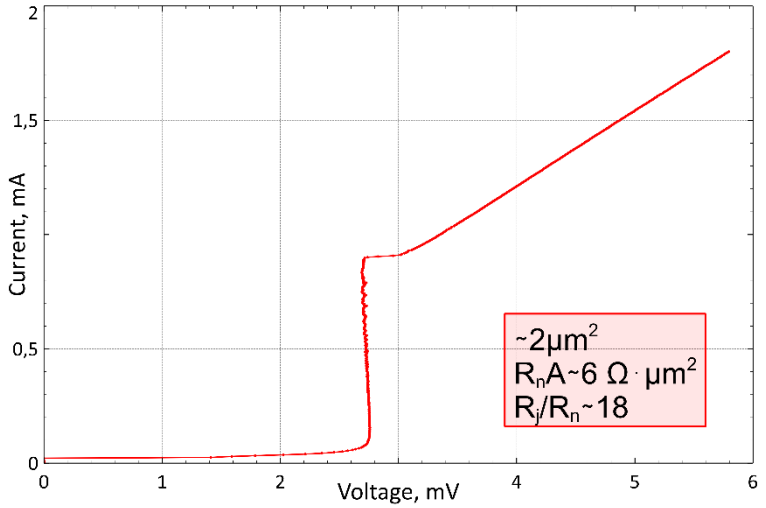


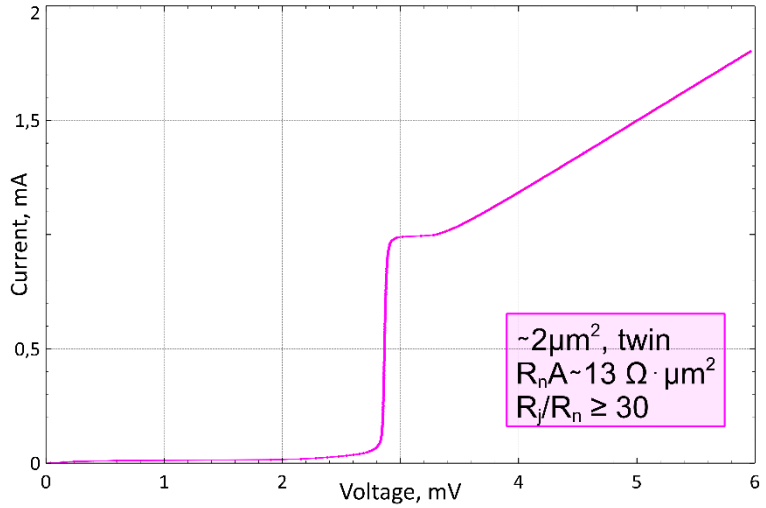
Instead:
AlN

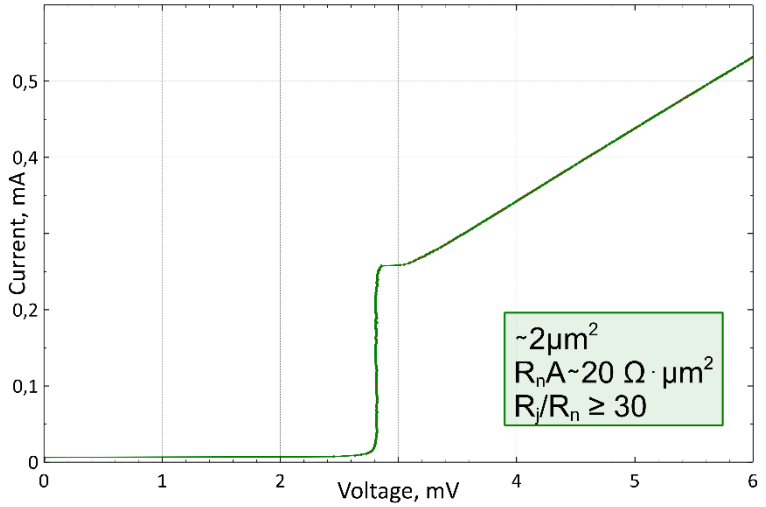


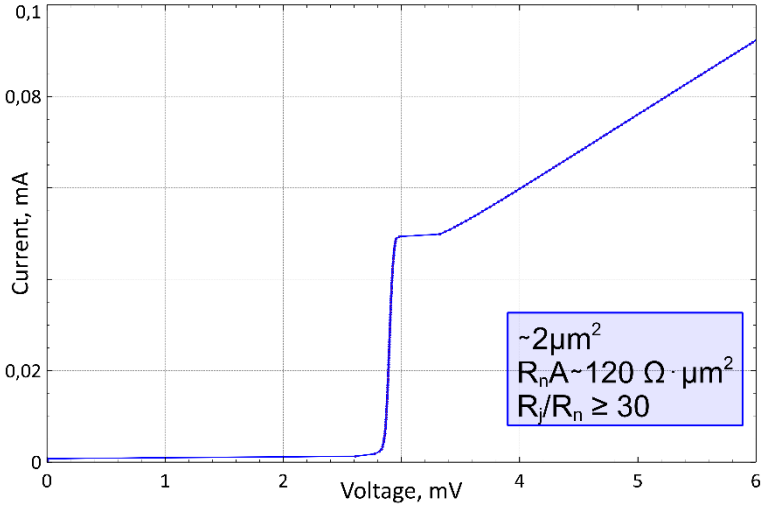
AlN-tunnel barrier SIS-junctions process

- **Stable** Nb/Al-AlN/Nb junctions process had been developed.
- **R_nA** between 5 to 120 Ω·μm^2
- All with low subgap current (**high R_j/R_n** ratio)



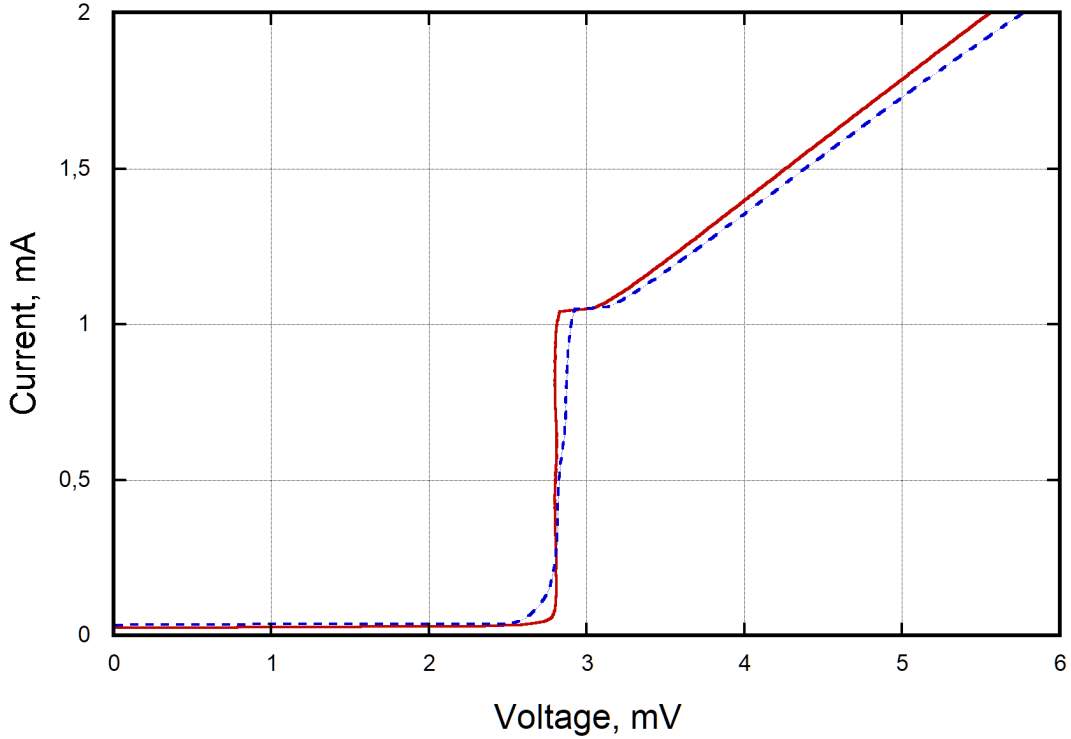






AlN-tunnel barrier SIS-junctions process

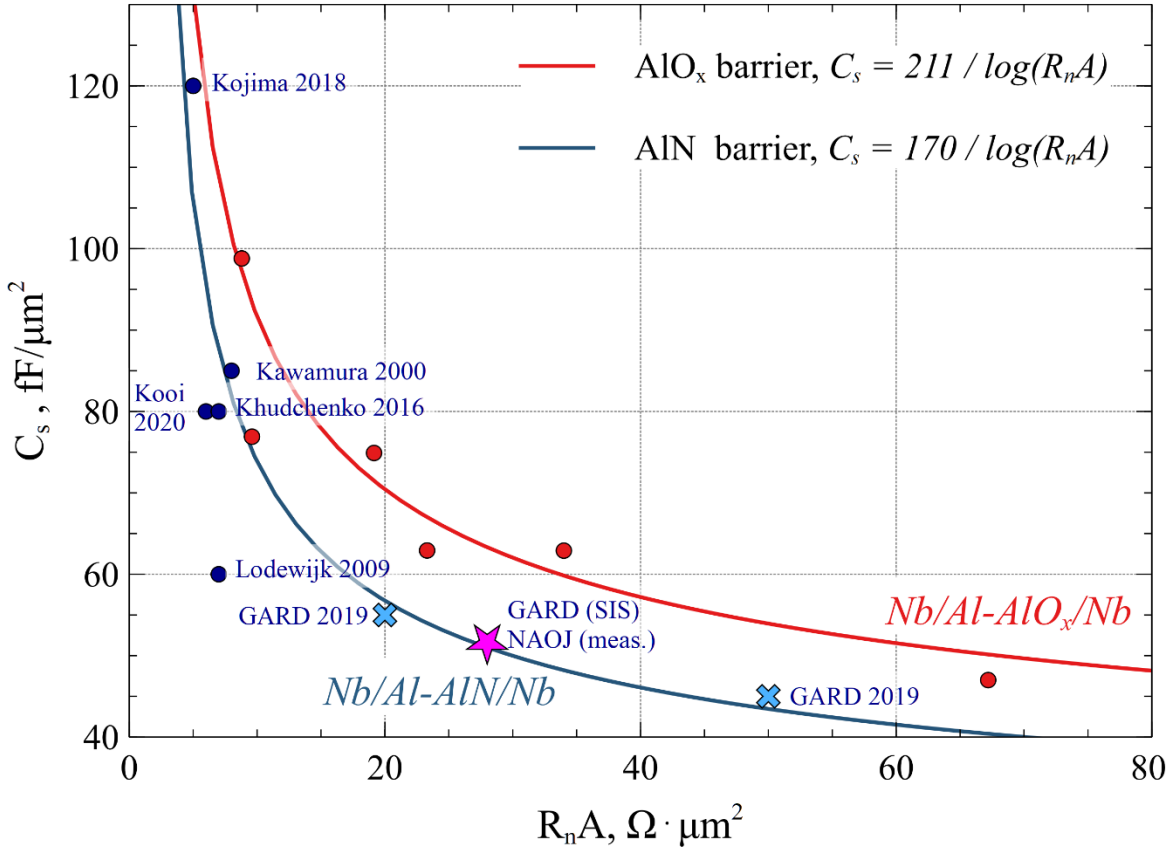
- Stable Nb/Al-AlN/Nb junctions process had been developed.
- R_nA between 5 to 120 $\Omega \cdot \mu m^2$
- All with low subgap current (high R_j/R_n ratio)
- **Stable for aging and annealing**, somewhat more stable than standard Nb/Al-AlOx/Nb junctions



red – as fabricated,
dashed blue – after annealing sequence 120°C, 130°C … 190°C, 200°C, 1 hour at each temperature

AlN-tunnel barrier SIS-junctions process

- Specific capacitance **C_s *vs* R_nA of GARD-made AlN-barrier SIS characterized** (cryogenic S-parameter measurements)
- The specific capacitance of Nb/Al-AlN/Nb junctions is proved to be **significantly lower** than that of Nb/Al-AlO_x/Nb junctions.
- **Independently confirmed** by measurements done at **NAOJ** (cryo-probe station, T. Kojima, S. Masui)
- **Compared and is consistent** with the C_s *vs* R_nA numbers reported by other groups for other AlN-SIS processes.



- *Nb/Al-**AlOx**/Nb junctions (measured at GARD)*
- *Nb/Al-**AlN**/Nb junctions (measured at GARD)*
- *Nb/Al-**AlN**/Nb junctions (measured in NAOJ, T. Kojima, S. Masui)*
- *Nb/Al-**AlN**/Nb junctions (data of Kojima 2018, Kawamura 2000, Kooi 2020, Khudchenko 2016, Lodewijk 2009)*

GARD SIS process upgrades

- ✓ **AlN-barrier SIS junctions process**
  lower specific capacitance and lower specific resistivity
  supported by ESO study 2017 – 2020

- ✓ **Smaller SIS junctions process**
  ≤ 1 μm^2
  supported by ESO study 2021 – 2024

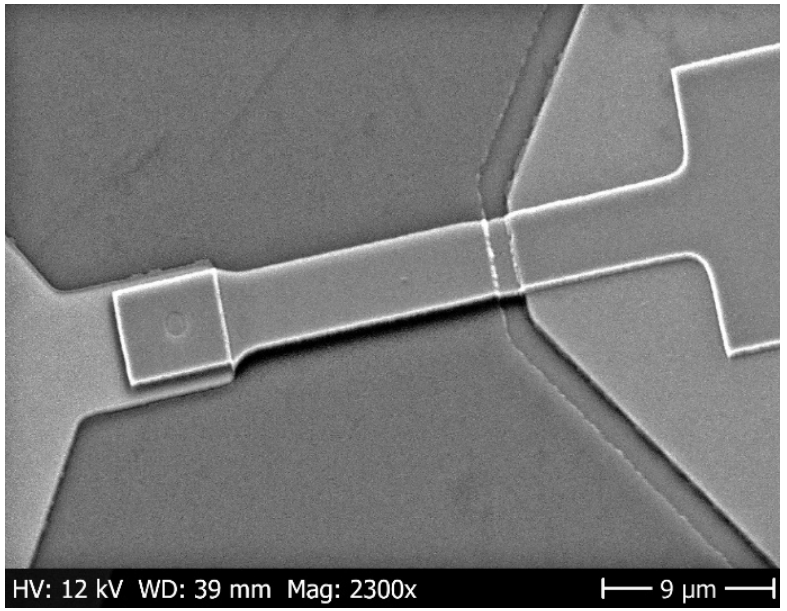
Strategy:

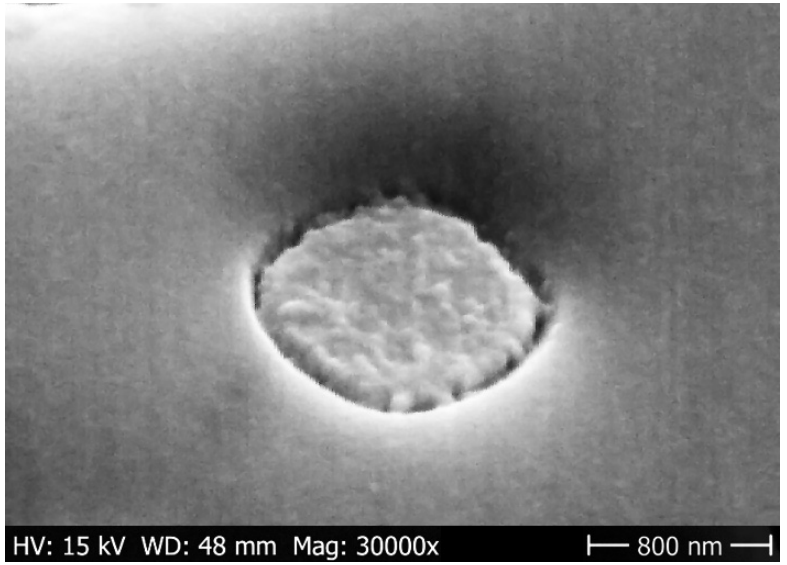
- **Do not change overall process integration** to preserve reliability of the process and its high yield
- **Modify only one key step at a time**:
  - Tunnel barrier plasma nitridation instead of thermal oxidation
  - Direct laser writing instead of contact photo lithography

Smaller SIS-junctions

Standard Nb-SIS process, but with **Direct Laser Writing** instead of contact photolithography:

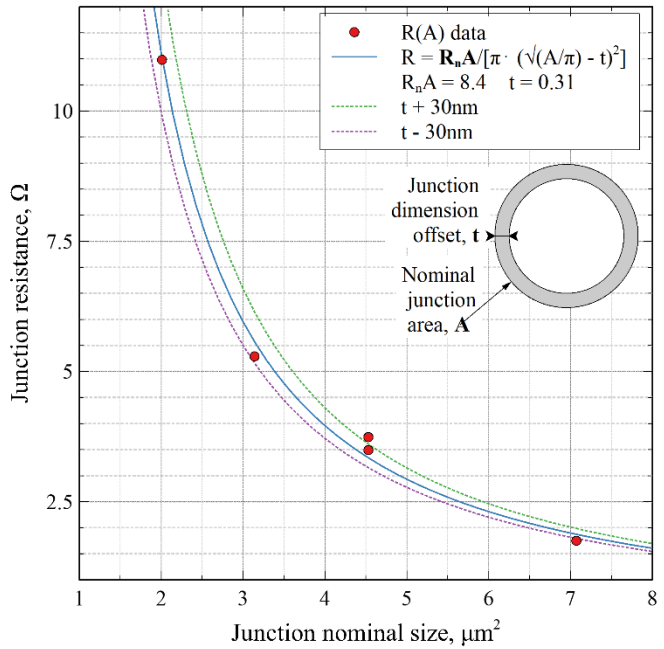
- Avoiding changes to other process component, i.e., preserving the stable fabrication process
- Keeping the process within existing budgetary framework
- Quick writing
- Backup equipment present

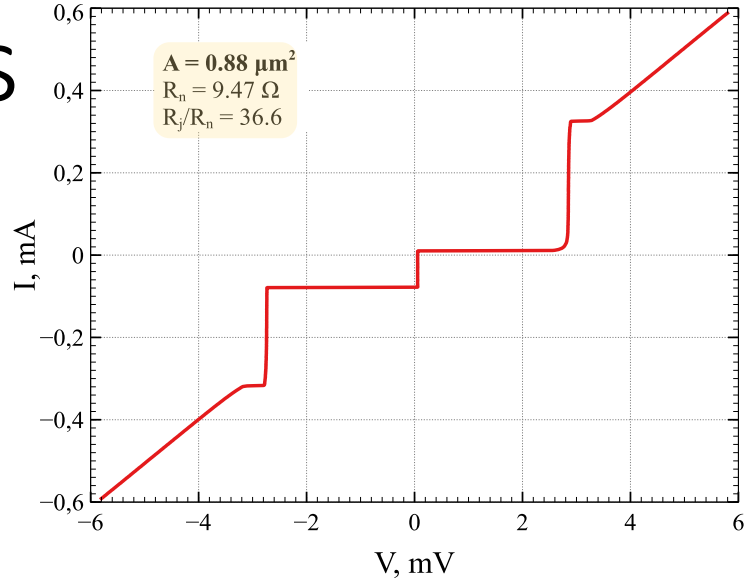


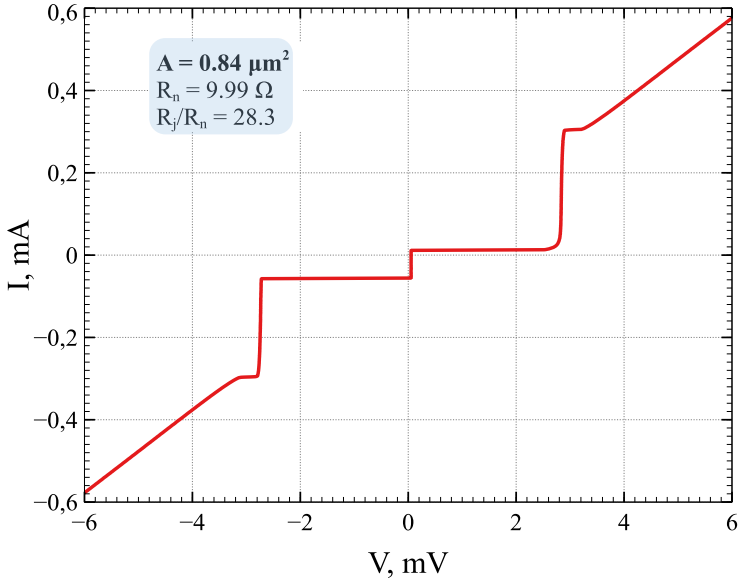


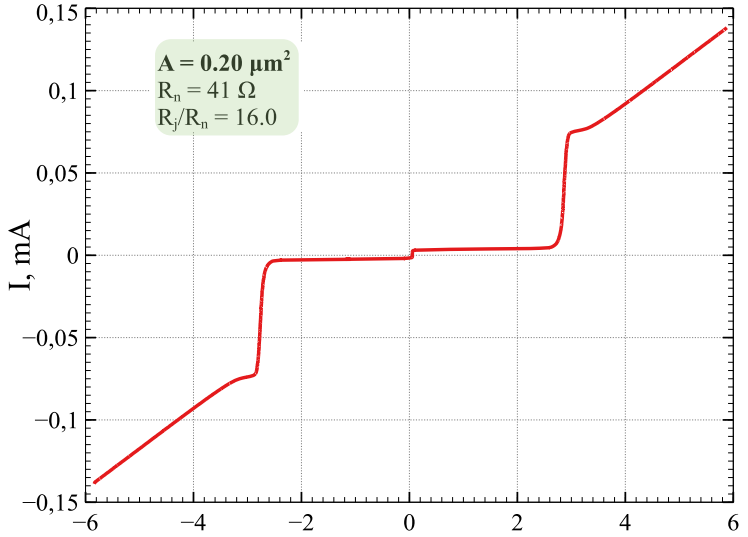
Smaller SIS-junctions

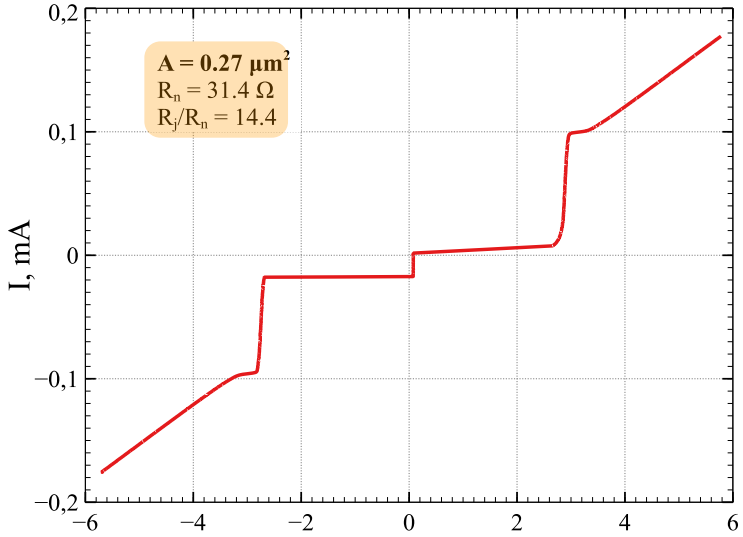
- Demonstrated to be possible to define as small as **≤1μm², and quite smaller** as well;
- **Extraction of true junction area** (along with the RnA) was used instead of measuring of the junction area on micrograph.







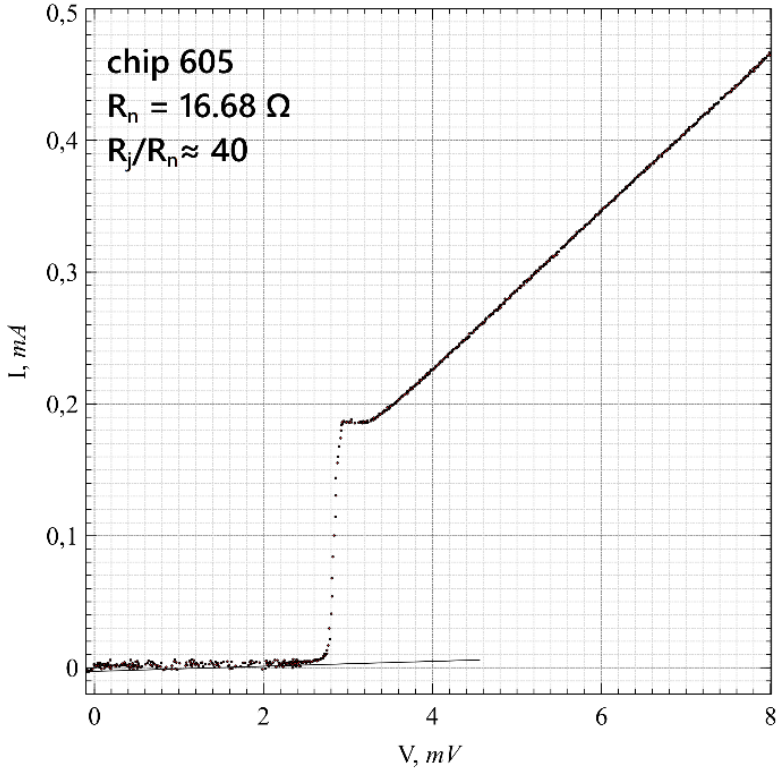




IVCs of Nb/Al-AlN/Nb SIS junctions with the R_nA product of 8.4 Ohm·μm² with the area of ca. 0.85 μm² (above), and ca. 0.25 μm² (below).

Demonstrator SIS devices: Band 9 mixer

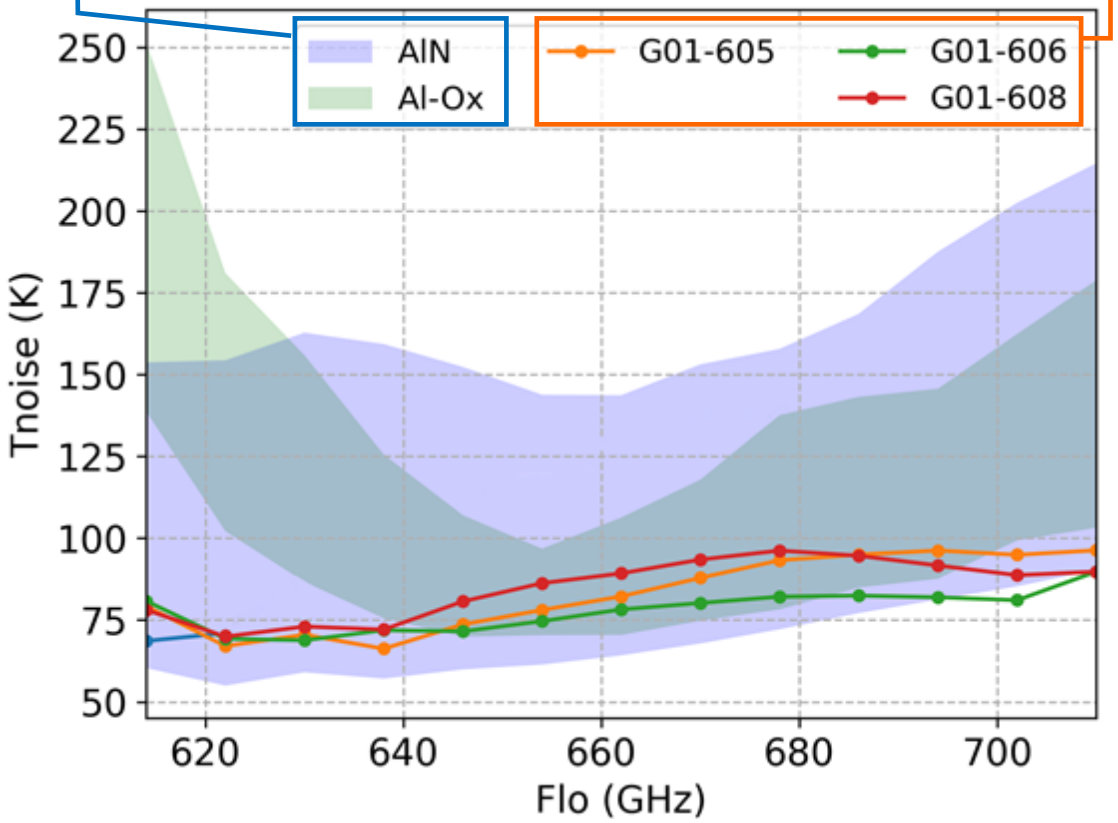
- Nb/AlN/Nb SIS junctions
- R_nA ~ 13 Ω·μm^2
- SIS area 0.8 μm^2
- Yield after dicing and lapping at NOVA - ca. 80%



Band 9 mixer design and measurements:
A. Baryshev, S. Realini, R. Hesper, R. de Haan Tijkel, M. Bekema, J. Barkhof, K. Rudakov (NOVA),
baseline SIS devices:
T.M. Klapwijk, T. Zijlstra, D. Toen (TUDelft)

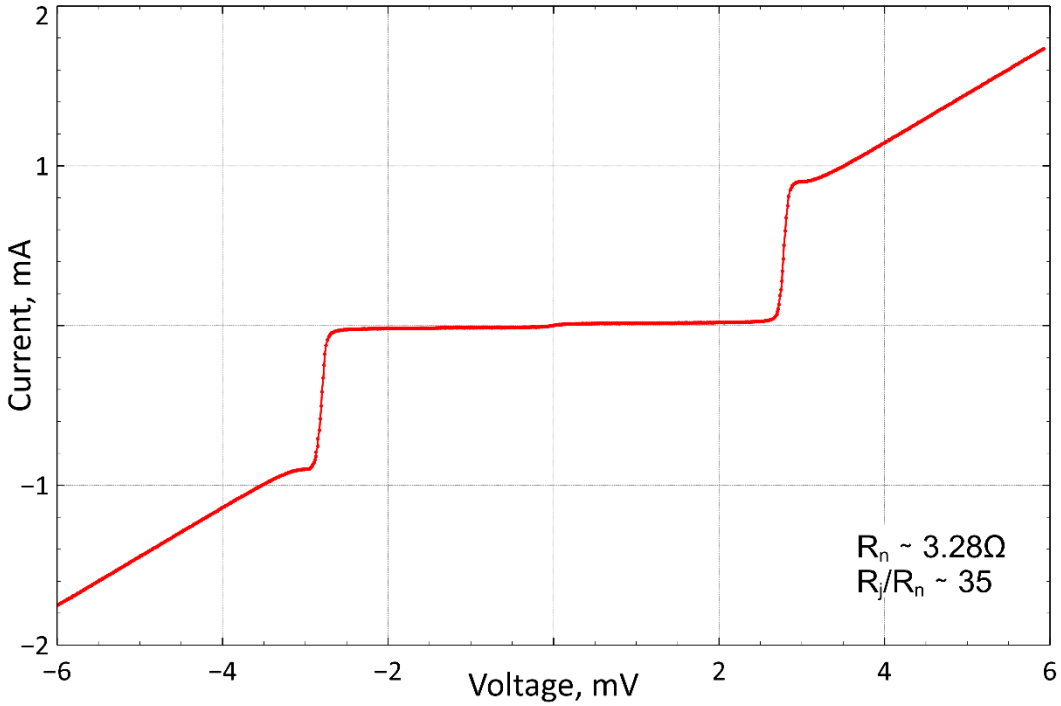
with GARD-made Nb/AlN/Nb SIS demo devices

All ALMA Band 9 ever produced – with the baseline SIS devices (TUDelft-made)



SIS devices for GARD Band 6 and 7 CCA demonstrator

- Nb/AlN/Nb SIS junctions
- R_nA ~ 13 Ω·μm^2
- SIS twin junction, area 2 μm^2 each

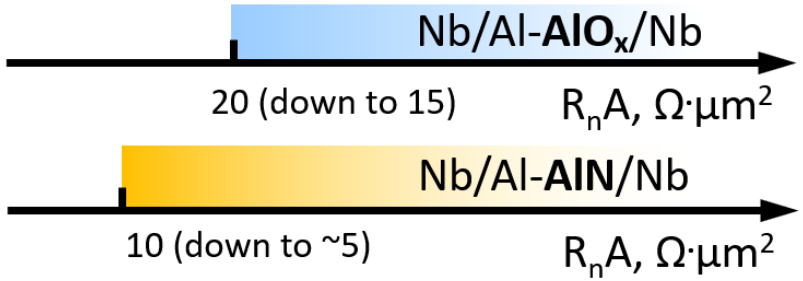


Design and performance:
see the talk
V. Belitsky "Exploring boundaries for wider RF and wider IF bands for ALMA SIS receivers"
on ***Thursday, June 27 at 9:55***

GARD SIS fabrication process to serve ALMA Wideband Sensitivity Upgrade

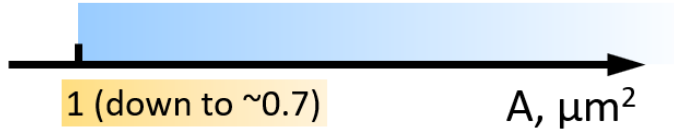
- **The ALMA 2030 Roadmap:** up to **4x bandwidth** compared to today's receivers
- GARD SIS fabricating process:
  - **Junctions with lower specific capacitance** and **specific resistance** (*AlN-barrier SIS junctions*)
  - **Smaller SIS junction area** (*≤ 1μm²*)

- **Junctions:**
  - R_nA:



  R_j/R_n – above 20 (usually, well above)

  - junction size:



- **Resistors:**

- **Nb tuning circuitry:**
  - stripe width:

GARD SIS technology team

Alexey Pavolotsky
Vincent Desmaris
Cristian López
François Joint

Seems,
ready and prepared
for the ALMA WSU
adventure…