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A 100-114 GHz GaAs MMIC Power Amplifier With Fully Integrated Dynamic Gate Bias Control for Linearization and Efficiency Enhancement

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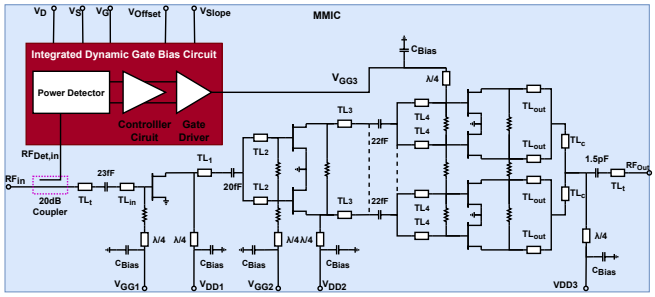
***Abstract*— This paper presents a dynamically gate-biased MMIC power amplifier (PA) operating in the 100 to 114 GHz frequency range and designed using a 100 nm GaAs pHEMT process. The design comprises a PA, power detector, controller, and gate bias driver - thus fully implementing a dynamically gate-biased PA with programmable complex gain characteristics. The paper demonstrates successful dynamic control over power consumption and gain of the PA through the integrated dynamic gate bias circuit. Quasi-static simulations based on the measured AM/AM and AM/PM responses demonstrate that, at the spectrum emission mask limit, with integrated dynamic gate biasing, the PA achieves a 1.67 dB increase in average output power and its average power added efficiency (PAE) with a 4QAM signal was increased by 20% when compared for static biasing. To the best of our knowledge, this represents the first millimeter-wave fully MMIC-integrated dynamic gate-biased power amplifier in an III-V pHEMT process.**

***Keywords*— power amplifiers, gate modulation, energy efficiency, GaAs, linearization, efficiency enhancement**

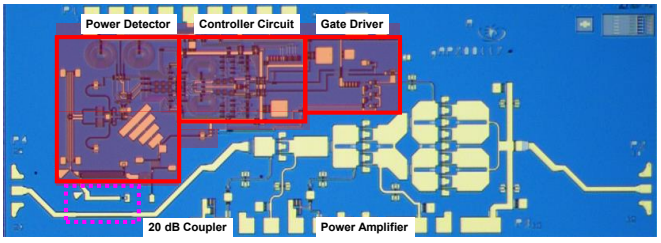
I. Introduction

Power amplifiers (PAs) are the components that dominate the energy consumption in the majority of front-end units. They are also the main source of non-linearity in front-end units. Due to these reasons, linear and efficient power amplification methods, such as digital pre-distortion, supply modulation, and load modulation, are all widely explored for enhancing the performance of PAs. Another technique, potentially well suited for linearization and efficiency enhancement in mm-wave and sub-THz applications is dynamic gate modulation.

Gate modulation is a method where the gate bias of an amplifier is dynamically adjusted in accordance with the time-varying envelope of the RF input signal. The principle of improvement in efficiency for amplifiers by dynamically biasing the gate terminal was theoretically described in [1] and [2]. In [3], base bias modulation is integrated into an MMIC based on GaAs HBTs to provide reduced power consumption and improved adjacent channel leakage ratio (ACLR) for W-CDMA applications. In [4] an integrated gate modulator was realized for linearization of CMOS FET amplifiers. In [5] and [6] the amplitude and phase linearization effect of gate modulation were presented for GaN power amplifiers. Likewise, in [7] amplitude and phase linearization was achieved by modulating more than one stage of a GaN PA. In [8], dynamic gate biasing was used to facilitate efficient auxiliary amplifier control in Doherty amplifiers up to 85GHz. Despite the demonstrated benefits of dynamic gate biasing, MMIC-integrated gate-modulated PAs have not yet been demonstrated in III-V pHEMT processes due to the limited integration possibilities there.



(a)



(b)

Fig. 1. (a) Block diagram, (b) photograph of the 1.4×4 mm MMIC.

In this work, illustrated in Fig. 1, a dynamic gate bias circuit (DGBC) is seamlessly integrated with a W-Band PA in a single MMIC implementation. The circuit offers integrated offset and slope control for the power tracking function. Leveraging these controls allows the optimization of the PA response for signals with different dynamic ranges, resulting in increased energy efficiency and output power within spectrum emission limitations. To the best of our knowledge, this paper presents the first fully integrated dynamic gate-biased PA MMIC in any III-V pHEMT process at millimeter-wave frequencies.

II. Circuit Implementation

The circuit is fabricated using the WIN Semiconductors PP10-20 pHEMT platform. The process provides $0.1\,\mu$m-gate D-mode transistors with 160 GHz ft and is qualified for $4\,$V operation. As presented in Fig. 1b, the designed circuit consists of a three-stage PA with a saturated output power of $23\,$dBm. The RF input signal to the amplifier is coupled to the integrated DGBC by a $20\,$dB coupler. The DGBC generates the gate bias voltage of the final PA stage based on a linear, programmable relationship to the instantaneous input power as will be outlined in the next subsections.

A. Power Amplifier

The PA is a three-stage nominally class-AB amplifier, designed for the 100-114 GHz frequency range. The first and second stages contain one and two 4×25 μm transistors, respectively. The final stage consists of four 4×30 μm transistors. The nominal bias conditions for the transistors at each stage are 4 V drain voltage and $300\,\mathrm{mA/mm}$ drain current density.

The circuit diagram for the input, output, and inter-stage matching networks is presented in Fig. 1a. The matching networks are initially designed to achieve maximum output power and energy efficiency, as load-pull analyses show that the optimum loads for both conditions are close to each other. Subsequently, the inter-stage matching networks were fine-tuned to achieve a flat gain response across the design frequency range. The characteristic impedances (Z_c) and electrical lengths (θ) of the transmission lines for matching networks are reported in Table1 at the $107\,$GHz center frequency.

To maximize the bandwidth of the gate modulation signal, the smallest possible bypass capacitors (C_Bias) were selected. These capacitors were chosen to create a resonant LC series network with the ground via, ensuring resonance within the desired frequency band. Electromagnetic simulations indicated that $175\,$fF capacitors meet this condition and provide the best RF-wise short.

Simulations show that, within the desired frequency band, the transistors are unconditionally stable. For other frequencies, stability is ensured by adding series resistance in gate bias networks and shunt capacitors at the bias terminals where required. Resistors are added between split or combined PA branches to dissipate and suppress parasitic odd-mode excitation.

Figure 2 compares small-signal simulations with on-wafer measurements conducted at nominal bias conditions, showing an overall good agreement.

B. Dynamic Gate Bias Circuit

The DGBC consists of three main components: the power detector, the controller circuit, and the gate driver. The RF input signal ($\mathrm{RF_{in}}$) to the PA is coupled to the power detector through a $20\,$dB coupler, as shown in Fig. 1. This power detector generates a differential signal proportional to the squared magnitude of the input RF signal by self-mixing the

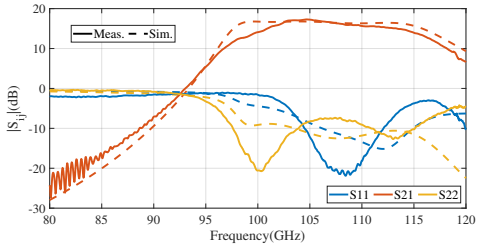


Fig. 2. Small-signal characterization of the power amplifiers at nominal bias condition comparing on-wafer measurements and simulations.

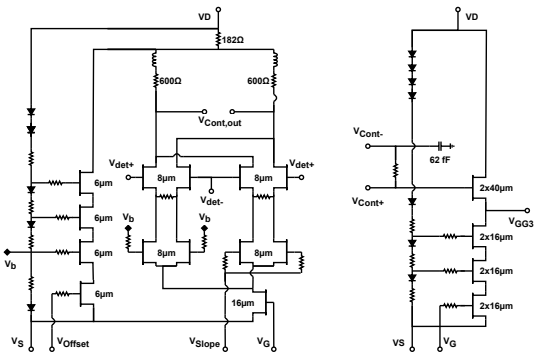
Table 1. Key parameters of Matching Transmission Lines

	$Z_\mathrm{c}(\Omega)$	θ_1 (°)		$Z_\mathrm{c}(\Omega)$	θ_2 (°)
$\mathrm{TL_{in}}$	25	53	$\mathrm{TL_4}$	30	64
$\mathrm{TL_1}$	25	82	$\mathrm{TL_{out}}$	30	94
$\mathrm{TL_2}$	25	63	$\mathrm{TL_t}$	41	90
$\mathrm{TL_3}$	25	87	$\mathrm{TL_c}$	70	50

coupled RF signal ($\mathrm{RF_{Det,in}}$). The mixing process employs a single-balanced Gilbert cell topology. In [9], the squared amplitude term was named the power envelope, and it was reported to be advantageous for gate modulation due to its inherently band-limited nature, in contrast to envelope tracking. The potential improvement through linear power envelope tracking-based gate modulation was presented in [10].

The circuit diagram of the controller circuit is provided in Fig.3a. It comprises a double-balanced Gilbert cell-based variable gain amplifier (VGA). The differential signal generated by the power detector is connected to the controller's $\mathrm{V_{det+}}$ and $\mathrm{V_{det-}}$ terminals. A series of diodes generate a nominal -3.3V bias at the node labeled $\mathrm{V_b}$ biasing one branch of the Gilbert cell. $\mathrm{V_{Slope}}$ adjusts the gain of the Gilbert cell: for voltages above -3.3V a positive gain in linear scale is applied to the power detector's output, for voltages below -3.3V the gain is negative. When biased with -3.3V the controller keeps its output voltage ($\mathrm{V_{Cont,Out}}$) constant against changing detector voltages. Fig. 3a also illustrates that the offset control voltage ($\mathrm{V_{Offset}}$) controls the current over a resistor between drain bias voltage ($\mathrm{V_D}$) and the differential circuit. This enables control over the DC offset of $\mathrm{V_{Cont,Out}}$.

Finally, the generated gate bias waveform from the power detector and controller must be delivered to the last stage gate terminal of the PA ($\mathrm{V_{GG3}}$). Simulations showed that the total capacitive loading at the gate bias terminal of the PA is 1.5 pF. To support a large instantaneous bandwidth, a fairly large transistor 2×40 μm is used in a common drain configuration with $145\,\mathrm{mA/mm}$ current density, as shown in Fig. 3b. This configuration has a small-signal transconductance (g_m) of 52 mS. Therefore, the impedance seen from the gate terminal of the PA can be approximated as $1/g_m = 19.2\,\Omega$. This low impedance presented by the common drain stage both aids stability at the gate terminal and provides a theoretical $3\,$dB bandwidth of 5.5 GHz.



(a) (b)

Fig. 3. Circuit Diagram of (a) controller, (b) gate driver.

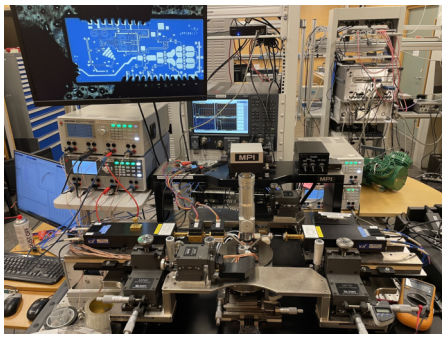


Fig. 4. Dynamic power measurements setup.

III. Dynamic Power Measurements and Results

The manufactured PA was mounted onto a brass carrier using silver epoxy. On-wafer measurements were conducted using a Keysight PNA-X equipped with mm-wave extenders from Virginia Diodes, as shown in Fig. 4. To achieve sufficient RF input power to saturate the device under test (DUT), additional driver PAs were added between the source extender and the DUT. After power calibration, the input power to the PA was swept. The complex gain and current consumption of the PA and DGBC were recorded at each sweep point. The tests were repeated with different V_{Offset} and V_{Slope} settings.

Fig. 5 shows the measured dynamic gate voltage V_{GG3} as a function of RF input power to the PA. The figure was obtained by deep-pinching off the first two stages of the PA

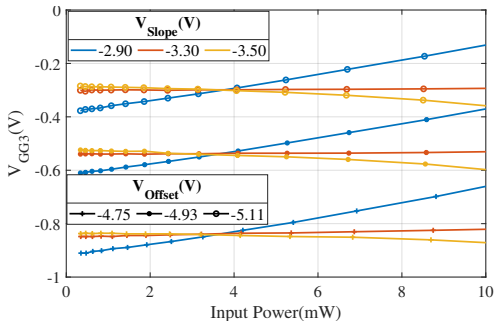
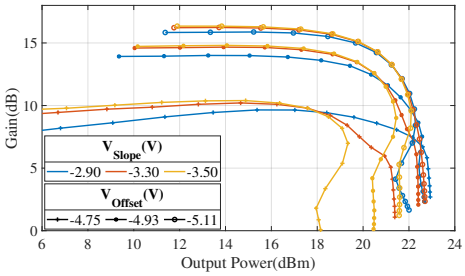
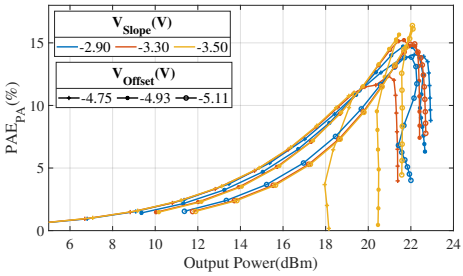


Fig. 5. Final stage dynamic gate bias voltages for different offset and slope settings of the DGBC.



(a)



(b)

Fig. 6. Measured gain (a) and PAE (b) of the PA.

to isolate RF input from the last stage. Drain, source, and gate bias voltages of the DGBC (V_D, V_S, and V_G) are set to 4.3 V, -4.7 V, and -4.82 V, respectively. The input power to the MMIC was swept, and the drain current of the last stage was recorded. Recorded drain currents were mapped to gate voltages by using the drain current versus gate voltage relation of the transistors. A linear voltage to RF input power relationship is observed, as intended. Moreover, it is evident that the control voltage V_{Offset} successfully offsets V_{GG3}. The V_{Slope} control applies negative or positive gain. Simulations predict a DGBC power consumption of 349 mW., which is confirmed in measurements. DC power consumption is distributed between the detector, controller, and gate driver as 56 mW, 189 mW, and 104 mW, respectively.

Fig. 6a shows that the V_{Offset} voltage successfully changes the operation class of the final stage of the PA. While the PA exhibits Class-C-like gain response for $V_{Offset} = -4.75$ V, it can be brought to Class-A/AB by reducing V_{Offset}. On the other hand, V_{Slope} dynamically changes the gain of the amplifier versus the input power. The combination of these two controls is now used for linearization and efficiency enhancement.

To explore the effects of dynamic gate modulation on linearization and efficiency improvement, simulations were conducted based on quasi-static modulated signal techniques described in [10], [11]. A fixed sequence of 800.000 bits was modulated with different quadrature amplitude modulation (QAM) formats and filtered with a root-raised cosine filter with a roll-off factor of 0.25. After filtering, modulated signals exhibit Peak-to-Average Power Ratio (PAPR) values of 4.9 dB, 7.3 dB, 7.6 dB and 7.9 dB for the 4QAM, 16QAM, 64QAM, and 256QAM formats, respectively. The resulting waveform is fed to PA models based on the measured AM/AM and

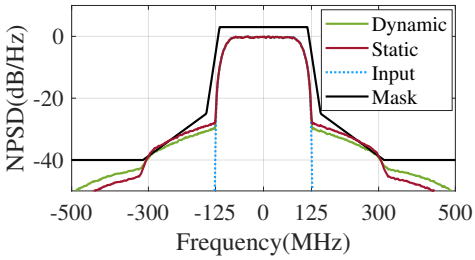


Fig. 7. Simulated output spectrum of the dynamic and static gate biased PA when driven with 16QAM signal. $\overline{\mathrm{P_{out}}}$ is 17.06 dBm for both cases.

AM/PM responses for different $\mathrm{V_{Offset}}$ and $\mathrm{V_{Slope}}$ settings. The drive level was increased to the point where the output spectrum of the DUT reached the spectrum emission mask limit. Key performance metrics for the settings that yielded the best average PAE ($\overline{\mathrm{PAE}}$) at the spectrum emission mask limit are summarized in Table 2. The efficiency of the PA ($\overline{\mathrm{PAE_{PA}}}$) and the efficiency of the entire MMIC including the power consumption of the DGBC, ($\overline{\mathrm{PAE_S}}$) was reported separately in the table. Furthermore, the table provides average output power ($\overline{\mathrm{P_{out}}}$) and $\overline{\mathrm{PAE}}$ for the static bias options that provide the best $\overline{\mathrm{PAE}}$. This demonstrates that for different modulation formats, DGBC is indeed able to provide enhanced output $\overline{\mathrm{P_{out}}}$ and $\overline{\mathrm{PAE}}$ at the mask limit. However, it is also shown that the efficiency enhancement is diminished when the power consumption of the DGBC is included. Still, it is important to note that when driving a larger PA with the same DGBC, this degradation would be smaller. Moreover, the controller circuit, which is the most power-hungry subcircuit of DGBC, has significant room for improvement.

To illustrate, in Fig. 7, the static and dynamic gate-biased cases yielding the best $\overline{\mathrm{PAE}}$, are driven with a 16QAM signal. The drive level is set such that $\overline{\mathrm{P_{out}}}$ for both cases is 17.06 dBm. Normalized power spectral density (NPSD) of the RF input and output of the PA was presented in the figure. It is evident from the figure that while the static-biased case violates the mask, thanks to the suppressed 3rd order inter-modulation products, dynamic gate-biased case can operate at this drive level without violating the mask.

Table 2. Key performance parameters at spectrum emission mask limit.

	Dynamic Bias					Static Bias		
	$\mathrm{V_{Offset}}$	$\mathrm{V_{Slope}}$	$\overline{\mathrm{PAE_S}}$	$\overline{\mathrm{PAE_{PA}}}$	$\overline{\mathrm{P_{out}}}$	$\mathrm{V_{GG3}}$	$\overline{\mathrm{PAE}}$	$\overline{\mathrm{P_{out}}}$
4QAM	-4.75	-2.90	8.54	12.53	20.81	-0.44	10.23	19.14
16QAM	-4.84	-2.90	4.71	7.52	17.06	-0.44	6.16	16.63
64QAM	-4.98	-2.93	3.14	4.74	15.47	-0.51	4.39	15.45
256QAM	-5.07	-3.05	2.27	3.21	14.54	-0.31	3.09	14.30

$\mathrm{V_{Offset}}$,$\mathrm{V_{Slope}}$, $\mathrm{V_{GG3}}$ in V; $\overline{\mathrm{PAE_S}}$, $\overline{\mathrm{PAE_{PA}}}$ in % ; $\overline{\mathrm{P_{out}}}$ in dBm

IV. Conclusion

In this work, we successfully demonstrate a fully integrated, dynamically gate-biased MMIC PA. Using on-chip circuitry, the gate bias voltage of the last PA stage is made linearly dependent on the RF envelope power, with adjustable slope and offset settings. This dynamic control enables a programmable gain characteristic of the PA and affects power consumption. Using the AM/ AM and AM/PM characterization of this PA for different control settings, we demonstrate optimized gain responses and reduced power consumption for four different modulation orders using quasi-static simulations. Specifically, using a spectrum emission mask, we demonstrate an improvement of up to 1.67 dB in output power at the mask limit. This results in a PAE improvement of 22% to 3.8% compared to the best static gate bias depending on the modulation order.

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