THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Advancing GaN HEMT Technology for Microwave Applications: Investigations of Ohmic Contacts, Passivation, and Buffer-Free Concepts

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Abstract

High electron mobility transistors (HEMTs) based on gallium nitride (GaN) exhibit significant performance in high-frequency and high-power applications due to unique properties. For instance, high electron mobility, substantial saturation velocity, and elevated breakdown voltage. However, challenges including forming low resistivity ohmic contacts, trapping effects, and Two-Dimensional Electron Gas (2DEG) confinement impede further improvement.

The formation of deeply recessed Ti/Al/Ti and Ta/Al/Ta sidewall ohmic contacts, using a low annealing temperature and achieving minimal contact resistance of 0.14 and 0.24 Ω·mm, respectively, were explored. The reduced annealing temperature mitigates Al metal melting risk, enabling sharper edges and improved surface morphology. Deep recessing beyond the barrier layers makes the process less susceptible to variations in etching depth since ohmic contacts are formed on the recessed sidewall. The bottom Ti and Ta layer, Al thicknesses, and recessed sidewall angle, were optimized, successfully demonstrating on epitaxial structures with varied barrier designs.

Passivation utilizing low pressure chemical vapor deposition (LPCVD) silicon nitride (SiN) has emerged as an effective method for mitigating surface-related trapping effects. However, surface traps could not be entirely eliminated with passivation, owing to the persistence of defects, dangling bonds and a native oxide layer at the interface between the passivation and epi-structure. Consequently, an in-situ NH_3 pretreatment method preceding LPCVD SiN deposition was investigated. The pretreated sample exhibited a 38% reduction in surface-related current collapse compared to the un-pretreated sample, culminating in a 30% augmentation in output power (3.4 vs. 2.6 W/mm) and an enhanced power-added efficiency (44% vs. 39%) at 3 GHz. Additionally, the pretreated samples demonstrated improved uniformity in device performance.

Traditionally, adequate buffer insulation and 2DEG confinement have been achieved through the intentional acceptor-like dopants (iron (Fe) and carbon (C)) or the AlGaN back-barrier in the GaN buffer. In this thesis, the impact of different carbon concentrations in AlGaN back-barrier and GaN buffer is studied. The results highlight that the back-barrier effectively screens the trapping effects underneath the back-barrier and the importance of optimization C-doping level in GaN channel, back-barrier and GaN buffer. However, solutions involving acceptor dopants, and a back-barrier have been reported to increase trapping effects and thermal resistivity, respectively. Therefore, a novel buffer-free epitaxial scheme, QuanFINE, was proposed. It removes thick Fe-/C-doped GaN buffer, enabling a GaN channel thickness of 250 nm to be directly grown on an AlN nucleation layer. Consequently, the AlN nucleation layer serves as a back-barrier. This approach results in a lower buffer-related current collapse (15% vs. 18%) compared to a conventional epi-structure with a thick Fe-doped GaN buffer. Furthermore, the reduction of GaN channel thickness from 250 nm to 150 nm is explored to facilitate the development of highly scaled devices. No degradation of 2DEG properties was observed in the epitaxial structure with the GaN channel thickness reduced to 150 nm. An exemplary drain-induced barrier lowering (DIBL) of 20 mV/V was measured on a device with a L_g of 70 nm. While the sought-after 2DEG confinement and buffer insulation can be achieved, QuanFINE is not devoid of traps. This thesis also investigates an epitaxial structure with a band structure engineering at the interface of GaN channel and AlN nucleation layer using Si delta doping, which exhibited a lower buffer-related current collapse (19.8% vs. 26.8%), a more rapid current recovery speed, and a mitigation of long time constant as compared to the standard QuanFINE structure.

Keywords: GaN HEMT, Ohmic contact, Pretreatment, Passivation, QuanFINE.

List of Publications

Appended publications

This thesis is based on the following publications:

[A] **D.Y. Chen**, A.R. Persson, V. Darakchieva, P.O.Å. Persson, J.T. Chen, and N. Rorsman, "Structural investigation of ultra-low resistance deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs based on Ti/Al/Ti-metallization", Semiconductor Science and Technology, Vol. 38, Issue 10, Sep. 2023.

[B] Y.K. Lin, J. Bergsten, H. Leong, A. Malmros, J.T. Chen, **D.Y. Chen**, O. Kordina, H. Zirath, E.Y. Chang, and N. Rorsman, "A versatile low low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs", Semiconductor Science and Technology, Vol. 33, Num. 9, Aug. 2018.

[C] **D.Y. Chen**, A.R. Persson, K.H. Wen, D. Sommer, J. Grünenpütt, H. Blanck, M. Thorsell, O. Kordina, V. Darakchieva, P.O.Å. Persson, J.T. Chen, and N. Rorsman, "Impact of *In Situ* NH_3 Pre-treatment of LPCVD SiN Passivation on GaN HEMT Performance", Semiconductor Science and Technology, Vol. 37, Issue 3, Jan. 2022.

[D] R. Ferrand-Drake Del Castillo, **D.Y. Chen**, J.T. Chen, M. Thorsell, V. Darakchieva, and N. Rorsman "Characterization of Trapping Effects Related to Carbon Doping Level in AlGaN Back-Barriers for AlGaN/GaN HEMTs", IEEE Transactions on Electron Devices, Vol. 71, Issue 6, Page 3596 - 3602, May. 2024.

[E] **D.Y. Chen**, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J.T. Chen, and N. Rorsman, "Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors" IEEE Electron Device Letters, Vol. 41, Issue 6, Apr. 2020.

[F] **D.Y. Chen**, K.H. Wen, M. Thorsell, M. Lorenzini, H. Hjelmgren, J.T. Chen, and N. Rorsman, "Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructures" Physica Status Solidi (a), Sep. 2022.

[G] **D.Y. Chen**, K.H. Wen, M. Thorsell, J.T. Chen, and N. Rorsman, "Investigation and Mitigation of Trapping Mechanisms in Buffer-Free AlGaN/GaN HEMTs" Manuscript with major revision submitted again to IEEE Transactions on Electron Devices, Jan. 2025.

Other publication

[h] J. Bremer, **D.Y. Chen**, A. Malko, M. Madel, N. Rorsman, S. E Gunnarsson, K. Andersson, T. MJ Nilsson, P. E Raad, P. L Komarov, T. L Sandy, and M. Thorsell, "Electric-Based Thermal Characterization of GaN Technologies Affected by Trapping Effects", IEEE Transactions on Electron Devices, Vol. 67, Issue 5, Page 1952-1958, Apr. 2020.

Patent

[i] **D.Y. Chen**, N. Rorsman, and J.T. Chen, "SEMICONDUCTOR DEVICE STRUCTURE WITH RECESSED OHMIC CONTACTS AND METHOD FOR PRODUCING THE SAME", [US20240363746A1, EP4123721A1, TW202315117A, JP2024526363A, KR20240056492A, CN117652032A, WO2023001762A1]

Conference

[j] **D.Y. Chen**, J. Bergsten, A. Malmros, M. Thorsell, H. Hjelmgren, J.T. Chen, O. Kordina, and N. Rorsman, "QuanFINE – High RF Performance AlGaN/AlN/GaN HEMTs with a Thin Buffer Layer", Oral presentation, 13th International Conference on Nitride Semiconductors (ICNS-13), July 2019.

[k] **D.Y. Chen**, K.H. Wen, M. Thorsell, O. Kordina, J.T. Chen, and N. Rorsman, "Thin $Al_{0.5}Ga_{0.5}N$/GaN HEMTs on QuanFINE® Structure", Oral presentation, 2021 International Conference on Compound Semiconductor Manufacturing Technology (CS-MANTECH 2021), May 2021.

[l] **D.Y. Chen**, K.H. Wen, M. Thorsell, M. Lorenzini, H. Hjelmgren, J.T. Chen, and N. Rorsman, "Improve 2DEG Confinement in 70 nm AlGaN/GaN HEMTs by Reducing the GaN Channel Thickness in Buffer-Free Heterostructures", Oral presentation, International Workshop on Nitride Semiconductors (IWN 2022), Oct 2022.

Thesis

[m] **D.Y. Chen** "Optimization of Ohmic Contacts and Surface Passivation for 'Buffer-Free' GaN HEMT Technologies" Tekn. Lic. Thesis, Department of Microtechnology and Nanoscience - MC2, Chalmers University of Technology, Gothenburg, Dec 2020.

As part of the author's doctoral studies, some of the work presented in this thesis has previously been published in [m]. Figures, tables, and text from [m] may therefore be fully or partially reproduced in this thesis.

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Chapter 1

Introduction

GaN HEMTs have showcased exemplary performance in high-frequency applications, especially those operated under substantial power density, with contributions related to the large bandgap. In comparison to conventional semiconductors utilized for high-frequency applications - such as Si (1.1 eV), SiGe (1.12 eV), InP (1.34 eV), and GaAs (1.42 eV) - GaN boasts a notably larger bandgap of 3.4 eV. This substantial bandgap enables GaN to function at elevated voltages while maintaining robustness under high ambient temperature and radiation environments. This is partly due to the mitigation of carrier excitation to the conduction band (E_c) induced by thermal and radiation effects [1]. Initially, GaN HEMTs were fabricated on AlGaN/GaN heterostructures, where a two-dimensional electron gas (2DEG) forms within the quantum well due to the epitaxial growth of a larger-bandgap III-nitride material on GaN, while the pronounced 2DEG concentration is further enhanced by polarization and piezoelectric fields. More recently, InAl(Ga)N/GaN, AlScN/GaN, and AlN/GaN heterostructures emerge as alternative considerations owing to their higher polarization fields, thereby resulting in an enhanced 2DEG concentration [1]. Within the energy well, high-concentration electrons can travel with less scattering effects, leading to high electron mobility and saturation velocity. An augmented saturation velocity in GaN HEMTs can facilitate a higher cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), thus bolstering high-frequency operating performance [1]. The combination of a higher 2DEG concentration with elevated mobility and saturation velocity results in a reduced 2DEG sheet resistance (R_{sh}) and an increased saturation source-drain current (I_{DS}), potentially improving high-power performance.

When combined with a high thermal conductivity SiC substrate, these advantages enable GaN HEMTs to operate at an escalated power density, maintaining high robustness. Compared to alternative transistors founded on Si,

SiGe, InP, and GaAs, utilized for high-frequency power amplifier (PA) applications up to 200 GHz, GaN HEMTs yield a higher output power (P_{out}) density [2]. These merits pave the way for GaN HEMTs to be used for compact PA designs, proving ideal for sensing technology, satellite, and wireless communication.

Despite the advantages of GaN HEMTs, several persisting issues limit their performance. The formation of low contact resistance (R_c) ohmic contacts on GaN HEMTs always presents a notable first challenge while processing GaN HEMTs. Establishing ohmic contacts with minimized R_c is important as it reduces resistance at the transistor's source and drain terminals, thereby enhancing device performance. One approach to form ohmic contacts involves regrowing n-GaN contact using metal-organic chemical vapor deposition (MOCVD) or molecular-beam epitaxy (MBE). Employing heavily Si-doped regrown GaN can achieve a low R_c (<0.15 Ω·mm) [3]. However, this methodology can be complex and is not typically compatible with industrial high-throughput requirements. An alternate approach encompasses alloyed Ti- and Ta-based ohmic contacts, which have been reported to have a R_c ranging from 0.06 to 0.40 Ω·mm [4-8]. In this work [Paper A], the formation mechanism of deeply recessed Ti-based ohmic contacts, utilizing a low annealing temperature, was explored. A R_c of 0.14 Ω·mm was achieved with Ti-based ohmic contact, employing an annealing temperature of 550 °C on AlGaN barrier epi-structures with various Al contents, building upon previous publication [Paper B], using Ta-based deeply-recessed sidewall ohmic contacts with a R_c of 0.24 Ω·mm.

Another performance-limiting factor for GaN HEMTs is the DC-RF dispersion effects, which result from surface- and buffer-related trapping effects, as well as thermal dissipation capability [9, 10][Paper h]. Surface trap states exist due to the surface defects, native oxides, and polarization-induced energy states. The accumulation of negative charges on the epi-structure's surface, acting as a virtual gate, occurs when the surface trap states, filled by electrons due to the electric field, are not instantaneously released, depleting 2DEG and resulting in knee-walkout and current collapse [9]. Although surface passivation with dielectric material is commonly employed to mitigate undesirable surface trap states, it does not fully eliminate surface traps. Various pre-treatments, including ex-/in-situ chemical- and plasma-based processes, have been studied. A non-plasma-based in-situ process is preferred to minimize contamination, re-oxidation, and plasma damage risks. Yet, no non-plasma-based in-situ pre-treatments have been reported for LPCVD SiN passivation [11]. Commonly used gases in LPCVD systems include Dichlorosilane (DCS), silane, ammonia (NH_3), and nitrogen, with NH_3 being effective in removing native oxide and recovering the dangling bond on the GaN surface [12]. Thus, [Paper C] proposes an in-situ NH_3 surface pre-treatment process before LPCVD SiN passivation layer deposition to mitigate surface-related trapping effects. Samples subjected to NH_3 pre-treatment exhibited a reduced surface-related current collapse (9% compared to 16% for untreated samples) and, consequently, a higher maximum P_{out} (3.4 W/mm vs. 2.6 W/mm) at 3 GHz as well as better on wafer uniformity.

In contrast to surface-related traps, which can be mitigated through passivation layers and surface pre-treatment, addressing buffer-related traps necessitates optimization in epi-structure design and epitaxial growth to diminish trap states

and undesirable impurities. Commonly, Fe and C are employed as acceptor-like dopants to facilitate buffer insulation and 2DEG confinement [10, 13]. Nonetheless, these dopants lead to trapping effects, limiting large-signal performance. In [Paper E], a novel "buffer-free" epi-structure, trademarked QuanFINE by SweGaN AB, is proposed, removing the conventional Fe- or C-doped thick GaN buffer. This structure comprises merely a 250 nm thin GaN channel, directly grown on an AlN nucleation layer (a stark contrast to the ~2 µm thick GaN buffer in conventional epi-structures), enabling the AlN nucleation layer to function as a back-barrier, confining the 2DEG. Furthermore, buffer-related trapping effects in QuanFINE are reduced compared to conventional Fe-doped epi-structures (15% vs. 18%) due to the elimination of the Fe-doped buffer.

To realize the desired 2DEG confinement for highly scaled GaN HEMTs, particularly those with a gate length (L_g) under 100 nm, an additional AlGaN back-barrier is commonly deployed in conventional thick buffer epi-structures. Nonetheless, this can inadvertently form an unwanted 2DEG channel at the interface of the back-barrier and GaN buffer, necessitating compensation through Fe- or C-dopants, and thereby introducing trapping effects. Therefore, [Paper D] investigates the impact of different carbon concentrations in AlGaN back-barrier and GaN buffer. The results highlight that the buffer-related trapping effects can be mitigated by the AlGaN back-barrier and the optimized carbon doping profile in AlGaN back-barrier and GaN buffer.

However, the creation of extra interfaces by the back-barrier could foreseeably impair thermal dissipation properties [14, 15]. An alternative strategy to enhance 2DEG confinement involves diminishing the GaN channel thickness atop the AlGaN back-barrier [16]. However, reducing GaN channel thickness without sacrificing 2DEG properties and structural quality in a buffer-free epi-structure presents a challenge [17]. Based on [paper E], a reduction of GaN channel thickness from 250 nm to 150 nm—achieved without compromising 2DEG and structural integrity—is demonstrated and further studied in [Paper F]. Moreover, this work investigates the tradeoff among 2DEG confinement, trapping effects, and large-signal performance.

Despite the elimination of the Fe- and C-doped thick buffer, QuanFINE is not entirely free from trapping effects [Paper E]. A noticeable increase in current collapse was characterized as the thickness of the GaN channel was reduced [Paper F]. Consequently, the dominant trap states are hypothesized to be situated at the bottom of GaN channel, or AlN nucleation layer, or within the semi-insulating SiC substrate or the interface between different epi-structure layers. Furthermore, a potential two-dimensional hole gas (2DHG) has been reported at the interface between GaN and the AlN nucleation layer [18] with the possibility of temporary traps the injected electron during device operation. [Paper G] explores trapping effects within QuanFINE with a band-structure engineering interface using Si delta doping between GaN channel and AlN nucleation layer and compares them to the standard QuanFINE. The QuanFINE with band structure engineered interface demonstrated a lower current collapse and a more rapid current recovery speed compared to the conventional QuanFINE structure. Additionally, the properties of the traps were analysed through temperature-dependent and filling time-dependent

drain current transient measurements.

The discussions and analyses within this thesis are structured as follows: Chapter 2 presents an introduction to GaN HEMTs, exploring its operation, fabrication process, and characterization methods. Chapter 3 delves into the fundamental aspects of ohmic contacts, including alloyed-based and regrowth ohmic contacts, and further discusses the formation mechanism of low-temperature, deeply recessed Ti- and Ta-based ohmic contacts [Paper A and Paper B]. Chapter 4 consolidates and compares different passivation materials and pre-treatments, placing particular emphasis on the proposed in-situ NH_3 pre-treatment for LPCVD SiN passivation [Paper C]. Chapter 5, which embodies the key of this thesis, introduces the buffer-free QuanFINE epi-structure [Paper E], benchmarks it against conventional materials, and examines different buffer designs aimed at enhancing 2DEG confinement and mitigating trapping effects [Paper D, F, and G]. Lastly, Chapter 6 encapsulates the conclusions drawn and delineates potential avenues for future research.

Chapter 2

GaN HEMTs technology

2.1 AlGaN/GaN heterostructure

Ever since the invention of the AlGaN/GaN heterostructure, recognized as a third-generation semiconductor, the development of GaN HEMTs has thrived over the past decades, thanks to the unique properties of GaN (Table 2.1) [2]. GaN exhibits a larger bandgap (E_g) than that of Si, GaAs, and InP. A larger E_g leads to a higher critical breakdown field (E_{crit}), resulting in a higher operation drain-source voltage (V_{DS}) for the transistor. Although 4H-SiC also possesses a bandgap similar to that of GaN, it displays lower mobility and saturation velocity. Consequently, SiC is more suited for power switching devices rather than high-frequency applications.

Table 2.1. Summary of semiconductors properties [2].

	Si	4H-SiC	GaAs HEMT AlGaAs/GaAs	InP HEMT InAlAs/InGaAs	GaN HEMT AlGaN/GaN
Bandgap [eV]	1.12	3.26	1.43	1.34	3.4
Critical breakdown field [10^6 V/cm]	0.3-0.4	2.5-4	0.4-0.5	0.5-0.7	3.5-5
Electron mobility @300 K [$cm^2/V{\cdot}s$]	1.5k	0.9k	5k-15k (2DEG)	10k-20k (2DEG)	2k (2DEG)
Thermal conductivity [W/m·K]	150-180	490	50	68	130
Lattice mismatch to GaN [%]	-17.0	+3.5	--	--	--

For THz applications, GaAs and InP offer higher electron mobility than GaN. Nevertheless, the output power of GaN can surpass that of GaAs and InP devices when the operation frequency is below 150 GHz, due to its higher breakdown voltage (V_{BR}). Furthermore, the high thermal conductivity of GaN allows for enhanced heat dissipation and improved device robustness.

2.1.1 Substrate for GaN epitaxy

In the early stages of III-nitride development, GaN grew on sapphire and used in light-emitting diodes (LEDs) due to its cost-effectiveness and reliability. However, sapphire's poor thermal conductivity (0.23 W/K·cm) and significant lattice mismatch with GaN (-16%) make it less ideal for high-frequency applications [19]. Nonetheless, with the right process optimization and thermal management, GaN-on-sapphire can be suitable for high-power switching applications that operate at lower frequencies (< 10 MHz) [20].

The Si substrate presents an alternative for GaN epitaxy, primarily due to its cost-effectiveness and the capability to support larger wafer sizes. These attributes render GaN on Si suitable for high-volume, low-voltage power devices with ratings below 1200 V [21]. However, the pronounced lattice mismatch with GaN necessitates a thick strain-relief buffer to maintain the desired structural quality and inhibit crystal relaxation. Similar to sapphire, the challenges of inadequate heat dissipation and significant trapping effects make Si a less optimal choice for high-power microwave devices.

Alternative substrates for GaN epitaxy are also free-standing GaN and diamond. GaN-on-GaN offers an ideal lattice match, eliminating the need for an AlN nucleation layer [22]. However, the current limitations in GaN substrate quality consistency and smaller wafer size make it more expensive and less viable for commercial production. In contrast, while diamond has a significant lattice mismatch of 12% with GaN, GaN-on-diamond holds considerable promise for high-end RF applications, such as satellite communication, thanks to its exceptional thermal conductivity (22.9 W/K·cm) [23].

Among the several substrate options for GaN epitaxy, the SiC substrate stands out with its high thermal conductivity and a relatively minor lattice mismatch (+3.5%). Furthermore, semi-insulating (SI)-SiC substrates can be realized either through a high-purity process using point defects or via vanadium doping, ensuring the desired resistivity. Also, SI-SiC made by high-purity process provides better thermal conductivity as compared to that by vanadium doping. These characteristics make the SiC substrate suitable for both high-power and high-frequency GaN HEMTs applications. For the research presented in this thesis, all GaN HEMTs heterostructures were grown on SI-SiC. To address the lattice mismatch between GaN and SiC, both an AlN nucleation layer and a thick strain-release GaN buffer are commonly employed in conventional epi-structures. Further details will be explored in Chapter 5.

2.1.2 Formation of 2DEG

A GaN HEMTs heterostructure is realized by epitaxially growing a III-nitride barrier, which has a larger bandgap than GaN, on a GaN channel layer. In the conventional AlGaN/GaN heterostructure, an increased Al content results in a more pronounced lattice mismatch with GaN. This mismatch raises the potential for crystal structure relaxation, dislocation, and defects, all of which can adversely affect device performance and surface properties including morphology. Consequently, barriers with higher Al content necessitate a reduction in barrier

thickness. This approach effectively mitigates short channel effects as well as maintains high 2DEG concentration for highly scaled GaN HEMT.

Electron affinity (E_{ea}) and E_g play crucial roles in the formation of an energy well and 2DEG. Electron affinity is defined as the energy required to detach an electron from the conduction band (E_c) to the vacuum state (E_{vac}). The barrier typically has a larger E_g and a smaller E_{ea} compared to the GaN channel. This difference leads to an energy offset at the interface, as illustrated in Fig. 2.1a. To equate the Fermi level (E_F) of the two semiconductor materials, both the E_c and valence band (E_v) bend. This bending facilitates the migration of electrons from the barrier to the GaN channel side because of the channel's lower energy state, depicted in Fig. 2.2a. Consequently, an energy well containing 2DEG forms at the interface between the barrier and the GaN channel.

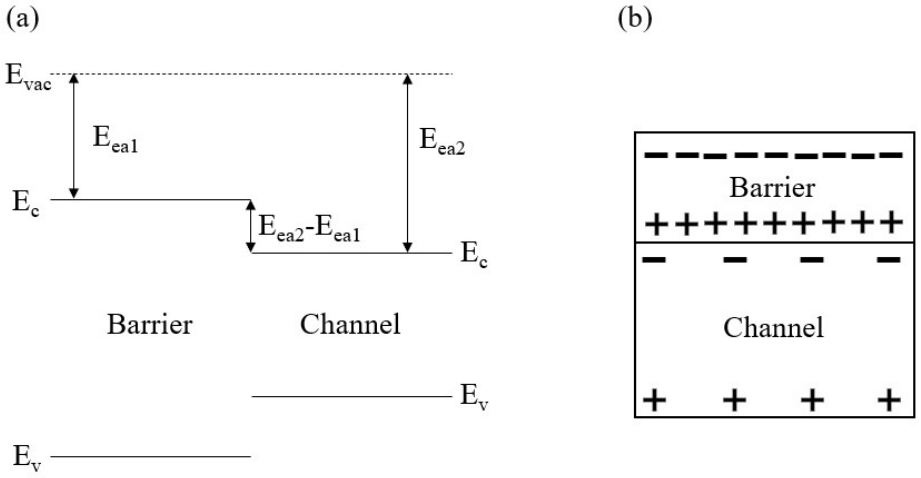

Fig. 2.1. Schematic of (a) band structure and (b) polarization charges in III-nitride heterostructure.

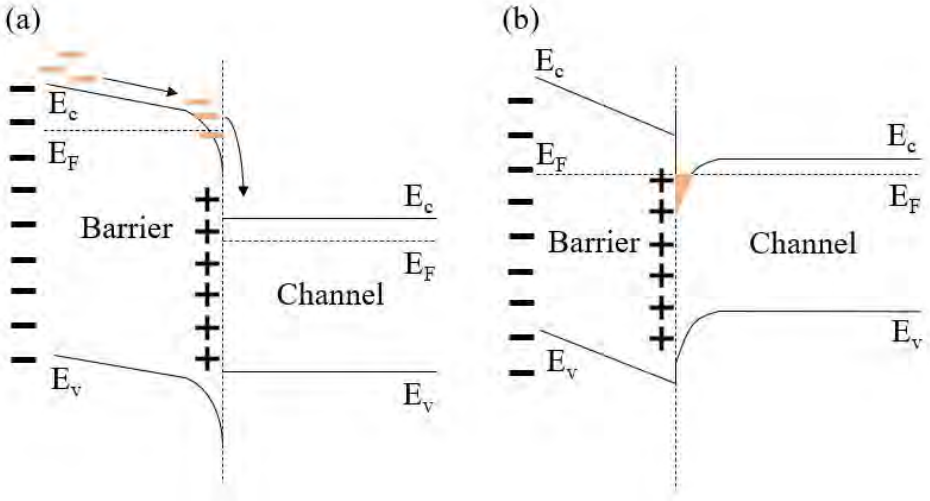

Fig. 2.2. Illustration of (a) electron migration due to band structure offset and polarization field, and (b) the formation of 2DEG in energy well.

In addition to the E_c offset between the barrier and the GaN channel, polarization fields within the III-nitride also play an important role in 2DEG formation. III-nitride materials possess a wurtzite crystal structure, inherently asymmetric in its lattice. This asymmetry gives rise to variations in electronegativity between distinct atoms. As a result, asymmetrical, dipole-like electron clouds emerge, known as the spontaneous polarization field (P_{sp}). Another type of polarization field in the III-nitride heterostructure is the piezoelectric polarization (P_{pz}), which arises due to the strain built within the barrier. The total polarization field (P_{tot}) is then defined as the sum of P_{sp} and P_{pz} [24].

The crystal orientation of GaN can be either Ga-faced or N-faced. For this thesis, all epi-structures grown using MOCVD were Ga-faced. The direction of P_{sp} in both AlGaN and GaN are from the Ga-face to the N-face, and is considered negative [24]. P_{pz}, for tensile strained barriers, has been verified to be negative [25]. Since the lattice constant of AlGaN is smaller than that of GaN, AlGaN grown on GaN is a tensile-strained barrier exhibiting a negative P_{pz}. The P_{tot} of the AlGaN barrier on GaN induces positive polarization charges on the AlGaN side at the AlGaN/GaN interface, and negative charges on the AlGaN barrier surface. This gives rise to an internal electric field (as shown in Fig. 2.1b). This internal field alters the band structure, prompting electrons to move to the GaN that has a lower energy state. These electrons then accumulate at the AlGaN/GaN interface, culminating in the formation of a 2DEG in the energy well (Fig. 2.2). Generally, a higher Al content and increased thickness of the AlGaN barrier lead to a more pronounced polarization-induced 2DEG concentration [26]. However, an AlGaN barrier with a higher Al content displays a larger lattice mismatch to GaN, constraining the maximum usable thickness before a barrier relaxation occurs. Since P_{pz} arises from strain, both the GaN cap layer and any added passivation layer on the barrier layer significantly influence the 2DEG formation and its properties [27].

Electron mobility (μ), electron density (n_s), and sheet resistance (R_{sh}) are standard metrics to gauge the performance of 2DEG. These characteristics can be measured using contactless Hall measurements (Leighton), eddy current measurements, and van der Pauw structure with Hall effects measurement. The effective μ encompasses various scattering effects, such as phonon scattering, interface scattering, carrier-carrier scattering, and impurities scattering [28-30]. Phonon scattering is triggered by lattice vibrations and is notably influenced by device operation and ambient temperature. The quality (particularly roughness) at the interface between the barrier and channel also imposes a limit on μ. High n_s values increase the likelihood of electron collisions, resulting in carrier-carrier scattering. Sometimes, higher n_s tends to extend into the barrier, which will lead to more pronounced alloy scattering. Impurity scattering originates from unintentional contaminants introduced during epi-structure growth. Thus, a GaN channel of high structural quality and minimal unintentional impurities is crucial to alleviate the scattering mechanisms. The sheet resistance can be derived from equation 2.1:

$$R_{sh} = \frac{1}{q \cdot n_s \cdot \mu} \tag{2.1}$$

where q represents the elementary charge (approximately $1.6 \cdot 10^{-19}$ C).

2.2 GaN HEMTs fabrication

The processes for fabricating GaN HEMTs on an epi-structure encompass the following steps in this thesis: deposition of the passivation layer, device isolation, formation of ohmic contacts, gate definition, and the creation of contact pads. It should be noted that this thesis does not cover the air bridge process for multi-finger devices or backside processes, which include substrate thinning and via-hole creation.

The passivation layer can be fabricated using either a "passivation-first" or "post-gate passivation" process scheme. Compared to the post-gate passivation scheme, the passivation-first approach offers better protection to the epi-structure against potential damage and contamination during processing [31]. Additionally, the deposition temperature of the passivation layer constrains the methods available for the post-passivation scheme, as elevated temperatures might degrade the ohmic and gate contacts.

Device isolation in GaN HEMTs can be achieved through either ion implantation or mesa recessed isolation methods. Ion implantation achieves isolation by bombarding the epi-structure outside the device's active area with high-energy ions, such as H+, He+, F+, Mg+, Ar+, N+, or O+. This process introduces defects and damages the structure, leading to material insulation [32]. By contrast, mesa recessed isolation is implemented using a dry etching process, which removes the 2DEG, a portion of the GaN channel, and some of the buffer. While ion implantation offers the advantage of a smooth surface morphology, mesa isolation can encounter some troubles such as gate leakage currents at the mesa sidewall and potential issues with the robustness of gate structure formation.

Ohmic contacts for HEMTs can be fabricated using either alloyed-based metal contacts or regrowth n-GaN contacts as source and drain terminals. Alloy-based contacts require annealing at high temperatures. These characteristics dictate that the formation of ohmic contacts must precede the gate process or ion implantation isolation to avoid potential gate degradation and inadvertent recovery of intentionally damaged crystal structures during annealing. On the other hand, regrowth n-GaN contacts involve Si doping during the GaN regrowth process, achieved either through molecular beam epitaxy (MBE) [33] or Metal organic chemical vapor deposition (MOCVD) [34, 35]. Though this method provides better precision, reduced resistance, improved reliability, and thermal stability, its complexity including soft mask, hard mask, dry etching, extra cleaning, pretreatment, and n-GaN growth makes it less attractive for commercial production of cost-driven large gate length devices compared to alloyed-based contacts.

In high-frequency GaN HEMTs, an Schottky field plate gate is a common choice. The nickel/gold (Ni/Au) metal stack is frequently utilized as the Schottky gate. Nickel offers excellent adhesion and a substantial work function, which produces a high Schottky barrier height. Meanwhile, gold provides excellent conductivity, leading to reduced gate resistance. To further enhance device reliability, other high work function metals such as palladium (Pd), iridium (Ir), and platinum (Pt) are often interposed between the Ni and Au layers. Another critical consideration for device performance is the parasitic capacitance induced by the gate. An advanced

mushroom gate structure, in comparison to the field-plate gate, can effectively decrease this capacitance. When considering power switching applications, a normally-off device is preferred. This can be realized with a gate deposited on a partially removed barrier or on a p-GaN cap layer.

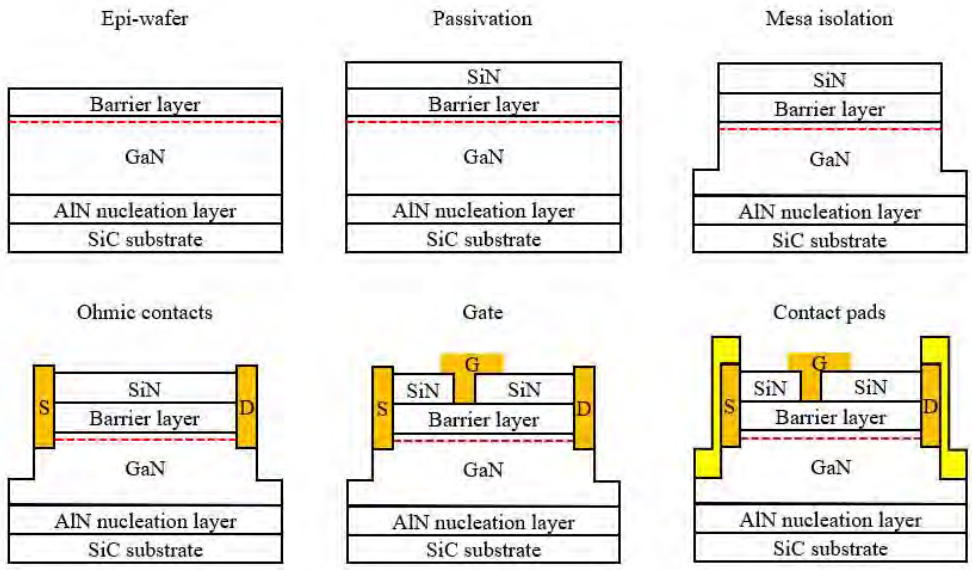

Fig. 2.3. Process steps of GaN HEMTs in this thesis.

In this thesis, a passivation-first process scheme was selected to fabricate GaN HEMTs, as depicted in Fig. 2.3. Initially, the epi-structure underwent standard cleaning processes (SC1 and SC2) and diluted NH_3 dipping. This was followed by an in-situ NH_3 pre-treatment and SiN deposition in LPCVD, the details of which will be covered in Chapter 4. Using mask-free laser writer photolithography, the device's active area was delineated, and then mesa recessed isolation was achieved through inductively coupled plasma-reactive ion etching (ICP-RIE). Two different plasma chemistries were used in this step: a fluorine-based one for the SiN and a chlorine-based one to etch the epi-structure, targeting a mesa depth of approximately 120 nm below the 2DEG. For the source and drain terminals, a Ta-based deeply recessed sidewall ohmic contact was used that required low annealing temperature. After defining the terminals using photolithography, the SiN and the epi-structure's barrier layer were opened up with ICP-RIE. Following a wet chemical oxide etching procedure using diluted buffer oxide etchant (BOE) and HCl, metal stacks of Ta/Al/Ta were deposited using an electron beam thermal evaporator. The annealing process was executed in a rapid thermal processing (RTP) system under N_2 ambient conditions. Further details on this topic will be explored in Chapter 3. The gate's design involved a two-step e-beam lithography process, first determining the gate length and then the gate's field-plate. A fluorine-based plasma etched the SiN, effectively defining the gate length. Subsequently, another round of e-beam lithography enabled the metallization of the Ni/Pt/Au Schottky gate metal stacks, resulting in a field-plate gate structure (Fig 2.3). The fabrication was finalized with an in-situ Ar^+ plasma cleaning to remove native surface oxide followed by the sputtering deposition of Ti/Au contact pads for device characterization.

2.3 GaN HEMTs characterizations

2.3.1 DC characterization

The DC-IV characteristics are the most basic method for evaluating the electrical performance of a transistor. As depicted in Fig. 2.4a, these characteristics provide insights into drain-source current (I_{DS}), on resistance (R_{on}), and drain-source resistance (R_{DS}). The I_{DS} is recorded over a range of gate-source voltages (V_{GS}) and drain-source voltages (V_{DS}). The saturated I_{DS} primarily depends on the properties of the 2DEG. In scenarios where V_{GS} and V_{DS} are both high and in the saturation region, any reduction in I_{DS} can often be attributed to inefficient thermal dissipation. Conversely, in the saturation region with a low V_{GS} and high V_{DS}, R_{DS} can be derived using equation 2.2:

$$R_{DS} = \frac{\delta V_{DS}}{\delta I_{DS}} \tag{2.2}$$

In the analysis of transistor characteristics, the drain-source resistance (R_{DS}) is instrumental in examining the short channel effects. These effects can be a limiting factor for the range of the high frequency load-line swing. A significantly lower R_{DS} value is indicative of pronounced short channel effects. Meanwhile, in the linear operational region of the transistor, the on resistance (R_{on}) provides valuable insights. Specifically, it helps identify the position of the knee voltage ($V_{DS\text{-}knee}$) and the knee current ($I_{DS\text{-}knee}$), both of which are crucial parameters for the load-line swing in microwave power amplifier (PA) applications. The transconductance (g_m), a measure of the capability of the transistor to control the current flow between the drain and source for given change in gate-source voltage, is given by equation 2.3. The higher the transconductance, the more effective the transistor is at modulating the current flow, making it a critical parameter in microwave HEMT evaluations.

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} \tag{2.3}$$

A higher g_m translates to a potentially higher cut-off frequency (f_T) and maximum oscillation frequency (f_{max}), which can be calculated as:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{2.4}$$

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_{in}+R_s+R_g}{R_{ds}}}+2\pi f_T R_g C_{gd}} \tag{2.5}$$

where C_{gs} and C_{gd} are intrinsic gate-source and gate-drain capacitance, respectively. R_s and R_g are extrinsic source and gate resistance, respectively. R_{in} and R_{ds} are intrinsic input and drain-source resistance, respectively. f_T represents the frequency at which the current gain of the transistor drops to unity, and is a commonly used figure of merit to characterize the potential speed of a transistor. Meanwhile, f_{max} gives the frequency at which the power gain drops to unity, indicating the upper limit where the transistor can effectively operate as an amplifier. Both parameters are crucial for high-frequency applications, such as RF amplifiers and oscillators.

In addition to the aforementioned characteristics, the off-state breakdown voltage (V_{BR}) is another pivotal parameter when assessing GaN HEMTs. The V_{BR} refers to

the V_{DS} at which a sudden rise in the I_{DS} occurs when the device is in its off state, i.e., when the V_{GS} pinches off the channel. During this characterization, the device remains in the pinch-off state, and V_{DS} gradually increases until the I_{DS} meets or surpasses a compliance level, typically set at 1 mA/mm for microwave transistor. A higher V_{BR} suggests that the device can handle larger voltages without undergoing catastrophic failure, indicating its robustness and reliability. The V_{BR} plays a critical role in defining the maximum load-line swing for a microwave transistor, representing the boundary at which the device transitions from its normal operational state to a breakdown regime. The ability to achieve a high V_{BR} directly correlates to the device's capacity to operate at higher power density levels and maintain its integrity. In power applications, transistors often face high-voltage scenarios, and a strong V_{BR} ensures that the device can handle these stresses without undergoing catastrophic failure. Hence, V_{BR} is a good indicator of the device's robustness and reliability in demanding conditions typical of power electronics.

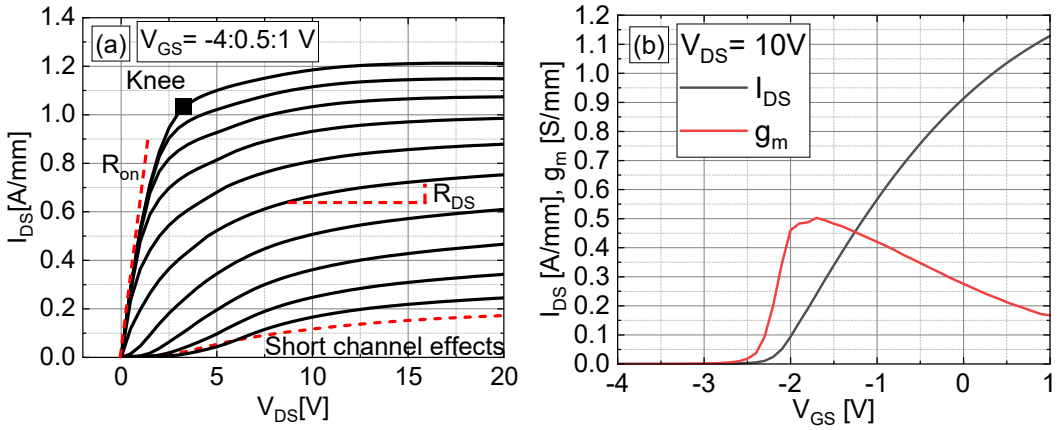

Fig. 2.4. Illustration of (a) DC-IV and (b) g_m characteristics.

Short channel effect

Decreasing the gate length (L_g) and increasing V_{DS} can result in the short channel effect. This effect occurs when electrons, propelled by the potent electric field produced by V_{DS}, traverse beneath the depletion region created by the reverse V_{GS}. As the L_g becomes shorter, the capability to deplete the channel diminishes. This situation limits the range of load-line movement, thereby reducing both the P_{out} and efficiency of HEMTs when used as power amplifiers (PA). Although reducing the barrier thickness can mitigate the short channel effect, it can also introduce tunneling leakage between the gate and channel as a downside. Hence, better 2DEG confinement requires the development of enhanced buffer designs, which will be discussed in the CH5.

During DC-IV measurements, the short channel effects can often be found in regions with high V_{DS} and low I_{DS} (as depicted in Fig. 2.4a). However, quantifying these effects directly using only the DC-IV characteristics can be challenging. Instead, the transfer characteristic offers a more insightful approach to assessing these short channel effects (illustrated in Fig. 2.5). In this method I_{DS} is measured against V_{GS}, with the I_{DS} values presented on a logarithmic scale on the Y-axis. As

V_{DS} increases, a more negative V_{GS} is required to achieve device pinch-off. The phenomenon of drain induced barrier lowering (DIBL) can be quantified using equation 2.6:

$$DIBL = \left| \frac{V_{po}^{high} - V_{po}^{low}}{V_{DS}^{high} - V_{DS}^{low}} \right| \tag{2.6}$$

which uses the pinch-off voltage (V_{po}) at V_{DS}^{low} and V_{DS}^{high} with the pinch-off criteria, typically I_{DS}= 1 mA/mm. The DIBL effect refers to the reduction in the pinch-off voltage (V_{po}) of a transistor due to an increase in the V_{DS}. As devices scale down (smaller L_g), short channel effects become more pronounced, impacting the device's performance. A larger DIBL value indicates a more pronounced short channel effect, which might pose constraints on the load-line swing in PA applications.

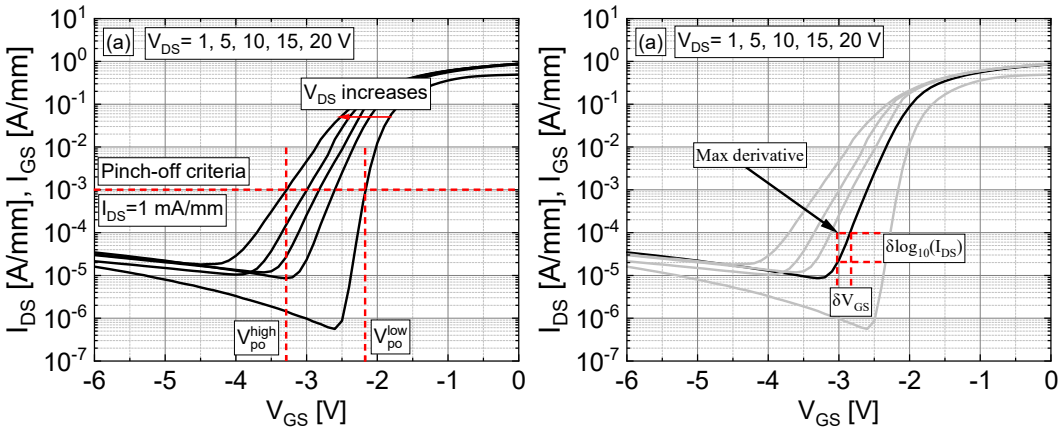

Fig. 2.5. Illustration of (a) DIBL and (b) SS extraction.

Another metric for assessing short channel effects is the subthreshold swing (SS), calculated using equation 2.7:

$$SS = \frac{\delta V_{GS}}{\delta \log_{10} I_{DS}} \tag{2.7}$$

SS quantifies the change in V_{GS} relative to the logarithmic change in I_{DS} below the V_{po}. This value is determined at the point of maximum derivative within the transfer characteristics, expressed in units of mV/decade. A lower SS value signifies enhanced pinch-off capabilities for the device, whereas a higher value suggests the opposite.

2.3.2 Trapping effects characterization

Trapping effects lead to phenomena such as current collapse, knee walk-out, and dynamic R_{on} degradation, all of which limit the high-frequency performance of HEMTs as illustrated in Fig 2.6 [36]. These effects can be characterized using a pulsed-IV system (AMCAD AM3200), which provides gate and drain voltage pulses at a quiescent point (pinch-off condition, $V_{GS} < V_{po}$) and an active point (on-condition, $V_{GS} > V_{po}$), while measuring the I_{DS}. Under the pinch-off condition for the quiescent point, the traps are filled due to the electric field induced by the quiescent bias points (V_{GSQ}, V_{DSQ}). This condition also facilitates nearly thermal-free

characterization. When the device is switched on at an active point, the pulse duration is sufficiently short to prevent heat generation. The typical duty cycle (equation 2.8) between the quiescent point and active point is kept below 1% to ensure the device is adequately cooled down.

$$duty\ cycle\ [\%] = \frac{pulse\ width\ at\ active\ point}{pulse\ width\ at\ quiescent\ point} \times 100 \tag{2.8}$$

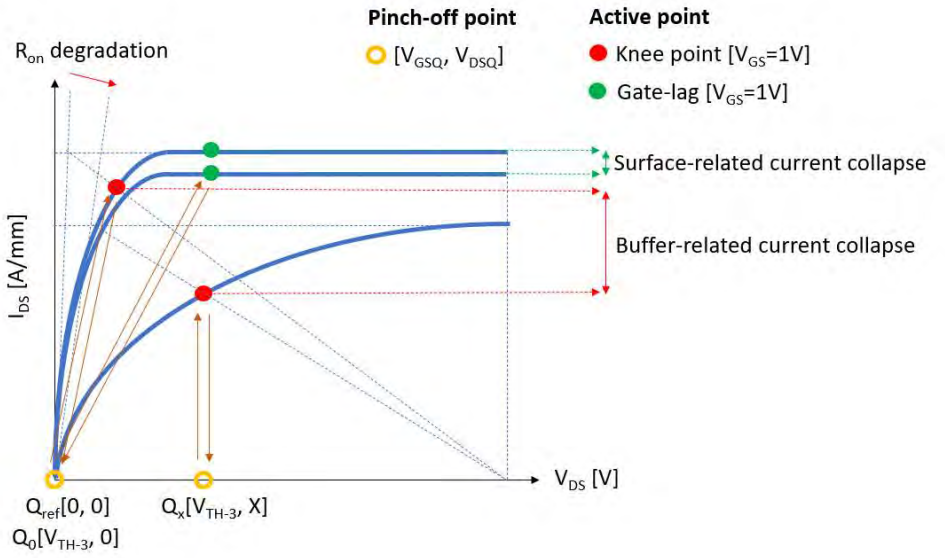

Fig. 2.6. Illustration of the characteristics of trapping effects of GaN HEMTs in pulsed IV measurements.

To assess the traps mainly related to the surface, two specific quiescent points are used on HEMTs: (V_{GSQ}, V_{DSQ}) of (0, 0), known as Q_{ref}, and (V_{TH}-3, 0), referred to as Q_0. The V_{DSQ} is maintained at 0 V to avoid activating the buffer-related traps. The current collapse associated with surface-related phenomena, denoted as Z_1 (represented by green dots in Fig 2.6) and also termed gate-lag, is defined as follows:

$$Z_1\ [\%] = \left|\frac{I_{DS}(Q_0) - I_{DS}(Q_{ref})}{I_{DS}(Q_{ref})}\right| \cdot 100 \tag{2.9}$$

When a drain voltage is applied under pinch-off conditions with quiescent biases, specifically (V_{GSQ}, V_{DSQ}) of (V_{TH}-3, X), termed as Q_X, the trap states within the buffer become occupied. This leads to the buffer-related current collapse, denoted as Z_2. Also referred to as drain-lag, it is defined as:

$$Z_2\ [\%] = \left|\frac{I_{DS-knee}(Q_X) - I_{DS-knee}(Q_{ref})}{I_{DS-knee}(Q_{ref})}\right| \cdot 100 \tag{2.10}$$

where $I_{DS\text{-}knee}$ is the current at knee point (red dots in Fig 2.6). Moreover, buffer-related trapping effects also lead to knee walk-out and degradation of dynamic R_{on}, which are commonly defined as:

$$Knee - walkout\ [V] = V_{DS,knee}(Q_X) - V_{DS,knee}(Q_{ref}) \tag{2.11}$$

$$dynamic\ R_{on}\ \text{degradation}\ [\%] = \left|\frac{R_{on}(Q_X) - R_{on}(Q_{ref})}{R_{on}(Q_{ref})}\right| \cdot 100 \quad (2.12)$$

where knee points ($V_{DS\text{-}knee}$) are defined as red dots in Fig. 2.6.

2.3.3 Drain current transient measurement

A technique to pinpoint the time constant and the energy state of traps has been developed as drain current transient (DCT) measurements, which use varying filling time durations and ambient temperatures [37]. Conducted using the AMCAD AM3200 in a temperature-controlled chamber, this method stresses the device under pinch-off conditions with a high V_{DSQ} for varying time spans. Given the pinch-off state of the device, thermal effects are negligible. Following the stress period, the device is transitioned to an active bias point (corresponding to PA operation biases, such as the knee point, the class-AB operation point, or linear region). Throughout this phase, the I_{DS} is tracked over a time span that is pertinent to modulated PA operation frequency. Typically, a lower stress bias is indicative of surface region traps, while a higher stress bias includes traps at both surface and buffer regions. As the stress is alleviated, electrons are de-trapped, causing a rise in the I_{DS} (as depicted in Fig. 2.7).

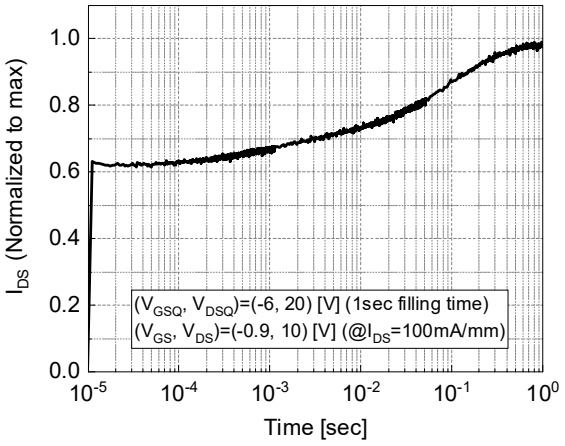

Fig. 2.7. Illustration of DCT measurement.

From the measured I_{DS}, the time constant of traps can be obtained by the following stretch model [37]:

$$I_{DS}(t) = I_{DS,final} - \sum_{i=1}^{N} A_i \cdot e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \quad (2.13)$$

where $I_{DS}(t)$ represents the I_{DS} observed after stress release, and $I_{DS,\,final}$ denotes the final monitored I_{DS} following a set time period. The amplitude of the trapping effects is symbolized by A_i, while τ_i is the time constant associated with the traps. β_i is the nonexponential stretching factor, which falls between 0 and 1, corresponding to the N identified processes in which electrons are either trapped (when A_i is positive) or released (when A_i is negative).

With the obtained time constant (τ_i) and applied different ambient temperature correction [38], the activation energy (E_a) and the capture cross section σ_n can be extracted by the Arrhenius' equation [38]:

$$\ln(\tau_i T^2) = \ln\left(\frac{h^3}{2(2\pi)^{\frac{3}{2}}\sqrt{3}m_e k_B \sigma_n}\right) + \frac{E_a}{k_B T} \tag{2.14}$$

where T is temperature, h is the Planck's constant, m_e is the effective mass of carriers ($0.22m_0$), and k_B is the Boltzmann constant. All data points measured at different T can be plot as Arrhenius plot with the X-axis of $q/k_B T$ and Y-axis of $\ln(\tau_i T^2)$. The slope of the data points is the E_a, while the σ_n can be extrapolated from the interception on Y-axis. The extracted E_a and σ_n can be compared to literatures to analyze the possible location and the formation mechanism of the traps [37].

2.3.4 Small-signal characterization

Small signal measurements on HEMTs are conducted using a high-frequency signal with power typically ranging from -10 to -20 dBm to ensure minimal non-linear behavior. These measurements aim to extract parameters such as f_T and f_{max}, and an equivalent small-signal circuit model by measuring the HEMTs' scattering parameters (s-parameters). The f_T is determined at the point where the current gain (h_{21}) reaches 0 dB. The h_{21} value is derived from the s-parameters as expressed in equation 2.15:

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{2.15}$$

The definition of f_{max} requires the consideration of device stability factor (K) and Δ, which are defined as:

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}||S_{21}|} \tag{2.16}$$

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}| \tag{2.17}$$

If K > 1 and Δ <1, the device is stable, and vice versa. If the device is stable over the measured frequency of s-parameters, the f_{max} can be extrapolated when maximum available gain (MAG) becomes 0 dB. The MAG is defined as:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2-1}\right) \tag{2.18}$$

If the device is unstable, the f_{max} can be extrapolated when unilateral power gain (U) or so-called Mason's gain becomes 0 dB. The U is defined as:

$$U = \frac{|S_{21}|^2}{(1-|S_{11}|)^2(1-|S_{22}|)^2} = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2K\left|\frac{S_{21}}{S_{12}}\right|-2Re\left(\frac{S_{21}}{S_{12}}\right)} \tag{2.19}$$

To extract the small signal equivalent circuit model (Fig. 2.8) through s-

parameters measurements, the bias independent extrinsic part of circuit is de-embedded through two additional cold-FET measurements including pinch-off condition and forward condition as defined:

#1. Pinch-off condition:

V_{GS}= (V_{po}-6) V

V_{DS}=0 V

#2. Forward condition:

V_{GS}= from 0 to 2 V (V_{GS} sweeps until I_{GS}= 1 mA/mm)

V_{DS}=0 V

Upon removing the extrinsic components, the bias-dependent intrinsic portion is ascertained through the direct extraction method outlined in [39]. Given that the intrinsic component is only applicable for a single bias point, this thesis employs the bias point that results in the f_{max} for comparing devices. The influences of varying intrinsic parameters will be elaborated upon in Chapters 4 and 5. By employing diverse bias points, small signal equivalent circuits serve as the preliminary method for simulating the large signal non-linear circuit model.

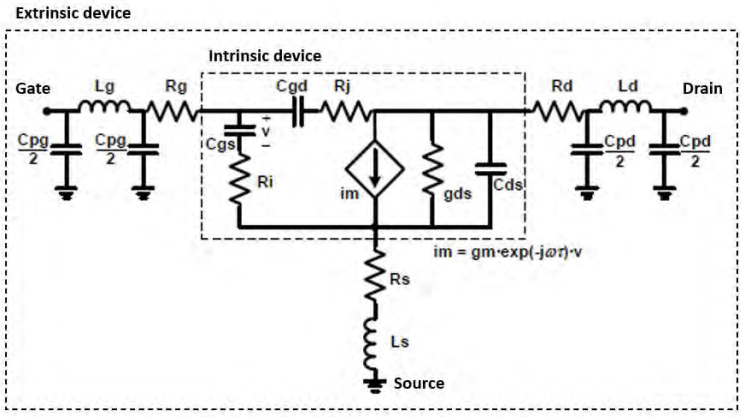

Fig. 2.8. Equivalent small signal circuit model for GaN HEMTs [39].

2.3.5 Large-signal characterization

The non-linear large signal measurements offer insights into the high-frequency capabilities of GaN HEMTs when functioning as a microwave power amplifier. In this thesis, parameters such as RF output power (P_{out}), gain, and power added efficiency (PAE) are characterized by load-pull measurements. The operational class of the device is determined by the I_{DSQ}, which is regulated by V_{GS}. When the HEMT operates in Class-A (conducting throughout the full cycle), it delivers the highest gain and P_{out} but has the lowest efficiency. On the other hand, Class-B operation, where the HEMT conducts for half a cycle, exhibits the opposite performance. This

thesis primarily focuses on Class-AB operation, which maintains a balance between the performances mentioned earlier. For an ideal Class-A operation (max 50% efficiency), the maximum P_{out} can be estimated as:

$$P_{out,class-A} = \frac{V_Q}{\sqrt{2}} \times \frac{I_Q}{\sqrt{2}} = \frac{1}{2} \times \frac{V_{max}}{2} \times \frac{I_{max}}{2} \cong \frac{(V_{BR} - V_{DS,knee}) \cdot (I_{DS,knee} - I_{po})}{8} \tag{2.20}$$

where V_{BR} is the breakdown voltage and I_{po} is the pinch-off current.

Under this condition, the operation voltage (V_{DSQ}) is set as:

$$V_{DSQ} = \frac{V_{br} + V_{DS,knee}}{2} \tag{2.21}$$

So, the RF signal is able to swing the entire load line (Fig. 2.9). The PAE is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.22}$$

where P_{in} is the RF power added to the input of HEMT, while the P_{DC} is the DC power consumption defined as:

$$P_{DC} = I_{DSQ} \cdot V_{DSQ} \tag{2.23}$$

Also, the drain efficiency (η_{eff}) is defined as:

$$\eta_{eff} = \frac{P_{out}}{P_{DC}} \tag{2.24}$$

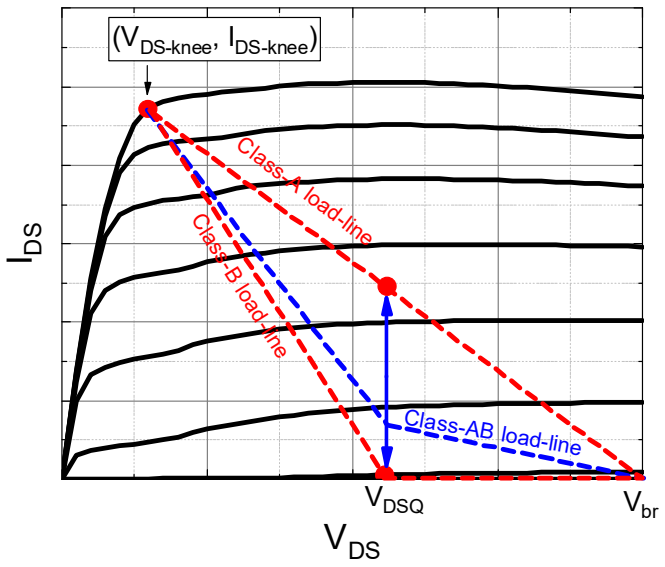

Fig. 2.9. Illustration of large signal operations in HEMTs under different operation classes.

Chapter 3

Ohmic contacts for GaN HEMTs

3.1 Introduction of ohmic contacts

Good ohmic contacts, characterized by a low contact resistance (R_c), are crucial for transistors that operate at high frequencies with high power density. A reduced R_c in ohmic contacts enhances the device's output power, efficiency, and reduces noise and heat generation. However, forming ohmic contacts on wide bandgap III-nitride semiconductors is challenging due to the substantial Schottky barrier height (Φ_B) present at the metal-semiconductor interface [40]. In contrast to intrinsic Si (i-Si), which has a smaller bandgap energy of 1.1 eV and a minor energy offset between the conduction band and the Fermi level, intrinsic GaN (i-GaN) possesses a large bandgap of 3.4 eV. This results in a significantly higher Φ_B and a reduced thermionic electron transport probability. Additionally, the broader width of the depletion region (W_d) caused by band bending beneath the metal-GaN junction further diminishes the electron tunneling probability (see Fig. 3.1).

Lowering the Schottky barrier height is one method to achieve low R_c ohmic contacts. This can be accomplished by choosing metals with a smaller work function (Φ_M), such as Ti (4.33 eV) and Ta (approximately 4.0-4.8 eV) [40, 41]. Another alternative is to adjust the Fermi level in GaN through intentional Si doping methods. These methods include regrown contacts [3], Si ion-implantation [6], and epitaxially grown Si-doped GaN [42]. This leads to n-GaN having a reduced depletion region width (shorter tunneling distance), which is inversely proportional to the n-type doping concentration (N_d) in the semiconductor:

$$W_d \propto \frac{1}{\sqrt{N_d}} \tag{3.1}$$

Nitrogen vacancies, which serve as n-type doping agents [7, 43], can also form during the annealing process of metal ohmic contacts. Metals used in ohmic contacts, such as Ti and Ta, extract nitrogen from GaN to produce TiN and TaN, thereby generating nitrogen vacancies. The work functions of Ti-N and Ta-N have been reported to be 3.74 eV and 4.75 eV, respectively, which contribute to a decreased Φ_B [44, 45]. However, an excessive amount of Ti in the bottom layer can result in the creation of voids beneath the TiN [43]. In the formation of ohmic contacts on AlGaN/GaN heterostructures, the Al layer plays multiple roles when combined with Ti and Ta. Al is frequently used in ohmic metal stacks, where it aids in a smooth transition of the work function and further promotes the extraction of nitrogen from GaN in the form of the Al-N phase. Yet, when Al is present in the metal stacks, it alloys with the Ti layer, causing Ti to lose its reactivity with GaN [43]. Conversely, the presence of Al in the AlGaN barrier hinders the extraction of N, given that the Al-N bond is stronger than the Ti-N bond. This protects the 2DEG from degradation during high-temperature processing. As a result, the thickness ratio between Ti or Ta and Al needs optimization. A limitation of using Al is that annealing temperatures exceeding its melting point (660 °C) often lead to inferior surface morphology and edge precision, posing challenges to the downscaling of the source-drain distance in HEMTs.

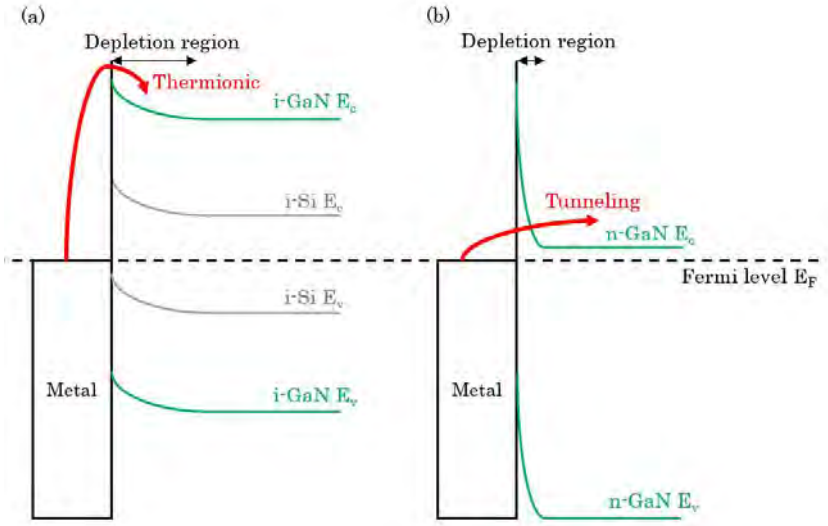

Fig. 3.1. Schottky barriers and band structures of (a) i-GaN and i-Si with thermionic transport dominated, and (b) n-GaN with Tunneling transport dominated.

The transmission line measurement (TLM) is a widely used method for characterizing the electrical properties of ohmic contacts. Through this technique, parameters such as R_c, R_{sh}, specific contact resistance, and transfer length can be accurately extracted [46]. A TLM characterization structure, illustrated in Fig 3.2a, comprises multiple ohmic contacts spaced at increasing distances (for instance, ranging from 5 to 30 µm, labelled as d_1 to d_5). The method employs a four-probe measurement, where two probes conduct the current and the remaining two measure the voltage. This configuration directly mitigates the influence of resistance of the probes.

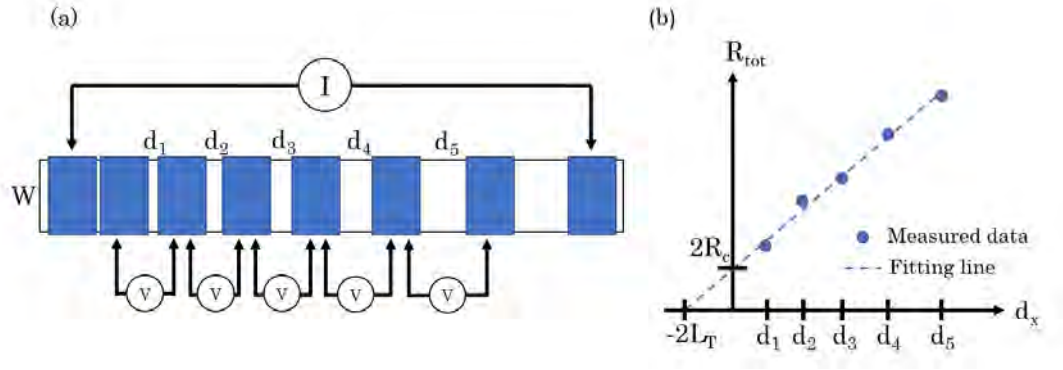

Fig. 3.2. (a) Schematic of TLM structure and (b) extrapolate method of R_c.

The total resistance (R_{tot}) for each spacing is determined from the voltage and current measurements. R_{tot} encompasses the R_c, the resistance of the ohmic metal electrodes (R_m), and the semiconductor (R_{semi}):

$$R_{tot} = 2R_m + 2R_c + R_{semi} \tag{3.3}$$

Given that R_m is typically much smaller than R_c, it can be disregarded. R_{semi} is derived from the R_{sh} of the 2DEG:

$$R_{semi} = \frac{R_{sh}}{W} \times d_x \tag{3.4}$$

By assessing R_{tot} across all spacings in the TLM structure, both R_c and R_{sh} can be extracted, as depicted in Fig. 3.2b and as per equation 3.3.

While the current flow through the semiconductor is uniform, it diminishes exponentially towards the contact edges. At the furthest edge, the current flow ceases, resulting in the current crowding effect. The transfer length (L_T), obtainable via TLM measurements as shown in Fig 3.2b, represents the average distance that carriers traverse from the semiconductor to the contact. An effective area can be deduced as L_T multiplied by W. Subsequently, the contact resistivity (ρ_c) is computed as:

$$\rho_c = R_c \times L_T W \tag{3.5}$$

3.2 Ohmic process and design

3.2.1 Planar contacts

The fabrication of planar contacts involves lithography, metal deposition, and annealing. During the lithography phase, the region designated for the ohmic is exposed, and after metal deposition, a lift-off process is conducted. Various pretreatments are employed within the exposed area, including both wet chemical and plasma methods. Wet chemical treatments such as HF, buffered HF, HCl, HNO_3, H_2SO_4, KOH, NaOH, NH_4OH, and $(NH_4)_2S_x$ aim to reduce surface contamination linked to carbon or oxygen [12, 47-51]. Plasma pretreatments,

encompassing H_2, N_2, O_2 (descum), Cl-based, SF_6, and Ar, have been designed to eliminate the surface's native oxide layer, any lithography residue, and to restore surface dangling bonds, enhancing surface termination and Ga-N stoichiometry [4]. Beyond surface pretreatment, Si ion-implantation has been introduced for both planar and recessed contacts prior to metal deposition. This process transforms the surface i-GaN into n-GaN, resulting in a more concise tunneling path [6]. Yet, activating the implanted Si demands high-temperature annealing (exceeding 1000°C). This is problematic as it can degrade the epitaxial properties since the epitaxial growth temperature is typically within a similar range. Ohmic metal stacks can be deposited via evaporation or sputtering, with further details on the metal stack design provided in section 3.2.3. Subsequently, the annealing of the ohmic metal stacks is executed in a rapid thermal processing (RTP) system in an oxygen-free environment. Commonly, either Ar or N_2 serve as ambient gases during this high-temperature procedure.

The creation of planar ohmic contacts with a low R_c can face issues in reproducibility and uniformity due to variations in barrier design and thickness. Broadly, a thicker barrier extends the tunneling distance between the metal and 2DEG. An increased Al content in the AlGaN barrier heightens the barrier height, leading to a diminished thermionic transport probability. In certain cases, an AlN exclusion (spacer) layer is introduced between the barrier layer and the 2DEG to further confine the 2DEG and provide a sharp interface. This additional layer can exacerbate the challenge of crafting ohmic contacts with a low R_c. Such complexities underscore the necessity for alternative strategies, such as deeply recessed sidewall contacts, as discussed in [Paper A and B].

3.2.2 Recessed contacts

While annealing in planar contacts can transform the barrier into an n-type semiconductor by producing nitrogen vacancies in the AlGaN/GaN barrier, the distance remains substantial, hindering efficient electron tunneling to the 2DEG. To address this, shallow recessed contacts have been introduced. These contacts minimize the tunneling distance by etching the barrier of the epi-structure using Cl-based dry etching through inductively coupled plasma-reactive ion etching (ICP-RIE). A reduced barrier thickness shortens the tunneling distance between the metal and the 2DEG, as illustrated in Fig. 3.3a. However, this thinning also diminishes the 2DEG concentration, which can compromise the carrier density required for optimal tunneling transportation. As a result, a delicate balance must be considered between barrier thickness and 2DEG density, necessitating innovative approaches to achieve contacts with a lower R_c. Some studies suggest that the ideal etching depth is about 1~5nm above the 2DEG [5, 8, 52]. However, commercially available ICP-RIE systems often fail to ensure consistent and reproducible etching depths across an entire wafer. To overcome this challenge, deeply recessed contacts—which etch through the barrier to the GaN region housing the 2DEG—were explored in [Paper A and B], as depicted in Fig. 3.3b (see section 3.3). Such deeply recessed contacts are less affected by variations in etching depth since the contact area is established on the recessed sidewall.

Fig. 3.3. (a) shallow recessed contacts and a trade-off between etching depth and 2DEG density, (b) deeply recessed contacts, and (c) patterned recessed contacts [5].

A viable solution to counteract the reduction in 2DEG density due to a thinner barrier is the use of patterned recessed contacts. The dimensions of the via hole pattern are tailored to be large enough for metal deposition to reach the base, yet sufficiently compact to mitigate the effect on 2DEG density. This results in a notably low R_c of 0.12 Ω·mm when utilizing Ti-based metal stacks, however, with a drawback of process complexity [5].

Regrown contacts present another innovation, merging the techniques of recess etching and Si n-type doping. This approach achieves an exceptionally low R_c (less than 0.1 Ω·mm), in contrast to traditional alloyed ohmic contacts which typically have a R_c exceeding 0.1 Ω·mm. This is achieved by lattice-matching the regrowth of n-GaN with a high concentration of Si-dopants using either molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) within the recessed region. This process furnishes an abundant electron supply while simultaneously minimizing the tunnelling distance between the semiconductor and the contact metal situated atop the regrown n-GaN [3, 53].

3.2.3 Contact metal designs

Metal stacks need to fulfill the two requirements to form good ohmic contacts with low R_c, including a low work function of the first (bottom) metal layer and a capability of extracting nitrogen from GaN. Several reported contacts are summarized in Table 3.1.

Table 3.1. OHMIC CONTACTS EXAMPLES REPORTED IN LITERATURE.

	Metal stacks	$Al_xGa_{1-x}N$ barrier [x], [nm]	AlN exclusion layer [nm]	Anneal temperature [°C]	R_c [Ω·mm]	Contact categories	Ref	Year
A	Ti/Al/Ni/Au	26%, 18	0	825	0.18	Planar contact	[54]	2013
B	Ti/Al/Ni/Au	30%, 25	0	830	0.1	Planar contact with plasma treatment	[4]	2018
C	Ti/Al/Ni/Au	30%, 24	1	850	0.12	Patterned shallow recessed contact	[5]	2018
D	Ti/Al/Ni/Au	30%, 27	0	Without anneal	0.4	Recessed, Si ion implantation	[6]	2006
E	Si/Ge/Ti/Al/Ni/Au	23%, 18	0	820	0.3	Planar contact	[55]	2017
F	Ta/Si/Ti/Al/Ni/Ta	26%, 18	0	850	0.22	Planar contact	[54]	2013
G	Ti/TiN	20%, 20	2	850	0.13	Planar contact	[56]	2014
H	Ti/TiN	35%, 20	0	850	0.6	Planar contact	[56]	2014

I	Ti/Al/Ti/TiN	25%, 20	1	550	0.21	Shallow recessed contact	[52]	2018
J	Ti/Al/W	26.4%, 23	0	500	0.35	Planar contact	[57]	2018
K	Ti/Al/Ni/TiN	23%, 19	1	830	1.1	Planar contact	[58]	2020
L	Ti_5Al_1/TiN	25%, 20	0	880	0.06	Planar contact	[59]	2020
M	$TiAl_3$/Au	20%, 22	0	850-900	0.23	Planar contact	[60]	2024
N	Ta/Al/Ta	25%, 25	0	575	0.28	Planar contact	[7]	2011
O	Ta/Al/Ta	14%, 22	0	550	0.06	Planar contact	[7]	2011
P	Ta/Al/Ta	30%, 15	0	550-600	0.21/0.27	Shallow recessed contact	[61]	2015
Q	Ta/Al/Ta	25%, 20	0	575	0.24	Deeply recessed contact	[Paper B]	2018
R	Ta/Al/Ta	25%, 19	1	575	0.21	Deeply recessed contact	[Paper B]	2018
S	Ta/Al/Ta	30%, 11	1	575	0.25	Deeply recessed contact	[Paper B]	2018
T	Ti/Al/Ti	30%, 11	1	550	0.14	Deeply recessed contact	[Paper A]	2023
U	Ti/Al/Ti	52%, 3.5	1.5	550	0.15	Deeply recessed contact	[Paper A]	2023
V	Ti/Al/Ni/Au	25%, 20	1	810	0.16	Shallow recessed contact	[62]	2024
W	--	25%, 22	0	Without anneal	0.2	MBE regrown contact	[63]	2011
X	Ti/Au	InAlN/GaN	0	Without anneal	0.05	MBE regrown contact	[3]	2020
Y	--	--	0	Without anneal	0.1	MOCVD regrown contact	[53]	2020

Conventional Ti/Al/Ni/Au contacts are showcased in examples A-C. Typically, it's simpler to achieve ohmic contacts with a low R_c on epi-structures that lack an AlN exclusion layer. Example B serves as a testament to this, contrasting with Example A, and underscores the importance of thorough surface pretreatments prior to metal deposition. This involves eliminating surface oxides and contaminants. Example C depicts a resilient low R_c achieved by patterning the recessed ohmic contact. By not fully removing the barrier layer, the 2DEG remains intact. Additionally, the tunneling distance is curtailed due to the presence of the recessed pit-hole.

Examples D-F illustrate the conventional Ti/Al-based metal arrangements paired with Si, an n-type dopant for GaN. However, Si, possessing a high work function of 4.85 eV, results in a significant Φ_B [64]. This translates to a reduced probability of thermionic transport at the metal-semiconductor junction. In Example F, Si is deposited atop the Ta layer, which has a smaller work function, culminating in a R_c lower than that in Examples D and E.

Al plays a pivotal role in ohmic contacts. It facilitates the extraction of nitrogen from GaN, resulting in the formation of Ti-Al-N or Al-N phase alloys. Yet, it tends to compromise surface morphology and edge precision. To circumvent this, there have been suggestions to either eliminate Al or employ TiN, TaN, and Tungsten (W) as cap layers. This alteration improves edge sharpness, especially vital for miniaturized devices, as depicted in Examples G-K. A recent study, as referenced in Example L and M, demonstrates that co-depositing Ti and Al as an alloy, rather than discrete layers, yields superior ohmic contact. This approach achieves a lower R_c than traditional multilayer configurations.

In our study [Paper B, Example Q-S], deeply recessed Ta/Al/Ta sidewall ohmic contacts were developed with a low R_c of ~0.24 Ω·mm. The results highlight the importance of process optimization including the metal coverage, sidewall angle, metal stack thickness ratio, and annealing temperature. These works lead to the innovation of the Ti/Al/Ti ohmic contacts [Paper A, Example T and U], which will be introduced in the following section. Moreover, Example V also showed that the Ti/Al metal stacks can provide very low R_c at high annealing temperature.

Diverging from the standard metal stack ohmic contacts, regrown contacts (Examples W-Y) forgo the annealing process. This is because the barrier is entirely eradicated through dry etching. Subsequently, a heavily Si-doped n-type GaN, which is lattice-matched, is regrown using MBE or MOCVD within the recessed area. This leads to a diminished Φ_B and a concise tunneling distance. R_c values below 0.1 Ω·mm have been reported across various epi-structures. Especially noteworthy are the regrown contacts on the InAlN barrier, which boasts a 2DEG concentration surpassing the conventional AlGaN barrier, recording an impressively low R_c of 0.05 Ω·mm [3].

3.3 Deeply recessed Ti based ohmic contacts

This study exhibits an innovative strategy for fabricating Ti/Al/Ti low-resistance ohmic contacts within AlGaN/GaN HEMTs, as outlined in [Paper A]. A contact resistance of approximately 0.15 Ω·mm has been achieved and characterized using TLM structure (Fig. 3.2a and Fig 3.4). This is achieved by initially etching the barrier of the heterostructure beyond the depth of the channel, and subsequently applying Ti/Al/Ti ohmic metallization to the recessed sidewalls. Annealing of this metallization is conducted at a low temperature of 550 °C. The investigation encompasses a thorough examination of the influences exerted by the recessed sidewall angle, the respective thicknesses of the Ti and Al layers, and the specifics of the annealing process. The utility of this ohmic contact method has been verified on HEMT structures (Epi I and Epi II) as indicated in Table 3.2.

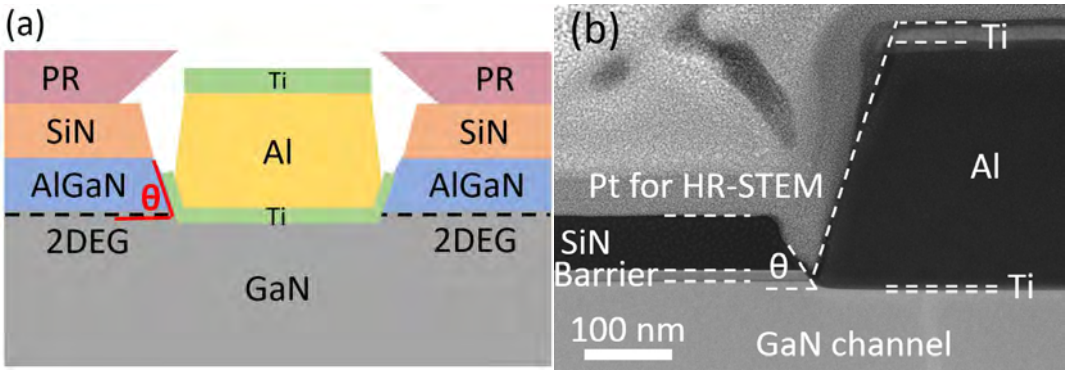

Fig. 3.4. (a) Schematic of TLM structure, (b) HR-STEM cross-section of annealed TLM with 10° tilted t_{Ti} of 3 nm on Epi II.

Table 3.2. EPI-STRUCTURE USED IN THIS WORK

	Epi I	Epi II
Cap layer	GaN, 1.4 nm	GaN, 2 nm
Barrier layer	$Al_{0.52}Ga_{0.48}N$, 3.3 nm	$Al_{0.3}Ga_{0.7}N$, 9.7 nm
Spacer layer	AlN, 1.5 nm	AlN, 1.2 nm
Channel layer	GaN, 260 nm	GaN, 255 nm
Nucleation layer	AlN, 60 nm	AlN, 60 nm
GaN RC <0 0 2>	94 arcsec	216 arcsec
GaN RC <1 0 2>	353 arcsec	443 arcsec
n_s [10^{13}/cm^2]	1.16	1.07
μ [cm^2/V·s]	1746	1966
R_{sh} [Ω/sq.]	316	298

3.3.1 TLM results

The establishment of ohmic contacts is continsgent upon the deposition of ohmic metal stacks—consisting of Ti and Al in this research—followed by an annealing process. The primary objective of annealing is to facilitate the extraction of N from the (Al)GaN, which leads to the formation of compounds such as titanium nitride (TiN), aluminum nitride (AlN), and ternary phases of aluminum-titanium nitride (AlxTiyN). This reaction sequence induces the generation of nitrogen vacancies (N-vacancies) within the (Al)GaN, which inherently function as donor-like dopants, thereby creating a conductive n-type region as referenced in [7, 65]. Nevertheless, this process is significantly influenced by the constitution of the metal stacks. Consequently, there is a pronounced interest in optimizing the thickness of the underlying Ti layer (t_{Ti}) and the Al layer (t_{Al}). Such optimization is pivotal as it facilitates the creation of N-vacancies.

In the initial experiment, samples with various thicknesses of the t_{Ti}, specifically 5, 10, and 15 nm, were fabricated on Epi I, maintaining a consistent thickness for the t_{Al} at 280 nm and the top titanium layer at 20 nm. The selection of a recessed sidewall angle (θ) of 55° was introduced by the findings of our preceding research [Paper B]. Due to the t_{Ti} being deposited at an inclination of 10°, the resultant effective thicknesses on the recessed sidewall for this layer were approximately 3, 7, and 12 nm, respectively, ascertained via Scanning Electron Microscopy (SEM). It was observed that the samples with a t_{Ti} of 15 nm exhibited the highest saturated R_c of approximately 0.6 Ω·mm. Conversely, a reduction in the t_{Ti} to 5 nm led to a substantial decrease in R_c, recording the lowest measured value of approximately 0.16 Ω·mm after undergoing a total annealing period of 6 minutes, as illustrated in Fig. 3.5a.

In the subsequent experiment, samples with a varying t_{Al} of 280, 140, and 70 nm were fabricated on Epi I, while maintaining a uniform t_{Ti} of 5 nm and a top titanium layer of 20 nm. An increment in t_{Al} beyond 280 nm was not contemplated owing to the resultant pronounced step height of the ohmic contacts, which could potentially hinder the miniaturization of the gate-source distance and complicate gate fabrication. The angle of deposition remained consistent with that of the first experiment, with identical lithography parameters being employed. It was observed that samples with a thinner t_{Al} manifested an earlier saturation of the R_c (Fig. 3.5b). Specifically, the sample with a t_{Al} of 140 nm reached a saturated R_c within 3

minutes of annealing, a swifter saturation compared to the sample with a t_{Al} of 280 nm. Notably, any annealing performed beyond the point of saturation was found to lead to a deterioration of R_c. Furthermore, the minimal R_c recorded increased from 0.16 Ω·mm to 0.35 and 0.4 Ω·mm for samples with a reduced t_{Al} of 140 and 70 nm, respectively. This effect can be ascribed to the deficient coverage of Al on the recessed sidewall, attributable to the method of metal deposition, which was conducted without tilting, leading to inadequate Al presence.

The 2DEG properties and the tunneling distance at the ohmic contact/semiconductor interface are significantly affected by the θ, which is determined by the photoresist profile (Fig. 3.4a). Varying exposure doses applied to the photoresist, while maintaining a constant reverse baking temperature of 125 °C, result in θ ranging from 47° to 63° following the recess etching process. A higher exposure dose generates a steeper photoresist profile due to the reduced dimension of undercut, leading to a steeper sidewall angle. A larger θ preserves the integrity of 2DEG characteristics but at the expense of an increased tunneling distance. Conversely, a smaller θ can reduce the tunneling distance but may compromise the 2DEG due to the remaining thin AlGaN barrier thickness after dry etching. The influence of θ on the R_c was further explored on Epi I (Fig. 3.5c). In this phase of the study, t_{Ti} of 3 and 1.5 nm was deposited with a 10° tilt, succeeded by a perpendicular deposition of t_{Al} of 280 nm and a top Ti layer of 20 nm. The samples underwent annealing using an identical procedure until R_c reached saturation. The most favorable outcome, a lowest R_c of 0.14 Ω·mm with excellent uniformity, was observed in samples with a t_{Ti} of 3 nm and a θ of approximately 55°. For θ within the 50° to 60° range, R_c remained below 0.2 Ω·mm, demonstrating high uniformity and indicating a generous process tolerance. Beyond this specified range of θ, a decline in R_c and uniformity was noted, likely due to suboptimal metal coverage on the recessed sidewall coupled with diminished electron density or a more extended tunneling distance. Samples with a t_{Ti} of 1.5 nm showed higher R_c values, a narrower θ process window, and larger variability, which is possibly attributable to the challenges associated with controlling the thickness and uniformity of the t_{Ti} layer.

The ohmic contacts were further assessed on epi-structure featuring distinct barrier configurations. According to the preceding outcomes, two samples with a tilting deposited t_{Ti} of 3 nm and 15 nm (referred to as T_3 and T_{15}, respectively) and a perpendicularly deposited t_{Al} of 280 nm capped with a 20 nm top Ti layer were prepared on Epi II. These samples were processed with an identical exposure dose and a recess etching depth established at approximately 12 nm beneath the 2DEG. The primary distinction between Epi I and Epi II resides in the aluminum concentration and the thickness of the AlGaN barrier. Upon evaluation, a low R_c of 0.15 Ω·mm accompanied by a R_{sh} of 280 Ω/sq. was recorded for T_3 (Fig. 3.5d), whereas T_{15} exhibited a higher R_c of 0.56 Ω·mm with an R_{sh} of 282 Ω/sq. A correlation between R_c and t_{Ti} similar to that observed for Epi I was also noted for Epi II, underscoring the versatility of this ohmic contact fabrication technique across different barrier configurations.

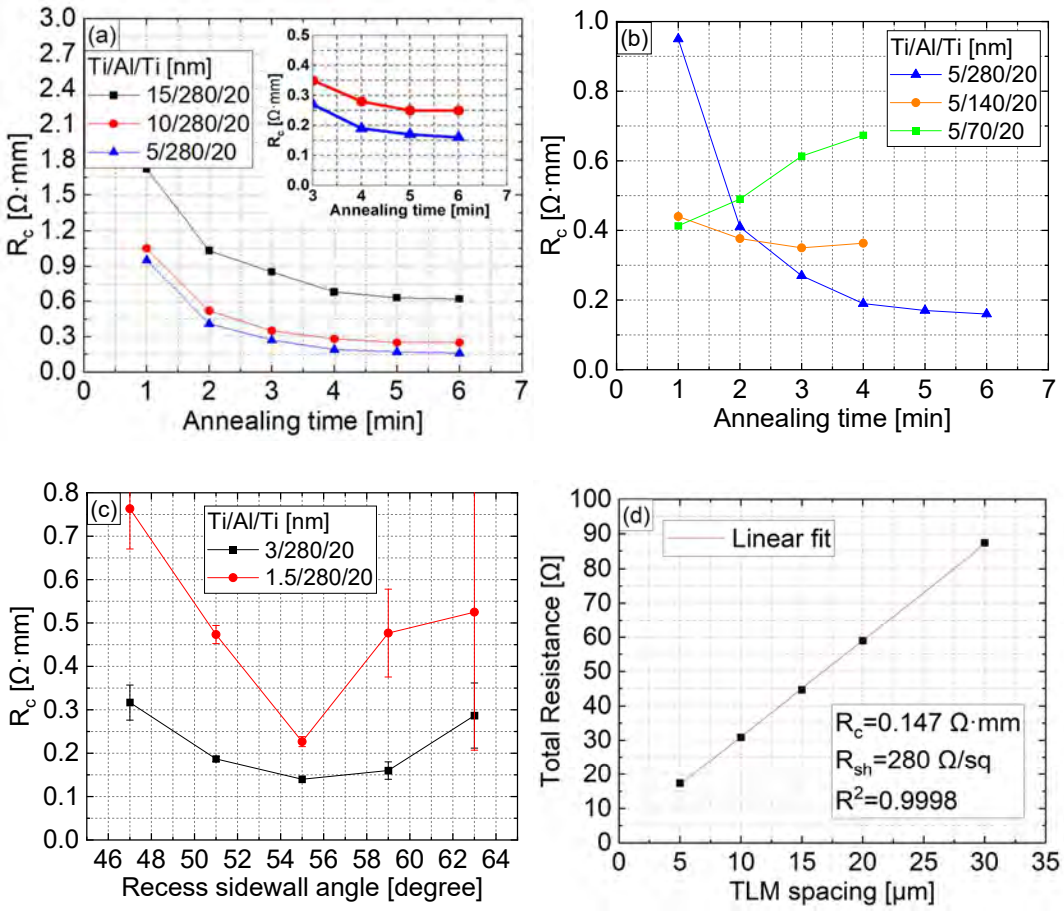

Fig. 3.5. R_c versus total annealing duration on Epi I for (a) different t_{Ti} (5, 10, and 10 nm). The inset shows the zoom-in for the samples with t_{Ti} of 5 and 10 nm. (b) different t_{Al} (70, 140, and 280 nm). (c) Rc versus θ with all the samples annealed until the R_c saturated. The accuracy of the measurement of θ with SEM is ±2.5°. (d) Linear fitting of the total resistance vs. TLM spacing on T_3. R^2 is the correlation coefficient of linear fitting.

3.3.2 TLM structural investigation

To understand the formation mechanism of ohmic contacts, structural and elemental analyses were conducted on T_3 and T_{15}, both fabricated on Epi II. The interface between the ohmic contacts and the epitaxial structure was examined using a combination of high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM), electron energy loss spectroscopy (EELS), and energy-dispersive X-ray spectroscopy (EDS). This advanced suite of analytical techniques provided a comprehensive characterization of the ohmic contact interfaces, yielding crucial insights into the contact formation mechanisms at the atomic scale.

The annealed TLM structure underwent scrutiny through high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM). This technique enables differentiation between various materials and their respective

interfaces by exploiting the variation in image intensity, which arises from mass contrast differences, as demonstrated in Fig. 3.6a and 3.6b. Upon analysis, T_3 and T_{15} revealed a noticeable distinction predominantly in the thickness of the bottom titanium (Ti) layer. Notably, in the case of T_{15}, there was evidence of diffusion, either of the bottom Ti layer migrating into the overlying aluminum (Al) layer or the Al into the Ti. This phenomenon of interlayer diffusion was manifested as contrast changes within the HAADF-STEM images and is highlighted in Fig. 3.6b-Ti with white arrows. These arrows point to regions where the density of the material changes, suggesting a mixing of the two distinct metallic layers as a result of the annealing process. EDS elemental maps of the ohmic contacts and the epitaxial structure, encompassing elements such as Ga, Al, N, O, and Ti, are depicted in Fig. 3.6a and 3.6b. Al is present in the metal stacks of the ohmic contacts as well as in the barrier layers for both sample types. An unexpected discovery was the presence of an Al 'tail' on the sidewall of the SiN passivation layer, denoted by white ovals in Fig. 3.6a-Al" and 3.6b-Al". This suggests a potential diffusion of Al at temperatures below its melting point (approximately 660 °C). The uniformity of the contrast in the images suggests that there is no discernible decomposition of the AlGaN barrier.

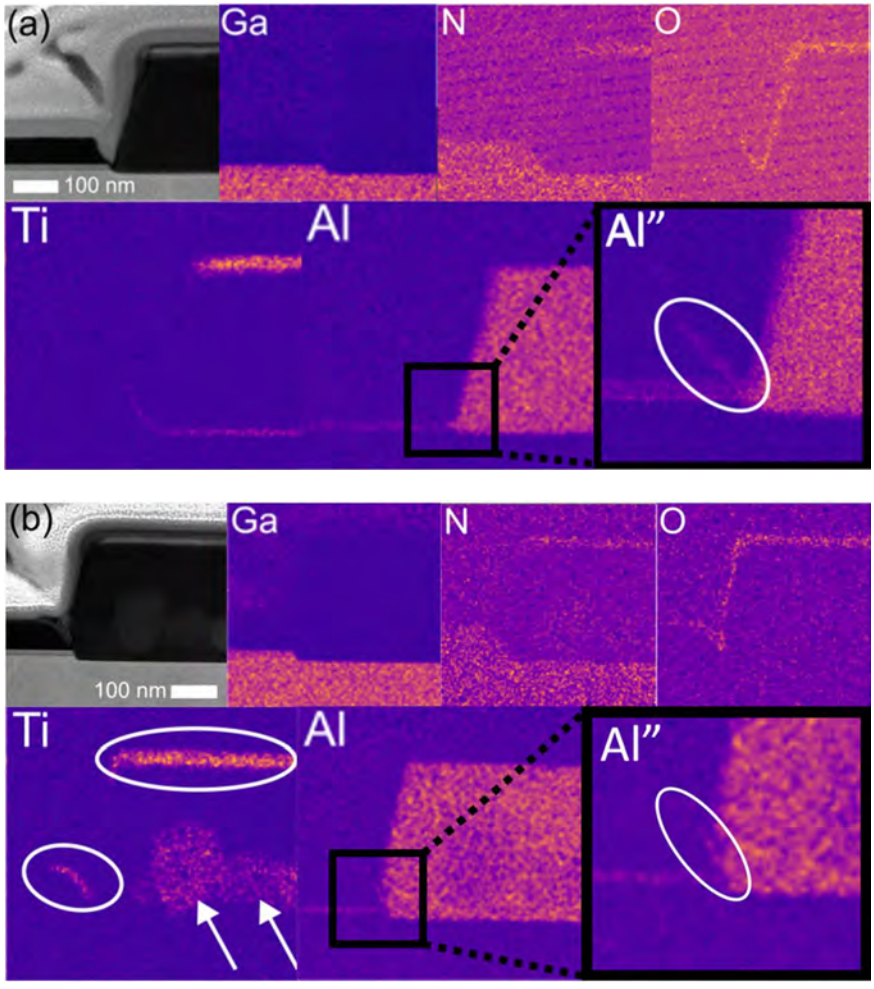

Fig. 3.6. HAADF-STEM images and EDS elemental maps from (a) T_3 and (b) T_{15}.

Given the proximity in energy of the N (0.392 keV) and Ti (0.452 keV) EDS signals, which hinders their differentiation, EELS was employed for further interface analysis. The corresponding EELS and EDS profiles are illustrated in Fig. 3.7a and 3.7b, respectively. The 10° tilted deposition of the bottom Ti layer is evidenced by the detection of Ti on the sidewall of SiN. For the T_3 sample, the relatively short out-diffusion span of ~8 nm permits the co-diffusion of Ti and Al, which is crucial for nitrogen extraction, culminating in a lower R_c of 0.15 Ω·mm. This reduction in R_c is attributed to the formation of a Ti-Al-N alloy with a lower work function. Conversely, for the T_{15} sample, the Ti out-diffusion extends 100-200 nm from the sidewall contact region and alloys with the Al layer, as indicated in Fig. 3.6b-Ti. This extensive diffusion leads to a higher R_c of 0.56 Ω·mm, which can be ascribed to the formation of a higher bandgap Al-N alloy at the sidewall contact region without sufficient Ti to act as a catalyst for nitrogen extraction by Al. Remarkably, no significant interaction between Al and the Ti on SiN or the top Ti layer was observed, as highlighted by the white oval in Fig. 3.6b-Ti. The interface analysis by EELS and EDS for the T_3 sample elucidated that while N and Al could not be spontaneously captured in EELS due to their differing energy edge onsets, the complementary EDS data (Fig. 3.7b) indicated that Ga and N are intermixed with Ti, with an Al diffusion into the Ti and GaN noted. The annealed Ti showcased an out-diffusion of approximately 10 nm, aligning with the EDS mapping in Fig. 3.6a-Ti. These observations might clarify the low R_c found in T_3, potentially due to the induced N-vacancies and the formation of a low work function Ti-Al-N alloy at the interface between the epitaxial structure and the ohmic contacts. Additionally, the presence of a native oxide layer at the interface is presumably a consequence of air exposure during the transfer of the sample prior to the deposition of the ohmic metal layers.

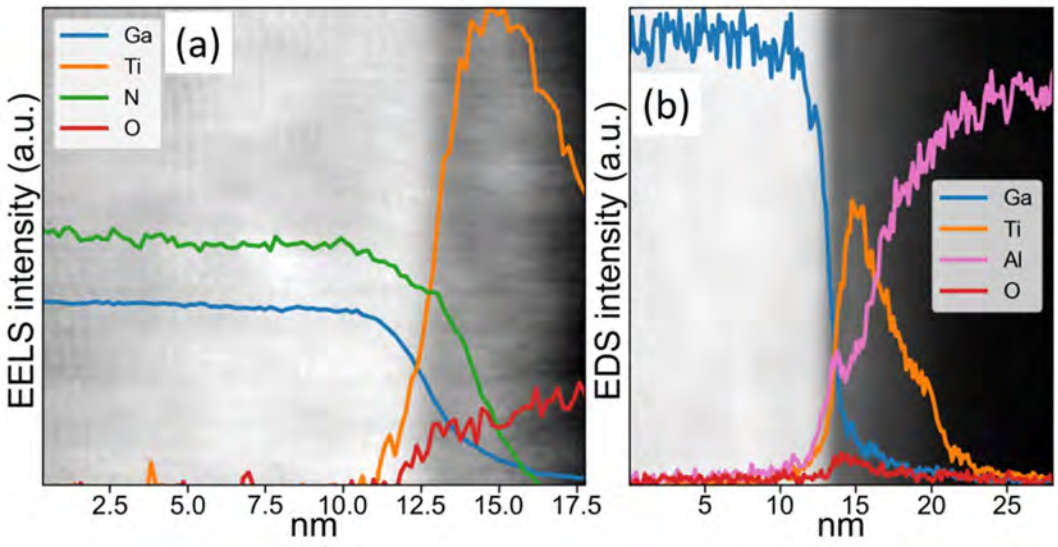

Fig. 3.7. Elemental profile of the T_3 measured with (a) EELS, and (b) EDS.

In Fig. 3.8, this work is benchmarked against other ohmic contact concepts. Compared to Ta-based ohmic contacts, Ti-based contacts potentially offer a lower R_c,

suggesting an exceptional process scheme for ohmic contacts suitable for both high-frequency and high-power applications.

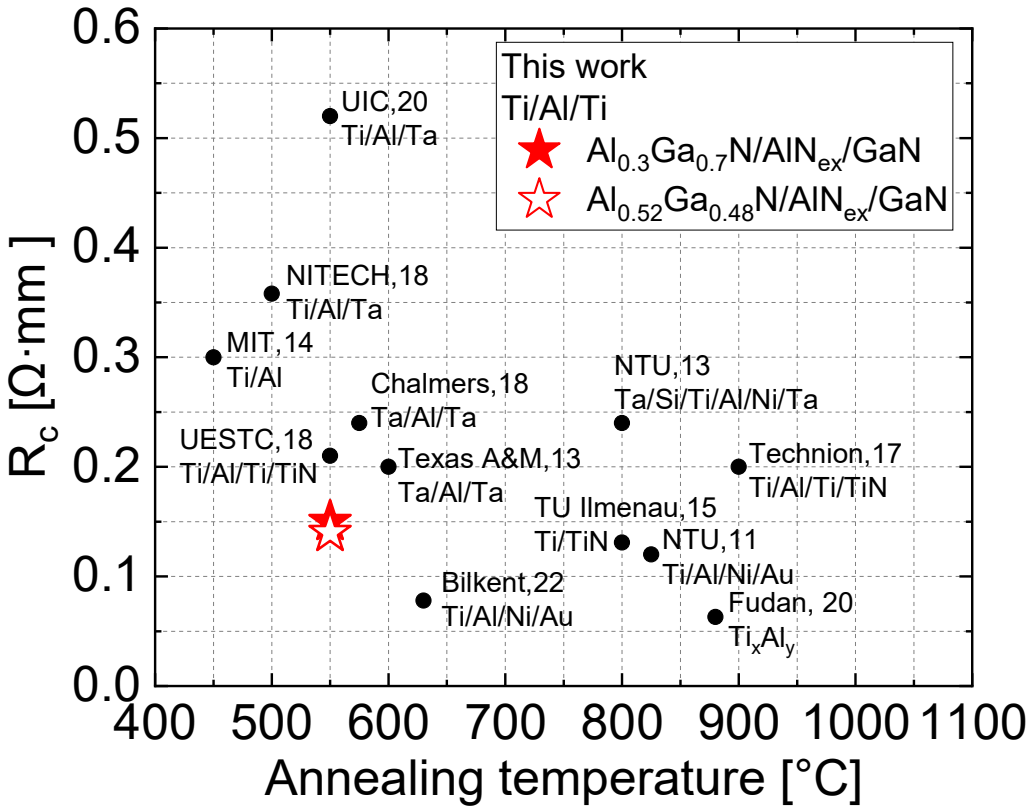

Fig. 3.8. Benchmark of R_c versus annealing temperature on $Al_xGa_{1-x}N/GaN$ (x> 0.22) HEMT epi-structures [57, 59, 65-73].

Chapter 4

Passivation and surface pretreatment for GaN HEMTs

4.1 Introduction of passivation layer

The primary functions of the passivation layer for AlGaN/GaN HEMTs are to reduce surface-related trapping effects, minimize surface leakage currents, maintain the device's breakdown voltage, adjust the surface stress, and shield the surface from environmental moisture and oxygen [74-76]. Numerous passivation techniques and materials have been explored for GaN HEMTs. These include SiN_x, SiO_x, and SiO_xN_y via plasma-enhanced chemical vapor deposition (PECVD); SiN_x through reactive sputtering; Al_2O_3, AlN, HfO_2, SiO_2 using atomic layer deposition (ALD); and SiN_x via LPCVD and MOCVD [74, 77].

The pivotal role of the passivation layer is to suppress surface trap states. Such trap states arise from defects like pits and threading dislocations, dangling bonds, and the native oxide layer [78, 79]. Electrons trapped in these states function as a virtual gate on the surface, leading to partial depletion of the 2DEG and elevated on-resistance [80]. The passivation process can either remove the surface oxide and reduce surface defects [81], or augment the positive charges at the interface between passivation and epi-structure. This neutralizes the AlGaN polarization charges, subsequently reducing the surface-related depletion of the 2DEG [82].

4.1.1 PECVD SiN_x, SiO_2, and SiO_xN_y passivation

Passivation layers, including SiN_x, SiO_x, and SiO_xN_y, are frequently deposited on GaN HEMTs using PECVD. This is because the material properties these layers

offer, are promising to reduce surface trapping effects and leakage current, as well as to provide the desired breakdown characteristics [83]. The reaction processes for SiN_x, when using either N_2 or NH_3, are as follows:

$$SiH_x + NH_x \rightarrow SiN_x + (H_2) \quad (4.1)$$

$$SiH_x + N \rightarrow SiN_x + (H_2) \quad (4.2)$$

While the reaction process for SiO_x is:

$$SiH_x + N_2O \rightarrow SiO_x + (H_2 + N_2) \quad (4.3)$$

A combination process (equation 4.1 and 4.3) can create a SiO_xN_y passivation layer:

$$SiH_x + N_2O + NH_3 \rightarrow SiO_xN_y + (H_2 + N_2) \quad (4.4)$$

A significant advantage of the PECVD process is its low deposition temperature, which is in a range of 200-400°C. This is especially suitable for post-passivation schemes and gate dielectrics, as the low processing temperature minimizes any adverse impacts on the device. The dielectric properties of materials deposited via PECVD are influenced by various factors, including precursor flow rates and ratios, RF power, chamber pressure, and deposition temperature (as detailed in Tables 4.1 and 4.2). A higher SiH_4 typically increases the available silicon precursor, leading to higher deposition rates and higher refractive index for both SiN_x and SiO_x. Increasing the NH_3 and N_2O ratio will decrease the deposition rate and yield lower refractive index due to N-rich or O-rich film. Higher RF power increases deposition rate due to enhanced reaction. However, extreme RF power might cause etching [84]. Temperature has different impact on SiN_x and SiO_x. The bonds in SiN_x (e.g., Si-N) are relatively short and strong, making the material less sensitive to thermal expansion and densification compared to SiO_x. Higher temperatures increase mobility, leading to tensile stress as atomic rearrangement occurs in SiN_x. However, higher temperatures promote densification of the SiO_x network, which increases the refractive index and results in compressive stress.

Table 4.1. Impact of PECVD SiN_x deposition by processing parameters.

SiN_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow rate	↑	↑	more compress
↑ NH_3: SiH_4 ratio	↓	↓	more tensile
↑ RF power	↑	↓	more tensile
↑ Temperature	--	↓	more tensile

Table 4.2. Impact of PECVD SiO_x deposition by processing parameters.

SiO_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow rate	↑	↑	more compress
↑ N_2O: SiH_4 ratio	↓	↓	more tensile
↑ RF power	↑	↓	more tensile
↑ Temperature	--	↑	more compress

4.1.2 ALD Al_2O_3, AlN, HfO_2, SiO_2 passivation

Materials such as Al_2O_3, AlN, HfAlO, and SiO_2, when deposited using atomic layer deposition (ALD), have been identified as effective passivation layers for GaN HEMTs. They offer conformal coverage and effectively reduce surface-related trapping effects. The deposition process involves introducing target elements, carried by precursors, to the substrate surface in a process termed chemisorption. The chamber is evacuated and purged between each monolayer deposition cycle, with each cycle approximating 1Å in thickness. Typically, an ALD monolayer deposition cycle lasts several seconds and operates at a temperature range of 200-500°C. This temperature range aligns with the low-temperature processing requirements seen in techniques like PECVD. A unique advantage of ALD is its conformal deposition capability. This enables a uniform thickness across the surface, regardless of its morphology or defects, making it especially suitable for uniform deposition within gate recessed trenches. Furthermore, ALD ensures excellent adhesion to the target surface, as a result of the covalent bonding inherent in the ALD deposition process.

4.1.3 LPCVD SiN_x passivation

LPCVD is differentiated into two systems: the cold wall and the hot wall. The cold wall system effectively minimizes the fallout of particles and reduces growth-related memory effects. In contrast, the hot wall system offers higher throughput. Although the deposition rate of LPCVD is relatively slow (around 10 nm/minute), It ensures exceptional deposition uniformity of the dielectric material on multiple wafers in a single run (with less than 3% thickness variation across a 4-inch wafer). The formation of SiN_x (specifically Si_3N_4) is achieved through the chemical reaction of dichlorosilane (DCS, $SiCl_2H_2$) and ammonia (NH_3) under high temperatures (ranging from 700 to 900°C) and low chamber pressures (below 500 mTorr). The reaction proceeds as:

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \quad (4.5)$$

Table 4.3. Impact of LPCVD SiN_x deposition by processing parameters.

SiN_x	Deposition rate	Refractive index	Film stress
↑ SiH_4 flow	↑	↑	more compress
↑ NH_3: SiH_4 ratio	--	↓	more tensile
↑ Chamber pressure	↑	--	more tensile
↑ Temperature	↑	↑	more compress

LPCVD SiN_x, due to its high deposition temperature, assures reduced thermal-related degradation during both the ohmic contacts annealing process and device operation under elevated power density. Furthermore, LPCVD SiN_x demonstrates superior dielectric properties and lower hydrogen incorporation compared to other low-temperature deposition methods [85, 86]. However, the high deposition temperature restricts process step flexibility, making LPCVD SiN_x suitable predominantly for the "passivation first" process scheme. Enhancing the flow rate,

chamber pressure, and deposition temperature boosts the deposition rate, attributable to more efficient chemical reactions [87-89]. Notably, the ratio between DCS and NH_3 significantly influences the refractive index and the internal stress of the SiN_x, as detailed in Table 4.3 [90].

4.1.4 Passivation layers on GaN HEMTs

Optimal passivation necessitates meeting several criteria: minimizing surface leakage current, reducing surface-related trapping effects, and ensuring a high breakdown voltage. Additionally, the stress introduced by the passivation layer significantly affects the polarization charges within the epi-structure. Nonetheless, there are trade-offs to consider among these parameters. Table 4.4 provides a summary of the advantages and challenges associated with different passivation layer materials and their respective fabrication methods.

Table 4.4. Examples of passivation layer reported in literatures.

	Passivation dielectric material	Deposition tool	Epitaxial barrier design	Advantages	Comments	Ref.
A	SiN_x	PECVD	AlGaN	Reduce current collapse Reduce gate lag Improve noise performance	Plasma damage	[75, 91]
B	Bilayer high freq./low freq. SiN_x	PECVD	GaN_{cap}/AlGaN	Reduce plasma damage Reduce R_{on} and dynamic R_{on}	--	[92]
C	SiN_x	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Reduce current collapse	Drain leakage	[93, 94]
D	SiO_x	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Large bandgap Reduce drain leakage	Trapping is more than PECVD SiN_x	[93, 94]
E	SiO_xN_y	PECVD	GaN_{cap}/AlGaN/ AlN_{ex}	Reduce drain leakage Improve transconductance Improve drain current	Trapping is more than PECVD SiN_x	[93, 94]
F	Si-rich/N-rich SiN_x	PECVD	GaN_{cap}/AlGaN	Reduce current collapse Reduce gate leakage Improve isolation	Stress engineering	[76]
G	Al_2O_3	ALD	GaN_{cap}/AlGaN	Large bandgap	Trapping is similar or lower than PECVD SiN_x	[95, 96]
H	HfAlO	ALD	GaN_{cap}/AlGaN	--	Trapping is more than PECVD SiN_x	[95]
I	AlN	ALD	AlGaN	Reduce gate leakage Reduce drain leakage	Trapping is similar or lower than PECVD SiN_x	[97]
J	AlN/SiN_x	ALD/PECVD	GaN_{cap}/AlGaN	Improve transconductance Reduce R_{on} and dynamic R_{on}	--	[98, 99]
K	Al_2O_3/SiO_2	ALD/PECVD	GaN_{cap}/AlGaN	Reduce gate-lag	--	[95]
L	SiN_x	LPCVD	GaN_{cap}/AlGaN/ AlN_{ex}	Improve breakdown voltage Reduce degradation after stress Reduce dynamic R_{on}	--	[100]
M	SiN_x	LPCVD	AlGaN/AlN_{ex}	Reduce lateral surface leakage Reduce gate and drain lag	Vertical leakage	[101]
N	Si-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce dynamic R_{on}	Drain-gate leakage Schottky gate leakage	[102]
O	N-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce drain-gate leakage Reduce Schottky gate leakage	Trapping effects	[102]
P	Bilayer Si-rich/N-rich SiN_x	LPCVD	AlGaN	Reduce current collapse Reduce gate leakage	--	[101]
Q	Si-rich SiN_x	LPCVD	GaN_{cap}/AlGaN	Reduce current collapse Reduce dynamic R_{on}	With in-situ NH_3 pretreatment	[Paper C]
R	In-situ SiN_x	MOCVD	AlGaN	Reduce trapping effects Improve radiation tolerance Resistant to electric/thermal stress	--	[103, 104]
S	SiN_x	Sputter	AlGaN	Reduce trapping effects	--	[105]
T	Sc_2O_3	MBE	AlGaN	Reduce trapping effects	--	[106]
U	MgO	MBE	AlGaN	Reduce trapping effects	React with ambient H_2O	[106]

Examples A-F discuss the passivation dielectrics deposited using PECVD. In Example A, it's evident that surface passivation reduces surface-related current collapse in comparison to a non-passivated epi-structure. However, the mitigation of trapping effects is constrained by plasma-induced surface defects. Example B showcases a bilayer SiN_x deposited by a high-frequency RF source during the first layer's deposition. This process diminishes plasma damage due to the decreased ion bombardment energy, leading to a more pronounced reduction in dynamic R_{on} degradation. Example C underlines the ability of passivation to reduce surface traps, irrespective of the GaN cap layer. Examples D and E suggest that SiO_x and SiO_xN_y are suitable for power devices that demand a high breakdown voltage, attributed to their larger bandgap of 8.9 eV and superior resistivity in comparison to SiNx. However, epi-structures passivated with SiO_x and SiO_xN_y grapple with issues like current collapse and knee voltage walkout, which stem from inferior dielectric/epi interface quality. Lastly, Example F illuminates stress engineering using Si-rich and N-rich SiN_x, aiming to strike the right equilibrium among trapping effects, leakage current, and device isolation.

Investigation of passivation layers deposited by ALD were also reported. Some of them are listed as Examples G-K Dielectrics composed of oxide components still exhibit trapping effects, echoing the behavior of PECVD SiN_x. A post-annealing process at around 800 °C for ALD dielectrics, including Al_2O_3 and AlN, has been advocated to enhance the dielectric/epi interface quality, yielding reduced trapping effects. Additionally, annealed ALD AlN augments the 2DEG properties due to the extra polarization force elicited by AlN. Placing additional PECVD SiN_x atop ALD AlN further diminishes dynamic R_{on} degradation.

Compared to PECVD or ALD, the passivation layer created with LPCVD, as depicted in Examples L-Q, might deliver superior dielectric quality. This is credited to the elevated deposition temperature and the absence of plasma-related damage to the epi-structure in this plasma-free process. LPCVD's Si-rich SiNx cuts down surface-related current collapse, likely by furnishing a leakage pathway for electrons to be de-trapped. Meanwhile, N-rich SiN yields a higher critical electric field paired with reduced leakage current, making it ideal as an additional layer over Si-rich SiN. This combination aims for the desired low trapping effects, minimal leakage currents, and robust breakdown performance. In the referenced work [Paper C], Si-rich SiN_x is chosen, having already demonstrated a reduction in current dispersion. More insights into the LPCVD SiNx and in-situ surface pretreatment are discussed in section 4.3.

Alternative passivation techniques, represented by Examples R-U, encompass methods like MOCVD, reactive sputtering, and MBE. Notably, MOCVD allows for the in-situ growth of SiN_x directly atop the epi-structure. This procedure avoids exposure to ambient conditions such as moisture and oxygen, facilitating the creation of an oxygen-free interface. Such an interface has shown promise in potentially reducing trapping effects [103, 104]. On the other hand, sputtered SiN_x demonstrates vulnerabilities akin to those found in PECVD SiN_x, especially concerning surface plasma damage [105]. Enhancements in this area might involve increasing the RF frequency during the deposition process. Furthermore, innovative

dielectric materials like Sc_2O_3 and MgO, when fabricated using MBE, are paving new avenues for the development of passivation layers in GaN HEMTs [106].

4.2 Pretreatment prior to deposition of passivation layer

Dangling bonds due to nitrogen-vacancy, defects from plasma damage, the native oxide layer, and carbon-related contamination are commonly identified as the primary causes behind the creation of surface leakage paths and trap states. To address these challenges, both ex-situ and in-situ surface pretreatments have been proposed.

4.2.1 Ex-situ pretreatment

Ex-situ pretreatments typically involve wet chemical processes and plasma treatments. There are also studies that highlight the use of high-temperature annealing with varied gas flows. Section 4.2.2 provides details on the plasma-based treatments. Table 4.5 offers a comprehensive summary of the functions and reactions associated with different chemical treatments applied to GaN HEMTs.

Table 4.5. Examples of ex-situ pre-treatment reported in literatures.

	Pretreatment	Epitaxial surface	Function	Comments	Ref.
A	HCl	GaN	Remove surface oxide Minor remove surface carbon	Form 3D nucleation point defects Chlorine residual	[12, 47-50]
B	HF	GaN	Remove surface oxide Remove surface carbon	Fluorine residual	[12, 47, 50]
C	Buffered HF	GaN	Remove surface oxide	Fluorine residual	[12]
D	NH_4OH	AlN and GaN	Remove surface oxide	Maintain III-N stoichiometry	[12, 51] [Paper C]
E	$(NH_4)_2S$	GaN	Remove surface oxide Provide defect-free surface Prevent surface re-oxide	Sulfide residual Enhance breakdown	[49, 107, 108]
F	KOH	GaN	Remove surface carbon	High surface roughness	[49]
G	RCA SC1	GaN	Remove organic residual Remove surface particles	Form a thin oxide layer	[109] [Paper C]
H	RCA SC2	GaN	Remove metallic contaminants	Left carbon on the surface Form a thin passivizing layer	[109] [Paper C]
I	Piranha	GaN	Remove hydrocarbons Remove hydroxylates	Provide smooth surface	[47]
J	UV/O_3	GaN and AlN	Remove surface carbon	Grow oxide layer	[12, 50]
K	Annealed with SiH_4	AlN	Remove surface oxide	Si deposition on the surface	[12]
L	Annealed with NH_3	In and GaN	Reconstruct GaN surface	Annealed at 700~900 °C	[12]

Example A highlights the use of HCl as a prevalent etchant to eliminate the Ga-O present on the epi-structure. This results in a notable reduction of yellow luminescence and undesired surface states, which in turn diminishes the surface trapping effects. Nevertheless, HCl only mildly addresses carbon-related contamination. A drawback is that immersing GaN in HCl solution introduces point defects, negatively impacting the morphology of the subsequent passivation layer. Additional studies confirm that the residuals from chlorine-based reactions predominantly bond with Ga on the surface, serving to saturate the dangling bond.

Example B and C highlight HF and Buffered HF, which are oxide etchants widely used in the silicon industry. These etchants efficiently remove surface oxides, with fluorine bonding to Al and Ga, leaving fluorine residues on the surface due to its strong electron affinity. This fluorine residue can be perceived in two ways: as a pretreatment process that diminishes leakage current and elevates V_{po}, or as an unwanted virtual gate that depletes the 2DEG channel. In contrast to the acids shown in Example A-C, NH_4OH, as presented in Example D, not only removes the surface oxide effectively but also ensures no residual traces remain on the epi-structure, preserving the stoichiometry of GaN and AlN. Example E, however, reveals that $(NH_4)_2S$ treatment results in sulfide residues on the surface. Lastly, Example F demonstrates that while KOH is adept at eradicating carbon-related contaminants from the surface, it compromises the surface morphology.

Examples G-I discuss treatments involving mixtures of chemicals. The RCA standard cleaning procedures, consisting of SC1 (H_2O_2+NH_4OH+H_2O) and SC2 (H_2O_2+HCl+H_2O), are adept at eliminating organic and metallic contaminants from the surface, respectively. Simultaneously, these treatments form a thin oxide layer on the surface, which serves as a protective shield against other contaminants. Another chemical mixture, the Piranha etchant – a potent oxidizing solution formed by blending sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) – results in a GaN surface characterized by a smooth morphology with negligible organic residues.

Gas-phase ex-situ treatments, highlighted in examples J-L, offer interesting outcomes against solution-based chemical treatments. UV/Ozone treatment is effective in removing carbon-related residues, but the downside is the formation of an oxide layer by ozone, introducing trapping effects in GaN HEMTs. Another method involves high-temperature annealing of GaN using SiH_4 and NH_3. While SiH_4 efficiently removes the surface oxide, the inadvertent formation of a Si layer might induce surface-related leakage currents.

In [Paper C], a sequence of different treatments is used and described as follows. First, RCA SC1 and SC2 ex-situ pretreatments are employed to remove organic and metallic residues from the epi-structure's surface. This is succeeded by an NH_4OH treatment to counteract and reduce the oxide layer introduced by the RCA procedures before proceeding with the LPCVD.

4.2.2 In-situ pretreatment

Despite the effective cleansing of the epi-structure surface by ex-situ treatments, there remains concerns about re-oxidation and re-contamination during the material transport to the passivation system. To address these challenges, in-situ pretreatments have gained attention, especially those administered right before the passivation layer deposition. The common methodologies enlisted for these treatments are predominantly plasma-based and encompass techniques like PECVD, PEALD, and reactive sputtering. For a clearer understanding, Table 4.6 furnishes a comprehensive breakdown of the functions and implications of various plasma treatments on AlGaN/GaN HEMTs.

Table 4.6. Examples of in-situ pre-treatment reported in literatures.

	Pretreatment	Epitaxial surface	Function	Comments	Ref.
A	Hydrogen plasma (H_2)	AlN	Remove carbon and halogen species Remove surface oxide	Hydrogen diffusion into the barrier Formation of Ga droplets	[9, 12, 110]
B	Ammonia plasma (NH_3)	AlGaN and GaN	Remove surface oxide Remove surface carbon	Hydrogen diffusion into the barrier Improve reliability Reduce current collapse	[110, 111]
C	Nitrogen plasma (N_2)	GaN	Remove surface oxide Remove surface fluorine Recover surface nitrogen-vacancy	Reduce surface leakage current Reduce virtual gate behavior Reduce degradation of dynamic R_{on}	[9, 11, 112, 113]
D	Fluorine plasma (NF_3, CF_4, SF_6)	AlGaN and GaN	Modify surface energy states Remove surface oxide	Virtual gate with lower drain current Lower V_{TH} hysteresis Faster surface de-trapping	[114-117]
E	NH_3 gas flow	GaN	Remove surface oxide	Reduce surface-related traps	[Paper C]

Several in-situ pretreatments using plasma have been explored in the literature, all of which aim to enhance the interface quality between passivation and the epi-structure. The goal is to effectively eliminate surface oxide and other contaminants without exposing the material to the atmosphere prior to passivation. Hydrogen plasma is particularly adept at erasing surface carbon residues and the oxide layer. Yet, its interaction with GaN results in nitrogen vacancies, attributed to the formation of Ga-H bonds. This interaction also contributes to the degradation of HEMTs when subjected to the hot electron stress condition. [9, 12, 110]. NH_3 plasma presents a similar issue. While the hydrogen ions in NH_3 plasma can seep into the barrier and mirror the degradation observed with hydrogen plasma, it compensates by having nitrogen radicals that restore the stoichiometry of GaN. [110, 111]. Pure nitrogen plasma pretreatment emerges as the most promising solution. It successfully removes the native oxide surface, carbon contaminants, fluorine residues, and aids in surface reconstruction. This leads to a notable reduction in current collapse and a minimized leakage path. [9, 11, 112, 113]. Fluorine-based plasma, on the other hand, exhibits varied effects on HEMTs. It can configure a device to be normally off, achieving a positive shift of V_{po}. However, the residual fluorine on the surface behaves as additional donor states, exhibiting a virtual gate effect, which consequently depletes the 2DEG channel in normally-on devices. [114-117]. In [Paper C], an in-situ NH_3 pretreatment was conducted prior to the SiN_x deposition using LPCVD.

4.3 In-situ NH_3 pretreatment for LPCVD SiN passivation layer

This work showcases an efficient, plasma-free, in-situ NH_3 pretreatment applied prior to LPCVD SiN passivation on GaN HEMTs. Prior to introducing them to the LPCVD chamber for in-situ NH_3 pretreatment, the epi-structure's surface underwent ex-situ wet chemical treatments. RCA SC1, RCA SC2, and diluted NH_4OH were chosen due to their minimal side effects. These treatments effectively removed organic and metallic contaminants from the epi-structure's surface and significantly reduced the surface oxide thickness. The in-situ NH_3 pretreatment durations varied: 0 minutes (T_0), 3 minutes (T_3), and 10 minutes (T_{10}), followed by SiN_x deposition.

4.3.1 Structural and chemical characterization

The interface between the passivation layer and the epi-structure was analyzed for structural and chemical properties using high-resolution scanning transmission electron microscopy (HR-TEM) paired with electron energy loss spectroscopy (EELS). The structural integrity of the SiN passivation layer, GaN cap, AlGaN barrier, and their respective interfaces were assessed (Fig 4.1). Notably, there were no discernible structural differences between the samples, suggesting that T_0 and T_{10} exhibited comparable structural quality.

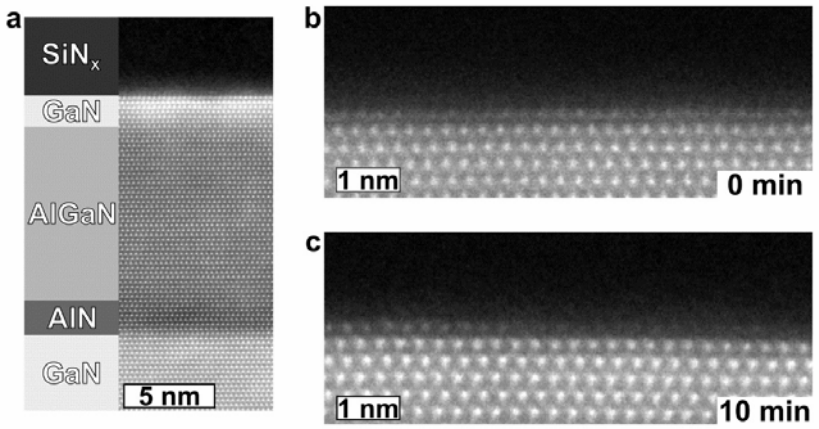

Fig. 4.1. HR-TEM dark field images of the (a) passivation layer and epi-structure. The interface of SiN and GaN cap of (b) T_0 and (c) T_{10} samples.

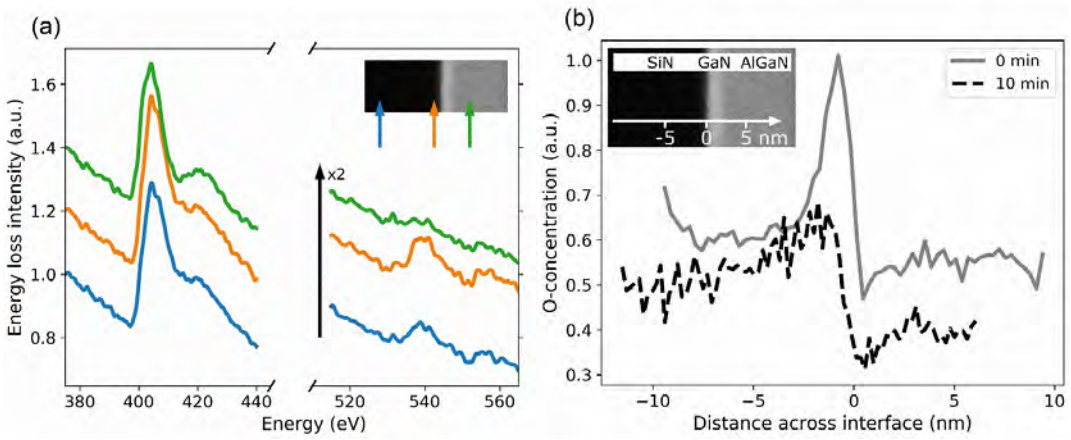

Fig. 4.2. (a) EELS spectra (nitrogen K-edge, left and oxygen K-edge, right) from different positions near the interface between SiN and epi-structure of the T_0 sample. The color-coding of the arrows shows the location of each spectrum (inset top right). (b) Qualitatively comparing pseudo-concentration line profiles of oxygen across the interface (inset top left) for the T_0 and the T_{10} sample.

In the T_0 sample, the EELS spectra displayed consistent nitrogen intensities across varying positions but fluctuated for oxygen intensities (Fig. 4.2a). When

comparing the normalized oxygen intensities against the background signal between the T_0 and T_{10} samples, a reduction in oxygen intensity at the interface of the T_{10} sample was observed (Fig. 4.2b). This suggests that the oxide layer's presence was diminished due to the interaction with the decomposed NH_3 at elevated temperatures during the in-situ NH_3 pretreatment.

4.3.2 HEMTs characterization

HEMTs with the L_g of 200 nm subjected to varying pretreatment durations (T_0, T_3, and T_{10}) were analyzed using DC, pulsed-IV, and both small- and large-signal measurements. The HEMTs from the T_0 and T_3 samples displayed comparable $I_{DS\text{-}max}$ of 0.9 A/mm and $g_{m\text{-}max}$ of 350 mS/mm. Conversely, T_{10} demonstrated a marginally reduced $I_{DS\text{-}max}$ and $g_{m\text{-}max}$, potentially due to undesired surface charges functioning as a virtual gate from prolonged NH_3 exposure. DIBL assessments indicated that both T_3 and T_{10} samples (with values of 14 mV/V and 17 mV/V, respectively) showcased reduced short channel effects in comparison to the T_0 sample's 20 mV/V. A similar pattern was observed in SS evaluations, where T_3 and T_{10} presented a smaller SS value of 200 mV/dec, contrasting with T_0's 270 mV/dec. These findings affirm that the NH_3 pretreatment enhanced gate control.

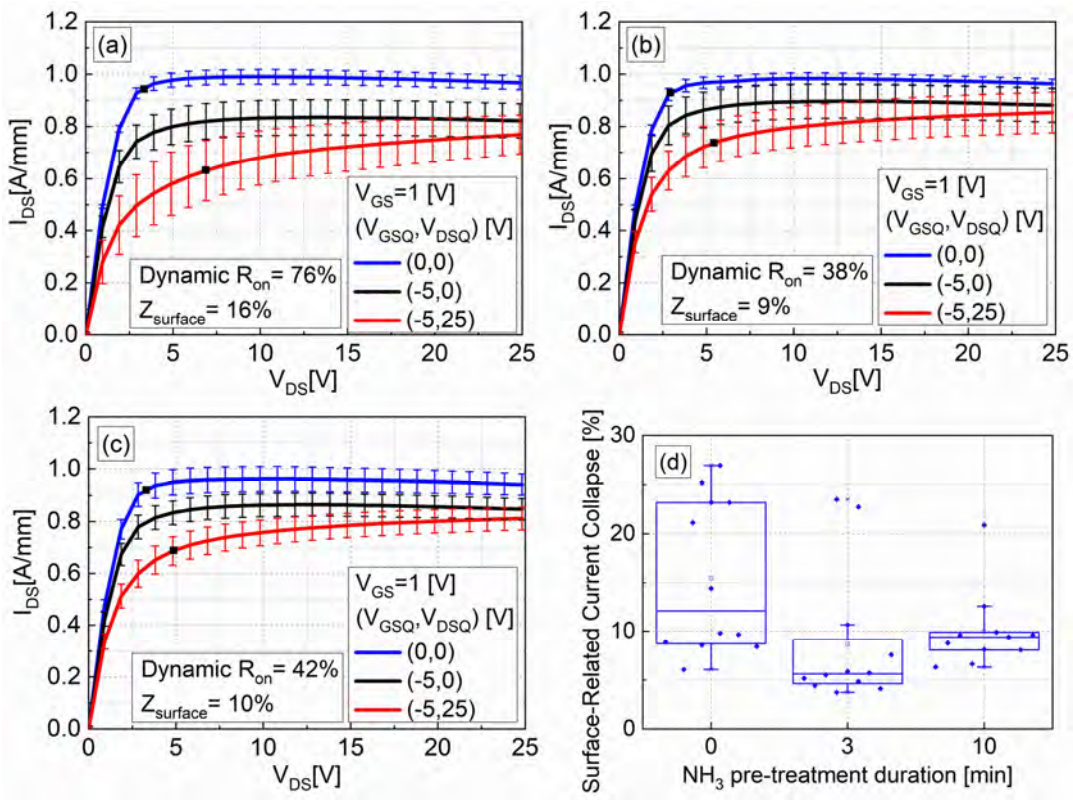

Fig. 4.3. Pulsed-IV measurements on HEMTs with different NH_3 pre-treatment duration of (a) T_0, (b) T_3, and (c) T_{10}. (d) Uniformity of surface-related current collapse response.

Pulsed-IV measurements were conducted at varying quiescent biases (Fig. 4.3). The T_0 sample displayed a higher Z_1, at 16%, in comparison to the 9% and 10% observed for T_3 and T_{10}, respectively. In line with this, T_3 and T_{10} samples also demonstrated a 50% decrease in dynamic R_{on} degradation at Q_{25} when contrasted with T_0. These findings suggest that the NH_3 pre-treatment was successful in eliminating surface traps at the SiN and epi-structure interface. A marginally increased dynamic R_{on} and Z_1 for T_{10} relative to T_3 might be attributed to an excessive duration of the NH_3 pre-treatment, which could introduce surplus nitrogen atoms at the SiN and epi-structure interface [12]. Additionally, a notable improvement in the uniformity of Z_1 was observed for T_3 (4.5%) and T_{10} (1.9%) in comparison to T_0 (14.5%). As a result, there exists potential to further optimize the balance between trapping effects and uniformity.

Large signal measurements were conducted on HEMTs under class-AB conditions and an I_{DSQ} of 20% $I_{DS\text{-}max}$ at 3 GHz (Fig. 4.4). Notably, HEMTs on T_3 and T_{10} reached a higher P_{out} of 3.4 W/mm at a V_{DS} of 30 V, surpassing the 2.6 W/mm achieved by T_0. In tandem with this, the T_0 sample exhibited a 5-10% reduction in PAE relative to T_3 and T_{10}. Given that all the samples showcased comparable DC performance, the diminished P_{out} and PAE in T_0 can be attributed to the pronounced surface-related trapping effects (Fig. 4.3). These effects result in a more significant gate-lag and $V_{DS\text{-}knee}$ walkout.

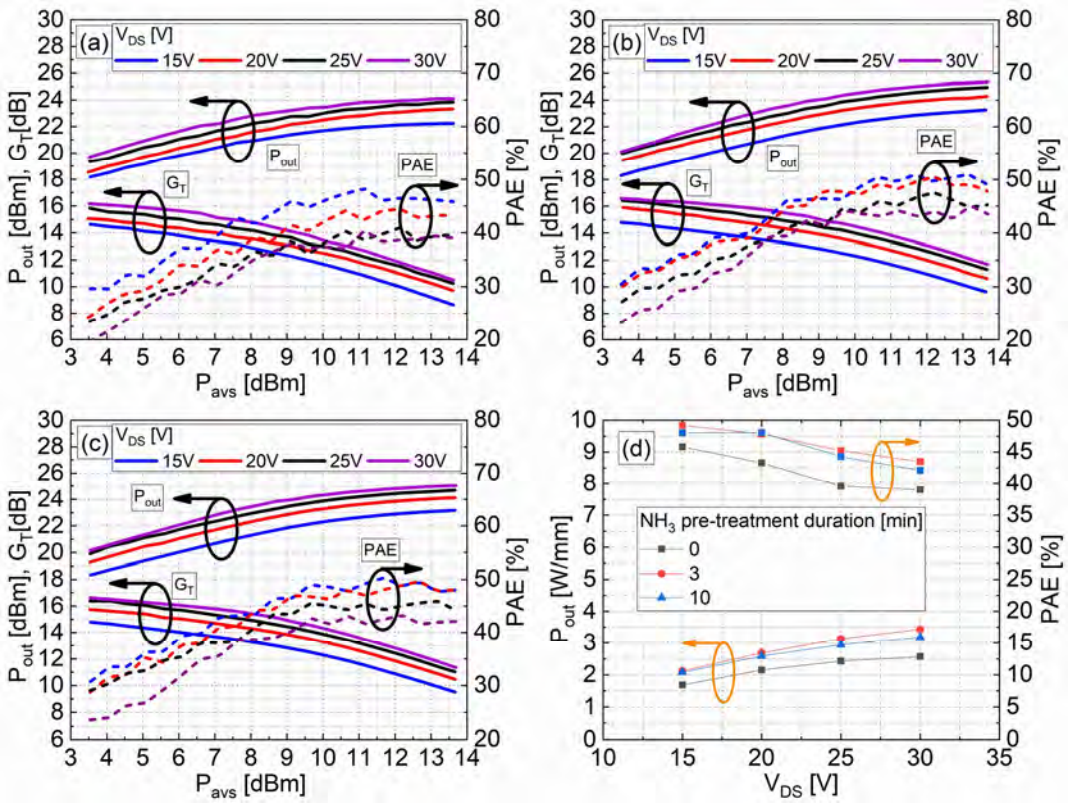

Fig. 4.4. Large-signal measurements on (a) T_0, (b) T_3, and (c) T_{10}. (d) summary of P_{out} and PAE.

Chapter 5

QuanFINE - a 'buffer-free' GaN HEMT heterostructure

5.1 Conventional GaN HEMT heterostructures

The typical epi-structure of GaN HEMTs on SiC substrates includes an AlN nucleation layer, a thick GaN buffer layer, a GaN channel, and a barrier layer. The AlN nucleation layer mitigates the lattice mismatch between SiC and GaN while also serving as a wetting layer, facilitating the two-dimensional nucleation of GaN. The GaN buffer further decimates density of structural defects due to the lattice mismatch, achieving proper structural quality at the GaN channel with the dislocation density around 10^6 cm^{-2} and XRD rocking curve GaN <0 0 2> FWHM values around 200-400 arcseconds . In an ideal scenario, the intrinsic GaN layers should be devoid of impurities. However, during the growth process in MOCVD chambers, unintended elements and contaminants can be incorporated into the epi-structure. These elements, such as silicon (Si) and oxygen (O), behave as unintentional n-type dopants in GaN, leading to a characteristic n-GaN behavior. This behavior can result in buffer-related leakages. Fortunately, MOCVD GaN always contains carbon, which behaves as an acceptor-like dopant to compensate for the n-type impurities, rendering the GaN semi-insulating. Additional dopants like Fe can be introduced as well to further increase the resistivity of the GaN, resulting in reduced buffer leakage. At the same time, these acceptor-like dopants help diminish short channel effects and provide enhanced 2DEG confinement. Alternative strategies to confine 2DEG, using an additional back-barrier or the buffer-free QuanFINE heterostructure, will be explored in subsequent sections.

5.1.1 2DEG confined by intentional acceptor-like doping

- **Iron (Fe)-doped GaN buffer**

Fe-doped GaN buffers are commonly utilized in HEMTs for microwave applications due to their faster drain current recovery speed. Notably, they exhibit a de-trapping time constant of approximately 10^{-3} seconds post device activation, in contrast to HEMTs with C-doped GaN buffers which have a longer de-trapping time constant of over 10^{-2} seconds [13, 118]. An optimal Fe-doping concentration of around 1.3×10^{19} cm^{-3} ensures a semi-insulating GaN buffer without compromising crystal properties or surface morphology [119, 120]. However, the doping memory effect of Fe with a slow reduction of Fe concentration after turning off the Fe precursor makes it impossible to achieve a sharp interface between regions with high and low Fe-doping concentration (Fig. 5.1). Depending on the specific epitaxial growth parameters, a Fe-doped GaN buffer ranging between 500 to 1000 nm in thickness is usually needed for the Fe doping concentration to diminish from 10^{18} to 10^{16} cm^{-3}. The slow decaying rate raises concerns about potential Fe contamination in both the channel and barrier [13, 121].

Numerous GaN HEMTs using Fe-doped GaN buffers have shown outstanding performance across various frequencies. For instance, AlGaN/GaN HEMTs with a L_g of 0.55 μm and double field plates have achieved a P_{out} of 41 W/mm and a PAE of 60% at 4 GHz [122]. Similarly, at 14 GHz, AlGaN/GaN HEMTs with L_g of 0.25 μm and source-connected field plates delivered a P_{out} of 5.2 W/mm and a PAE of 57.4% [123]. Moving up the frequency of 40 GHz, AlGaN/GaN HEMTs with a L_g of 0.1 μm and a thin GaN channel managed a P_{out} of 2 W/mm alongside a PAE of 35% [124].

- **Carbon (C)-doped GaN buffer**

Carbon (C) is another acceptor-like dopant frequently used in epi-structures to counterbalance unintentional impurities introduced during epitaxial growth, ultimately achieving the desired semi-insulating GaN buffer. A notable advantage is that higher buffer resistivities can be achieved compared to Fe-doped buffers, thanks to a deeper energy state of approximately 0.9 eV above valance band [125]. This results in superior breakdown performance and diminished buffer leakage [10]. However, carbon is deep level trap, the C doping profile requires meticulous optimization to strike the right balance between 2DEG confinement, breakdown voltage, and trapping effects.

The C doping profile can be modified between regions of high and low concentration within the epi-structure (see Fig. 5.1). This modulation is influenced by several growth parameters, including temperature, chamber pressure, precursor, growth rate, and the carrier gas used. Increasing the flow rate of trimethylgallium (TMGa) can enhance carbon incorporation. Using nitrogen (N_2) or a mixture of N_2 and hydrogen (N_2+H_2) as carrier gases promotes carbon doping due to their lower reactivity compared to pure hydrogen (H_2). Additionally, reducing the growth temperature can increase carbon concentration, as the decomposition of carbon-containing precursors becomes less efficient at lower temperatures. Furthermore,

raising the V/III ratio (NH_3/TMGa) favors carbon doping by creating conditions that enhance carbon incorporation into the GaN lattice. Lowering the reactor pressure also contributes to higher carbon incorporation by altering the chemical equilibrium and slowing the decomposition of precursors [126]. Nonetheless, challenges arise as tweaking the C doping concentration might jeopardize the structural integrity, defect density, and surface morphology of the material. In light of this, alternate C doping methodologies have been proposed. These include introducing supplementary carbon or utilizing hydrocarbon-based precursors like propane (C_3H_8) or methane (CH_4), all in an effort to mitigate the impacts on structural quality of GaN during epitaxial growth with C doping [127, 128].

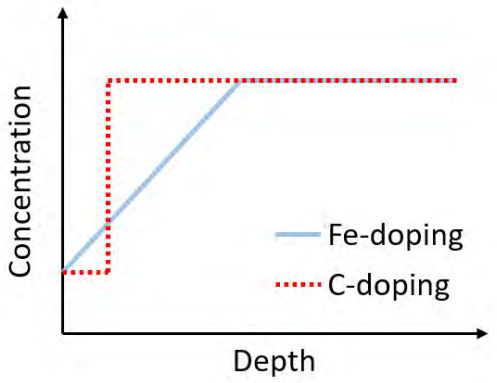

Fig. 5.1. Fe-doping and C-doping profile in epi-structure.

Carbon (C) doping in GaN can manifest in various forms. Typically, C will bond with either Ga or N. When it substitutes for Ga, it results in a shallow donor, termed C_{Ga}. Conversely, when C substitutes for N, it acts as a deep acceptor, known as C_N [10]. Additionally, interstitial C can be formed in wurtzite GaN. In p-type GaN, this is recognized as a deep donor, whereas in n-type GaN, it serves as a deep acceptor [129]. Despite the deeper trap state often reported for C-doped GaN, with a carefully optimized C doping profile, exceptional high-frequency performance can be realized. A case in point is the step C doping profile, which has been introduced with promising results. Devices featuring this profile have exhibited a commendably low leakage current of 10^{-4} A/mm alongside minimized trapping effects. Consequently, these devices have achieved a high P_{out} of 2.3 W/mm and drain efficiency (D_{eff}) of roughly 45% at 3 GHz [130]. For more advanced, highly-scaled devices with a L_g of 0.11 μm built on an epi-structure that combines a thin undoped GaN channel with a thick C-doped GaN buffer—the results are also promising. Such structures have delivered a P_{out} of 3.8 W/mm and a PAE of 48% at 40 GHz [131].

5.1.2 2DEG confined by AlGaN back-barrier

Implementing a back-barrier in the epi-structure of HEMTs is a strategic approach within band structure engineering, which primarily aims to enhance 2DEG confinement, especially for highly scaled HEMTs. At its essence, the back-barrier establishes a double heterostructure, which offers an improved barrier

height beneath the 2DEG. This acts to effectively confine the 2DEG within the channel (Fig. 5.2). AlGaN frequently emerges as the material of choice for the back-barrier, but it comes with its own set of challenges. For one, the thermal resistance of AlGaN surpasses that of GaN and AlN, which can compromise the reliability and performance of the device [132]. Moreover, inherent defects and dislocations in the AlGaN back-barrier – predominantly induced by its lattice mismatch with GaN and the nuances of epitaxial growth – can act as trap states, further undermining device performance. Another concern involves the potential for a parasitic 2DEG channel and polarization charges to form beneath the AlGaN back-barrier. This can introduce leakages, thereby deteriorating the desired channel confinement [16, 133]. Addressing this parasitic 2DEG channel might require the use of intentional doping (e.g., with C or Fe), but this can introduce undesired trapping effects. Although there are issues for AlGaN back-barrier, several studies have demonstrated epi-structure using AlGaN back-barrier with proper optimization can enhance device performance. Stepped graded AlGaN back-barrier with a total epi stack thickness of 450nm on Si substrate provide an excellent DIBL < 50mV/V together with RF P_{out} of 1.1 W/mm and PAE of 45.6% at 40 GHz on device with L_g of 100 nm [134]. By tunning the Al% in AlGaN back-barrier, an improved DIBL from 600mV/V to 26mV/V can be achieved with Al% increased from 4% to 25% for L_g of 100nm HEMTs. Moreover, this 25% AlGaN back-barrier epi-structure with proper design of carbon doping in the buffer can achieve state of the art RF P_{out} >3 W/mm combined with PAE >65% at 40 GHz [135].

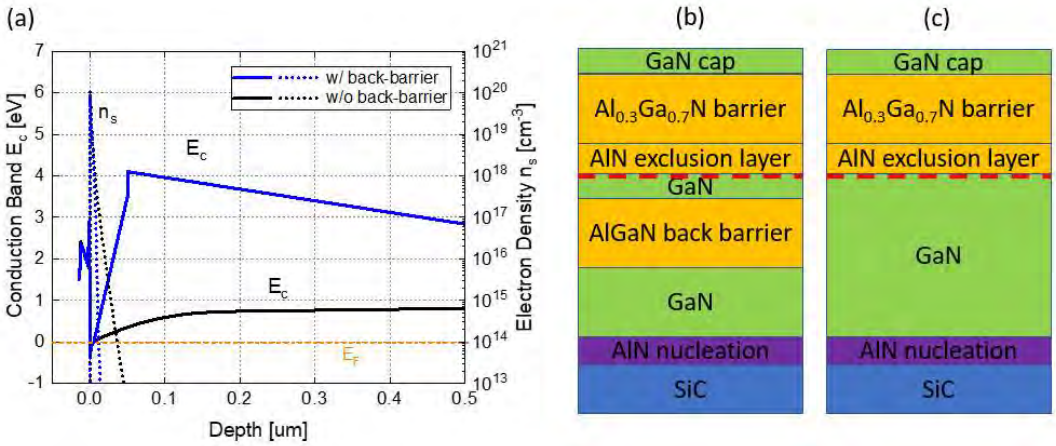

Fig. 5.2. (a) TCAD simulation of the conduction band (E_c) and electron density (n_s) for heterostructure (b) with and (c) without AlGaN back-barrier.

In this work, we investigate the impact from various carbon doping concentrations (Fig 5.3) and verified by SIMS (Fig 5.4) in AlGaN back-barrier and GaN buffer to GaN HEMTs performance.

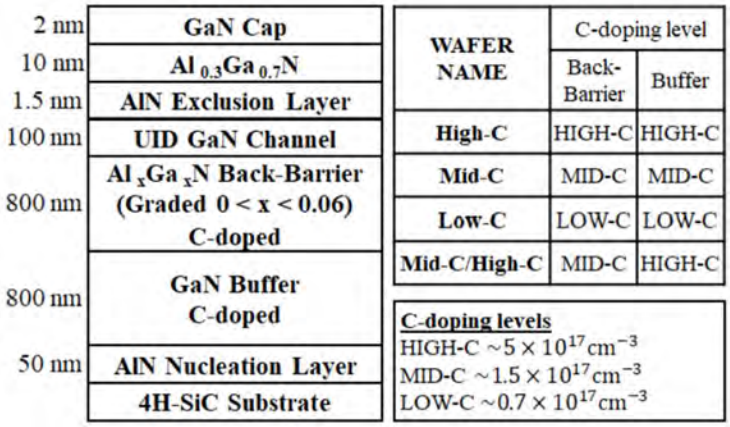

Fig. 5.3. Schematic of epi-structure and C-doping concentration.

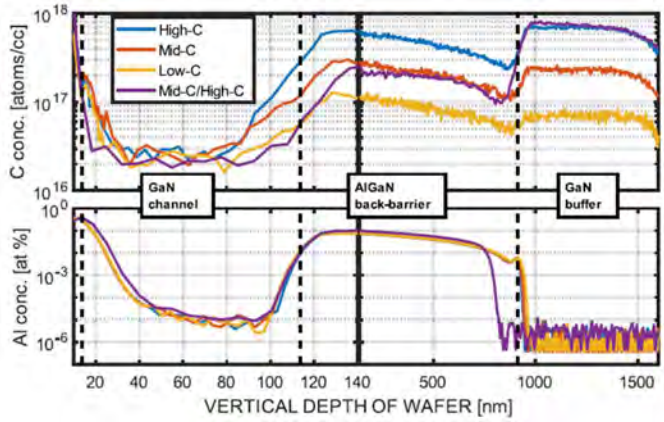

Fig. 5.4. SIMS data of C-doping profile and Al concentration for four different epi-structures.

DC measurements showed a similar I_{DS} (>600 mA/mm) and g_m (>300mS/mm) for all samples. A slightly higher I_{DS} for Mid-C/High-C may be due to lower C-doping level at 2DEG channel compared to High-C and Mid-C. Moreover, higher C-doping samples showed a higher degradation of R_{on} (Table 5.1).

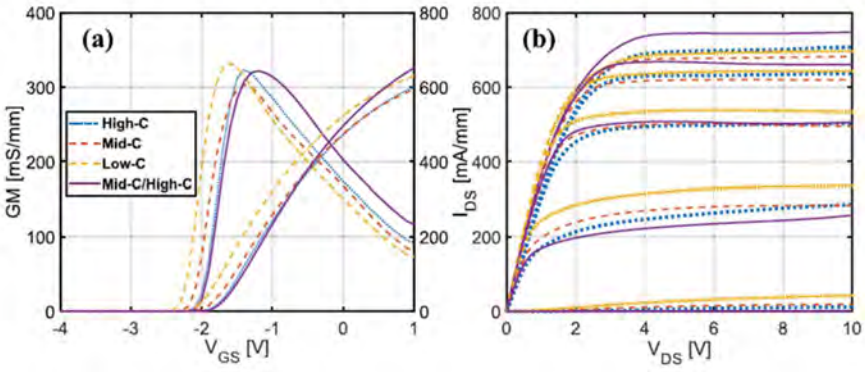

Fig. 5.5. DC (a) transfer characteristics and (b) I-V measurements.

Short channel effects were characterized by DIBL and SS (Table 5.1). Low-C sample showed a larger degradation of DIBL and SS due to poor electron confinement. Comparing DIBL of Mid-C/High-C and Mid-C indicates that the high C-doping level in GaN buffer cannot contribute to the 2DEG confinement; while comparing DIBL of Mid-C/High-C and High-C indicates that the C-doping in GaN channel region and the interface between GaN channel/AlGaN back-barrier plays an important role of 2DEG confinement.

Table 5.1. Summary DC results.

	L_g = 200nm (L_g = 100nm)						
WAFER	R_{on} [Ω·mm]	SS @2.1V [mV/dec.]		SS @20.1V [mV/dec.]		DIBL [mV/V]	
High-C	3.5	66	(72)	78	(87)	2.0	(2.8)
Mid-C	2.9	68	(75)	77	(93)	5.4	(5.3)
Low-C	2.0	69	(76)	92	(102)	8.1	(14)
Mid-C/High-C	2.2	71	(74)	81	(96)	5.9	(11)

Further analysis of traps on these four samples were performed by pulsed-IV characteristics (Fig. 5.6). Similar surface-related trapping effects were obtained for all samples (~ -20%) due to identical SiN passivation, barrier design, and process scheme. Slightly higher gate-lag on High-C is probably due to residual C-doping level at the surface of epi-structure. A higher C-doping level in the GaN channel and back-barrier results in a larger R_{on} degradation and current collapse for all wafers. Comparing the current collapse of Mid-C and Mid-C/High-C sample shows that the AlGaN back-barrier can effectively prevent electron trapping in the GaN buffer beneath the back-barrier.

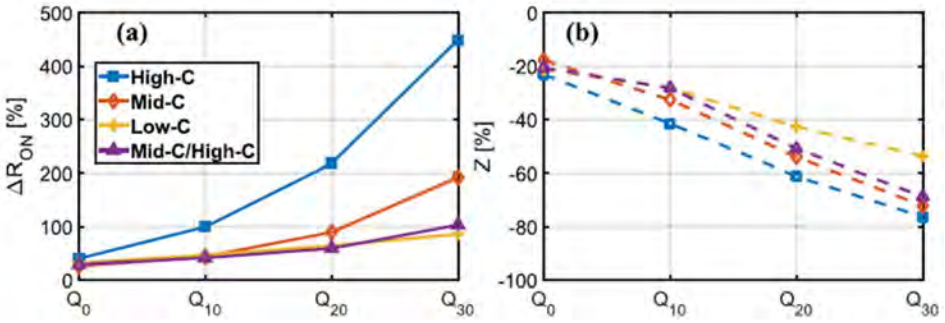

Fig. 5.6. (a) dynamic R_{on} degradation and (b) surface- and buffer-related current collapse ratio at different quiescent biases.

This study demonstrates that higher carbon doping effectively mitigates short-channel effects, however, with the trade-off of increased trapping effects. The carbon tail in the GaN channel plays a significant role in trapping effects, even under low electric fields. Notably, an AlGaN back-barrier with a low aluminum composition (6%) can effectively screen the field, thereby preventing buffer-induced trapping effects.

5.2 QuanFINE - a 'buffer-free' concept

One potential approach to mitigate trapping effects while preserving the 2DEG confinement is a buffer-free heterostructure, trademarked "QuanFINE" by SweGaN AB. This design entirely removes the thick Fe-/C-doped GaN buffer, leading to a thin unintentionally doped (UID)-GaN channel situated between the barrier layer (e.g., AlGaN barrier, as referred to in this study) and the AlN nucleation layer, as shown in Fig. 5.7. Given the slimness of the UID-GaN channel, the AlN nucleation layer can effectively serve as the back-barrier to confine the channel.

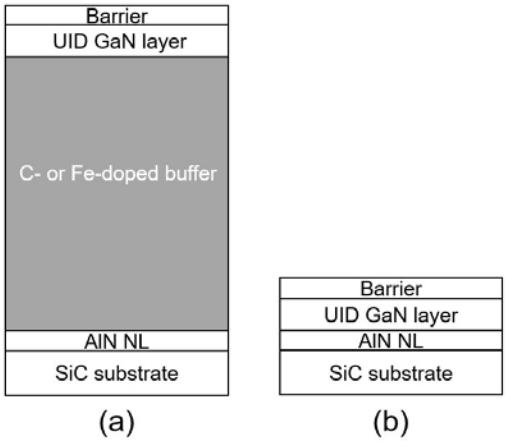

Fig. 5.7. The concept of (a) conventional thick intentional-doped GaN buffer and (b) 'buffer-free' QuanFINE epi-structures.

The band diagram and electron distribution for both the QuanFINE and conventional Fe-doped GaN buffer epi-structures were simulated using Synopsys Sentaurus TCAD (Fig 5.8). Based on the electron distribution results, the QuanFINE appears to offer superior 2DEG confinement compared to the traditional Fe-doped buffer epi-structure.

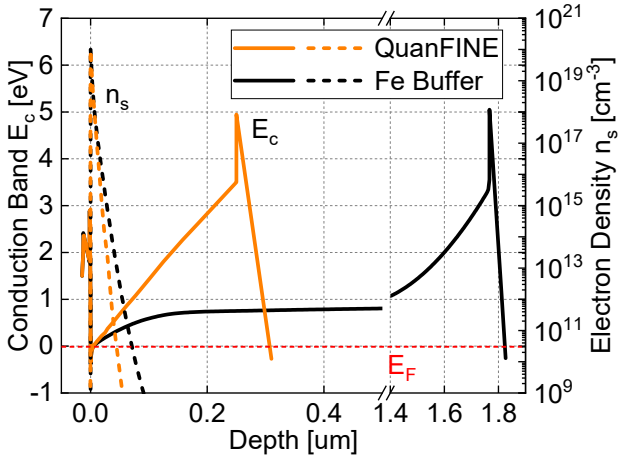

Fig. 5.8. Conduction band (E_c) (solid line) and electron density (n_s) (dashed line) of QuanFINE and "Fe buffer" at the V_{DS} of 0 V.

5.3 Benchmark QuanFINE to conventional Fe-doped thick GaN epi-structure

Performance benchmarking for HEMTs was conducted on the QuanFINE and compared to the conventional Fe-doped thick GaN epi-structures (referred to as "Fe-buffer", supplied from a commercial source) with nominally identical barrier designs. HEMTs were fabricated using an identical process flow (as detailed in Chapter 2.2.). The barrier design comprises a 2 nm GaN cap, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier, and a 1 nm AlN exclusion layer. Below the barrier, the QuanFINE features a thin 250 nm UID-GaN channel layer, whereas the "Fe-buffer" epi-structure includes an 1800 nm thick Fe-doped GaN buffer layer. Both were epitaxially grown atop a thin AlN nucleation layer on a semi-insulating SiC substrate. HEMTs on both epi-structures were designed with an L_g of 200 nm (and 100 nm for the variant in parentheses).

Table 5.2. Summary of 2DEG properties before and after device processing.

	QuanFINE	Fe-buffer
2DEG properties before and (after) device processing		
n_s [10^{13}cm^{-2}]	1.16 (1.02)	N/A (1.08)
μ [cm^2 V^{-1}s^{-1}]	2030 (2000)	N/A (2090)
R_{sh} [Ω sq.$^{-1}$]	268 (306)	N/A (276)

The 2DEG properties were evaluated post-device processing using van der Pauw structures and were then compared to the properties of the as-grown epi-structures, as shown in Table 5.2. A decrease in carrier concentration (n_s) and mobility (μ) was observed for the QuanFINE, leading to an increased sheet resistance (R_{sh}). This reduction might be attributed to the external compress strain induced by the LPCVD SiN passivation [27, 136]. On the other hand, the "Fe-buffer" exhibited a slightly higher n_s and μ, which could be a result of minor differences in the thickness and Al composition of the barrier design.

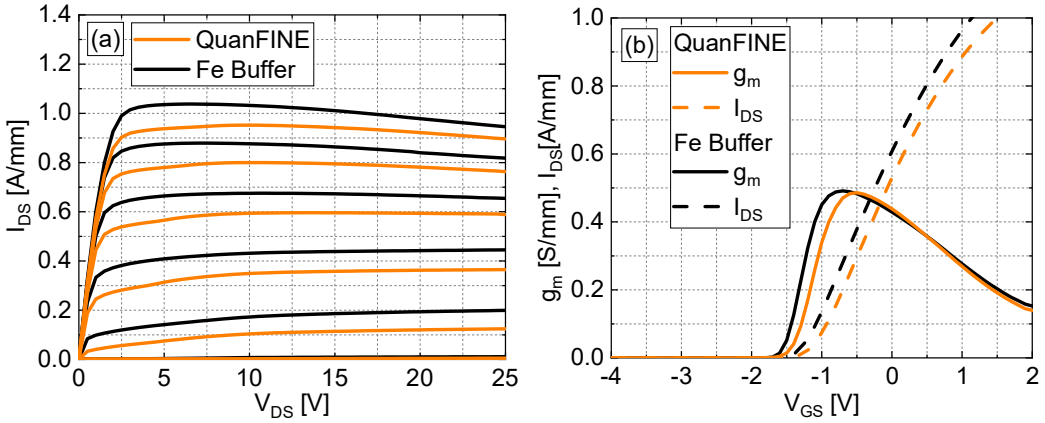

Fig. 5.9. DC characteristics for HEMTs with an L_g of 200 nm on both materials. (a) I_{DS} versus V_{DS} for V_{GS} = -4:0.5:1 V, (b) shows I_{DS} and g_m versus V_{GS} for V_{DS} of 10 V.

DC measurements performed on HEMTs with a L_g of 200 nm for both epi-structures reveal an I_{DS} of approximately 1 A/mm at a V_{GS} of 1 V and a peak g_m of around 500 mS/mm, as depicted in Fig. 5.9. Given a similar V_{TH}, the HEMTs on the "Fe-Buffer" display a marginally higher I_{DS}. This could be attributed to a slightly increased μ, higher n_s, and reduced R_c.

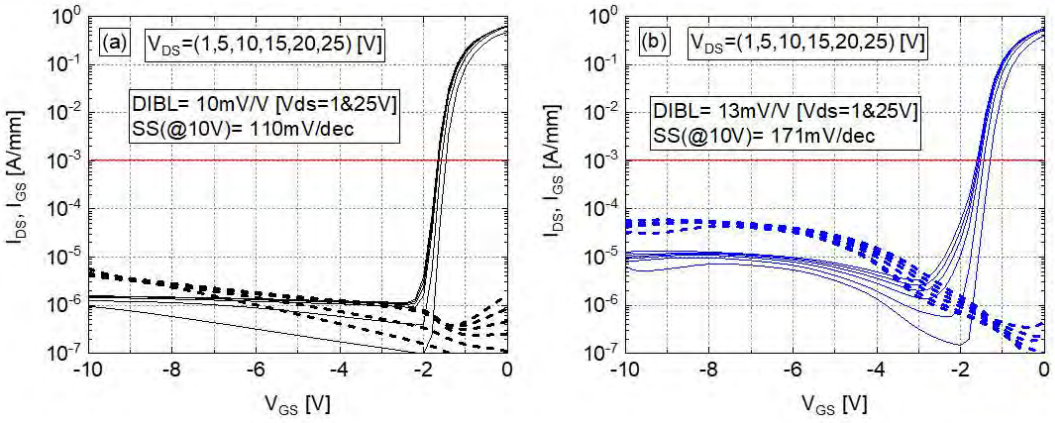

Fig. 5.10. Short channel effects characteristics by DIBL and SS on HEMTs with the L_g of 200 nm, (a) "Fe Buffer" and (b) QuanFINE.

The short channel effects are evaluated by examining DIBL and SS, as described in Equations 2.6 and 2.7. DIBL was determined at V_{DS} of 1 V and 25 V, while SS was ascertained from the transfer characteristics, using the minimum SS value at V_{DS} = 10 V. HEMTs with a L_g of 200 nm on the QuanFINE epi-structure exhibit a DIBL of 13 mV/V. This is in the same range as the DIBL value of 10 mV/V for the HEMTs on the "Fe-Buffer" epi-structure, as illustrated in Fig. 5.10. Nonetheless, these DIBL results are not in agreement with the TCAD simulations shown in Fig. 5.8, which could result from un-intentional impurities at the GaN or the interface between GaN/AlN nucleation layer during growth of QuanFINE. Furthermore, HEMTs based on the QuanFINE epi-structure display a leakage current with an order of magnitude higher during deep pinch-off conditions (V_{GS} < -4V). This could be attributed to the direct interaction between the gate and the 2DEG at the mesa sidewall and within the UID-GaN layer, which lacks Fe/C doping. Additionally, there is a notable subthreshold leakage in the QuanFINE HEMTs at a V_{GS} of -2 V, possibly stemming from internal leakage channels within the epi-structure.

The pulsed-IV measurements were carried out on HEMTs with a L_g of 100 nm for both epi-structures, as depicted in Fig 5.11. The QuanFINE structure exhibits a lower I_{DS} at a V_{GS} of 1 V. This could be attributed to its lower n_s and μ, as well as minor variations in the as-grown barrier compared to the Fe-buffer. Additionally, QuanFINE demonstrates a reduced buffer-related current collapse (14.6% compared to 17.8%) and a smaller dynamic R_{on} degradation (21% as opposed to 36.7%). However, both epi-structures display a consistent surface-related current collapse of 4%. These findings underscore the advantages of omitting the Fe-doped GaN buffer, which inherently contributes to trapping effects.

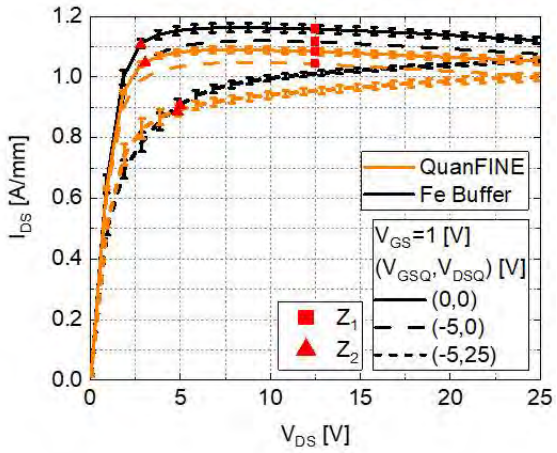

Fig. 5.11. Pulsed-IV measurements were performed at different quiescent biases. The results were extracted from 12 randomly selected HEMTs with a L_g of 100 nm on QuanFINE and Fe Buffer samples.

High-frequency small-signal performances of both epi-structures were analyzed up to 145 GHz. HEMTs with L_g of 100 nm and 200 nm exhibited similar f_T (72 and 46 GHz) GHz and f_{max} (130 and 115GHz) , respectively. These findings suggest that the removal of the thick GaN buffer in QuanFINE does not adversely affect the high-frequency performance.

Large-signal measurements were conducted on HEMTs under class-AB conditions (approximately 20% of the maximum I_{DS}) using an active load-pull system at 3 GHz [137]. The P_{out} performance was assessed by referencing the $P_{out,\ class\text{-}A}$ as described in Equation 2.20. Both epi-structures achieved a peak P_{out} of 4.1 W/mm and a similar PAE of 40% at a V_{DS} of 30 V (Fig. 5.12). The comparable large-signal performance can be attributed to the similar channel confinement and breakdown voltage. Furthermore, the higher I_{DS} observed in the Fe-buffer is offset by the reduced current collapse in QuanFINE, leading to a consistent $I_{DS,\ knee}$ and, consequently, a similar maximum P_{out}.

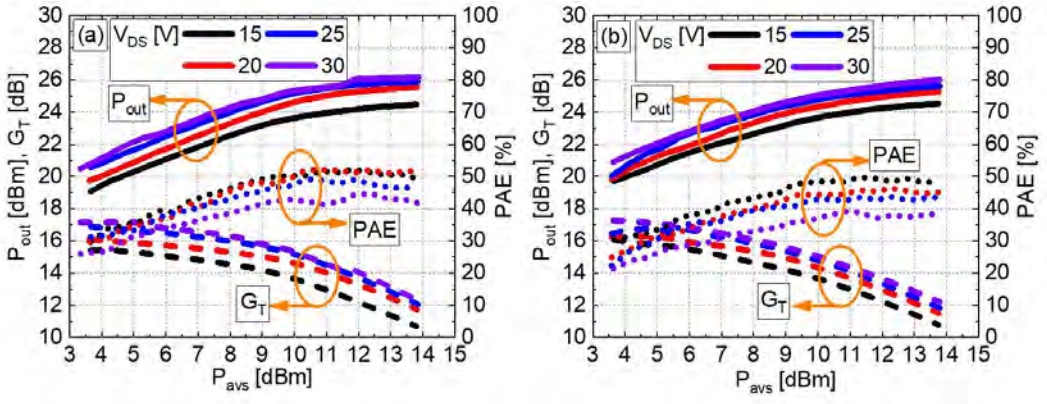

Fig. 5.12. 3 GHz active load-pull measurements of HEMTs with an L_g of 200 nm performed at different drain bias on (a) "Fe-Buffer" and (b) QuanFINE.

5.4 Impact of GaN channel thickness in QuanFINE

Highly scaled GaN HEMTs require buffer designs incorporating Fe, C dopants, or back-barriers to effectively confine the 2DEG channel. For these devices, achieving proper confinement requires high doping concentration and precise placement of the dopants and back-barrier close to the 2DEG channel. However, these methods often introduce severe trapping effects. The QuanFINE structure utilizes an AlN nucleation layer to achieve 2DEG confinement comparable to traditional AlGaN back-barrier approach. The trade-off between 2DEG confinement and trapping effects as influenced by GaN channel thickness has been systematically investigated in this section.

The performance of GaN HEMTs on QuanFINE was explored for varying GaN channel thicknesses. HEMTs were fabricated following the process flow outlined in chapter 2.2. All epi-structures shared a similar barrier design, comprising a 2 nm GaN cap, 10 nm $Al_{0.3}Ga_{0.7}N$ barrier, and a 1 nm AlN exclusion layer. Below this barrier, GaN channels with thicknesses of 150 nm, 200 nm, and 250 nm (labeled as QF150, QF200, and QF250) were epitaxially grown over a 60 nm AlN nucleation layer, which was atop a semi-insulating SiC substrate. The structural integrity was verified by measuring the full width at half maximum (FWHM) of the X-ray diffraction (XRD) rocking curve on both GaN (002) and (102) planes, as detailed in Table 5.3. No discernible structural degradation was observed in epi-structures with reduced GaN channel thickness. HEMTs across all epi-structures feature a L_g of 40, 70, 100, 150, and 200 nm. The devices employ deeply recessed Ta/Al/Ta ohmic contacts, achieving contact resistances of approximately 0.3 Ω mm. Notably, these devices do not incorporate a source-connected field-plate, a design decision aimed at reducing parasitic capacitance and preventing the masking of trapping effects.

Table 5.3. FWHM from XRD rocking curves and 2DEG properties of QF150, QF200, and QF250 before and after HEMT processing.

	QF150	QF200	QF250
GaN (002) ["]	72	83	60
GaN (102) ["]	312	340	315
2DEG properties before (and after) processing			
n_s [10^{13}cm^{-2}]	0.91 (1.00)	0.94 (1.01)	0.98 (1.05)
μ [cm^2 V^{-1}s^{-1}]	2210 (1970)	2150 (1940)	2110 (1870)
R_{sh} [Ω sq.$^{-1}$]	315 (317)	320 (318)	303 (318)

The 2DEG properties were evaluated post-device processing using Van der Pauw structures and were compared with those from the as-grown epi-structures, as presented in Table 5.3. No noticeable degradation in R_{sh} was observed following the processing. A slight variation in n_s and μ could be attributed to the added strain introduced by the SiN passivation layer [27, 136] or batch-to-batch variations of the materials.

The conduction band (E_c) and n_s distributions for QF150, QF200, and QF250 were simulated using Sentaurus TCAD, as illustrated in Fig. 5.13. By integrating across the entire simulated depth, the estimated n_s values for QF150, QF200, and QF250 are 1.02, 1.06, and 1.08 × 10^{13} cm^{-2}, respectively. Notably, QF150 demonstrates superior electron confinement in comparison to QF200 and QF250, attributable to the steeper gradient of the conduction band.

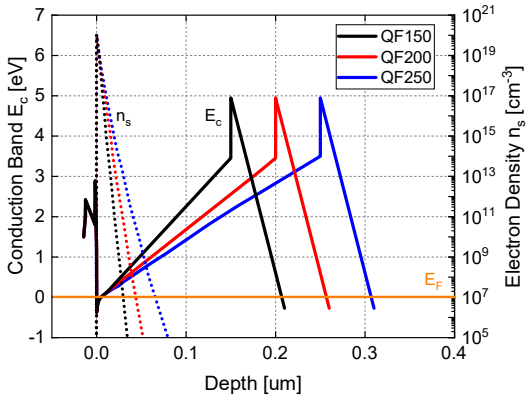

Fig. 5.13. Simulated E_c and n_s of QF150, QF200, and QF250.

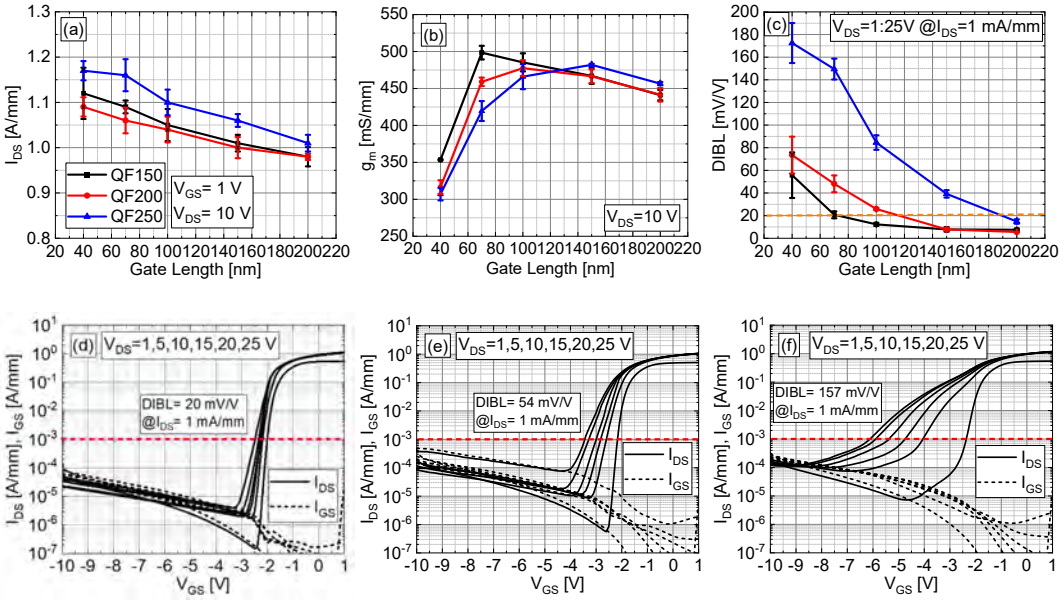

Fig. 5.14. Average DC results on HEMTs with L_{GD} of 2.5 μm, (a) I_{DS}, (b) peak g_m, (c) DIBL, and transfer characteristics of a typical HEMT with an L_g of 70 nm on (d) QF150, (e) QF200, and (f) QF250.

DC measurements were performed on HEMTs with various L_g on each epi-structure (Fig 5.14). The HEMTs exhibited an average I_{DS} above 1 A/mm at a V_{GS} of 1 V. A higher I_{DS} for HEMTs fabricated on QF250 can be attributed to the higher n_s compared to those on QF200 and QF150. The highest extrinsic transconductance g_m of 500 mS/mm was measured for the devices with an L_g of 70 nm on QF150.

Significant degradation of g_m was observed in devices with an L_g of 40 nm, primarily due to short channel effects across all epi-structures. Short-channel effects were assessed using the DIBL from Equation 2.6, utilizing a V_{po} of 1 and 25 V. Compared to conventional epi-structures for highly scaled devices (Table 5.4), QF150 demonstrates exceptional 2DEG confinement with a DIBL of 20 mV/V and 11 mV/V for HEMTs with L_g of 70 nm and 100 nm, respectively, as shown in Fig. 5.15d. By contrast, QF200 and QF250 exhibited higher DIBL values of 54 mV/V and 157 mV/V, respectively (Fig 5.15c, 5.15e, and 5.15f), correlating with the trend in g_m. These findings corroborate superior 2DEG confinement in QF150, as depicted in Fig. 5.15. Efforts to further reduce the GaN channel thickness to below 150 nm are underway, aiming to establish a platform for HEMTs with L_g smaller than 100 nm.

Table 5.4. Benchmark of DIBL in literature.

Barrier	Buffer	L_g [nm]	DIBL [mV/V]	Ref.
AlGaN	QF150	70	20	[paper F]
AlGaN	QF150	100	11	[paper F]
AlGaN	back-barrier	100	11	[138]
AlGaN	proprietary thick buffer	150	2	[139]
AlN	C-doped thick buffer	120	131	[140]
AlN	back-barrier	120	62	[140]
AlN	back-barrier	140	39	[141]

Breakdown measurements were conducted on HEMTs with L_g of 40, 70, and 100 nm and a L_{GD} of 1 µm across various epi-structures, employing a V_{GS} of -10 V and a breakdown criterion of 1 mA/mm (Table 5.5). This method ensures uniform depletion beneath the gate for a given L_g. A thinner GaN channel and a larger L_g were found to increase the V_{BR}. Notably, an HEMT with a L_g of 100 nm on the QF150 structure achieved an impressive critical electric field of 0.95 MV/cm. These outcomes are promising for efficient power amplification with a reduced L_{GD} [142].

Table 5.5. Breakdown performance of HEMTs with a L_g of 40, 70, and 100 nm with L_{GD} of 1 µm.

	QF150	QF200	QF250
V_{BR}- L_g 40 nm [V]	67	50	37
V_{BR}- L_g 70 nm [V]	83	63	50
V_{BR}- L_g 100 nm [V]	95	70	52

Pulsed-IV measurements were conducted under varying quiescent biases on HEMTs with an L_g of 70 nm and a L_{GD} of 1 µm across each epi-structure. Z_1 and Z_2 current collapses were quantified using Equations 2.9 and 2.10, with the knee points (black dots) indicated in Figure 5.15. QF200 exhibited the highest Z_1 and Z_2 dispersion, as well as dynamic R_{on} degradation, as compared to QF150 and QF250 (Table 5.6). With an identical SiN passivation layer applied, the larger Z1 might suggest that QF200 might have worse surface termination, higher surface defect density, or surface morphology. When comparing QF250 to the previous study of benchmarking between QuanFINE and Fe epi-structure, this batch of QF250 shows a higher buffer induced current collapse, which might be due to the growth in

different MOCVD (impurities, growth parameters) and different gate length. When comparing QF150 and QF250, which possess similar structural qualities, QF150 displays more pronounced trapping effects and dynamic R_{on} degradation. This behavior is likely due to the thinner GaN channel in QF150, which facilitates easier trap filling at the interface between the GaN/AlN nucleation layer (potentially leading to a two-dimensional hole gas [18]) or the semi-insulating SiC substrate, where long time constant traps such as Vanadium dopants or intrinsic point defects may exist. [143, 144].

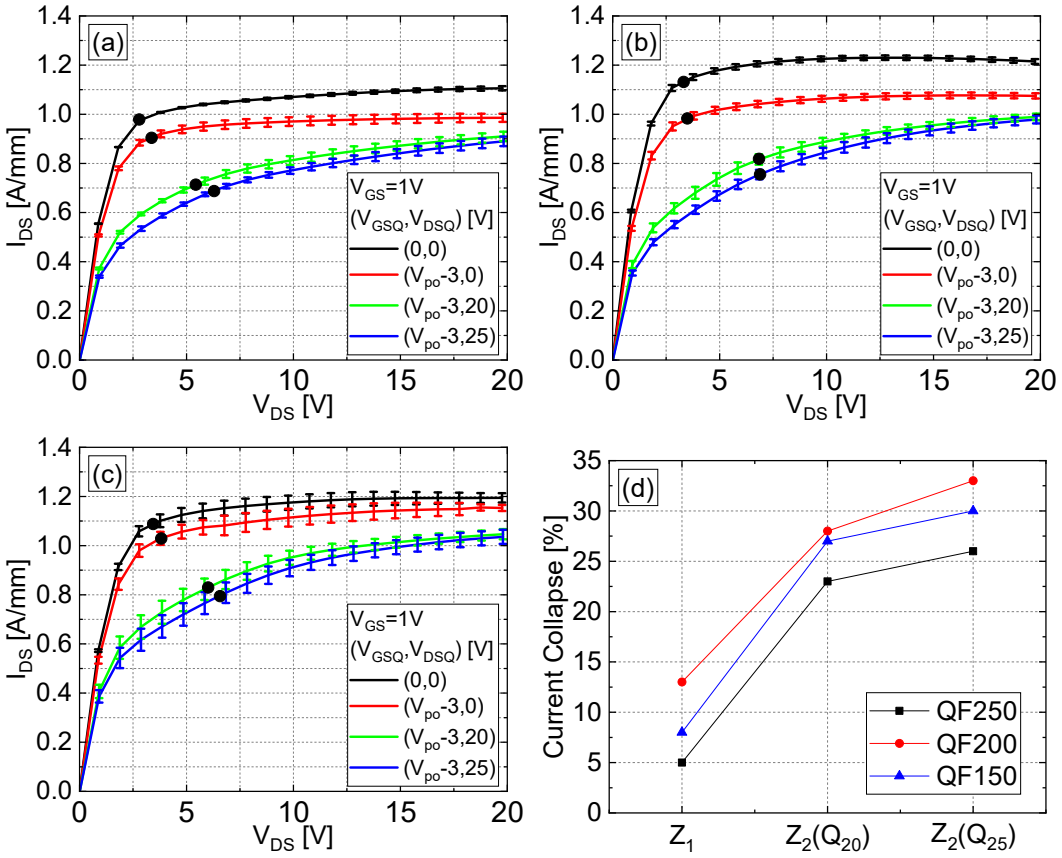

Fig. 5.15. Pulse-IV measurements on (a) QF150, (b) QF200, and (c) QF250. (d) Summary of current collapse on each epi-structures.

Table 5.6. Extraction figure of merit from pulsed IV measurements.

	QF150	QF200	QF250
R_{on} (Q_{ref}) [Ω mm]	1.58	1.43	1.53
R_{on} (Q_{25}) [Ω mm]	2.73	2.61	2.37
Dynamic R_{on} [Increase %]	72	82	55

High-frequency small-signal performance was evaluated on HEMTs with a L_g of 70 nm and an L_{GD} of 1 μm for each epitaxial structure. Average values of the equivalent circuit parameters for the small-signal model, which include gate-drain capacitance C_{gd}, gate-source capacitance C_{gs}, drain-source capacitance C_{ds}, input

resistance R_i, output resistance R_{ds}, and g_m, were extracted from the same devices using a direct extraction method, as shown in Table 5.7 [39]. f_T/f_{max} are constrained to below 120 GHz due to the significant parasitic capacitance resulting from the field-plate gate design, which could be mitigated by employing a mushroom gate concept. Furthermore, the f_T/f_{max} values are comparable across all structures because increases in C_{gs} and g_m are connected. The elevated C_{gs}, R_{ds}, and g_m observed in QF150 can be associated with the superior two-dimensional electron gas (2DEG) confinement, as depicted in Figure 5.14.

Table 5.7. Small-signal equivalent circuit parameters, f_T, f_{max}, and large-signal performance of HEMTs with a L_g of 70 nm.

	QF150	QF200	QF250
C_{gd} [fF]	7	7	8
R_i [Ω]	15	15	15
C_{gs} [fF]	109	103	95
R_{ds} [Ω]	470	435	401
C_{ds} [fF]	25	25	28
g_m [mS]	58	54	52
f_T [GHz]	86	76	74
f_{max} [GHz]	111	103	101
$P_{out, 3dB}$ [W/mm]	2.0	2.3	3.3
$P_{out, max}$ [W/mm]	2.8	2.6	3.6
Linear Gain [dB]	13.8	10.9	7.7
PAE_{max} [%]	47	43	42
PAE @ $P_{out, max}$ [%]	44	42	38

Large-signal performance was assessed on HEMTs with a L_g of 70 nm and a L_{GD} of 1 μm at 28 GHz using an active load-pull system (MT2000) by Anteverta Maury [145, 146] (Fig 5.16). The HEMTs were biased (un-pulsed) at an I_{DSQ}= 100 mA/mm (class-AB) with the RF power sweeps carried out under both continuous wave (CW) and pulsed conditions. The pulsed operation had a pulse width of 50 μs and a duty cycle of 10%. Up to a P_{out} of 23.5 dBm (2.27 W/mm) at a V_{DS} of 25 V, the RF performance of the HEMTs exhibited no discernible difference between CW and pulsed RF modes, which could be attributed to efficient heat dissipation in the QuanFINE structure [147]. Large-signal performance was analyzed at V_{DS} = 20 V (Table 5.6) by comparing it to the $P_{out, max}$ for ideal class-A operation, as defined by Equation 2.20. QF250 demonstrated the highest P_{out} of 3.6 W/mm, likely due to its higher I_{DS} and reduced trapping effects. Conversely, QF150 and QF200 yielded lower P_{out} values of 2.8 W/mm and 2.6 W/mm, respectively, which can be attributed to their lower I_{DS} and larger trapping effects. The influence of short-channel effects on the $V_{DS, max}$ and the $I_{DS, off}$ is considered less significant due to the dominant trapping effects on HEMTs that lack a source-connected field-plate. A superior gain and PAE on QF150 can be linked to a higher g_m, as shown in Fig. 5.14b, and a diminished short-channel effect, as seen in Fig. 5.14c. In Fig. 5.16, HEMTs on QF150 demonstrated a commendable gain of 15 dB and a P_{out} of 25 dBm (3.2 W/mm), with an associated PAE of 40% measured at a V_{DS} of 25 V. Lowering the V_{DS} to 15 V led to an increased peak PAE of 48%. A P_{out} of 3.2 W/mm on QF150 and 4.8 W/mm on QF250 was attainable at a V_{DS} of 25 V. Additionally, a PAE of 56%,

with an associated P_{out} of 2 W/mm at 15 V, was achieved on QF150 when tuned for maximum PAE.

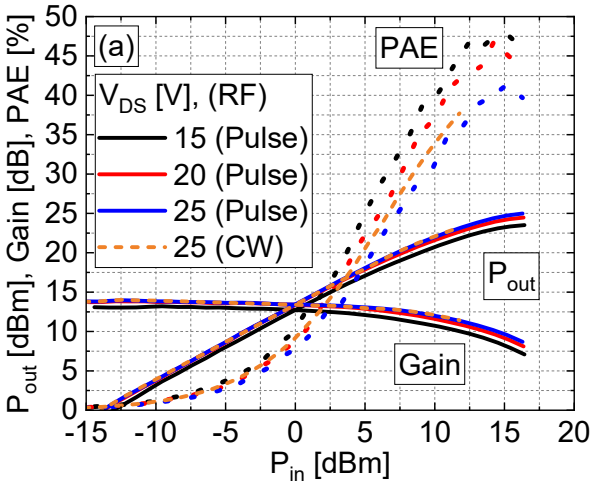

Fig. 5.16. Power sweeps at different V_{DS} on QF150.

5.5 Investigation and mitigation of trapping mechanisms in QuanFINE

The QuanFINE concept eliminates the thick Fe-/C-doped GaN buffer layer to mitigate trapping effects and leverages the AlN nucleation layer as a back-barrier to confine the 2DEG channel through band structure engineering. Despite achieving high epitaxial quality, as verified by transmission electron microscopy and X-ray diffraction rocking curve analyses, QuanFINE still exhibits some trapping effects. This section investigates the trapping and de-trapping mechanisms in two QuanFINE structures: QF-A, the baseline structure, and QF-B, which incorporates Si delta doping (concentration: 3×10^{18} cm^{-3}) at the interface of GaN channel and AlN nucleation layer to perform band structure engineering by modifying the Fermi level (Fig. 5.17a). Si delta doping reduces the valence band (E_v) level, thereby lowering the two-dimensional hole gas (2DHG) density from 2.5×10^{13} cm^{-2} to 8×10^{12} cm^{-2}, according to TCAD simulations (Fig. 5.17b). Both structures share a similar epitaxial design, comprising a 60 nm nucleation layer, a 250 nm GaN channel layer, and an active layer consisting of a 1 nm AlN exclusion layer, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2 nm GaN cap layer (Fig. 5.17a).

The structure quality of both epi-structures was characterized by the full width at half maximum (FWHM) of the XRD rocking curve on GaN (002) and (102) planes, while the 2DEG properties, including n_s, μ, and R_{sh}, were determined using contactless Hall effect measurements (Lehighton) and Eddy current measurements (Table 5.8). The slightly higher FWHM observed in QF-B can be attributed to the modifications made to the interface between the GaN channel and the AlN nucleation layer. As result, the slight reduction in μ observed in QF-B can be attributed to electron scattering resulting from the lower structural quality or batch to batch MOCVD reproducibility.

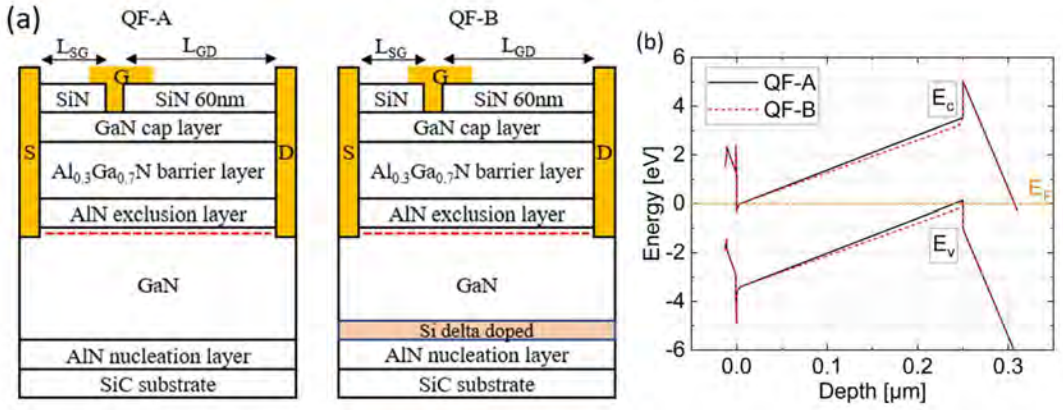

Fig. 5.17. (a)The concept of QF-A and QF-B epi-structures and (b) E_c and E_v of QF-A and QF-B.

Table 5.8. FWHM from XRD rocking curves and 2DEG properties of QF-A and QF-B before and after HEMT processing.

	QF-A	QF-B
GaN (002) ["]	122	216
GaN (102) ["]	336	443
2DEG properties before (and after) processing		
n_s [10^{13}cm^{-2}]	1.06 (1.02)	1.07 (1.00)
μ [cm^2/Vs]	2057 (2002)	1966 (1911)
R_{sh} [Ω/sq.]	286 (306)	298 (327)

HEMTs for both epi-structures feature a L_g of 200 nm. They have a L_{GS} of 0.9 μm, L_{GD} of 2.2 μm, and a gate width (W_g) of 2×50 um. The devices utilize deeply recessed Ta/Al/Ta ohmic contacts with a low annealing temperature, resulting in contact resistances of ≈0.3 Ω·mm. It's worth noting that these devices do not include a source-connected field-plate. This deliberate design choice aims to minimize parasitic capacitance and prevent masking of trapping effects. A detailed device fabrication flow can be found in chapter 2.2.

The properties of the 2DEG were assessed after device processing using van der Pauw structures and were compared with those of the as-grown epitaxial structures, as outlined in Table 5.8. There was no discernible degradation in the R_{sh} following processing. However, a minor fluctuation in n_s and μ was noted, likely due to an additional compressive strain induced by the Si-rich SiN passivation layer [27, 136].

The DC characteristics showed an I_{DS} of 0.82 and 0.73 A/mm, along with R_{on} of 1.9 and 2.1 Ω·mm on QF-A and QF-B, respectively. The higher I_{DS} and lower R_{on} observed in QF-A can be partially attributed to the enhanced properties of the 2DEG and a threshold voltage (V_{TH}) shift of approximately 0.15 V. This V_{TH} shift may be a result of minor variations in the barrier thickness. Moreover, the higher g_m of 450 mS/mm in QF-A, compared to 423 mS/mm in QF-B, primarily arises from reduced short channel effects, leakage current, enhanced pinch-off characteristics and uniformity of epi-wafers and devices. QF-A exhibits better 2DEG confinement,

boasting a DIBL of 17 mV/V, whereas QF-B exhibits a worse DIBL of 34 mV/V. This trend aligns well with the g_m between two epi-structures. Furthermore, the off-state leakage current in QF-B is one order of magnitude higher than that in QF-A. Mesa isolation measurements were conducted using separate pads with a 15 µm separation and a bias voltage of 200 V [148]. The mesa isolation of QF-B is lower than that of QF-A, suggesting that the GaN channel layer in QF-B possesses lower resistivity compared to QF-A due to a Si delta doping at the interface of GaN and AlN nucleation layer (Table 5.9).

Table 5.9. Summarized average DC parameters for QF-A and QF-B.

	QF-A	QF-B
$I_{DS\text{-}max}$ [A/mm]	0.82	0.73
g_m [mS/mm]	450	423
V_{TH} [V]	-1.15	-1.00
DIBL [mV/V]	17	34
Off-state I_{DS} [A/mm]	1E-5	1E-4
R_{on} [Ωmm]	1.92	2.06
Mesa isolation [10^9 Ω]	208	0.230

The f_T and f_{max} were calculated from s-parameter measurements (Table 5.10). A small-signal equivalent circuit model was extracted and averaged from the same devices using the bias ([V_{GS}, V_{DS}] = [-0.9, 20] V) that gives highest f_{max}, employed a direct extraction method [39]. A similar ratio between the g_m and C_{gs} tends to yield a similar f_T and f_{max}. The observed slight decreased in g_{ds} in QF-B can be correlated with the short channel effects discussed above.

Table 5.10. Summarized of f_T, f_{max}, and small signal equivalent circuit parameters for QF-A and QF-B.

	QF-A	QF-B
f_T [GHz]	46	46
f_{max} [GHz]	105	100
C_{gd} [fF]	10	11
R_i [Ω]	7	6
C_{gs} [fF]	232	215
g_{ds} [Ω^{-1}]	0.82	0.75
C_{ds} [fF]	31	34
g_m [mS]	60	52

Table 5.11. Extracted figure of merit from pulsed-IV measurements.

	QF-A	QF-B
R_{on} (Q_{ref}) [Ω·mm]	2.06	2.14
R_{on} (Q_{40}) [Ω·mm]	3.28	3.07
R_{ON} [Increase %]	59.2	43.4
Z_1 [%]	7	7
Z_2 [%]	27	20

Trapping effects on devices for both epi-structures were characterized by pulsed-IV measurements using a pulse width of 1 µs with a duty cycle of 0.001% (Fig. 5.18).

Four different quiescent bias points (V_{GSQ}, V_{DSQ}) were considered: (0, 0), (V_{TH}-4, 0), (V_{TH}-4, 20), (V_{TH}-4, 40) V, referred to as Q_{ref}, Q_0, Q_{20}, and Q_{40} to extract the Z_1, Z_2, and R_{on} (Table 5.11). Both QF-A and QF-B HEMTs exhibit a comparable Z_1 of approximately 7 %, which is due to the identical SiN passivation applied in both epi-structures. However, QF-A displays a higher Z_2 at 40 V of 27 %, in contrast to the 20 % observed in QF-B. These findings are consistently reflected in the dynamic R_{on} values of QF-B, which are smaller than those of QF-A, as detailed in Table 5.10. These results highlight the advantages of QF-B, which effectively reduces buffer-related trapping effects.

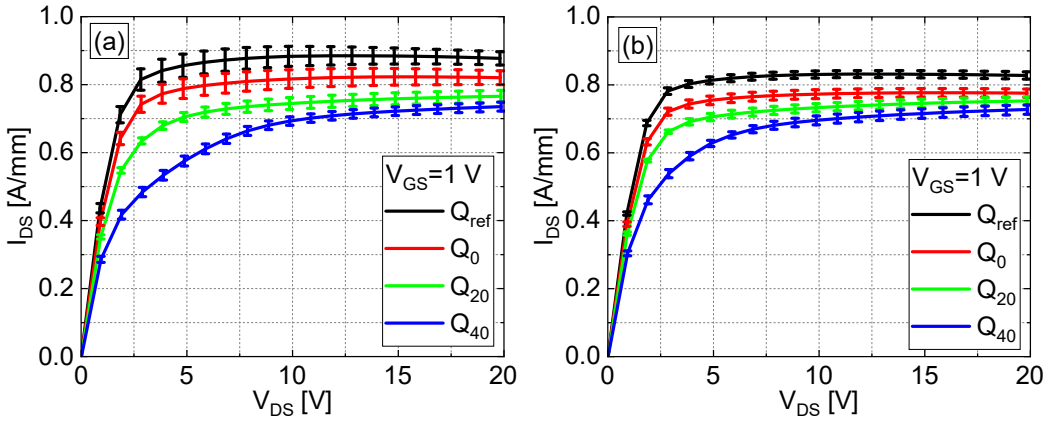

Fig. 5.18. Pulsed-IV measurements performed at different quiescent biases on (a) QF-A and (b) QF-B.

Drain current transient (DCT) measurements were performed on the same devices as the pulsed-IV measurements. In these DCT measurements, the devices were pulsed to the off-state with a bias of ([V_{GSQ}, V_{DSQ}] = [V_T-4, 40] V) for a filling time duration of 1 sec. Subsequently, the current recovery was monitored under an on-state bias setting of ([V_{GS}, V_{DS}] = [1, 7] V) for a period of 10 sec. The V_{DSQ} setting remained consistent with that employed in the pulsed-IV measurements, intended to activate the majority of traps in epi-structures. DCT measurements were conducted at three different temperatures (40, 60, 80, and 100 °C) (Fig. 5.19). Notably, QF-B demonstrated a smaller I_{DS} drop at 10^{-6} sec (compared to reference saturated I_{DS} at 10 sec) than QF-A. Two distinct traps, denoted as T1 and T2, were identified. T1 was shown in both epi-structures, while T2 was exclusively present in QF-A.

A reduction in the amplitude of the T1 trap at higher temperatures was revealed for both QF-A and QF-B. These indicate that T1 traps may result from threading dislocation [149]. Alternatively, this may indicate that the de-trapping processes are dominated by hopping [150] or tunneling [151] mechanisms. The T1 trap for QF-A exhibits a deviation at 100 °C (Fig. 5.20), resulting in non-Arrhenius behavior, which prevents the determination of activation energy. This phenomenon, previously reported, can be attributed to a leakage process mediated by a defect band [152]. Trap T1 in QF-B revealed small activation energies (E_A) and ß values, suggesting the formation of continuous trap energy levels. In contrast, QF-B

effectively mitigates trap T2, which exhibits a long time constant. The E_A associated with trap T2 demonstrates low thermal activation energy and a large time constant, in the order of 1-10 seconds. This trap bears similarities to traps reported previously [37, 153-155]. Possible explanations for trap T2 include electron trap-assisted tunneling mechanisms [37], the presence of carbon or hydrogen impurities from trimethylgallium (TMGa) in C-doped epi-structure [118, 153], the charging and discharging between the 2DEG and buffer [154, 155], and the formation of 2DHG [18, 156, 157]. Another possible location for the T2 trap could also be the threading dislocations since the E_A and ß are small, which indicates they are likely continuous trap energy states. By introducing the Si delta doping at the interface of GaN and AlN nucleation layer, it reduce the potential 2DHG, and provides a lateral leakage path for an faster de-trapping procedure [158, 159].

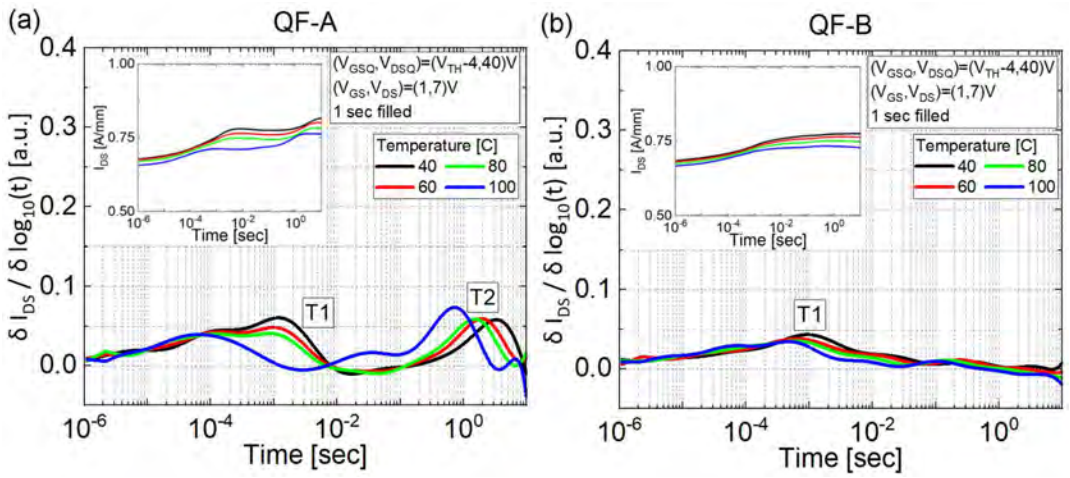

Fig. 5.19. Differential data (main figure) of the DCT measurements (inset) measured at different temperatures under the pinch off condition with V_{DS} of 40 V and 1 s filling time on (a) QF-A and (b) QF-B.

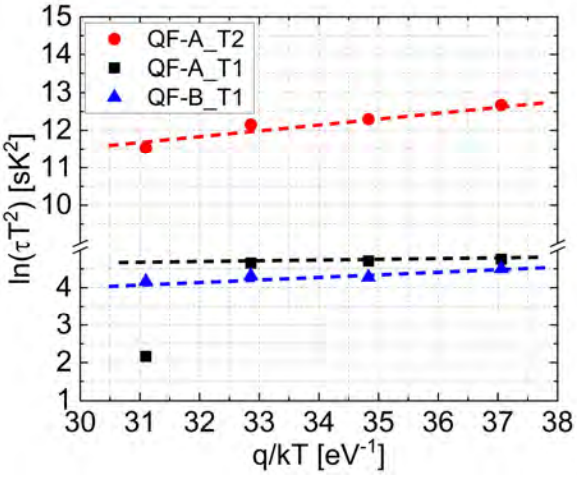

Fig. 5.20. Arrhenius plot of the identified energy levels in the temperature dependent DCT measurements.

Table 5.12. Extracted active energies, capture cross sections, and stretching terms of the traps found in Fig. 5.19 and Fig. 5.20.

	QF-A T1	QF-B T1	QF-A T2
E_A [eV]	-	0.05	0.13
σ [cm²]	-	$1.9 \cdot 10^{-21}$	$1.3 \cdot 10^{-19}$
ß	-	~0.5	~0.5

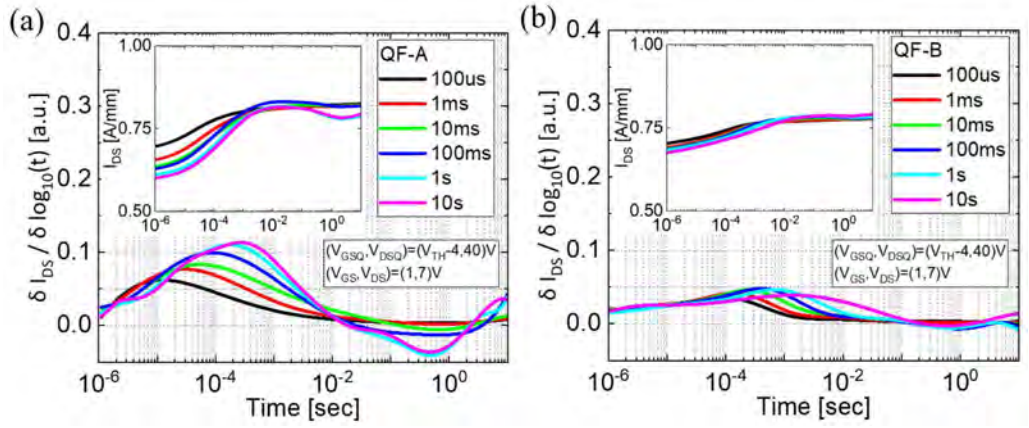

Fig. 5.21. Differential data (main figure) of the DCT measurements (inset) measured at different filling times under the pinch off condition with V_{DS} of 40 V at 25 °C on (a) QF-A and (b) QF-B.

DCT measurements were also conducted with varying filling times. These measurements were performed at 25°C with filling times ranging from 100 µs to 10 sec, maintaining the same quiescent bias settings as temperature dependence DCT measurement (Fig. 5.21). One key observation is that the time constants associated with T1 in both QF-A and QF-B were dependent on the filling time. An increased amplitude of T1 was found in QF-A for longer filling durations. Moreover, the T1 peaks for both epi-structures shifted toward a longer time constant as the filling time increased. These behaviours suggest that traps are located at threading dislocations [37, 160]. Interestingly, the amplitude of T1 in QF-A saturated at filling times ranging from 1 s to 10 s, whereas in QF-B, this saturation occurred earlier, at a filling time of 100 ms. These findings suggest a relationship between the trap states and dislocations, where the design of QF-B appears to reduce trap states related to T1 by providing a controlled leakage path, which may be correlated with lower crystal quality, characterized by higher GaN <002> and <102> FWHM, that enhances the de-trapping process. Also, tunnelling leakage is likely responsible for electron transport during the de-trapping procedure. For filling times longer than 1 s (T2 trap state in QF-A), a pattern of charging followed by discharging was evident at time constants around 0.1 to 1 s for both epi-structures. This behavior may be attributed to the charging and discharging processes occurring between the 2DEG and buffer layers [154, 155]. Since the T2 trap in QF-B is fully suppressed by the Si doping, it indicates that the Si delta doping at the GaN/AlN interface could effectively facilitate the de-trapping procedure and/or reduce the formation of 2DHG. However, the un-optimized Si delta doping resulted in more leakage, higher DIBL, and lower isolation property.

Chapter 6

Conclusions and future work

The primary aim of this study is to address key challenges limiting the performance of GaN HEMTs, including issues with ohmic contacts, surface- and buffer-related trapping effects, and 2DEG confinement. To tackle these challenges, various improvement strategies were proposed, spanning device processing techniques to epi-structure design optimizations. These include implementing ultra-low contact resistance Ti/Al/Ti and Ta/Al/Ta sidewall ohmic contacts, utilizing in-situ NH_3 pretreatment before depositing the LPCVD SiN passivation layer, introducing an AlGaN back-barrier, and adopting the innovative 'buffer-free' QuanFINE concept.

The ultra-low resistance Ti/Al/Ti and Ta/Al/Ta deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs was developed. Key achievements include reducing the R_c to approximately 0.14 and 0.24 Ω·mm, respectively, through a deep recess that bypasses the need for precise control of recess etching. The method involves recessing the barrier beyond the 2DEG, thereby exposing the 2DEG to the sidewall and ensuring coverage during ohmic metal deposition. Low-temperature annealing at 550 - 575 °C contributes to the good surface morphology and edge acuity of the contacts. Investigations into the thickness of Ti (Ta) and Al layers, as well as the recessed sidewall angle, highlight their significant impact on R_c and contact uniformity. Furthermore, the study demonstrates the applicability of this approach across different barrier designs, indicating its potential for enhancing HEMT performance and suitable for industrial production. Future work should focus on the in-situ ohmic process by in-situ plasma cleaning followed by metal deposition to minimize the oxide layer between ohmic contacts and epi-structure.

Besides, localized strain by SiN passivation, epi-structure, and ohmic metal stacks influence the localized 2DEG properties, which has a strong impact on carrier tunneling possibility between ohmic contacts and the 2DEG channel. Further improvement of contact resistance by introducing extra Si doping through implantation is also favorable.

The implementation of a plasma-free in-situ NH_3 pretreatment prior to LPCVD SiN deposition significantly mitigates the DC-RF dispersion in HEMTs. Extending the pretreatment duration diminishes the surface-related trapping effects by 40% compared to samples without pretreatment. This enhancement is reflected in improved high-frequency performance, evidenced by a 26% increase in output power at 3.3 W/mm. Additionally, on-wafer uniformity benefits from this pretreatment process. Despite these advances, samples subjected to a 10-minute pretreatment still show a minor surface-related current collapse. Future research should concentrate on refining surface treatment techniques to create an epi-structure with minimized surface-related traps. Furthermore, investigating the impact of LPCVD SiN on strain-enhanced 2DEG properties, potential Si diffusion from SiN to barrier, hydrogen incorporation in SiN, and MOCVD in-situ SiN may yield further device performance and reliability enhancements.

In the AlGaN back-barrier study, it demonstrates that the AlGaN back-barrier effectively screens the GaN buffer, preventing the activation of trap states underneath the back-barrier. The sample containing a high concentration of carbon shows improved 2DEG confinement but with a trade-off in the form of more severe trapping effects, leading to a reduction in maximum P_{out}. In contrast, the sample containing a low concentration of carbon exhibits the opposite behavior. These findings highlight the critical role of carbon doping profile optimization in enhancing performance for GaN HEMTs with AlGaN back-barrier.

The epi-structure with a buffer-free concept, QuanFINE, featuring a 250 nm GaN layer, demonstrates impressive DC performance with a current saturation of 1 A/mm and peak g_m of 500 mS/mm for HEMTs with a gate length of 100 nm. The structure ensures effective 2DEG confinement, as evidenced by a DIBL of 13 mV/V for HEMTs with a L_g of 200 nm, attributed to its double heterostructure. QuanFINE exhibits reduced trapping effects compared to traditional Fe-doped GaN buffers, thanks to its thin UID-GaN channel which harbors fewer impurities and structural defects. The RF performance of QuanFINE is on par with that of established Fe-doped buffer epitaxial wafers. These findings suggest that QuanFINE, with its elimination of intentional dopants and application of band structure engineering for 2DEG confinement, holds substantial promise.

The QuanFINE GaN channel thicknesses were further reduced from 250 nm down to 150 nm without compromising structural quality and 2DEG properties. The HEMTs with 70 nm gate length displayed outstanding DC characteristics, with peak transconductances of 500 mS/mm and drain currents above 1 A/mm. Enhanced 2DEG confinement was achieved through a thinner GaN channel, utilizing the AlN layer as an effective back-barrier, evidenced by a low DIBL of 20 mV/V at 25 V and a high E_{crit} of 0.95 MV/cm. Moreover, at 28 GHz, the devices

showed robust large-signal performance with P_{out} of 2.0 and 3.2 W/mm and PAE of 56% and 40% at 15 V and 25 V, respectively, highlighting the potential for sub-100 nm gate length HEMTs with high operation voltage in high-frequency applications.

The trapping phenomena in QuanFINE was further examined and a novel QuanFINE with Si delta doping at the interface of GaN and AlN nucleation layer was introduced. The study compared devices on both the novel and traditional QuanFINE epi-structures, finding similar 2DEG properties and crystal qualities but epi-structure with Si delta doping shows a lower mesa isolation resistance, indicating reduced buffer resistance. Pulsed-IV measurements demonstrated a lower reduction in buffer-related current collapse for the QuanFINE structure with Si delta doping, and drain current transient measurements showed that it effectively mitigated trap states with longer time constants. This improved the recovery speed of drain current and increased the initial current after device turn-on. The findings suggest that the band-structure engineering at the interfaces of the QuanFINE epi-structures could lead to new avenues to mitigate trapping effects and enhance the performance of AlGaN/GaN HEMTs.

Future work should further improve the buffer-free concept, making the characteristics towards trap-free QuanFINE epi-structure combined with a compatible device process flow. Though the QuanFINE epi-structures studied in this thesis comprised only AlGaN barriers, it is possible to establish new barrier designs that include InAl(Ga)N and pure AlN for high frequency devices, multi-channel barrier, polarized super heterojunctions (PSJ), P-GaN caps for power switch applications. Besides, advanced epitaxial design can be foreseen, such as super lattice, intentional doping including Fe, C, and Mg, as well as graded/stepped AlGaN back-barrier in QuanFINE concept. Moreover, adapting the buffer-free concept to other substrate materials such as free-standing GaN diamond, QST substrate, sapphire could be worth exploring for different applications owing to advantages each substrate can offer including cost reduction and performance enhancement.

Chapter 7

Summary of appended papers

This chapter summarizes the publications included in this work. The abstract and my contributions are presented for each publication.

Paper A

D.Y. Chen, A.R. Persson, V. Darakchieva, P.O.Å. Persson, J.T. Chen, and N. Rorsman, "Structural investigation of ultra-low resistance deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs based on Ti/Al/Ti-metallization", Semiconductor Science and Technology, Vol. 38, Issue 10, 2023.

This publication invents and investigates the deeply recessed gold-free Ti/Al/Ti ohmic contacts for III-N HEMTs technology. The low contact resistance of 0.14 Ω·mm can be achieved when the metal stacks are deposited on the sidewall of the recess and annealed at 550 °C. This approach allows a less sensitive of recessed etching depth. Important parameters of the ohmic process include the bottom Ti thickness, Al thickness, recessed sidewall angle, and annealing procedure are studied. Moreover, these contacts are successfully implemented on epi-structure with different Al content in AlGaN barrier.

My contribution: DYC designed the experiments, fabricated the TLM structures, performed the TLM measurements. ARP performed the TEM measurements on the cross section of TLM structure. DYC wrote the paper with feedback from co-authors.

Paper B

Y. K. Lin, J. Bergsten, H. Leong, A. Malmros, J. T. Chen, **D. Y. Chen**, O. Kordina, H. Zirath, E. Y. Chang and N. Rorsman, "A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs", *Semiconductor Science and Technology,* Vol. 33, Issue. 9, pp. 095019, 2018.

This publication investigates the deeply recessed gold-free Ta/Al/Ta ohmic contacts for III-N HEMTs technology. The low contact resistance of 0.24 Ω·mm can be achieved when the metal stacks are deposited on the sidewall of the recess and annealed at 575 °C. This approach allows a less sensitive of recessed etching depth. Important parameters of the ohmic process include the metal coverage, slope angle of etching sidewall, bottom Ta-layer thickness, and annealing temperature and duration are studied. Moreover, these deeply recessed contacts are successfully implemented on different heterostructures with different AlGaN barrier thickness as well as with and without the AlN exclusion layer.

My contribution: YKL, JB, HL, AM, and **DYC** designed the experiments, fabricated the TLM structures, performed the measurements. YKL wrote the paper with feedback from co-authors.

Paper C

D.Y. Chen, A.R. Persson, K.H. Wen, D. Sommer, J. Grünenpütt, H. Blanck, M. Thorsell, O. Kordina, V. Darakchieva, P.O.Å. Persson, J.T. Chen, and N. Rorsman, "Impact of *In Situ* NH_3 Pre-treatment of LPCVD SiN Passivation on GaN HEMT Performance", *Semiconductor Science and Technology,* Vol. 37, Number 3, 2022.

This publication investigates the impact of GaN HEMTs high-frequency performance by in-situ plasma-free NH_3 pretreatment before the SiN passivation layer deposited by LPCVD. Time duration-dependent of in-situ NH_3 pretreatment is studied including 0-, 3-, and 10-mins pretreatment time duration. TEM analyzation shows a reduction of native oxide layer on the sample with longer pretreatment duration, which effectively reduces 40% of the surface-related trapping effects, resulting in better on-wafer uniformity and large signal performance with 27% higher output power and better efficiency.

My contribution: DYC designed the experiments, fabricated the HEMTs. ARP performed the TEM-EELS measurements and elements analyzation. DYC performed the device measurements. DYC wrote the paper with feedback from co-authors.

Paper D

R. F-D. D. Castillo, **D. Y. Chen**, J. T. Chen, M. Thorsell, V. Darakchieva, and N. Rorsman, "Characterization of Trapping Effects Related to Carbon Doping Level in AlGaN Back-Barriers for AlGaN/GaN HEMTs", *IEEE Transactions on Electron Devices,* Vol. 71, Issue. 6, 2024.

This study examines the 2DEG confinement and trapping effects in epi-structures with varying carbon doping profiles in the AlGaN back-barrier and GaN buffer. Results indicate that the highest carbon doping profile yields the best confinement, while the lowest carbon doping profile optimizes large-signal performance. Additionally, the study confirms that the AlGaN back-barrier effectively mitigates buffer-related trapping effects by restricting the electric field from penetrating below the back-barrier. These findings underscore the importance of optimizing the doping profiles in both the AlGaN back-barrier, GaN buffer, and the interface of GaN channel/AlGaN back-barrier for enhancing microwave GaN HEMT performance.

My contribution: RFDDC and DYC designed the experiments. DYC fabricated the HEMTs on Low-C, Mid-C, and High-C samples and performed DC and PIV characterizations. RFDDC fabricated the HEMTs on Mid-C/High-C sample and performed DC, PIV, DCT, and Loadpull characterizations. RFDDC wrote the paper with feedback from co-authors.

Paper E

D. Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J. T. Chen, and N. Rorsman, "Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors", *IEEE Electron Device Letters,* Vol. 41, Issue. 6, 2020.

This publication studies the high-frequency performance of the QuanFINE double-heterostructure AlGaN/UID-GaN/AlN on SiC, which has a thin UID-GaN layer with the thickness of 250 nm in between AlGaN barrier and the AlN nucleation layer. This approach allows the AlN nucleation layer to act as a back-barrier to confine the 2DEG and minimize the buffer leakage current. The device is also benchmarked to conventional Fe-doped thick GaN buffer heterostructure with nominally the same barrier design from Cree. HEMTs with the Lg of 100 nm on QuanFINE shows similar DC performance with a saturation current of 1 A/mm and peak transconductance of 500 mS/mm as compared to Fe-doped material. Lower trapping effects are proven for the HEMTs on QuanFINE, which directly transfer to good high-frequency performance with the output power of 4.1 W/mm at 3 GHz.

My contribution: DYC designed the experiments, fabricated the HEMTs, and performed the device measurements. AM supported the transistor model extraction. HH supported the TCAD simulation. DYC wrote the paper with feedback from co-authors.

Paper F

D.Y. Chen, K.H. Wen, M. Thorsell, M. Lorenzini, H. Hjelmgren, J.T. Chen, and N. Rorsman, "Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructures" Physica Status Solidi (a), 2022.

This publication investigates the 2DEG confinement properties in highly scaled AlGaN/GaN HEMTs on the buffer-free QuanFINE epi-structure with different undoped GaN channel thickness from 250 to 150 nm. A thin GaN channel with a thickness of 150 nm can be grown without degradation of the structural qualities and 2DEG properties. TCAD simulation, DIBL, and small-signal measurements show significant improvement of 2DEG confinement with a thin GaN channel layer of 150 nm. An excellent DIBL of 20mV/V on HEMTs with an L_g of 70 nm can be achieved on AlGaN/GaN epi-structures without intentional dopants or back-barrier. Moreover, QuanFINE with an outstanding critical electric field of 0.95 MV/cm provides the possibility of reduced L_{GD}, resulting in an efficient power amplification capability. An improved 2DEG confinement prompts good large signal performance with higher gain and efficiency at 28 GHz. The benchmarking results confirm that buffer-free thin GaN channel epi-structure is suitable for high-frequency applications.

My contribution: DYC designed the experiments, TCAD simulation, fabricated the HEMTs, performed the device measurements, and wrote the paper with feedback from co-authors.

Paper G

D.Y. Chen, K.H. Wen, M. Thorsell, J.T. Chen, and N. Rorsman, "Investigation and Mitigation of Trapping Mechanisms in Buffer-Free AlGaN/GaN HEMTs", Manuscript with major revision submitted again to IEEE Transactions on Electron Devices, Jan. 2025.

This study examines trapping mechanisms in QuanFINE, presenting a new QuanFINE epi-structure with band structure engineering at the interface of GaN channel and AlN nucleation layer to mitigate these effects. Comparable 2DEG properties and crystal quality between the new and conventional QuanFINE resulted in similar DC-IV characteristics. The new epi-structure showed a higher DIBL of 34 mV/V versus 17 mV/V for the standard, indicating reduced buffer resistance. Pulsed-IV tests revealed a 20% in current collapse on the new structure, better than the 27% on the conventional. Drain current transients confirmed the new epi-structure's effectiveness in mitigating long-time-constant traps, enhancing recovery speed, and boosting initial current, suggesting improved performance for AlGaN/GaN HEMTs.

My contribution: DYC designed the experiments, fabricated the HEMTs, performed the device measurements, and wrote the paper with feedback from co-authors.

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Paper A

Structural Investigation of Ultra-Low Resistance Deeply Recessed Sidewall Ohmic Contacts for AlGaN/GaN HEMTs Based on Ti/Al/Ti-Metallization

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Structural investigation of ultra-low resistance deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs based on Ti/Al/Ti-metallization

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Abstract

This study presents a novel approach to forming low-resistance ohmic contacts for AlGaN/GaN HEMTs. The optimized contacts exhibit an outstanding contact resistance of approximately 0.15 Ω·mm. This is achieved by firstly recessing the barrier of the heterostructure to a depth beyond the channel. In this way, the channel region is exposed on the sidewall of the recess. The coverage of the Ti/Al/Ti ohmic metalization on the sidewall is ensured through tilting of the sample during evaporation. The annealing process is performed at a low temperature of 550 °C. The approach does not require precise control of the recess etching. Furthermore, the method is directly applicable to most barrier designs in terms of thickness and Al-concentration. The impact of recessed sidewall angle, thickness and ratio of Ti and Al layers, and the annealing procedure are investigated. Structural and chemical analyses of the interface between the ohmic contacts and epi-structure indicate the formation of ohmic contacts by the extraction of nitrogen from the epi-structure. The approach is demonstrated on HEMT-structures with two different barrier designs in terms of Al-concentration and barrier thickness. The study demonstrate large process window in regard to recess depth and duration of the annealing as well as high uniformity of the contact resistance across the samples, rendering the approach highly suitable for industrial production processes.

Keywords: AlGaN/GaN HEMTs, ohmic contact, annealing temperatures, recessed, sidewall

(Some figures may appear in colour only in the online journal)

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1. Introduction

GaN HEMTs have demonstrated considerable promise in the realm of high-frequency and high-power applications, owing to their inherent advantages including high electron mobility and saturation velocity combined with high breakdown voltage [1, 2]. Nevertheless, the formation of reliable and repeatable low resistivity ohmic contacts is still a concern in the fabrication of high performance HEMTs. Reducing the contact resistance (R_c) yields lower losses, resulting in less heat generation, higher output power, higher efficiency, and lower noise [3].

Ohmic contacts for GaN HEMTs are commonly fabricated using Ti- or Ta-based metal stacks or regrown contacts. Planar metal-based contacts typically exhibit an R_c of 0.2–0.4 Ω·mm, while regrown contacts achieve an R_c smaller than 0.1 Ω·mm using molecular-beam epitaxy [4] or metalorganic chemical vapor deposition (MOCVD) [5, 6]. However, the process of regrown contacts involves considerable complexity and planar metal-based ohmic contacts are therefore still the industrial standard.

In the metal-based contacts, nitrogen (N-) vacancies (acting as n-type dopants) are formed in the epi-structure during the annealing process [7–9]. The Ti/Al/Ni/Au stack is the most commonly used ohmic contact for GaN HEMTs owing to the low work function of Ti (4.33 eV) [10, 11], with the high conductivity Au layer also serves as an anti-oxidation layer [7]. However, annealing temperature above 800 °C is normally required for this type of contact, resulting in poor edge acuity, due to the diffusion of melted Al, and hampering downscaling of the drain- and source-to-gate distance. Moreover, high annealing temperature may degrade the GaN crystal structure, increase traps [12], and reduce 2DEG density due to strain relaxation [13].

To address these challenges, Ta/Al/Ta, Ti/Al/Ti, and Ti/Al/Ni/Au ohmic contacts, formed at a low annealing temperature below the melting point of Al at 660 °C, exhibiting better edge acuity and low R_c of 0.06–0.30 Ω·mm have been demonstrated [8, 14–17]. However, R_c is usually highly dependent on the barrier thickness, Al concentration, and the presence of an AlN exclusion layer. Generally, achieving a low R_c on a thick barrier with high Al content and the inclusion of AlN exclusion layer is challenging due to the longer tunneling distance. Therefore, partially recessed ohmic contacts (to reduce tunneling distance) with ultra-low R_c of 0.07 Ω·mm (Ti-based) and 0.06 Ω·mm (Ta-based) can be achieved with a recess depth close to the thickness of barrier have been investigated [8, 14]. However, it should be noted that the partial removal of the AlGaN barrier results in the degradation of the 2DEG density, which adversely affects carrier transport between the ohmic contacts and the 2DEG channel. Moreover, the spread in R_c is large (0.06–0.70 Ω·mm), mainly due to poor control of etching depth [8, 14].

The degradation of the 2DEG caused by the partially removed barrier and the sensitivity to variations in recess etching depth may be addressed by performing recess etching beyond the 2DEG and form the ohmic contacts on the resulting sidewall. Recently, we reported on deeply recessed Ta/Al/Ta sidewall ohmic contacts formed at a low annealing temperature with a high uniformity and low R_c of 0.24 Ω·mm [18]. Insensitivity to both etching depth and barrier designs were verified. However, the Ta-N alloy formed from N-extraction process during the ohmic annealing, limits the reduction of R_c. To further reduce R_c, the implementation of Ti-based metal stacks is preferred, given that the resistivity of TiN is lower compared to that of TaN [19].

In this study, we demonstrate ultra-low contact resistance ohmic contacts formed by deep recessing and Ti/Al/Ti metallization with high uniformity, large process window, and low annealing temperature for source and drain terminals on high frequency and high power transistors. Critical parameters, including the thickness of the bottom Ti layer, the Al layer, and the recessed sidewall angle (θ), were investigated. Two epi-structures with different barrier designs were utilized to verify the general applicability of this concept. The mechanism of ohmic contact formation was investigated using scanning transmission electron microscopy (STEM) in combination with energy dispersive x-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS).

2. Experimental

Two AlGaN/GaN epi-structures (Epi I and Epi II) were grown on a semi-insulating SiC substrate using MOCVD by SweGaN (table 1) [20, 21]. Both epi-structures were grown on a 'buffer-free' QuanFINE®, which eliminates the need for a thick GaN buffer layer [22]. High structural quality was measured on both wafers by the full width at half maximum (FWHM) of the x-ray diffraction (XRD) rocking curve on the GaN <0 0 2> and <1 0 2 >. The similarity of crystal quality ensures limited impact of R_c in this work. The 2DEG density (n_s) and electron mobility (μ) were measured by contactless Hall effect measurements (Lehighton), while the sheet resistance (R_{sh}) was characterized by eddy current. The lower μ observed in Epi I, as compared to Epi II, can be attributed in part to electron scattering effects resulting from a higher n_s or the enhanced alloy-scattering from the higher Al-content in the barrier layer.

The wafers were diced into 16 × 16 mm^2 samples and subsequently cleaned using RCA-1 and RCA-2 followed by diluted NH_4OH to eliminate organic, metallic contaminants, and oxide. A passivation-first process was conducted by performing *in-situ* NH_3 pretreatment, followed by a 60 nm SiN deposition with low-pressure chemical vapor deposition (LPCVD) [23].

The test structure is a transfer length method (TLM) structure with ohmic contact distance ranging from 5 to 30 μm and a contact width of 100 μm. Device isolation was achieved by mesa etching to a depth of ~120 nm below the 2DEG. The ohmic contact lithography was performed using a laser writer (Heidelberg Instruments DWL 2000). The development was performed with a developer spinner to ensure precise control and uniformity of the resist profile. The θ, which influences the 2DEG concentration and tunneling distance, is determined by the angle of the resist profile (controlled by the exposure dose, reversal baking temperature, and developing time). The

Table 1. Epi-structures used in this work.

	Epi I	Epi II
Cap layer	GaN, 1.4 nm	GaN, 2 nm
Barrier layer	$Al_{0.52}Ga_{0.48}N$, 3.3 nm	$Al_{0.3}Ga_{0.7}N$, 9.7 nm
Spacer layer	AlN, 1.5 nm	AlN, 1.2 nm
Channel layer	GaN, 260 nm	GaN, 255 nm
Nucleation layer	AlN, 60 nm	AlN, 60 nm
GaN RC <0 0 2>	94 arcsec	216 arcsec
GaN RC <1 0 2>	353 arcsec	443 arcsec
n_s [10^{13} cm^{-2}]	1.16	1.07
μ [cm^2 V^{-1} s]	1746	1966
R_{sh} [Ω/sq.]	316	298

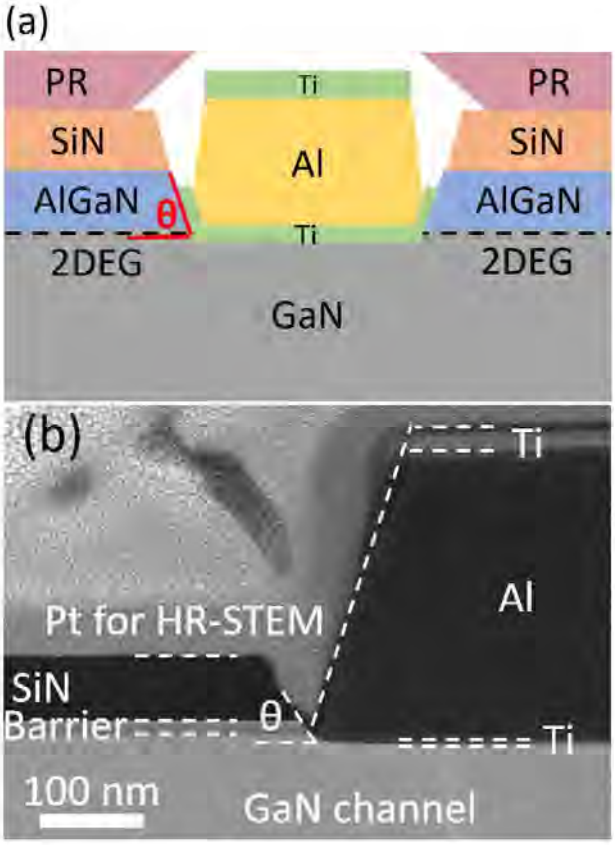

Figure 1. (a) Schematic of TLM structure. (b) HR-STEM cross-section of annealed TLM with 10° tilted t_{Ti} of 3 nm on Epi II.

image reversal photoresist (PR) (AZ5214E) was employed for ohmic lithography, producing an undercut suitable for the lift-off process [18, 24]. Following resist development, the SiN passivation in the ohmic region was etched with inductively coupled plasma reactive ion etching (ICP-RIE) using NF_3 gas with 50 sccm flow rate, 25 W forward power, 60 W ICP power, and chamber pressure of 5 mTorr. The ohmic recess was performed immediately without exposure to ambient air using Cl_2 gas with 40 sccm flow rate and Ar gas with 10 sccm flow rate, 25 W forward power, 25 W ICP power, and chamber pressure of 3 mTorr resulting in a recess depth of ~12 nm below the 2DEG. The samples were then dipped into diluted buffered HF and diluted HCl to remove the native oxide layer at the recessed sidewall. Subsequently, the Ti/Al/Ti metal stacks with a thickness of $t_{Ti}/t_{Al}/20$ nm were deposited by electron-beam evaporator, followed by the lift-off process. The ohmic recess and the metallization are realized with the same resist making the ohmic contact self-aligned to the recessed region. The first Ti layer was deposited with a 10° tilt and a low deposition rate of 0.05 Å sec^{-1} to ensure good sidewall coverage and better thickness control, while the other two layers were deposited without tilt (figure 1) [18]. All fabricated TLM structures were annealed repeatedly at 550 °C in a rapid thermal process system under N_2 ambient for 1 min and unloaded for measurement until the R_c was saturated [18].

The R_c was measured using the TLM structures with four point probe measurement method with a DC parameter analyzer system (Keithley 4200SCS). The average R_c with standard deviation were calculated from the measurements of four randomly selected TLM structures.

3. TLM results

The formation of ohmic contacts requires deposition of ohmic metal stacks (Ti and Al in this work) followed by annealing to extract N from (Al)GaN, yielding compounds such as TiN, AlN, and Al_xTi_yN. This process hence creates N-vacancies in the (Al)GaN, which act as donor-like dopants, resulting in a n-type region [8, 18]. However, this approach is highly dependent on the type of metal stacks. Therefore, optimizing the metal stacks to facilitate the creation of a high concentration of N-vacancies is of significant interest. Both t_{Ti} and t_{Al} play critical roles in this process and require separate investigations and optimization.

In the first experiment, samples with different t_{Ti} (5, 10, and 15 nm) were fabricated on Epi I with the identical t_{Al} of 280 nm and top Ti layer (20 nm). The θ of 55° was chosen based on our previous work [18]. As the t_{Ti} was deposited at a 10° tilt, the effective thicknesses on the recessed sidewall of this layer were ~3, ~7, and ~12 nm, respectively, as measured with scanning electron microscopy (SEM). Figure 2(a) shows the impact of t_{Ti} on R_c after annealing. The samples with t_{Ti} of 15 nm demonstrated the highest saturated R_c of ~0.6 Ω·mm. Reducing the t_{Ti} to 5 nm significantly decreased the R_c, yielding the lowest R_c of ~0.16 Ω·mm after a total annealing duration of 6 min. All samples with different t_{Ti} exhibited a lower R_{sh} (~304 Ω/sq.) compared to that on the unprocessed Epi I (R_{sh} = 316 Ω/sq.). A small difference in R_{sh} before and after processing could be attributed to the strain-induced polarization charge modification by the SiN passivation layer [25, 26].

In the second experiment, samples with different t_{Al} (280, 140, and 70 nm) were fabricated on Epi I with an identical t_{Ti} of 5 nm and a top Ti layer of 20 nm (figure 2(b)). Further increase of t_{Al} was not considered due to a large step height of the ohmic contacts, which potentially limits the downscaling of the gate-source distance and gate fabrication. The same θ was processed with the identical lithography parameters as in the first experiment. The sample with reduced t_{Al} shows an

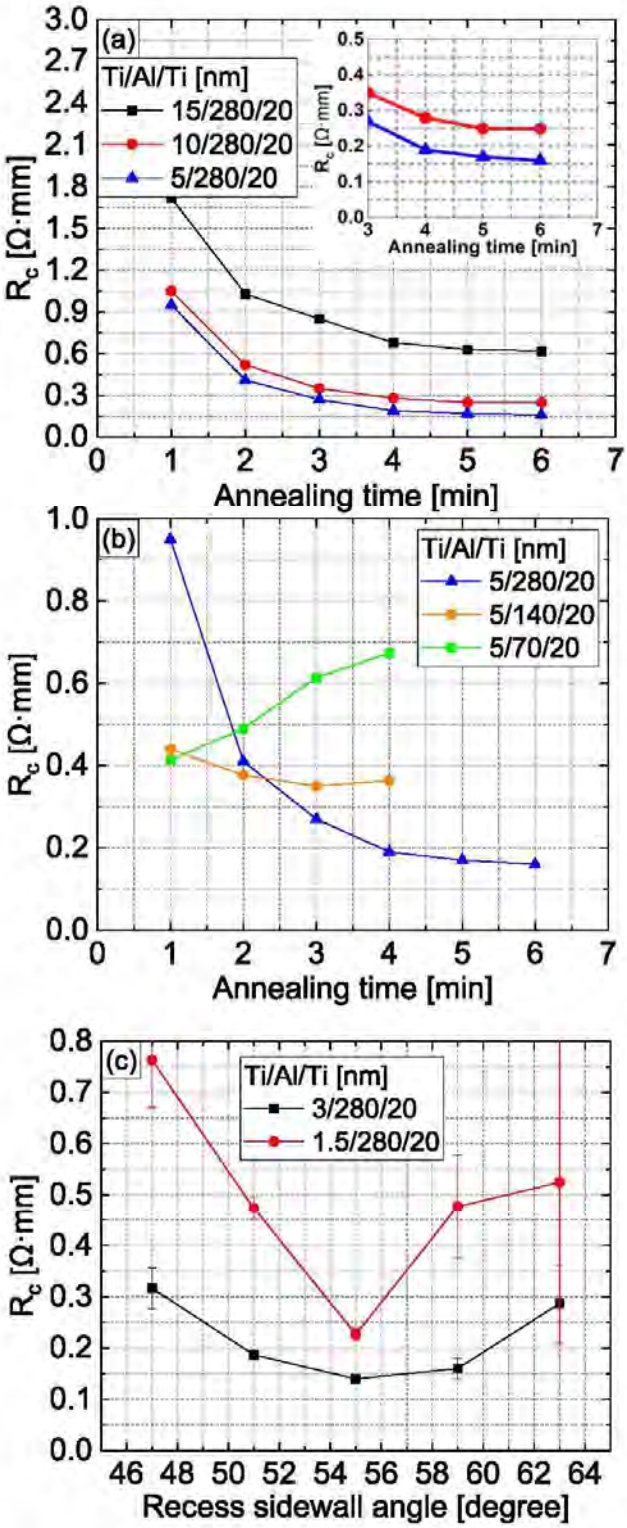

Figure 2. R_c versus total annealing duration on Epi I for (a) different t_{Ti} (5, 10, and 10 nm). The inset shows the zoom-in for the samples with t_{Ti} of 5 and 10 nm. (b) Different t_{Al} (70, 140, and 280 nm). (c) R_c versus θ with all the samples annealed until the R_c saturated. The accuracy of the measurement of θ with SEM is $\pm 2.5°$.

earlier saturation of R_c. Compared to the sample with a t_{Al} of 280 nm, the sample with a t_{Al} of 140 nm shows a saturated R_c after 3 min. Annealing beyond saturation time leads to a degradation of R_c. Moreover, the minimum R_c increases from 0.16 Ω·mm to 0.35 and 0.4 Ω·mm on samples with reduced t_{Al} of 140 and 70 nm, respectively. This phenomenon can be explained by the insufficient Al on the recessed sidewall due to metal deposition without tilting.

The 2DEG properties and tunneling distance at the contact/semiconductor interface are strongly influenced by the θ, which is controlled by the resist profile (figure 1(a)). Photoresist exposed with different doses, but with the same reverse baking temperature of 125 °C yields a θ from 47° to 63° after recess etching. A higher dose forms a steeper photoresist profile due to a smaller undercut dimension. A larger θ (steeper sidewall) tends to preserve 2DEG properties with a trade-off of longer tunneling distance, and vice versa for a smaller θ, due to the remaining thickness of AlGaN barrier after the dry etching process.

The impact of θ on R_c is investigated on Epi I (figure 2(c)). According to the t_{Ti} investigation above, a small t_{Ti} results in a lower R_c. In the investigation of the impact of θ, the t_{Ti} of 3 and 1.5 nm is deposited with 10° tilt, followed by the untilted deposition of t_{Al} of 280 nm and top Ti layer of 20 nm. The samples were then annealed with the same procedure until R_c saturated. The lowest R_c of 0.14 Ω·mm was measured with excellent uniformity on the samples with t_{Ti} of 3 nm and θ of ~55°. For θ ranging from 50° to 60°, an R_c below 0.25 Ω·mm with high uniformity is shown, indicating a wide process window. Outside this θ-range, the degradation of R_c and the uniformity are probably due to non-optimum metal coverage on the recessed sidewall and lower electron density or longer tunneling distance. The samples with a t_{Ti} of 1.5 nm exhibit a higher R_c, a smaller θ process window, and a larger error bar, likely due to difficulties in controlling the t_{Ti} thickness and uniformity.

These ohmic contacts were further evaluated on epistructure with different barrier designs. Based on the results above, two samples with the tilted t_{Ti} of 3 and 15 nm (denoted as T_3 and T_{15}, respectively) and the un-tilted t_{Al} of 280 nm followed by 20 nm top Ti layer were deposited on Epi II with identical exposure dose and a recess etching depth of ~12 nm below the 2DEG. The main difference between Epi I and Epi II is the Al concentration and thickness of the AlGaN barrier. A low R_c of 0.15 Ω·mm with an R_{sh} of 280 Ω/sq. was measured on T_3 (figure 3), while the T_{15} yields a higher R_c of 0.56 Ω·mm with an R_{sh} of 282 Ω/sq. A similar trend as for Epi I of R_c versus t_{Ti} was found for Epi II. This result indicates that this ohmic contact method can be applied for different barrier designs.

4. TLM structural investigation

To get further insight into the contact formation mechanism, structural and elemental analyses on T_3 and T_{15} fabricated on Epi II were performed. The specimens for STEM were

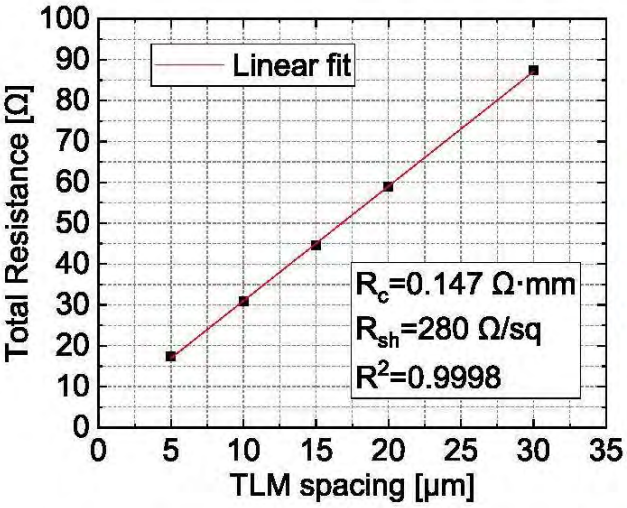

Figure 3. Linear fitting of the total resistance vs. TLM spacing on T_3. R^2 is the correlation coefficient of linear fitting.

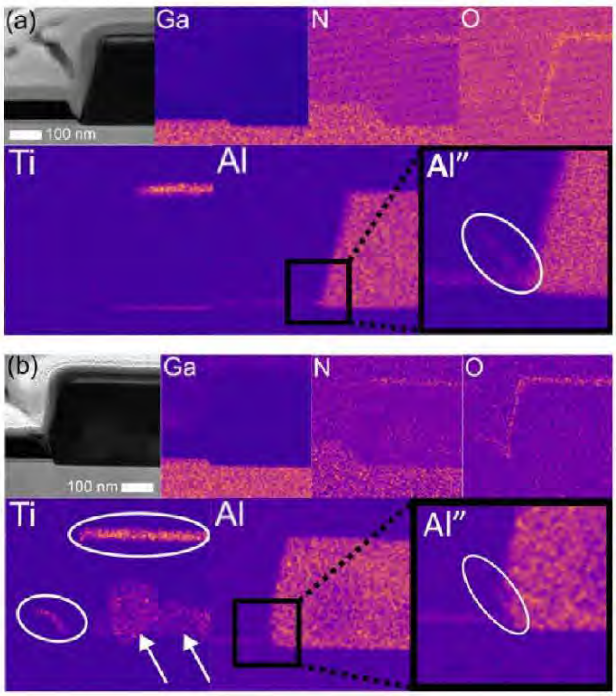

Figure 4. HAADF-STEM images and EDS elemental maps from (a) T_3 and (b) T_{15}.

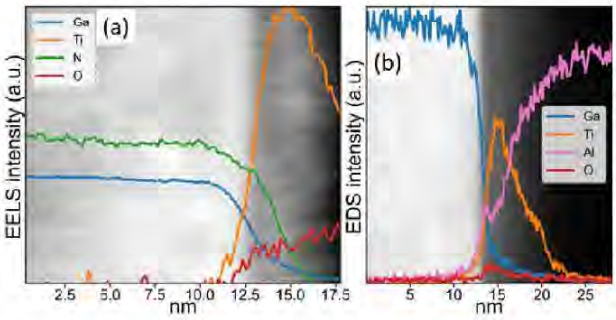

Figure 5. Elemental profile of the T_3 measured with (a) EELS, and (b) EDS.

prepared by focused ion beam (Carl Zeiss crossbeam 1540 ESB) using lift-out and thinning in cross-section view using Pt deposition and Ga-ions (30 keV, 50 pA to 2 nA) to achieve electron transparency.

The interface between ohmic contacts and epi-structure was characterized by high-angle annular dark-field (HAADF)-STEM in combination with EELS (using a GIF Quantum ERS spectrometer) and EDS (Super-X/Quantax, Bruker), using a double corrected STEM (Titan3 60–300), operated at 300 kV. The embedded energy filter was employed in dual EELS mode with a dispersion of 0.1–0.5 eV/channel, a dwell time of 0.02–0.05 sec, with convergence and collection angles of 22.0 and 56.5 mrad, respectively. Elemental distribution mapping was conducted using HyperSpy for Python [27].

The annealed TLM structure was analyzed by HAADF-STEM, where different materials and their interfaces could be distinguished using image intensity differences due to mass contrasts (figures 4(a) and (b)). Analysis of T_3 and T_{15} showed only a difference in the bottom Ti layer. The diffusion of the bottom Ti layer into the middle Al layer, or vice versa, was observed in T_{15} and is indicated in figure 4(b-Ti) with white arrows.

EDS elemental maps of the ohmic contacts and epi-structure, including elements Ga, Al, N, O, and Ti are shown in figures 4(a) and (b). Al is identified in the metal stacks of the ohmic contacts and the barrier layers for both samples. Surprisingly, a tail of Al (marked in white oval in figures 4(4-Al″) and (b-Al″)) was found on the sidewall of SiN for both samples, indicating a possible diffusion below the Al melting point. Moreover, no sign of AlGaN barrier decomposition was found due to homogenous contrast color. Since the energy of N (0.392 keV) and Ti (0.452 keV) in the EDS spectrum are difficult to distinguish, further interface analysis by EELS was performed. The EELS and EDS profiles are shown in figures 5(a) and (b), respectively. Due to the 10° tilting deposition of the bottom Ti layer, a Ti signal is revealed on the sidewall of SiN. The T_3 with the out-diffusion span of only ~8 nm allows both Ti and Al incorporation for N-extraction, yielding a lower R_c of 0.15 Ω·mm, which is mainly due to the formation of a lower work function Ti-Al-N alloy. Unlike T_3, Ti signal in the T_{15} out-diffused 100–200 nm away from the sidewall contact region and mixed with the Al layer (figure 4(b-Ti)), resulting in a higher R_c of 0.56 Ω·mm. This is probably due to that only large bandgap Al-N alloy has formed at the sidewall contact region and insufficient amount of Ti which can act as a catalyst to enhance the N-extraction by Al [14]. Surprisingly, there is no apparent reaction of Al with the 'Ti on SiN' and 'top Ti layer' (marked by a white oval in figure 4(b-Ti)).

EELS and EDS measurements were also performed at the interface between the epi-structure and the ohmic contacts on T_3. Due to the edge onsets of N (402 eV) and Al (1560 eV),

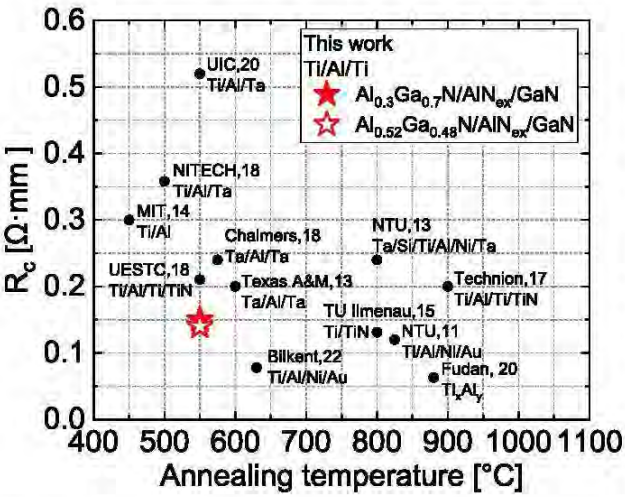

Figure 6. Benchmark of R_c versus annealing temperature on $Al_xGa_{1-x}N/GaN$ ($x > 0.22$) HEMT epi-structures [14, 15, 17, 18, 28–34].

both elements cannot be simultaneously included in the EELS measurement (figure 5(a)). Instead, EDS was used to complement the measurement (figure 5(b)). The Ga and N appear to be mixed with Ti with a tail of ~5 nm. The Al appears to have diffused into the Ti and GaN. The annealed Ti exhibits an out-diffusion of ~10 nm span, which is consistent with the EDS map in figure 4(a-Ti). These results may explain the low R_c on T_3 due to possible formation of N-vacancies and low work function Ti-Al-N alloy at the interface between the epi-structure and ohmic contacts [8, 18]. The native oxide layer observed at the interface probably originates from the sample transfer before ohmic metal deposition.

In figure 6, this work is benchmarked to other ohmic contacts concepts. Compared to Ta-based ohmic contacts, Ti-based contacts potentially provide a lower R_c and these works prompt an excellent ohmic contacts process scheme for both high-frequency and high-power applications.

5. Conclusion

High uniformity low contact resistance Ti/Al/Ti deeply recessed sidewall ohmic contacts for AlGaN/GaN HEMTs were demonstrated. This approach provides a large process window without the requirement of precise control of the recessed etching depth. The thickness of the bottom Ti and Al layers was investigated, indicating a critical impact on R_c, and the optimal θ was found through optimization. Degraded R_c and uniformity were found when the θ is beyond the desired process window. The lowest contact resistance of 0.14–0.15 Ω·mm with high uniformity combined with a low annealing temperature of 550 °C was measured on Al concentration of 30% and 52% AlGaN/GaN HEMTs with t_{Ti} of 3 nm. Further reducing of R_c can be foreseen with a slightly higher annealing temperature (lower than the Al melting point).

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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Paper B

A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs

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A versatile low-resistance ohmic contact process with ohmic recess and low-temperature annealing for GaN HEMTs

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Abstract

Deeply recessed ohmic contacts for GaN-based high electron mobility transistors (HEMTs) are demonstrated. It is shown that low-resistance ohmic contacts can be achieved with recessing beyond the AlGaN Schottky barrier where the ohmic contacts are formed on the sidewall of the recess. This makes the process versatile and relatively insensitive to the exact recess depth. The ohmic contact is based on a gold-free metallization scheme consisting of a Ta/Al/Ta metal stack requiring a low-temperature annealing. Important parameters for this type of ohmic contact process include the metal coverage, slope of the etched sidewall, bottom Ta-layer thickness, as well as annealing temperature and duration. The optimized contact resistance is as low as 0.24 Ω mm after annealing at 575 °C. Moreover, this sidewall contact approach was successfully implemented on different epitaxial heterostructures with different AlGaN barrier thickness as well as with and without AlN exclusion layer. All the samples exhibited excellent contact resistances in a wide range of recess depths. The Ta-based, sidewall ohmic contact process is a promising method for forming an ohmic contact on a wide range of GaN HEMT epitaxial designs.

Keywords: GaN, HEMT, ohmic recess, sidewall contact, gold-free, contact resistance

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN-based high electron mobility transistor (HEMT) is a promising candidate for high-frequency and high-power applications due to its outstanding material properties, such as high electric breakdown field and high peak electron drift velocity [1–3]. A low contact resistance (R_c) is essential for the device performance including output power, high efficiency, high-frequency and noise performances.

To obtain low ohmic contact resistances, several studies using different metallization schemes have been reported [4–8]. A standard Ti/Al/Ni/Au metal stack is conventionally evaporated for ohmic contacts of GaN HEMTs [9, 10]. However, the Ti-based metal stack generally requires a high annealing temperature (above 800 °C) to form ohmic contacts. Annealing at such a high temperature sometimes results

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Table 1. Epitaxial heterostructures used in this paper.

	Epi I	Epi II	Epi III
Cap layer	—	—	GaN, 2 nm
Barrier layer	$Al_{0.25}Ga_{0.75}N$, 20 nm	$Al_{0.25}Ga_{0.75}N$, 19 nm	$Al_{0.30}Ga_{0.70}N$, 11 nm
Spacer layer	—	AlN, 1 nm	AlN, 1 nm
Buffer layer	C-doped GaN	C-doped GaN	Fe-doped GaN

in thermal degradation of the epitaxial heterostructure, where the sheet resistance increases after annealing at temperatures close to the epitaxial growth temperature [11, 12]. The Ti-based ohmic contacts commonly have a rough surface morphology and reduced edge acuity that affect accurate alignment of the gate electrode for downscaled GaN-based HEMTs. To alleviate these phenomena, a Ta/Al/Ta metal stack with relatively smooth surface and low contact resistances has been developed [13, 14]. This alternative metallization scheme has achieved low contact resistances with the annealing temperature lower than 600 °C. Ta-based ohmic contacts have excellent stability in terms of intermetallic reactivity and surface morphology due to the high melting point and high atomic number of Ta [15].

Ohmic contacts rely on carrier tunneling through the barrier layer of the heterostructure. Therefore, several research groups have recently improved the contact resistance using ohmic recess technique [16–20]. Bergsten *et al* reported that a low R_c of 0.27 Ω mm can be obtained by recess etching prior to metallization with an almost removed AlGaN barrier layer [19]. Wang *et al* demonstrated a very low R_c of 0.26 Ω mm with a completely removed AlGaN barrier layer making a direct contact between the TiN and two-dimensional electron gas (2DEG) channel [20]. Nevertheless, precise control of ohmic recess depth is needed since high contact resistances have previously been shown for deeper ohmic recess etching [16, 17, 20]. Although excellent ohmic contacts can be achieved by ohmic regrowth [4, 5], a deep ohmic recess technique is more attractive because of its compatibility with standard GaN HEMT processes.

In order to avoid the requirement of exact control of the recess depth, an ohmic recess beyond the 2DEG channel with low contact resistance is desirable. However, the optimal process parameters have previously not been established. In this paper, we investigated the influence of various process parameters on ohmic contacts including the ohmic metal coverage, slope of the etched sidewall, bottom Ta-layer thickness, etching depth, as well as annealing temperature and duration. Section 2 describes the epitaxial heterostructures and fabrication of test structures. Results and discussion are presented in section 3. Conclusions are drawn in section 4.

2. Fabrication

2.1. Epitaxial heterostructures

The AlGaN/GaN epitaxial heterostructures (Epi I, Epi II, and Epi III) were grown by metal-organic chemical vapor deposition on SiC substrates as shown in table 1. Epis I and II were grown by SweGaN AB and Epi III was grown by Cree Inc. Epi I consisted of a 50 nm AlN nucleation layer, a 1.3 μm carbon-doped GaN buffer layer, a 200 nm i-GaN layer, and a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The structure exhibited a sheet carrier density of 9.10×10^{12} cm^{-2}, an electron mobility of 2266 cm^2 V^{-1} s^{-1} and a sheet resistance of 306 ohm sq^{-1}, respectively. The high electron mobility of Epi I was due to the AlGaN/GaN interface sharpening achieved by using an optimized interface growth process with a low flow rate of trimethylaluminum prior to the AlGaN growth. Details of the interface sharpening have been presented elsewhere [19, 21]. Epi II featured an AlN spacer layer compared to Epi I with the same barrier layer thickness. This material exhibited a 2DEG mobility of 1948 cm^2 V^{-1} s^{-1} and a sheet carrier density of 1.10×10^{13} cm^{-2} resulting in a sheet resistance of 305 ohm sq^{-1}. Epi III featured an iron-doped GaN buffer layer with a thinner barrier layer (11 nm) and an AlN spacer layer. The sheet carrier density, electron mobility and sheet resistance of Epi III were measured to be 1.15×10^{13} cm^{-2}, 1820 cm^2 V^{-1} s^{-1}, and 299 ohm sq^{-1}, respectively.

2.2. Transfer length method (TLM) structure

All the samples used to optimize the ohmic contact process were diced from the same epitaxial wafer (Epi I). The wafer was diced into squares of 15 × 15 mm^2. The process started with a standard RCA clean, where the samples were cleaned in NH_4OH:H_2O_2:H_2O (1:1:5) and HCl:H_2O_2:H_2O (1:1:5) to remove organic and metallic contaminants, respectively. A 70 nm SiN_x passivation layer was deposited by low-pressure chemical vapor deposition. The SiN_x layer was deposited at 820 °C with a dichlorosilane (DSC) flow of 224 sccm, an ammonia (NH_3) flow of 23 sccm, and a pressure of 250 mTorr. This SiN_x have previously been shown to be an excellent surface passivation for GaN HEMTs [22].

Mesa isolation and ohmic contact lithography were defined with a laser writer (Heidelberg Instruments DWL 2000), which enables better control of the photoresist profile compared to contact lithography. The 100% exposure intensity of laser writer represents the dose of 107 mJ cm^{-2} on the substrate. A spin developer was used for increased repeatability and uniformity of the resist profile. The mesas were formed by dry etching, while the ohmic contacts were formed with evaporation and lift-off. Since the ohmic contact is formed at the sidewall between the 2DEG channel and ohmic metal, the sidewall angle at 2DEG is an important factor for

ohmic contact. Therefore, the AZ5214 photoresist profile for ohmic lithography was investigated. AZ5214 is a positive photoresist originally, which is changed to negative photoresist after reversal bake for lift-off purpose [23]. Accordingly, reversal baking temperatures and intensity-dependent experiments by laser writer were investigated. The photoresist was not possible to be fully developed for exposure intensities lower than 80%. After ohmic contact lithography, we had measured the pad distances and widths of the TLM structures by optical microscope. The pad distances and widths were the same for the samples with different baking temperatures and exposure intensities.

Silicon nitride film in the ohmic region was etched with inductively coupled plasma reactive ion etching (ICP-RIE) using NF_3 gas with 5 sccm flow rate, Ar gas with 50 sccm flow rate, 30 W RIE power, and pressure of 2.5 mTorr. After removal of the SiN_x film, the ohmic recess was performed by the same ICP-RIE immediately without exposure to air. The ohmic recess was performed using Cl_2 gas with the following parameters: 50 sccm flow rate, 15 W RIE power and 10.7 mTorr chamber pressure, yielding an etching rate of $\sim$0.25 nm s^{-1}. After ohmic recess etching, an oxygen descum process was used to remove etching residues. Then, the samples were etched in HF:H_2O (1:10) and HCl:H_2O (1:10) for 4 min and 1 min, respectively. A Ta (t_{Ta1})/Al (280 nm)/Ta (20 nm) metal stack was evaporated for ohmic contact using the same photoresist mask as for the recess etch, which means that the ohmic metals were self-aligned to the recess trenches. The top 20 nm Ta layer was utilized to prevent Al oxidation.

Finally, the samples were diced into smaller pieces; one group of the pieces were annealed, and while other pieces were used for scanning electron microscopy (SEM) analysis (Zeiss Supra 60 VP). A Ti/Au conducting layer was evaporated to prevent charge build-up to obtain a better quality and resolution of the images. Contact resistances were measured using the TLM structures by a DC parameter analyzer system. The average contact resistance was calculated from the measurements of three different TLM structures and is presented in the following figures. The TLM structures showed slight variations in contact resistances (<0.04 Ω mm).

In the first investigation, the purpose was to study the impact of sidewall metal coverage on the ohmic resistance. Samples were fabricated with and without tilted Ta-evaporation. Temperature-dependent annealing experiments were performed for the samples. Secondly, the sidewall angle at 2DEG channel was investigated by using different exposure intensities and reversal baking temperatures from which an optimum sidewall angle range could be deduced. Thirdly, the thickness of the bottom Ta-layer thickness (t_{Ta1}) was investigated. Time- and temperature-dependent annealing experiments were carried out and analyzed. Thereafter, the annealing temperature and duration were optimized. Finally, this sidewall contact approach was performed on different epitaxial heterostructures using the optimum parameters from these experiments.

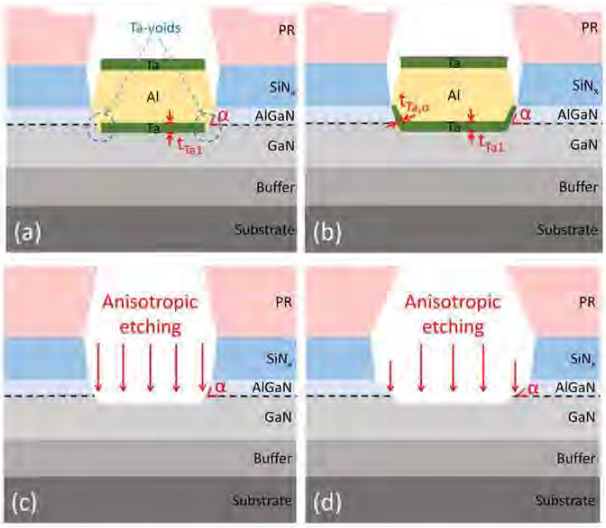

Figure 1. Schematic cross sections of samples (a) without tilted Ta-evaporation, (b) with tilted Ta-evaporation, (c) with steep sidewall of photoresist and (d) with gentle sidewall of photoresist.

3. Results

3.1. Impact of metal coverage

First, the impact of metal coverage on the 2DEG channel was studied. A major problem of the ohmic recess beyond the 2DEG channel is the void between 2DEG and ohmic metal due to the bad metal coverage resulting from e-beam evaporation as shown in figure 1(a). In order to study the metal coverage on the sidewall, the bottom Ta layer was evaporated with tilt angles of 0° and 10° (figures 1(a), (b)). Both of the samples were fabricated with a reversal bake at 120 °C and exposure intensity of 120%. SEM images of samples before annealing with and without tilted Ta-evaporation were taken by SEM (figure 2). In figure 2(a), there was no coverage on the sidewall for a tilt angle of 0°. The Ta-void was filled with Al due to the relatively thick Al layer. However, the sidewall is clearly covered with the bottom Ta layer after evaporation with a tilt angle of 10° as shown in figure 2(b). The recess depth was approximately 30 nm as measured from the SEM images. The tilted evaporation at this small angle did not cause any lift-off problems.

Figure 3 shows the contact resistance dependence on the evaporation angle and annealing temperature. Samples were fabricated using different reversal baking temperatures (120 °C, 125 °C, and 130 °C), which will change the photoresist profile for a given exposure dose. The samples were annealed for 4 min in N_2 ambient at increasing temperatures from 500 °C to 625 °C. The exposure intensity of laser writer was 120%. The contact resistances of the samples with tilt were apparently better than those without tilt resulting in a minimum ohmic resistance of 0.30 Ω mm. The samples baked at 130 °C without tilt never became ohmic due to bad coverage of the first Ta-layer on the sidewall. In general, the contact resistances increased after annealing at and above 600 °C. The sheet resistances of the samples after annealing at

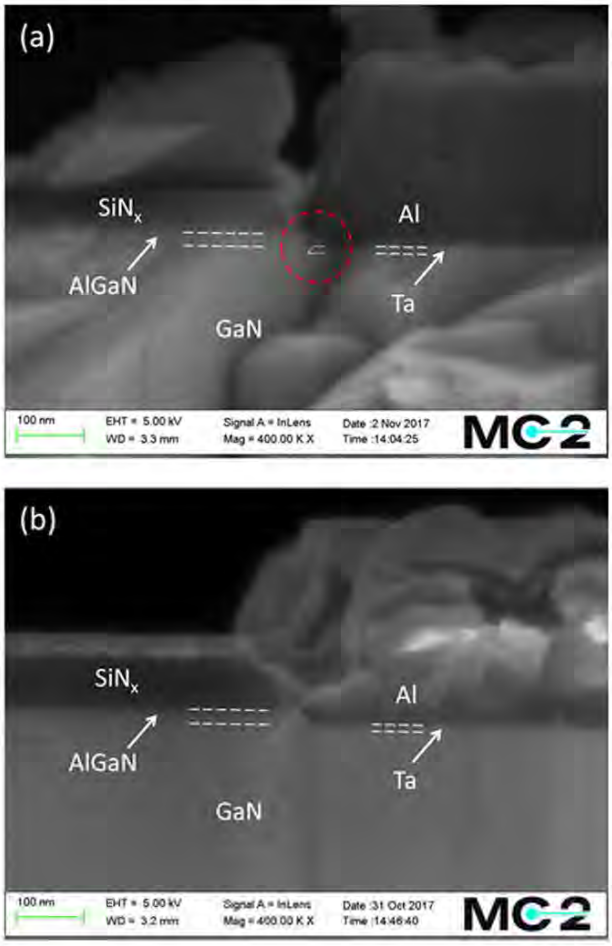

Figure 2. SEM images before annealing of (a) a sample without tilt and (b) a sample with tilt angle of 10° during evaporation process. Both of the samples were fabricated with bottom Ta-layer thickness of 10 nm, reversal bake at 120 °C and exposure intensity of 120%.

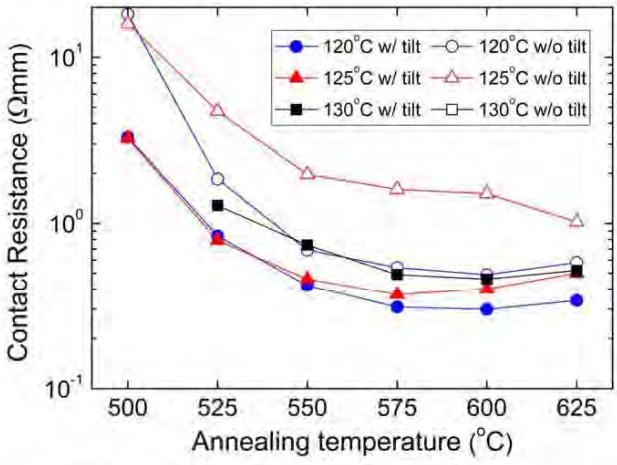

Figure 3. Contact resistance dependence on evaporation angle and annealing temperature with bottom Ta-layer thickness of 10 nm evaporated with or without tilt and for three different reversal baking temperatures (120 °C, 125 °C, and 130 °C). The samples were annealed for 4 min at each temperature. The exposure intensity of laser writer was 120%.

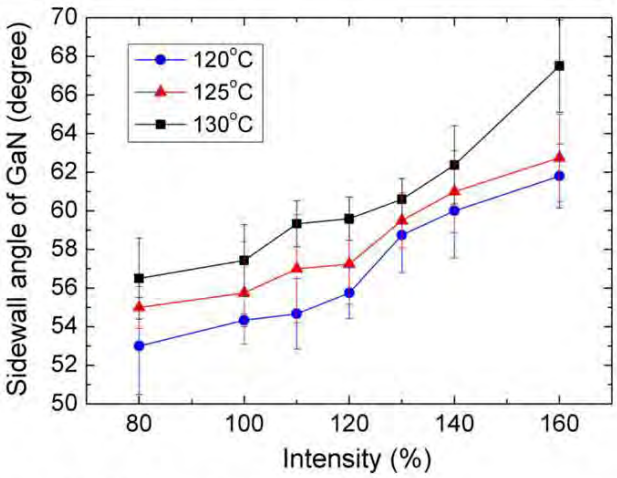

Figure 4. Sidewall angles of GaN after ohmic recess etching as a function of exposure intensity of laser writer for three different reversal baking temperatures (120 °C, 125 °C, and 130 °C) under the lithography process.

625 °C increased by 0.6% on average in comparison with those after annealing at 575 °C. Therefore, the optimal annealing temperature was around 575 °C where the ohmic contact was efficiently formed.

3.2. Impact of sidewall angle

To optimize the sidewall angle (α) at the 2DEG channel as shown in figure 1, samples with different exposure intensities of laser writer from 80% to 160% and reversal baking temperatures (120 °C, 125 °C, and 130 °C) were investigated. In figure 4, the sidewall angles were measured from SEM images for different combinations of exposure intensities and reversal baking temperatures. The error bars shown in figure 4 represent the spread of the sidewall angles. The sidewall angle at the 2DEG channel increased with increasing reversal baking temperature and exposure intensity of the lithography process. The profile of the photoresist played a key role in determining the angle of the sidewall. The steeper sidewall of photoresist resulted in larger sidewall angle at the channel due to the weaker shadowing effect of the photoresist, which means that the anisotropic ion bombardment was enhanced during recess etching as shown in figures 1(c) and (d).

The impact of exposure intensity (and resulting sidewall angle) and different reversal baking temperatures on contact resistance is shown in figure 5. Based on the results above (section 3.1), the bottom Ta layer was evaporated with a tilt angle of 10° for all the samples. All the samples were annealed for 4 min at each temperature (500 °C + 525 °C + 550 °C + 575 °C). The contact resistances of the samples baked at 125 °C or 130 °C increased monotonously with increasing exposure intensity. The lowest contact resistance of 0.28 Ω mm in figure 5 was obtained with a combination of 125 °C reversal bake and 80% exposure intensity. The samples with reversal baking temperatures of 120 °C had a lowest contact resistance of 0.31 Ω mm with intensity of 120%. According to inset in figure 5, the sidewall angles for the

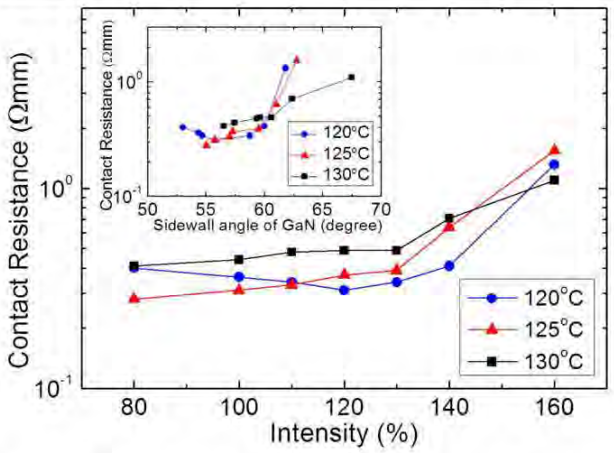

Figure 5. Contact resistance plotted versus exposure intensity of laser writer for three different reversal baking temperatures (120 °C, 125 °C, and 130 °C). The bottom Ta layer was evaporated with a tilt angle of 10° for ohmic contact for all the samples. All the samples were annealed for 4 min at each step (500 °C + 525 °C + 550 °C + 575 °C). The inset shows the contact resistance dependence on sidewall angle at 2DEG channel.

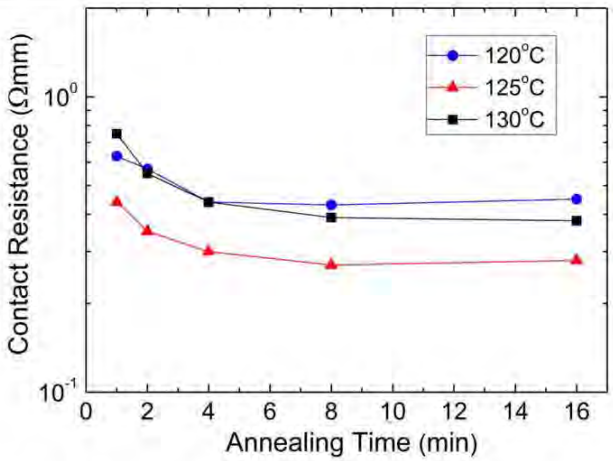

Figure 6. Contact resistance as a function of annealing time at 575 °C for three different reversal baking temperatures (120 °C, 125 °C, and 130 °C) with exposure intensity of 80%.

lowest contact resistances of samples with an anneal temperature of 120 °C or 125 °C were around 55°. The contact resistances remained below 0.40 Ω mm for sidewall angles in the range of 54°–60°. The increasing ohmic resistance for gentler slopes (smaller α) is the increasing length of depleted GaN due to the lack of AlGaN above, which prevents the formation of a 2DEG [24]. For the samples with steeper sidewalls (larger α), the sidewall contact leads to a smaller contact area that increases the contact resistance [18]. Based on these results, the remaining part of this paper mainly focuses on the samples with reversal baking temperatures of 125 °C and exposure intensity of 80% (yielding a sidewall slope angle of 55°).

Figure 6 shows the contact resistance dependence on annealing time at an annealing temperature of 575 °C with exposure intensity of 80% for different reversal baking temperatures. The contact resistances using reversal baking temperature of 125 °C were lowest for all the annealing durations. The lowest value of 0.27 Ω mm was obtained using an annealing time of 8 min. The contact resistances saturated at approximately 0.3 Ω mm after annealing time of 8 min at 575 °C.

3.3. Impact of metallization

The formation of metal-nitrogen compounds such as TaN and AlN at the metal-semiconductor interface results in the creation of nitrogen vacancies which act as donors in (Al)GaN-layers [13, 18, 25]. The exact thickness of the first Ta-layer is expected to play a major role in the resulting ohmic resistance. Therefore, samples with different bottom Ta-layer thicknesses were fabricated with the same thicknesses of Al layer (280 nm) and top Ta layer (20 nm). The thickness of bottom Ta layer was varied from 5 to 30 nm. SEM images of the samples evaporated with tilt and different bottom Ta-layer thicknesses before annealing are shown in figure 7. The sidewalls of 2DEG channel were covered with Ta with varied thicknesses. The Ta-layer thicknesses on sidewall at the 2DEG channel ($t_{Ta,\alpha}$) were 3, 7, 16, and 26 nm for the samples evaporated with the evaporated thicknesses (t_{Ta1}) of 5, 10, 20, and 30 nm, respectively. The influence of bottom Ta-layer thickness on contact resistance after annealing is shown in figure 8. For the samples with 5 nm Ta layer, the contact resistances were higher than 3 Ω mm no matter what annealing temperature or duration. It indicates that the amount of formation of TaN was not enough to yield a heavily-doped interface for ohmic contact [10, 13]. In the case of 10 nm Ta-layer thickness, a lowest contact resistance of 0.27 Ω mm was measured after annealing at 575 °C for 8 min and increased slightly for longer annealing durations. It was found that longer annealing time was needed for thicker bottom Ta-layer thickness. The lowest contact resistances were measured for evaporated Ta-layer thicknesses (t_{Ta1}) of 10 and 20 nm resulting in a thickness on the sidewall at the 2DEG channel ($t_{Ta,\alpha}$) of 7 and 16 nm, respectively, which was consistent with the optimum Ta-layer thickness in the literature [13, 18]. The best contact resistance of 0.24 Ω mm was achieved for the samples annealed at 575 °C for 26 min with 20 nm bottom Ta-layer thickness. The sheet resistance was not affected at 575 °C during the time-dependent annealing experiment. At a higher annealing temperature of 600 °C, the contact resistances of the samples with Ta of 20 nm or 30 nm were lower than those annealed at 575 °C and a duration of 8 min. The contact and sheet resistances increased after annealing at a higher annealing temperature of 600 °C for 16 min or more. This phenomenon has previously been observed in other Ta-based ohmic contacts in the literature [13, 18].

Samples with very deep ohmic recess of 45 nm beyond 2DEG channel were also fabricated. The samples were evaporated with a bottom Ta-layer thickness of 20 nm. A contact resistance of 0.33 Ω mm was measured after annealing at

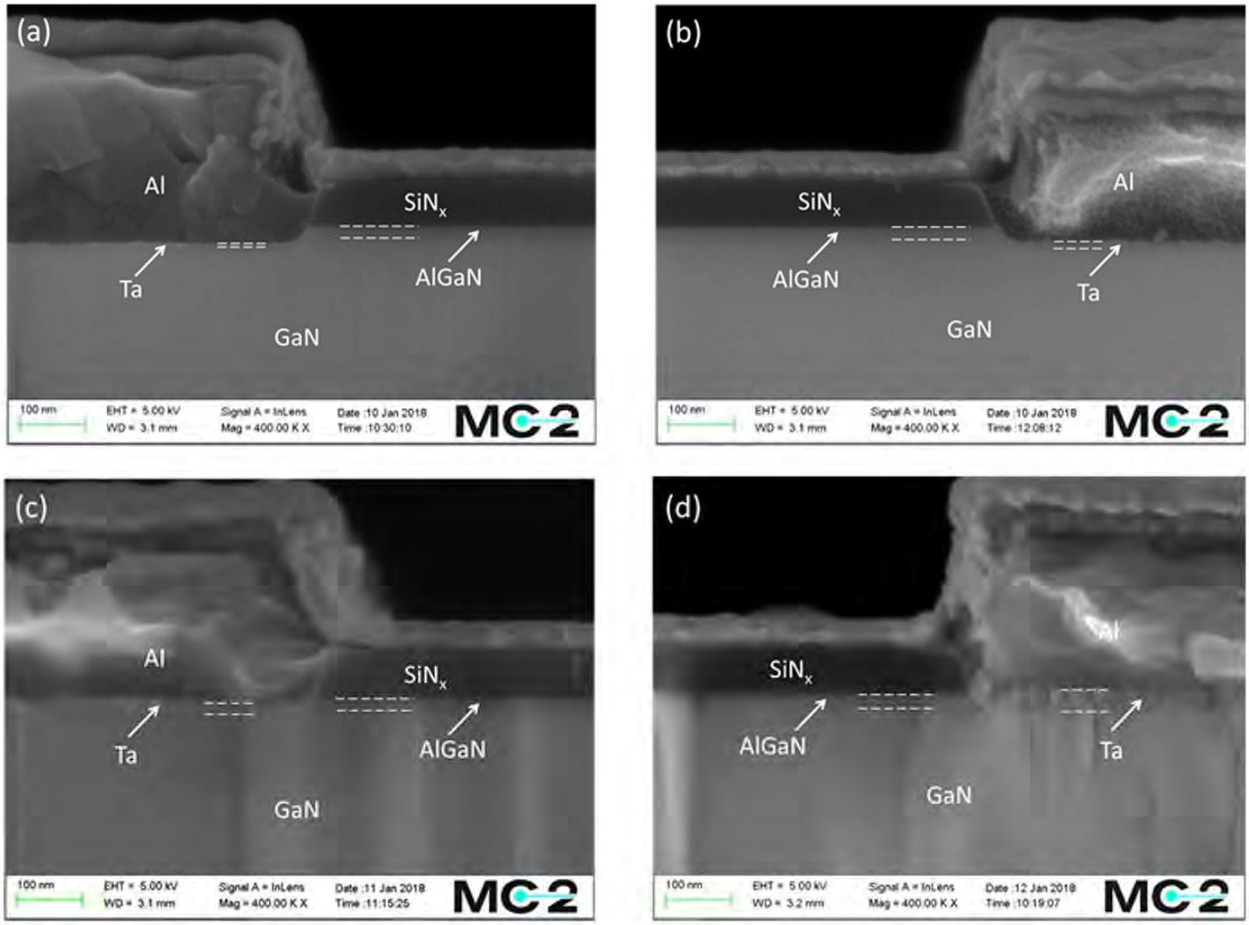

Figure 7. SEM images of the samples evaporated with a tilt angle of 10° with the bottom Ta-layer thickness of (a) 5 nm, (b) 10 nm, (c) 20 nm and (d) 30 nm before annealing. All the samples were fabricated with reversal bake at 125 °C and exposure intensity of 80%. The sidewall angles at 2DEG channel for the samples were around 55°.

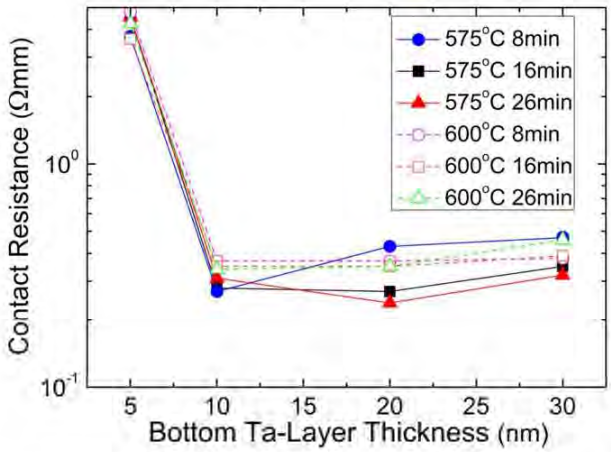

Figure 8. Contact resistance as a function of bottom Ta-layer thickness, annealed at 575 °C or 600 °C. The bottom Ta-layer was evaporated with tilt. All the samples were fabricated with reversal bake at 125 °C and exposure intensity of 80%. The sidewall angles at 2DEG channel for the samples were around 55°.

575 °C for 26 min. The higher contact resistance may be explained by an increased level of plasma-induced defects, such as ion bombardment and ultraviolet photons during the longer dry etching process [26–28]. A longer annealing time was performed to recover the plasma damage. After this, the contact resistances improved from 0.33 to 0.29 Ω mm after annealing at 575 °C for 34 min.

3.4. Impact of different epitaxial designs

The contact approach was further evaluated using different epitaxial heterostructures (Epi II and Epi III) with the following optimum ohmic contact process parameters: a bottom Ta-layer thickness of 20 nm evaporated with a tilt angle of 10°, an annealing temperature of 575 °C, and an annealing time of 26 min. The contact resistances are shown in table 2. Note that these results were achieved at the first attempt using the optimized process developed above. The difference between Epi I and Epi II was the AlN spacer layer with the same total barrier layer thickness ($t_{barrier}$). An AlN spacer

Table 2. List of the TLM results of different epitaxial structures after annealing at 575 °C for 26 min.

Epitaxial structure	Etching depth (nm)	Contact resistance (Ω mm)
I	$t_{barrier}$ + 10	0.24
	$t_{barrier}$ + 25	0.33
II	$t_{barrier}$ + 10	0.21
	$t_{barrier}$ + 20	0.36
III	$t_{barrier}$ + 10	0.25
	$t_{barrier}$ + 15	0.25

layer is known to complicate ohmic contact formation. The contact resistances of Epi I and Epi II with a recess depth of $t_{barrier}$ + 10 nm were 0.24 Ω mm and 0.21 Ω mm, respectively. Epi III featured an iron-doped GaN buffer layer, an AlN spacer layer, and a thinner barrier layer with a larger Al content compared to Epi I. For a recess depth of $t_{barrier}$ + 10 nm, all the epitaxial heterostructures provided contact resistances lower than 0.25 Ω mm. A slight increase in contact resistance was observed for the samples with etching depth larger than $t_{barrier}$ + 20 nm. This phenomenon was possibly related to more amount of plasma-induced defects during the longer etching process as discussed above. Overall, all the samples exhibited very good contact resistances with different etching depths. It indicates a wide process window for a good ohmic contact formed by the sidewall contact with the 2DEG channel.

4. Conclusion

Low-resistance ohmic contacts formed by sidewall contacts with ohmic recess for GaN HEMTs were demonstrated. A gold-free Ta-based metal stack was utilized for ohmic contact. To develop a general and viable method for low contact resistances without the need of exact control of the recess depth, an ohmic recess beyond the 2DEG channel was investigated. The impact of tilt during evaporation to provide better ohmic metal coverage on the 2DEG was discussed. A tilt angle of 10° resulted in better metal coverage as well as better and more uniform ohmic contact resistance. The thickness of the bottom Ta-layer was demonstrated to have a crucial impact on the ohmic resistance, where a thickness of 10–20 nm provided the best result. The influence of the sidewall angle at 2DEG channel on the contact resistance was also studied. The sidewall angle can be controlled by reversal baking temperature or exposure intensity of the process. A steeper sidewall of the developed photoresist is transferred to a larger sidewall angle of the recess at the channel. The lowest contact resistances were as low as 0.24 Ω mm after annealing at low temperature of 575 °C with a bottom Ta-layer thickness of 20 nm.

Finally, the proposed ohmic contact method was applied on different epitaxial heterostructures with different Schottky barrier thickness as well as with and without AlN spacer layer. All the samples exhibited excellent contact resistances, demonstrating the wide process window for low contact resistances using sidewall contacts. These results attest the great potential of sidewall contacts for high-frequency applications.

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Paper C

Impact of *In Situ* NH_3 Pre-treatment of LPCVD SiN Passivation on GaN HEMT Performance

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Impact of *in situ* NH_3 pre-treatment of LPCVD SiN passivation on GaN HEMT performance

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Abstract

The impact on the performance of GaN high electron mobility transistors (HEMTs) of *in situ* ammonia (NH_3) pre-treatment prior to the deposition of silicon nitride (SiN) passivation with low-pressure chemical vapor deposition (LPCVD) is investigated. Three different NH_3 pre-treatment durations (0, 3, and 10 min) were compared in terms of interface properties and device performance. A reduction of oxygen (O) at the interface between SiN and epi-structure is detected by scanning transmission electron microscopy (STEM)-electron energy loss spectroscopy (EELS) measurements in the sample subjected to 10 min of pre-treatment. The samples subjected to NH_3 pre-treatment show a reduced surface-related current dispersion of 9% (compared to 16% for the untreated sample), which is attributed to the reduction of O at the SiN/epi interface. Furthermore, NH_3 pre-treatment for 10 min significantly improves the current dispersion uniformity from 14.5% to 1.9%. The reduced trapping effects result in a high output power of 3.4 W mm^{-1} at 3 GHz (compared to 2.6 W mm^{-1} for the untreated sample). These results demonstrate that the *in situ* NH_3 pre-treatment before LPCVD of SiN passivation is critical and can effectively improves the large-signal microwave performance of GaN HEMTs.

Keywords: GaN HEMTs, microwave, LPCVD, NH_3 pretreatment, traps

(Some figures may appear in colour only in the online journal)

1. Introduction

GaN HEMTs are suitable in applications where high power and high frequency properties are essential. This owes to the intrinsic III-N heterostructure properties such as a large bandgap, high electron saturation velocity combined with a high electron mobility [1]. However, the full potential of GaN HEMTs in large-signal operation at high frequency is limited by trapping effects, leakage currents, and hot-electron-related damages at the interface between the epi-structure and passivation layer [2, 3]. A silicon nitride (SiN) passivation layer has commonly been used to mitigate electron trapping at the surface by providing extra positive charges to neutralize

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trapped negative electrons on the surface [4, 5]. However, dangling bonds and oxygen (O) at the interface between the SiN passivation layer and the epi-structure remain a source of trap states [6, 7]. Therefore, effective pre-treatment methods before SiN passivation are critical. SiN is commonly deposited with plasma-enhanced chemical vapor deposition (PECVD) or low-pressure chemical vapor deposition (LPCVD), where LPCVD provides better dielectric properties thanks to the higher deposition temperature [8], and less hydrogen incorporation [9].

Ex situ pre-treatment methods, including etching in HF, HCl, and NH_4OH, effectively remove the surface O and surface contaminants before passivation [10, 11]. However, fluorine or chlorine residues [12–14], as well as surface re-oxidation, are detected on the epi-surface after such pre-treatments. *In situ* plasma-based pre-treatments, such as hydrogen-, fluorine- and nitrogen-based plasmas [12, 15–24], circumvent re-oxidation. However, plasma treatments involve unwanted effects from high-energy ions. Hydrogen ions diffuse into the active layers of epi-structure, which degrades device reliability [15]. Similarly, pre-treatment with fluorine-based plasma incorporates donor-like fluorine ions at the surface and in the epi-structure. This causes an unwanted depletion of the two-dimensional electron gas (2DEG) channel resulting in a positive shift of the threshold voltage [21, 22]. In contrast, nitrogen-based plasma pre-treatment simultaneously removes surface dangling bonds (by reoccupying nitrogen vacancies) and the native O layer on the surface [18, 19]. Several studies investigate plasma-based *in situ* pre-treatment methods followed by PECVD SiN deposition [15, 18, 19, 21, 22]. However, there is a lack of reports correlating *in situ* plasma-free gas-phase pre-treatment before deposition of SiN with LPCVD to device performance [12].

In this study, a plasma-free *in situ* NH_3 pre-treatment of the epi-structure is applied before deposition of SiN with LPCVD for GaN HEMTs. The effect of the NH_3 pre-treatment on the SiN/GaN interface was investigated by high resolution scanning transmission electron microscopy (HR-STEM) in combination with electron energy loss spectroscopy (EELS), while the effect on GaN HEMT performance was characterized by DC, pulsed-IV, s-parameters, and active load-pull at 3 GHz.

2. Experimental

The GaN HEMT heterostructure was grown on a semi-insulating SiC substrate by SweGaN using metal organic chemical vapor deposition (MOCVD). A 60 nm thick AlN nucleation layer was grown on the SiC substrate followed by a 1.85 μm thick Fe-doped GaN buffer layer, a 1 nm AlN exclusion layer, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, and a 2 nm GaN cap layer. A 2DEG concentration of 9.4×10^{12} cm^{-2} and an electron mobility of 2085 cm^2 Vs^{-1} were measured by contactless Hall effect measurements (Lehighton).

The HEMT fabrication started with wafer cleaning using the RCA-standard cleaning process (SC1 and SC2) to remove the surface ionic and organic contaminants followed by oxide removal in diluted ammonia (NH_3). Before the deposition of the SiN (55 nm) with LPCVD [25], the surface was exposed to an *in situ* NH_3 pre-treatment at the temperature of 820 °C, the flow rate of 23 sccm, and the chamber pressure of 250 mTorr with different duration (0, 3, and 10 min), denoted as samples T_0, T_3, and T_{10}, respectively. HEMT isolation was achieved through mesa etching with a depth of 230 nm. Deeply recessed Ta/Al/Ta ohmic contacts were fabricated, resulting in a contact resistance of 0.35 Ω·mm as extracted by transmission line measurement (TLM) measurements [26, 27]. The gate process includes two electron beam lithography (EBL) steps. The first step defines the etch mask for the recess in the SiN, which defines the L_g of 200 nm. The gate recess of SiN was performed by 6 min $CF_4 + Ar$ plasma etching with an etching rate of ~9 nm min^{-1} followed by 1 min 20 s NF_3 plasma over-etching with a negligible etching rate to GaN cap layer. The over-etching is approximately 20 s. The second step defines the pattern for the gate metallization (Au/Pt/Ni) with an integrated source and drain field plate of 0.1 and 0.25 μm, respectively. There is no source-connected field-plate on these devices. The total gate width of the HEMTs characterized in this study is 2×50 μm with a source-drain distance of 2.7 μm and a gate-drain distance of 1.7 μm.

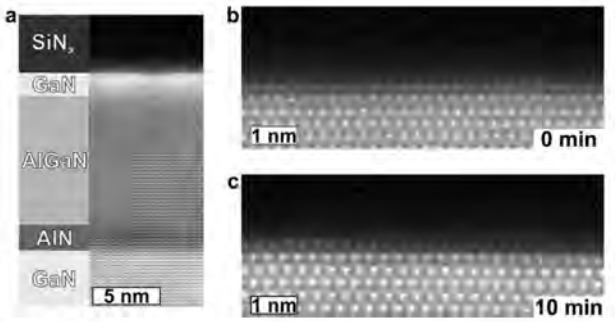

Figure 1. HR-STEM HAADF images of the interface. (a) shows the overview (right) with a schematic of the SiN and the epi-structure (left). (b) and (c) show the GaN–SiN interface at high magnification of the T_0 and the T_{10} samples, respectively.

Two samples were specifically processed for structural and chemical analysis. This process only included the RCA-cleaning, diluted NH_3 O etching, and the deposition of the SiN with LPCVD with no or 10 min of NH_3 pre-treatment, respectively. Both samples were cut, fixed in titanium grids, and mechanically polished, followed by ion-milling to electron transparency.

The SiN/epi interface was structurally and chemically characterized by high-angle annular dark-field (HAADF)-STEM in combination with EELS, using a double corrected STEM (Titan^3 60-300), operated at 300 kV and an embedded imaging filter (GIF Quantum ER System). EELS spectra were recorded using 0.25 eV/channel dispersion, 0.2 s dwell time, and convergence and collection semi-angles of 22 and 56.5 mrad respectively (28.2 mrad collection semi-angle for the T_{10} sample).

The crystal structure was investigated by HAADF-STEM, where the AlGaN, GaN, and amorphous SiN layers and their

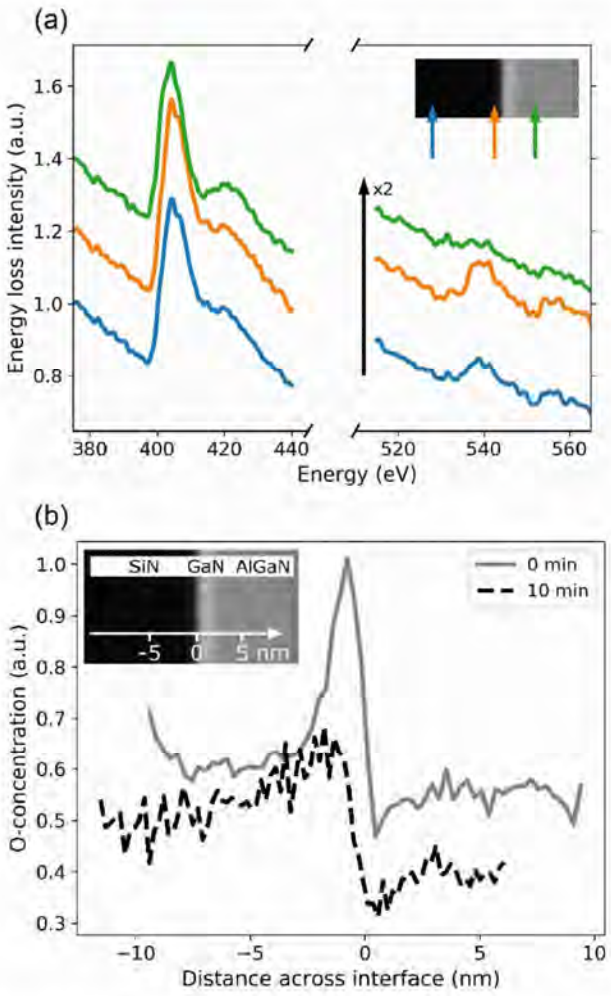

Figure 2. (a) EELS spectra (N K-edge, left and O K-edge, right) from different positions near the interface between the passivation and the HEMT structure of the untreated (T_0) sample (inset top right). The color-coding of the arrows shows the location of each spectrum. (b) Pseudo-concentration line profiles of O across the interface (inset top left) for the T_0 and the T_{10} sample, qualitatively comparing no pre-treatment and using pre-treatment.

interfaces could be distinguished, using image intensity differences due to mass contrasts (figure 1). A comparison of the T_0 and T_{10} samples (figures 1(b) and (c), respectively) revealed no apparent difference in the intensities of the atoms in the top layer, which indicate similar crystal crystalline quality of the top barrier layers in both cases.

However, EELS analysis of the T_0 sample revealed an uneven distribution of O, with an elevated concentration of O in the SiN, near the GaN/SiN interface (figure 2(a)). The EELS spectra show constant intensities for Nitrogen (N K-edge, at ~400 eV), but different intensities for O (O K-edge, at ~530 eV) for three different locations at the SiN/semiconductor interface. For a clearer comparison between the T_0 and T_{10} samples, to illustrate the qualitative effect of NH_3 pre-treatment, the relative edge intensities were normalized vs. the background signal, creating pseudo-concentration profile (figure 2(b)). A distinct accumulation of O is detected within 2–3 nm from the GaN/SiN interface for the T_0 sample. In contrast, the T_{10} sample exhibits a reduced O-concentration at the interface. This indicates that the O is removed by hydrogen from decomposed NH_3 [12]. Furthermore, the O distribution is more detached from the interface, as seen by an apparent shift of the peak intensity away from the interface.

3. HEMT results

The 2DEG properties after device processing were characterized by Hall measurement on van der Pauw structures. The samples show identical electron density of 1×10^{13} cm^{-2} and electron mobility of 2100 cm^2 V s^{-1}. These results indicate (as compared to contactless Hall measurements directly after growth) that different NH_3 pre-treatment duration and device processing do not affect the 2DEG properties negatively.

DC measurements were performed on 12 randomly selected HEMTs on each sample and the results (figure 3) are the average results of 12 devices with a parameter analyzer (Keysight B1500A). The HEMTs on all samples show a maximum source-drain current (I_{DS-max}) of 900 mA mm^{-1} (figure 3(a)) and a maximum transconductance (g_{m-max}) of 350 mS mm^{-1} (figure 3(b)) with threshold voltages (V_{TH}) of ~−1.9 V for T_0 and T_3. However, T_{10} presents a slightly lower I_{DS-max} and g_{m-max} (within the range of error bars), which might imply unwanted surface charges which depletes the 2DEG channel due to overexposing of NH_3 [12]. A small positive shift of V_{TH} (0.05 V) on both T_3 and T_{10} indicates an effect of the NH_3 pre-treatment on the Schottky contact compared to T_0. Moreover, similar off-state breakdown of 70–80 V were characterized for all samples with the breakdown criteria of 1 mA mm^{-1}.

Short channel effects of HEMTs were characterized by drain-induced barrier lowering (DIBL) and subthreshold swing (SS) (figure 3(d)). DIBL was calculated as $|\Delta V_{po}/\Delta V_{DS}|$, where the pinch-off voltage (V_{po}) is defined as the V_{GS}, resulting in an I_{DS} of 1 mA mm^{-1}, and V_{DS} ranges from 1 to 20 V. SS was extracted from the transfer characteristics at V_{DS} = 20 V. All samples present a leakage current of 0.1–1 mA mm^{-1}, which is mainly caused by the direct contact of gate metal to the 2DEG channel at the mesa sidewall. The NH_3-pre-treatment results in smaller DIBLs (14 and 17 mV V^{-1} on the T_3 and T_{10}-samples, respectively), compared to a DIBL of 20 mV V^{-1} on the T_0 sample. Moreover, SS reveals a similar trend as DIBL where the T_0-sample shows a larger SS of 270 mV dec^{-1} compared to 200 mV dec^{-1} for the T_3 and T_{10} (figure 3(d)). These results indicate that the gate control is improved by the NH_3 pre-treatment. A lower gate leakage currents of the T_{10}-sample (figure 3(c)) may be due to an improved interface at SiN/epi, which reduces surface-related leakage paths and improves the Schottky contact.

Furthermore, the cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were calculated from s-parameter measurements up to 145 GHz at room temperature on three randomly selected HEMTs in each sample. The small-signal high frequency performance was improved by longer

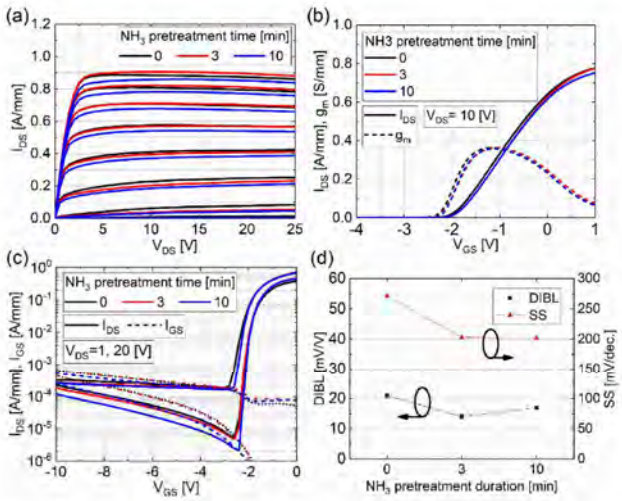

Figure 3. DC measurements, (a) *I*–*V*, (b) g_m, (c) transfer characteristics, and (d) DIBL/SS summary.

Table 1. Extracted intrinsic parameters.

	C_{gs} (fF)	C_{gd} (fF)	g_{m-in} (mS)	R_{ds} (Ω)	R_i (Ω)
T_0	162	10.5	39	1170	6.25
T_{10}	177	11.0	43	1310	5.36

NH_3-pre-treatment. The f_T/f_{max} were 43/83, 46/95, and 52/109 GHz for the T_0, T_3, and T_{10}-samples, respectively. An equivalent small-signal electrical model was extracted for the HEMTs on the T_0 and T_{10} samples by the direct extraction method [28]. The intrinsic parameters (table 1) were obtained at the bias settings yielding the highest f_{max}. Comparing equivalent circuit parameters of HEMTs on T_0 and T_{10}, shows an increase of intrinsic transconductance ($g_{m,int}$), gate-source (C_{gs}), gate-drain (C_{gd}) capacitance, and output resistance (R_{ds}). These effects as well as reduced input resistance (R_i) can be explained by the reduction of the oxide thickness at the SiN/GaN and Schottky metal/GaN interface with improved gate control, which improves the high frequency performance.

Pulsed-IV measurements (using AMCAD AM3200) were performed with a pulse width of 1 μs and a duty cycle of 0.001% on 12 randomly selected HEMTs for all samples at different quiescent biases (V_{GSQ}, V_{DSQ}) of [(0, 0), (−5, 0), and (−5, 25)], denoted as [Q_{ref}, Q_0, and Q_{25}] (figure 4). The surface and buffer-related current collapse are defined as:

$$Z_{surface} = \left| \frac{I_{DS}(Q_{ref}) - I_{DS}(Q_0)}{I_{DS}(Q_{ref})} \right| \quad (1)$$

$$Z_{buffer} = \left| \frac{I_{DS}(Q_{ref}) - I_{DS}(Q_{25})}{I_{DS}(Q_{ref})} \right| \quad (2)$$

where $I_{DS}(Q_{xx})$ is the current in the pulse at V_{GS} = 1 V and V_{DS} = 0–25 V for Q_{ref}, Q_0, and Q_{25}, respectively. HEMTs on the T_0 sample show a higher $Z_{surface}$ of 16% as compared to that on T_3 and T_{10} samples of 9% and 10%, respectively. This

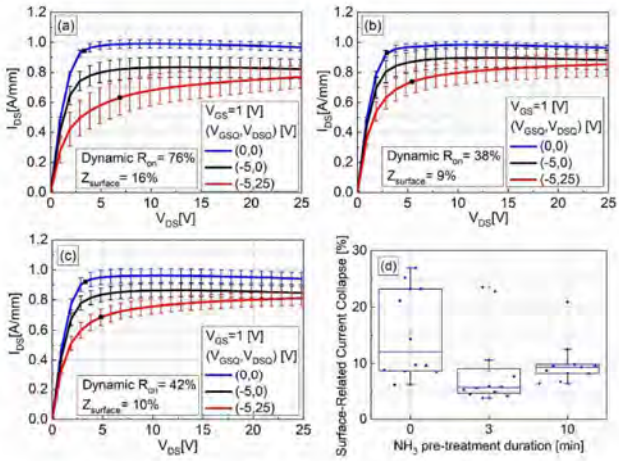

Figure 4. Pulsed-IV measurements on 12 randomly selected HEMTs on each sample with different NH_3 pre-treatment duration, (a) T_0, (b) T_3, and (c) T_{10}. (d) Uniformity of surface-related current collapse response.

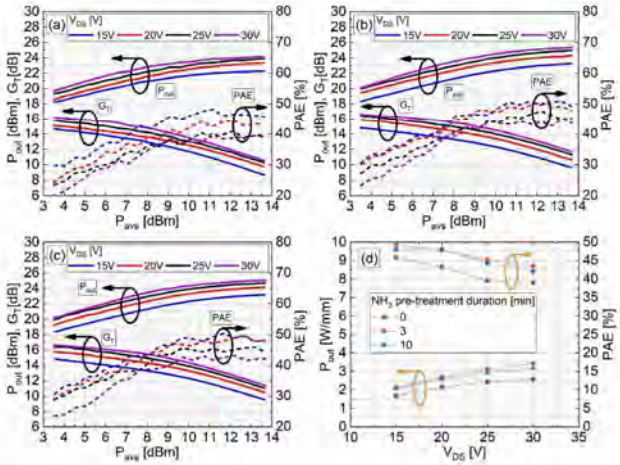

Figure 5. Active load-pull measurements at 3 GHz on HEMTs with different NH_3 pre-treatment duration, (a) T_0, (b) T_3, and (c) T_{10}. (d) Summary of P_{out} and PAE.

indicates that the NH_3 pre-treatment effectively removes the surface traps at the SiN/GaN interface. Consistently, T_3 and T_{10} samples also present a 50% lower dynamic on-resistance (R_{on}) at Q_{25} compared to the T_0 sample. A slightly higher dynamic R_{on} on T_{10} sample compared to T_3 sample might be due to an overexposing of NH_3 pre-treatment, resulting in extra unwanted nitrogen atoms at the interface of SiN/epi [12]. The level of the dynamic R_{on} degradation is impacted by the GaN buffer design (Fe-doped), device dimensions (L_g and L_{gd}) and design (no source-connected field-plate).

Furthermore, a longer NH_3 pre-treatment duration results in strikingly improved uniformity of $Z_{surface}$ with 4.5% and 1.9% on the T_3- and T_{10}-samples, respectively, compared to 14.5% on the T_0-sample (figure 4(d)). A balance of low current collapse with high device uniformity can be further optimized with NH_3 pre-treatment duration.

The large signal performance in class-AB with (I_{DS} 20% of I_{DS-max}) was characterized at 3 GHz with an active load-pull system on three randomly selected HEMTs in each sample [29] (figure 5). A higher output power (P_{out}) of 3.4 W mm^{-1} for the HEMTs is achieved on T_3 and T_{10} samples at a drain bias of 30 V as compared to the T_0 sample with P_{out} of 2.6 W mm^{-1}. Due to the surface-related trapping effects, the T_0 sample has an overall 5%–10% lower PAE than T_3 and T_{10} samples (figure 5(d)). Since all samples show similar I_{DS-max}, short channel effects, and breakdown voltage, the lower output power and efficiency of the T_0 sample are likely caused by a higher concentration of surface traps, which result in larger gate-lag and knee-voltage walkout.

4. Conclusion

This study investigates the impact of plasma-free *in situ* NH_3 pre-treatment before LPCVD SiN passivation on HEMT device characteristics and interface properties. 2DEG properties and DC performance are not degraded and comparable for all samples after the NH_3 pre-treatment. Higher f_T/f_{max} are extracted on the sample with longer pre-treatment duration. Pulsed-IV measurements reveal a reduction of surface-related trapping effects and a much better device uniformity after 3 and 10 min NH_3 pre-treatment. The lower current collapse directly translates to higher output power and efficiency on large-signal performance. The observed improvement is attributed to the reduced O concentration and its proximity to the interface between the SiN passivation and the GaN cap layers, which are revealed by STEM-EELS analysis. Further study on nitrogen re-occupation with the eliminating of O at the interface is required. These promising results demonstrate a simple pre-treatment method for LPCVD SiN passivation for processing of GaN HEMTs with improved microwave power performance. Moreover, this pre-treatment potentially also offers an ion damage free method to clean and restore the surface of III-nitride material during processing, e.g. gate recess step.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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Paper D

Characterization of Trapping Effects Related to Carbon Doping Level in AlGaN Back-Barriers for AlGaN/GaN HEMTs

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Characterization of Trapping Effects Related to Carbon Doping Level in AlGaN Back-Barriers for AlGaN/GaN HEMTs

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***Abstract*— The impact of different carbon concentrations in the $Al_{0.06}Ga_{0.94}N$ graded back-barrier and GaN buffer of high electron mobility transistors (HEMTs) is investigated. Four epi-wafers with different carbon concentrations, ranging from 1×10^{17} to 5×10^{17} cm^{-3}, were grown by metal organic chemical vapor deposition (MOCVD). HEMTs with 100 and 200 nm gate lengths were fabricated and characterized with dc, Pulsed-IV, drain current transient spectroscopy (DCTS), and large-signal measurements at 30 GHz. It is shown that the back-barrier effectively prevents buffer-related electron trapping. The highest C-doping provides the best 2DEG confinement, while lower carbon doping levels are beneficial for a high output power and efficiency. A C-doping of 1×10^{17} cm^{-3}offers the highest output power at maximum power added efficiency (PAE) (1.8 W/mm), whereas 3×10^{17} cm^{-3} doping provides the highest PAE (>40%). The C-profiles acquired by using secondary ion mass spectroscopy (SIMS), in combination with DCTS, is used to explain the electron trapping effects. Traps associated with the C-doping in the back-barrier are identified and the bias ranges for the trap activation are discussed. The study shows the importance of considering the C-doping level in the back-barrier of microwave GaN HEMTs for power amplification and generation.**

***Index Terms*— AlGaN/GaN, back-barrier, dispersion, double heterostructure, high electron mobility transistors (HEMTs), short channel effect (SCE).**

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I. Introduction

GAN-BASED high electron mobility transistors (HEMTs) on SiC have become an important semiconductor technology for power amplification and generation in microwave and millimeterwave applications. The high-frequency optimization of GaN-based HEMTs requires both lateral downscaling, to reduce electron transit time, and vertical downscaling, to improve electron confinement and modulation [1]. The electron confinement may be further improved by including an $Al_xGa_{1-x}N$ back-barrier or deep-level (C or Fe) doping beneath the channel. Lack of electron confinement may lead to short channel effects (SCEs), limiting the frequency performance, maximum output power, and power added efficiency (PAE) [2]. Fe and C with various doping profiles have been utilized to enhance buffer isolation and mitigate poor gate modulation [3], [4], [5]. One main difference between Fe and C doping is that Fe doping entails a growth memory effect inhibiting abrupt doping profiles [6], whereas C-doping allows for sharp doping profiles, enabling larger degrees of freedom for optimization. However, deep level doping always leads to different types of electron trapping effects with time constant varying from μs to 10 s of seconds [7]. Hence, many studies have been devoted to understanding C trapping and detrapping mechanisms [8], [9].

Different back-barrier designs, including AlGaN, p-GaN, InGaN, and AlN layer, have been proposed resulting in the suppression of the SCE and higher output power density [10], [11], [12], [13]. The trapping effects due to the deep level doping in the back-barrier and the buffer have previously been investigated, where a trap state located at $E_c-0.6$ eV was identified in an intentionally C-doped AlGaN back-barrier [14]. Furthermore, it has been demonstrated that an undoped AlGaN back-barrier can effectively prevent electron trapping in the highly doped buffer [15], [16]. Interesting

2 nm	GaN Cap
10 nm	$Al_{0.3}Ga_{0.7}N$
1.5 nm	AlN Exclusion Layer
100 nm	UID GaN Channel
800 nm	Al_xGa_xN Back-Barrier (Graded $0 < x < 0.06$) C-doped
800 nm	GaN Buffer C-doped
50 nm	AlN Nucleation Layer
	4H-SiC Substrate

WAFER NAME	C-doping level	
	Back-Barrier	Buffer
High-C	HIGH-C	HIGH-C
Mid-C	MID-C	MID-C
Low-C	LOW-C	LOW-C
Mid-C/High-C	MID-C	HIGH-C

C-doping levels
HIGH-C $\sim 5 \times 10^{17}\text{cm}^{-3}$
MID-C $\sim 1.5 \times 10^{17}\text{cm}^{-3}$
LOW-C $\sim 0.7 \times 10^{17}\text{cm}^{-3}$

Fig. 1. To the left, schematic of epitaxial structure (not to scale). Top right, the back-barrier and buffer C-doping levels for all wafers are stated, with the nominal C-doping levels in the bottom right.

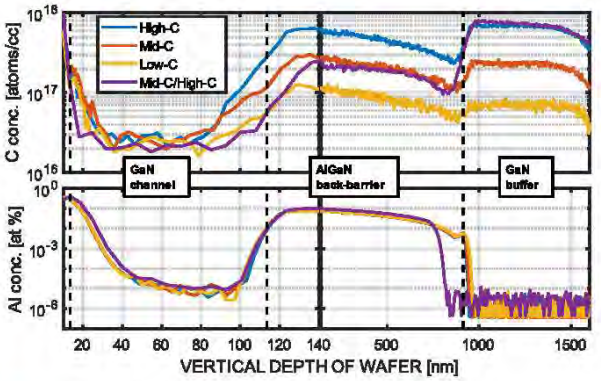

Fig. 2. SIMS data of (a) C concentration and (b) Al concentration for all four wafers. The vertical dashed lines mark the channel, back-barrier, and buffer layers according to nominal design.

work on C-doped back-barrier design has led to promising results concerning reduced dynamic R_{on} (reduced trapping) with preserved 2DEG confinement, providing a future path for optimization [17]. Our previous study on the impact of the channel thickness of GaN HEMTs with back-barrier indicated that there is electron trapping occurring in the C-doped back-barrier [13]. However, to this date, there is a lack of studies on the impact of deep level doping in the back-barrier on the large signal performance of GaN HEMTs and the trap mechanisms involved.

In this study, we investigate the influence of the C-doping level in AlGaN back-barriers and buffers on dc, small- and large-signal performance, and analyze the results regarding electron-trapping effects.

II. Experiments

A. Back Barrier Epitaxy

The epitaxial wafers used in this study are grown on quarter 4-in semi-insulating 4H-SiC substrates with metal-organic chemical vapor deposition (MOCVD) by SweGaN AB [18]. The nominal design of the four heterostructures is shown in Fig. 1. The epitaxial growth starts from a 50 nm-thick AlN nucleation layer, followed by an 800 nm-thick C-doped GaN buffer layer. Above the buffer layer, an 800 nm-thick C-doped $Al_xGa_{1-x}N$ back-barrier is grown with linearly graded Al stoichiometry from 0% at the (AlGaN back-barrier/GaN buffer) interface to 6% at the top of the back-barrier. On top of the back-barrier, an undoped GaN channel is grown with a thickness of 100 nm. The barrier consists of an AlN exclusion layer (1.5 nm), an AlGaN barrier with 30% Al composition (10 nm), and a GaN cap-layer (2 nm). Apart from the C-doping of the buffer and the back-barrier, the epitaxial design is nominally identical for all four structures.

The study of the impact of the doping of the back-barrier (and the buffer) is facilitated by the variation of the C-doping level in the back-barrier and the buffer. Three wafers are epitaxially grown with the nominal doping: $\sim 5 \times 10^{17}\text{cm}^{-\text{m}}$ (denoted HIGH-C), $\sim 1.5 \times 10^{17}\text{cm}^{-\text{m}}$ (MID-C), and $\sim 0.7 \times 10^{17}\text{cm}^{-\text{m}}$ (LOW-C), respectively, (Fig. 1). The carbon incorporation was controlled by the growth process parameters, primarily temperature, and pressure, TMG flow, etc., described in [19]. Therefore, the steepness of the C profile will be directly correlated with the rate of temperature change.

The C-concentration in AlGaN back-barrier followed roughly the same concentration as in the buffer. A fourth wafer was grown with the HIGH-C doping in the buffer and with MID-C doping in the back-barrier (denoted Mid-C/High-C), facilitating the separation of the effect of the carbon doping level in the buffer and the back-barrier.

The composition was verified through secondary ion mass spectroscopy (SIMS) shown in Fig. 2. Notably, both the Mid-C and High-C epi-structures have nonnegligible trailing C-levels into the channel, resulting in an approximately two times larger carbon concentration at the interface region compared to Mid-C/High-C and Low-C, which needs to be considered in the analysis below. The Al concentration in the back-barrier channel transition is sharply defined and occurs at the same depth for all wafers [Fig. 2(b)].

B. HEMT Fabrication

Samples with a size of 16×16 mm^2 were cut from the 4-in wafers. The samples were cleaned with RCA-1, RCA-2, and diluted ammonia to remove organic, metallic contamination, and oxide before the deposition of the passivation layer. A 65 nm-thick Si-rich silicon nitride (SiN_x) passivation layer was deposited at 820 °C by low-pressure chemical vapor deposition (LPCVD). Device isolation is accomplished through mesa-etching. Recessed Ta-based ohmic contacts are realized with laser writer (Heidelberg Instruments DWL 2000) and evaporation of a Ta/Al/Ta metal stack annealed at 550 °C. A contact resistance of $\sim$0.35 Ω·mm was measured on TLM structures of all epitaxial designs.

The gate–source distance was 0.65 and 0.75 μm, while gate–drain distance was 1 and 2 μm for the HEMTs with gate lengths of 100 and 200 nm, respectively. The gate was defined with two electron beam lithography (EBL) steps. The first step defines the recess in the SiN_x-passivation, and the second step defines the gate metallization (Ni/Pt/Au) including an integrated field plate. The field plates are 0.15 and 0.25 μm for the 100 and 200 nm gate lengths, respectively). Finally, the gate, drain, and source electrodes (Ti/Au) were defined and

TABLE I
ELECTRONIC PROPERTIES OF PROCESSED EPI-WAFERS

WAFER	Hall (Contactless Eddy Current and Lehighton)					
	R_{sh} [Ω/sq]		μ [cm²/V-s]		n_s [10^{13}cm^{-2}]	
High-C	319	(301)	2000	(2150)	0.98	(0.96)
Mid-C	320	(307)	2050	(2150)	0.95	(0.94)
Low-C	306	(304)	2100	(2150)	0.97	(0.95)
Mid-C/High-C	324	(315)	2000	(2050)	0.97	(0.96)

TABLE II
DC CHARACTERIZATION RESULT

WAFER	L_g = 200nm (L_g = 100nm)							
	R_{on} [Ω·mm]	SS @2.1V [mV/dec.]		SS @20.1V [mV/dec.]		DIBL [mV/V]	
High-C	3.5	66	(72)	78	(87)	2.0	(2.8)
Mid-C	2.9	68	(75)	77	(93)	5.4	(5.3)
Low-C	2.0	69	(76)	92	(102)	8.1	(14)
Mid-C/High-C	2.2	71	(74)	81	(96)	5.9	(11)

metallized with sputtering. Two-finger, coplanar HEMTs with a gate width of 2 × 50 and 2 × 100 μm were used in the characterization presented below.

III. DEVICE CHARACTERIZATION

A. Electronic Properties of Epi-Wafers

After growth, the electron mobility (μ) and sheet carrier density (n_s) of the 2DEG are measured by a contactless Lehighton system. The electron properties of the different epi-wafers are summarized in Table I. A high mobility resulting in a low sheet resistance is achieved for all wafers thanks to the insertion of AlN exclusion layer and optimized growth of the barrier/channel interface. Van der Pauw structures were fabricated together with the HEMTs of the same samples. The Hall measurements indicate that LPCVD passivation combined with the low annealing temperature for the formation of the Ta-based ohmic contact preserves the sheet resistance (Table I). The epi-wafers exhibit near-identical mobility and electron density, demonstrating a repeatable growth of the barrier-, spacer-, and cap-layer. The slight disparities in R_{sh} and μ between wafers may be tied to the differences in interface sharpness or compositional control of the AlN exclusion layer according to the usual uniformity of sheet resistance (2%–3%) of as-grown GaN HEMT epi-wafers. Strengthening the case that interwafer variations are to a major part due to C-level differences.

B. DC and Small Signal Characterization

The dc performance of 2 × 50 μm HEMTs with L_g of 100 nm and 200 nm was characterized using a parameter analyzer (Keithley 4200-SCS). The transfer and output characteristics of HEMTs with L_g of 200 nm of all epi-designs are shown in Fig. 3. Similar maximum transconductance $g_{m,\max}$ (>300 mS/mm) and I_{DS} at $V_{GS} = +1$ V(>600 mA/mm) are achieved for all designs. The I_{DS} at $V_{GS} = +1$ V is lower than expected for the used barrier design, which is probably due to a slight over-etching of the recess into the SiN_x-passivation, creating a positive V_T shift [20]. However, this does not affect the analysis of the impact of the different back-barrier and the buffer designs. It is believed that the higher saturation current (I_{DSS}) for Mid-C/High-C may be due to lower C level in the channel compared to High-C and Mid-C, while at the same time having better confinement than Low-C due to higher back-barrier doping. All samples show an I_{on}/I_{off} ratio of $\sim 1 \times 10^7$, and a drain leakage current of $\sim 1 \times 10^{-0}$ mA/mm, which is in line with previous back-barrier

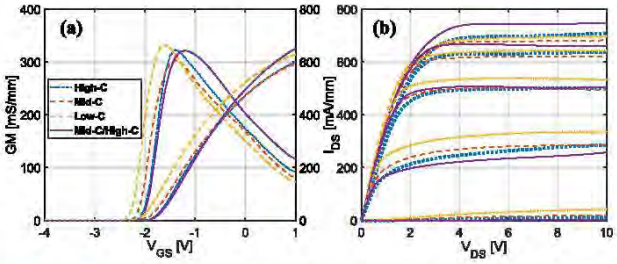

Fig. 3. (a) Transfer characteristics for $V_{GS} = -4{:}0.1{:}1$ V at $V_{DS} = 6$ V and (b) output characteristics for $V_{DS} = 0{:}0.1{:}10$ V, $V_{GS} = -3{:}1{:}1$ V.

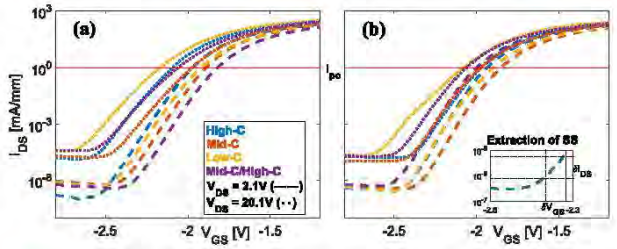

Fig. 4. Transfer characteristics in log-scale used to extract DIBL and SS. V_{DS} is kept constant, while V_{GS} is swept, $V_{DS} = 0.1$ and $V_{DS} = 20.1$ V, $V_{GS} = -3{:}0.1{:}-1$ V. A red horizontal line indicates the pinch-off current. (a) $L_g = 100$ nm. (b) $L_g = 200$ nm.

studies [21], [22]. The drain-induced barrier lowering (DIBL) was calculated by DIBL $= \Delta V_{po}/\Delta V_{ds}$ using the pinch-off voltages (V_{po}) at $V_{DS} = 2.1$ and 20.1 V and a pinch-off current (I_{po}) of 1 mA/mm (Fig. 4). The subthreshold swing (SS) was extracted at the maximum derivative of $I_{DS}(V_{GS})$ in the subthreshold region (Fig. 4). For the lower electric field (at $V_{DS} = 2.1$ V), the SS is similar for all back-barrier designs. However, at a higher electric field ($V_{DS} = 20.1$ V), it is clear that SS (and DIBL) degrades with lower C-doping in the back-barrier (Table II) due to poor electron confinement. The electron confinement is evidently improved with a higher C-doping likely due to electric field-induced charging of the deep-levels associated with the C-doping.

Comparing the dc parameters of the High-C and Mid-C/High-C suggests that the trap states in the buffer are not activated to the same degree as in the back-barrier. This demonstrates the capacity of the back-barrier to effectively minimize trapping effects originating in the buffer. Notably, the High-C suffers from the high C-concentration, demonstrated by a higher R_{on} (extracted from the output characteristics, hence influenced by memory effects), which is due to a back-gating

effect caused by filling of trap states in the back-barrier and the channel/back-barrier interface region at high electric fields. This explains the discrepancy between the results in Tables I and II since the electric field present in the Hall measurement is much smaller.

S parameters were measured up to 145 GHz of six 2×50 μm, $L_g = 100$ nm devices per wafer. The V_{GS} is swept from -3.5 to 1 V with a step of 0.5 V, and V_{DS} is swept from 0 to 20 V with a step of 0.5 V. The samples showed similar maximum extrinsic f_T (56–58 GHz) obtained at (V_{GS}, V_{DS}) = (-1.5, 4.5 V) and maximum f_{max} (66–68 GHz) obtained at (V_{GS}, V_{DS}) = (-1.5, 10 V). The samples demonstrate similar small-signal performance since significant C-related trapping does not occur for $V_{DS} \leq 10$ V. Raising V_{DS} to 20 V increases the carbon-related trapping in the back-barrier (and the channel) causing a larger drop in f_{max} for High-C as compared to Low-C (21% and 13%, respectively). Although a higher C doping leads to better 2DEG confinement, hence, lower output conductance (g_{ds}); it does not necessarily entail an improvement in f_{max} [13]. These results indicate that for the C-doping level variation within this study, the dispersion effects dominate over SCE in reducing f_{max} at high electric fields.

C. Large Signal Characterization

Large signal characterization at 30 GHz was performed using a passive load-pull setup. The 2×100 μm devices with 200 nm gate-length were measured at class AB condition (quiescent current 15%–20% of I_{DSS}) with V_{DS} ranging from 5 to 25 V in steps of 5 V. The load impedance (Γ_L) was optimized for maximum output power (P_{out}). The PAE is calculated by assuming that input power equals available source power ($P_{in} = P_{avs}$); hence, the obtained PAE may be slightly underestimated. In this study, the output power P_{out} at maximum PAE (P_{PAE}) is used as a figure of merit, providing a comparison at a relevant operation point, displayed together with highest PAE for each V_{DS} bias in Fig. 5. Both dispersion effects and SCE (which appear at higher V_{DS} values) have detrimental impacts on the delivered output power, by limiting the output voltage and current waveforms. Dispersion invokes knee-walkout, hence, increasing knee-voltage (V_{knee}) and reducing knee-current (I_{knee}), whereas SCE causes an increase in $I_{DS,off}$ [13]. By measuring devices with $L_g = 200$ nm, the SCE is largely curtailed (Table II); hence, dispersion effects will have a more dominating impact on P_{out} as opposed to devices with shorter gate lengths ($L_g = 100$ nm).

All epi-structures demonstrate similar performance at $V_{DS} = 5$ V (Fig. 5), where both SCE and dispersion effects are low. However, at $V_{DS} = 10$ V and above, a general trend of worse power scaling as well as lower PAE for HEMTs with higher C-doping in the back-barrier is demonstrated. This is explained by an increased electron trapping in the back-barrier, causing an increase in (V_{knee}) and lower I_{max}. For $V_{DS} \geq 10$ V, all devices show a declining trend in PAE, where Low-C maintains the best performance up to $V_{DS} = 25$ V, further demonstrating that dispersion effects due to C-related trapping dominate over SCE. The doping level of the buffer has a seemingly minor impact on the electron trapping as

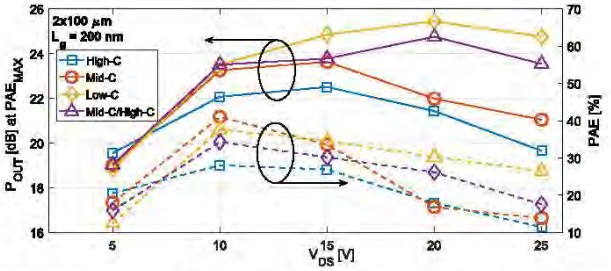

Fig. 5. P_{out} extracted at maximum PAE (P_{PAE}) for all wafers in the V_{DS} range 5–25 V.

demonstrated by the similar P_{PAE} and PAE up to $V_{DS} = 15$ V of the HEMTs on the Mid-C and Mid-C/High-C. Interestingly, the P_{PAE} and PAE at $V_{DS} > 15$ V of the HEMTs on Mid-C/High-C sample are higher compared to the HEMTs on the Mid-C sample. This is probably due to the difference in the trailing C-doping level at the channel/back-barrier interface (Fig. 2), where the Mid-C/High-C sample exhibits a lower doping level.

Overall, the HEMTs on the Low-C sample have the highest P_{PAE} and PAE in the measured voltage range, demonstrating that the C-doping level in the back barrier (and at the channel/back-barrier interface) has a major impact on the large-signal performance. The highest P_{PAE} was found for Low-C and Mid-C/High-C reaching >25.5 dBm, (~1.8 W/mm), while the P_{PAE} of High-C is affected by the C-doping in the back-barrier resulting in a P_{PAE} of 22.4 dBm. The highest PAE at $V_{ds} = 25$ V was achieved for Low-C (26.5%) as compared to the PAE of the High-C (11.8%). These results are similar to the performance recorded using stepped carbon profile as buffer doping [4].

IV. Trap Analysis

A. Pulsed-IV Measurements

Pulsed-IV was measured at room temperature on the GaN HEMTs (eight devices measured on each epi-structure) with a gate width of 2×50 μm and a gate length of 200 nm. R_{on} is defined as the minimum value of $R_{DS} = \Delta V_{DS}/\Delta I_{DS}$ at $V_{GS} = +2$ V. The quiescent bias points (V_{GSQ}, V_{DSQ}) were (0, 0), (-5, 0), (-5, 10), (-5, 20), and (-5, 30) V, denoted as Q_{ref}, Q_0, Q_{10}, Q_{20}, and Q_{30}, respectively. The pulsewidth was 1 μs with a duty cycle of 1%. The current slump ratio ($Z(Q_x)$) is defined as

$$Z(Q_x)[\%] = \frac{I_{DS}(Q_x) - I_{DS}(Q_{ref})}{I_{DS}(Q_{ref})} \cdot 100 \quad (1)$$

where $I_{DS}(Q_x)$ is the current level at Q_x. The slump ratio (Z) is calculated at $V_{GS} = 2$ V and $V_{DS} = 4$ V. The parameters extracted from the pulsed IV measurements are summarized in Fig. 6. It can be seen that the gate-lag is similar for all samples ($Z(Q_0) \approx -20\%$). The gate-lag is to a large extent dependent on surface-related trapping, thus dependent on SiN_x passivation layer, top epitaxial barrier design, and device processing [23]. In this study, the top barrier design, passivation, and gate process module are the same, and a similar gate-lag for all samples is expected, [Fig. 6(b)].

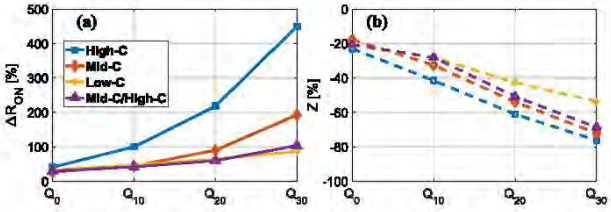

Fig. 6. In (a) ΔR_{ON} and in (b) Z, at different quiescent biases relative to Q_{ref}.

Therefore, any differences in lag-behavior should be related to the back-barrier and buffer design.

In contrast, there is a clear trend in drain-lag with respect to increasing V_{DSQ}. A higher C-doping level in the channel and back-barrier results in a larger current collapse for all wafers [Fig. 6(b)]. Since more electrons can get trapped in deep traps in the higher doped back-barriers at large electric fields, $Z(Q_{20})$ and $Z(Q_{30})$ show clear dependency on C-doping in the back-barrier; hence, these fields are sufficient to activate the back-barrier traps. The difference in $Z(Q_{10})$ for the Mid-C and Mid-C/High-C samples is explained by the trailing C-doping profiles into the channel region of the Mid-C (Fig. 2), which invokes a noticeable current collapse [Fig. 6(b)].

Furthermore, the similarity in the $Z(Q_{30})$ of the Mid-C and Mid-C/High-C samples (same C-doping level in the back-barrier, but different C-doping levels in the buffer) demonstrates that the back-barrier effectively prevents electron trapping in the buffer beneath the back-barrier, which was also demonstrated by the high P_{out} of Mid-C/High-C at $V_{DS} = 25$ V (Fig. 5). The effect of the electron trapping is clearly demonstrated by ΔR_{ON} at different quiescent biases [Fig. 6(a)], where a higher C-doping level in the back-barrier results in an increase in the dynamic R_{on}, from 4.0 to 13.5 Ω·mm.

B. Drain Current Transient—Temperature and Filling Time Dependence

The trapping behavior was further investigated through drain current transient spectroscopy (DCTS) with different filling times on 2 × 50 μm GaN HEMTs with a gate length of 200 nm devices. The filling time was varied from 1 ms to 10 s, with two different filling bias conditions, (V_{GF1}, V_{DF1}) = (−5, 10 V) to predominately study gate-dependent trapping and (V_{GF2}, V_{DF2}) = (−5, 30 V) to study drain-dependent trapping. The filling bias condition was followed by an ON-state condition in the saturation region ($V_{GS,ON}$, $V_{DS,ON}$) = (1, 6 V) for 10 s. For comparison, the same measurements were conducted on a reference wafer with similar top barrier but without back-barrier and any intentional buffer doping. The measurements were performed at chuck-temperatures ranging from 40 °C to 100 °C by steps of 20 °C. The self-heating effect results in a channel temperature ∼ 25 °C above the chuck temperature (assuming a thermal resistance of 5 K·mm/W) [4], [24].

Fig. 7 depicts the ON-state measured I_{DS} differentials and the transients obtained at different temperatures, using (V_{GF2}, V_{DF2}) with a filling time of 10 s. The transients

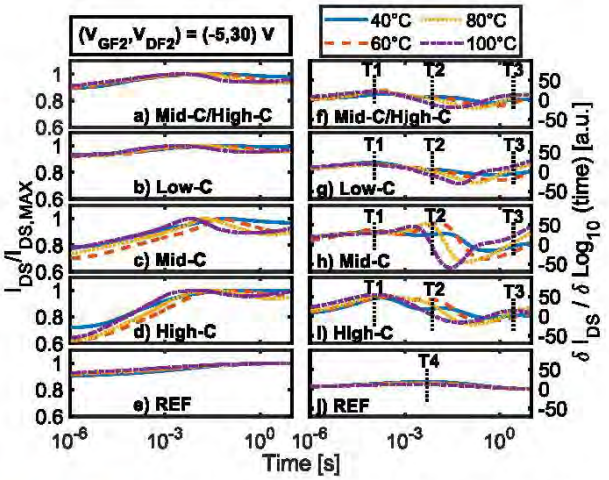

Fig. 7. (a)–(e) I_{DS} transients normalized to highest current with (f)–(j) corresponding differentials, for (V_{GF2}, V_{DF2}). ON-state and filling time was 10 s. Detrapping transients of C-doped wafers labeled T1, T2, T3 (and reference wafer labeled T4). Chuck temperatures ranging from 40 °C to 100 °C.

TABLE III
ACTIVATION ENERGIES, CROSS-SECTIONS, STRETCHING TERMS, AND TIME CONSTANTS FOR ALL TRAP STATES

	T1	T2	T3	T4
E_a [eV]	0.15	0.45	0.59	0.12
σ [cm^2]	1.4×10^{-19}	5.7×10^{-17}	2.4×10^{-18}	$1.0 \cdot 10^{-21}$
β	∼0.5	∼0.8	∼0.6	∼0.2
τ [s]	$\sim 1 \times 10^{-4}$	$\sim 1 \times 10^{-2}$	∼1 − 10	$\sim 1 \times 10^{-2}$

[Fig. 7(a)–(e)] are modeled using stretched exponentials [7], which can be used to calculate the differentials [Fig. 7(f)–(j)]. From the differential characteristics, three distinct detrapping transients found in all carbon-doped wafers are detected, denoted as T1, T2, and T3 with time constants τ_1, τ_2, and τ_3 of ∼0.1 ms, ∼10 ms, and ∼1–10 s, respectively [Fig. 7(f)–(i)]. The time-constants vary with chuck temperature, which is utilized in Arrhenius plots to extract E_a and σ (Fig. 8 and Table III). In line with PIV-measurements, all samples reveal a large I_{DS} transient dependency of the C-doping level in the back-barrier and at channel/back-barrier interface. It is also evident that trapping also occurs in the channel region as revealed by Mid-C [Fig. 7(c)] having a substantially larger current collapse (∼30%) compared to Mid-C/High-C (∼10%).

The T1 and T2 activation energies (0.15 and 0.45 eV) and cross sections (1.4×10^{-4}cm^{-m} and 5.7×10^{-7}cm^{-m}) of T1 and T2, respectively, are similar to what has been reported for carbon trap-states in MOCVD-grown GaN; T1 previously reported as a likely C-related defect (0.08 eV, [4]) and (0.14 eV [25]), similar origins are reported for T2 (0.49 eV [25]). In the DCTS, the I_{DS} decreases at ∼1–10 ms, which has been attributed to retrapping [26], or self-heating [24]. PIV measurements showed that back-barrier trapping was largely avoided at a quiescent bias of (V_{GSQ}, V_{DSQ}) = (−5, 10 V) (Fig. 6). The trapping occurring at this

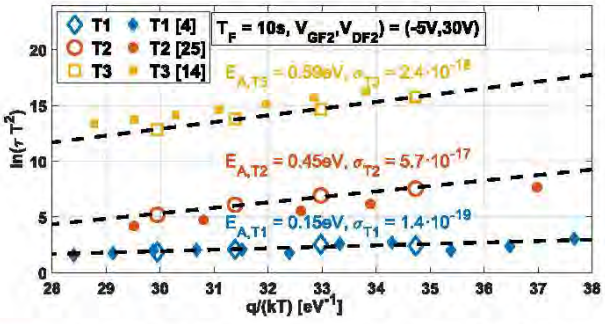

Fig. 8. Arrhenius plotting by averaging τ value obtained for T1, T2, and T3 (hollow marks) at each estimated channel temperature. The striped lines show the fitting used for obtaining E_a and σ (values given). Filled marks are the corresponding trapping reported in literature.

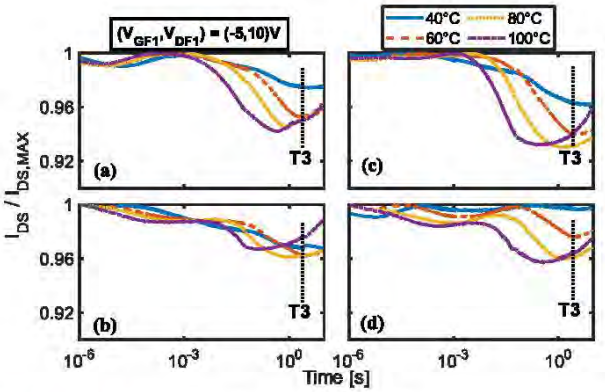

Fig. 9. (a)–(d) I_{DS} transients normalized to highest current, for (V_{GF1}, V_{DF1}). ON-state and filling time was 10 s. Detrapping transient labeled T3. Chuck temperatures ranging from 40 °C to 100 °C.

filling bias is therefore more likely due to surface and barrier traps as well as traps residing in the channel. Therefore, the absence of T1 and T2 in the transients at (V_{GF1}, V_{DF1}) = (−5, 10 V) indicates that they likely reside in the back-barrier [Fig. 9(a)–(d)]. T3 is still present; hence, a trap located in the surface or channel region.

The E_a of 0.59 eV for T3 point to either a nitrogen antisite, carbon, and/or AlGaN-related trapping (0.60 eV) [14], [16], [27]. Considering the low β, the amplitude, and time constant shifting, the nitrogen anti-site seems less likely since T3 does not behave like a point defect. Additionally, T3 shows no clear tendency with respect to the C-doping level [Fig. 9(a)–(d)]. Instead, its long trapping constant of 1–10 s and E_a value indicates a native defect (e.g., dislocations) generated during epitaxial growth of C-doped AlGaN back-barriers, hence, indirectly linked to C-doped AlGaN back-barriers [14], [16]. Comparative measurements were performed on the reference wafer at (V_{GF2}, V_{DF2}) [Fig. 7(e)], revealing one single transient T4 with a low stretching term [Fig. 7(j)], ($\beta = 0.2$) and a small temperature dependency combined, indicating a distribution of energy levels and/or detrapping effect partly governed by mechanisms such as hopping or tunneling (Table III). T4 may be either surface-related [28], impurity-related (carbon or hydrogen) [29], or stem from nitrogen vacancies [30]. T4 may be present in the detrapping transient in all wafers, but due to the low β and E_a with τ close to that of T2, its contribution to the transient is likely masked. The absence of T1, T2, and T3 for the reference wafer indicates that these transients are related to C-doping in the back-barrier or the channel.

V. Conclusion

This study investigates the impact of carbon doping concentration in the back-barrier of AlGaN/GaN DHFETs. DC, small-signal, and large-signal measurements are used to demonstrate the trade-off between limiting SCE and maintaining a low dispersion. DC measurements show that higher C-doping provides low SCE. However, small signal measurements reveal similar f_T and f_{max} obtained at low bias conditions, $V_{DS} \leq 10$ V, whereas for large fields $V_{DS} > 10$ V dispersion effects dominate over SCE, rendering lower f_{max} for high C-doping. Dispersion dominating over SCE is further confirmed through large-signal measurements, manifesting a general trend of worse power scaling and lower PAE for HEMTs with higher C-doping in the back-barrier. The dispersion correlated well to C-doping profile obtained from SIMS, revealing that small variations in a trailing profile from back-barrier into the channel region can cause considerable differences in dispersive behavior at low fields $V_{DS} \leq 10$ V.

PIV measurements demonstrate a strong drain-dependency (most notable for High-C) of the current collapse and dynamic R_{on} which would be expected of C-trapping located in the back-barrier. Additionally, PIV further confirms that the nominal deviation of the trailing carbon profile into the channel region leads to considerable trapping for High-C and Mid-C at low fields $V_{DS} \leq 10$ V. DCTS measurements showed that three trap states T1 and T2 are confirmed to be C-trap states residing in the back-barrier, whereas T3 is activated at low fields and located in the channel. Nonetheless, it demonstrates characteristics which previously have been reported to indirectly stem from carbon-doped back-barriers.

It is here shown that back-barrier effectively prevents buffer-related electron trapping. Furthermore, apart from back-barrier C-doping level, the trailing C-doping profile at the channel/back-barrier interface region is found to be important to control the optimization of microwave AlGaN/GaN DHFETs for large-signal operation.

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Paper E

Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors

D. Y. Chen, A. Malmros, M. Thorsell, H. Hjelmgren, O. Kordina, J. T. Chen, and N. Rorsman

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Microwave Performance of 'Buffer-Free' GaN-on-SiC High Electron Mobility Transistors

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***Abstract*—High performance microwave GaN-on-SiC HEMTs are demonstrated on a heterostructure without a conventional thick doped buffer. The HEMT is fabricated on a high-quality 0.25 μm unintentional doped GaN layer grown directly on a transmorphic epitaxially grown AlN nucleation layer. This approach allows the AlN-nucleation layer to act as a back-barrier, limiting short channel effects and removing buffer leakage. The devices with the 'buffer-free' heterostructure show competitive DC and RF characteristics, as benchmarked against the devices made on a commercial Fe-doped epi-wafer. Peak transconductances of 500 mS/mm and a maximum saturated drain current of ~1 A/mm are obtained. An extrinsic f_T of 70 GHz and f_{max} of 130 GHz are achieved for transistors with a gate length of 100 nm. Pulsed-IV measurements reveal a lower current slump and a smaller knee walkout. The dynamic IV performance translates to an output power of 4.1 W/mm, as measured with active load-pull at 3 GHz. These devices suggest that the 'buffer-free' concept may offer an alternative route for high frequency GaN HEMTs with less electron trapping effects.**

***Index Terms*—GaN, HEMTs, microwave, 'buffer-free' heterostructure.**

I. Introduction

GaN HEMTs are used in applications requiring high output power at high frequencies due to the large electric breakdown field and high electron velocity offered by group III-nitride heterostructures. However, RF performance is still limited by different electron trapping effects, where DC-RF dispersion and memory effect are partly caused by traps located in the buffer [1]–[3]. Traps in the buffer have been shown to cause long gain recovery time in low noise amplifiers after an input overdrive pulse [4]. Furthermore, the high frequency performance of GaN HEMTs is limited by short-channel effects, which is partly caused by poor electron confinement in the 2DEG channel. In GaN HEMT structures grown on silicon carbide, silicon, or sapphire, the buffer needs to be thick enough to minimize growth defects, due to the lattice mismatch between the substrate and the GaN [5]. Defects, extending to the channel region will affect electron mobility in the 2DEG and thus reduce HEMT performance [5], [6]. The buffer also needs to be highly insulating in order to limit leakage currents, increase breakdown voltages, and reduce short-channel effects [7]. The GaN buffer is usually rendered insulating by incorporating deep acceptors, commonly C or Fe [1], [2]. However, the deep acceptors also form electron traps, which contribute to dispersion effects. Several studies have discussed the tradeoff between dispersion and isolation [8]–[10]. One possibility to mitigate the trapping effect and sustain good isolation is a thin unintentionally doped (UID) GaN layer combined with the AlN nucleation layer acting as a back barrier. Previous attempts with a thin buffer layer exhibit two times higher threading dislocation density [11], and a degraded electron mobility [12], [13] compared to a thicker buffer.

In this letter, we present high performance microwave HEMTs fabricated on epi-structures without a conventional thick buffer layer. The 'buffer-free' concept QuanFINE (shown in Fig. 1) allows for a thin 250 nm-thick UID GaN layer grown in between an AlGaN barrier and an AlN nucleation layers without compromising the 2DEG properties. The performance of HEMTs on QuanFINE is validated in this work, as compared to HEMTs on a commercial HEMT material with a thick, Fe-doped buffer. The device characterizations include DC, pulsed-IV, high frequency s-parameters and the large signal performance with active load-pull at 3 GHz.

II. Experimental

The QuanFINE® GaN HEMT heterostructures were grown on semi-insulating SiC substrates using MOCVD by SweGaN AB. The high-quality thin GaN is enabled by the transmorphic epitaxial growth of AlN nucleation layer on SiC substrate [14]. The 60 nm thick AlN nucleation layer was grown on the SiC substrate followed by a 250 nm unintentionally doped (UID) GaN layer. The active layers nominally consist of 1 nm AlN exclusion layer, 10 nm of AlGaN barrier layer with 30 % Al content, and a 2 nm GaN cap layer. More details on the growth can be found in [14], [15]. From contactless Hall measurements (Lehighton), a 2DEG concentration of

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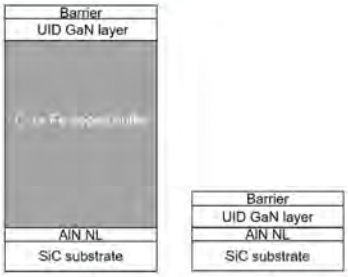

Fig. 1. The concept of (a) conventional thick buffer and (b) 'buffer-free' epi-structures.

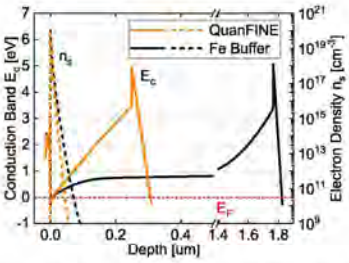

Fig. 2. Conduction band (E_C) (Line) and electron density (n_S) (dashed line) of QuanFINE and "Fe buffer" at the V_{DS} of 0 V.

$1.16 \cdot 10^{13}$ cm^{-2} and an electron mobility of 2030 cm^2/V·s were measured. These values show that the 2DEG transport properties are not compromised when significantly reducing the GaN layer thickness. HEMTs on QuanFINE are compared to transistors fabricated in the same process on a commercial epi-wafer with nominally the same barrier design, and a thick (1.8 μm) and Fe-doped buffer layer (denoted "Fe Buffer"). Fig. 2 presents the simulation result (Synopsys Sentaurus TCAD) of conduction band diagram and electron density distribution for QuanFINE and "Fe Buffer". The simulations show that the QuanFINE structure potentially offers a better 2DEG confinement.

The HEMTs processing follows the procedure described in [16]. The passivation-first devices were passivated using a 55 nm SiN layer, deposited with low pressure chemical vapor deposition (LPCVD) [17]. The device isolation was achieved through mesa etching to a depth of 220 nm. Recessed, Ta-based ohmic contacts produced contact resistances of 0.32 Ωmm and 0.28 Ωmm as extracted from TLM measurements for QuanFINE and "Fe buffer", respectively [18], [19]. HEMTs with a gate length (L_g) of 200 (100) nm, which have a source-drain distance of 2.75 (1.75) μm, and a gate-drain distance of 1.75 (0.95) μm, and a drain-side field plate of 0.25 (0.15) μm, were fabricated. The total gate width of the HEMTs characterized in this study is 2×50 μm.

III. HEMT Results

The 2DEG properties were measured after processing on van der Pauw structures. The electron densities are $1.02 \cdot 10^{13}$ cm^{-2} and $1.08 \cdot 10^{13}$ cm^{-2}, and the electron mobilities are 2000 cm^2/V·s and 2090 cm^2/V·s for QuanFINE and "Fe Buffer", respectively. These results as compared to Lehighton measurements show that the 2DEG properties are not affected by the device processing and that almost identical 2DEG properties are achieved independent on buffer design.

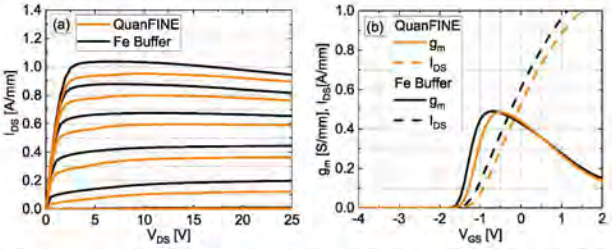

Fig. 3. DC characteristics for HEMTs with a L_g of 200 nm on both materials. (a) I_{DS} versus V_{DS} for $V_{GS} = -4 : 0.5 : 1$ V, (b) shows I_{DS} and g_m versus V_{GS} for V_{DS} of 10 V.

DC characteristics were measured with a parameter analyzer (Keithley 4200-SCS) (Fig. 3). The HEMTs on both materials exhibit a kink-free characteristics, a maximum drain-source current (I_{max}) of ~1 A/mm, and a transconductance (g_m) of ~490 mS/mm. HEMTs on "Fe Buffer" show a slightly higher maximum current which could be due to a higher mobility, a higher n_s, and a lower contact resistance. However, it shall be noticed that the difference in the maximum current between QuanFINE and "Fe Buffer" also falls in a range of our batch-to-batch variation. The breakdown voltage increases in proportion to the increase of gate-drain distance, indicating that the breakdown is largely laterally limited. HEMTs with a L_g of 200 nm on both materials show comparable catastrophic breakdown voltage of ~80 V. Short channel effects (SCEs) are characterized by drain induced barrier lowering (DIBL), defined as $|\Delta V_{TH}/\Delta V_{DS}|$ and subthreshold swing (SS) extracted from $\partial V_{GS}/\partial \log_{10}(I_{DS})$. DIBL was calculated using the pinch-off voltage (V_{po}), defined at $I_{DS} = 1$mA/mm, at $V_{DS} = 1$ V and 25 V. SS was calculated from the transfer characteristics as the minimum SS at $V_{DS} = 10$ V. HEMTs with a gate length of 200 nm on QuanFINE has a DIBL of ~13 mV/V, which is comparable to the DIBL of ~10 mV/V for the "Fe Buffer" material. The DIBL results are not in agreement with the simulations (Fig. 2) and further investigation is needed to understand the origin of the discrepancy. Furthermore, an f_T (f_{max}) of ~70 GHz (~130 GHz), were extracted from the s-parameters for the QuanFINE HEMTs. These results compare well with the HEMTs fabricated in the same process on "Fe Buffer" and thick C-doped buffer materials [16].

The pulsed-IV characteristics at different quiescent bias (V_Q) were measured on HEMTs for both materials (Fig. 4). The pulse width of 0.1 μs with the duty cycle of 0.001% were defined. The quiescent bias points (V_{GSQ},V_{DSQ}) were set at [(0,0), (−5,0), and (−5,25) V], denoted as [Q_{ref}, Q_0, and Q_{25}]. Surface (Z_1) and buffer (Z_2) related current slump were defined and calculated according to the equations 1 and 2:

$$Z_1[\%] = \frac{I_{ds}(Q_0) - I_{ds}(Q_{ref})}{I_{ds}(Q_{ref})} \cdot 100 \quad (1)$$

$$Z_2[\%] = \frac{I_{ds-knee}(Q_{25}) - I_{ds-knee}(Q_{ref})}{I_{ds-knee}(Q_{ref})} \cdot 100 \quad (2)$$

QuanFINE and "Fe Buffer" HEMTs show comparable Z_1 dispersion of ~4% due to the identical passivation layers. The "Fe Buffer" buffer exhibits higher Z_2 dispersion of 18% and 14% compared to 15% and 12% on QuanFINE on

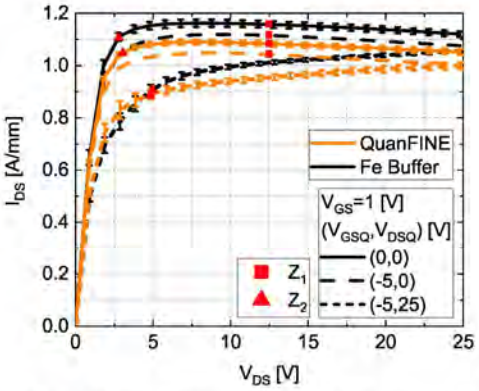

Fig. 4. Pulsed-IV measurements performed at different quiescent biases. The results were extracted from 12 randomly selected HEMTs with L_g of 100 nm on QuanFINE and "Fe Buffer" samples.

TABLE I
EXTRACTED FIGURES OF MERIT FROM DC, PULSED-IV, AND SMALL SIGNAL MEASUREMENTS

Sample	QuanFINE		"Fe Buffer"	
Gate length (nm)	200	100	200	100
$I_{DS,max}$ (A/mm)	0.95	1.06	1.04	1.14
Max g_m (mS/mm)	485	493	491	508
DIBL (mV/V)	13	50	10	40
SS (mV/dec.)	171	577	110	379
Off-state breakdown (V)	79	49	80	30
V_T (V)	-1.1	-1.5	-1.3	-1.5
R_{ON} (Q_{ref}) (Ω·mm)	1.78	1.47	1.68	1.36
R_{ON} (Q_{25}) (Ω·mm)	2.06	1.78	2.08	1.86
Dynamic R_{ON} (Increase %)	15.7	21	23.8	36.7
Z_1 (%) @V_{ds}=12.5V	3.5	4	3.5	4
Z_2 (%)	11.5	14.6	13.9	17.8
f_T (GHz)	46	71	47	73
f_{max} (GHz)	114	129	117	130

HEMTs with L_g of 100 and 200 nm, respectively. Consistently, the dynamic R_{ON} of the QuanFINE transistors is also smaller than that of "Fe Buffer". These results highlight the advantage of removing the thick Fe-doped GaN buffer layer, which inevitable leads to trapping effects [2]. The Z_2 dispersion for QuanFINE is likely caused by the background impurity in the UID GaN layer (carbon concentration of $\sim 4{\cdot}10^{16}$ cm^{-3} measured by secondary ion mass spectrometry, not shown here), threading dislocations, and/or trapping effects at the interafaces of AlN, which could be further reduced by optimizing the growth process [10].

The load-pull measurements were performed at 3 GHz with an active load-pull system [20] (Fig. 5). The transistors for both samples were biased at class-AB condition (~20% of maximum drain current). The output performance was analyzed by comparing the ideal class-A output power ($P_{out,class-A}$) defined as equation 3:

$$P_{out,class-A} = \frac{(V_{DS,max} - V_{DS,knee}) \times (I_{DS,knee} - I_{DS,off})}{8}, \quad (3)$$

where $V_{DS,max}$, $V_{DS,knee}$, $I_{DS,knee}$, and $I_{DS,off}$ are the voltages and currents at the knee- and off-region, respectively. The highest output power (P_{max}) for the device with the L_g

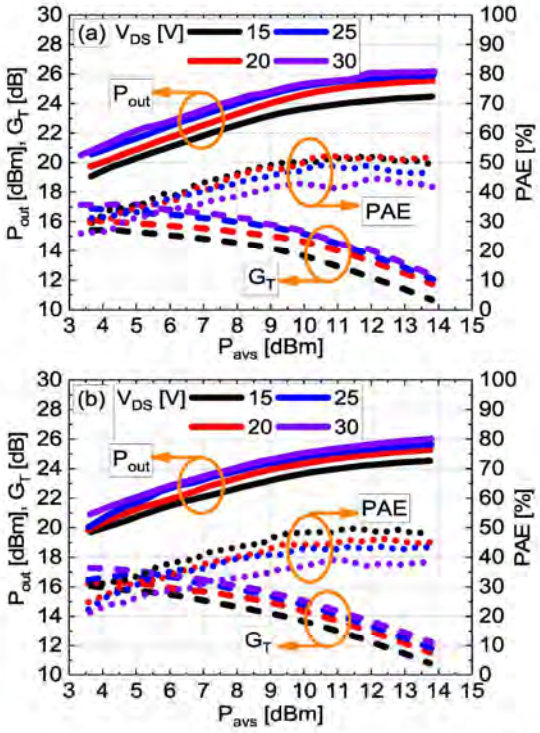

Fig. 5. 3 GHz active load-pull measurements of HEMTs with an L_g of 200 nm performed at different drain bias on (a) "Fe Buffer" and (b) QuanFINE.

of 200 nm on both materials are 4.1 W/mm at 3 GHz (Fig. 5). The similar performance is explained by the comparable values of DIBL and off-state breakdown voltage, resulting in a similar $I_{DS,off}$ and a $V_{DS,max}$. Furthermore, the higher $I_{DS,max}$ exhibited by "Fe Buffer" is compensated by the lower current slump (Z_2) of QuanFINE, which results in similar values of $I_{DS,knee}$. The highest power added efficiency (PAE) of ~50% is extracted at low drain bias of 15 V for both materials. Increasing the bias leads to a reduction of PAE to ~40% which is due to thermal effects as well as to trapping effect as discussed above in the context of the pulsed-IV.

IV. CONCLUSION

This study investigates a 'buffer-free' concept (QuanFINE) of GaN HEMT heterostructures without a conventional thick, doped buffer for microwave applications. The new concept with a total thickness of the GaN layer of 250 nm does not compromise the crystal quality as revealed by similar 2DEG mobility compared to a standard HEMT-structure with a thick Fe-doped buffer. Physical simulations (TCAD) indicate that the QuanFINE could be favorable for improved electron confinement. The pulsed-IV measurements demonstrate an advantage of the QuanFINE concept, which shows a lower buffer-induced dispersion compared to the conventional thick, Fe-doped buffer. The large signal measurements demonstrate the QuanFINE concept can provide a competitive output power levels and efficiency. Further studies of the carbon impurity and the thickness of the UID GaN layer, are anticipated to further improve the 'buffer-free' QuanFINE.

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Paper F

Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructures

D.-Y. Chen, K.-H. Wen, M. Thorsell, M. Lorenzini, H. Hjelmgren, J.-T. Chen, and N. Rorsman

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RESEARCH ARTICLE

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Impact of the Channel Thickness on Electron Confinement in MOCVD-Grown High Breakdown Buffer-Free AlGaN/GaN Heterostructures

Ding-Yuan Chen, Kai-Hsin Wen, Mattias Thorsell, Martino Lorenzini, Hans Hjelmgren, Jr-Tai Chen, and Niklas Rorsman*

The 2D electron gas (2DEG) confinement on high electron mobility transistor (HEMT) heterostructures with a thin undoped GaN channel layer on the top of a grain-boundary-free AlN nucleation layer is studied. This is the first time demonstration of a buffer-free epi-structure grown with metal–organic chemical vapor deposition with thin GaN channel thicknesses, ranging from 250 to 150 nm, without any degradation of the structural quality and 2DEG properties. The HEMTs with a gate length of 70 nm exhibit good DC characteristics with peak transconductances of 500 mS mm^{-1} and maximum saturated drain currents above 1 A mm^{-1}. A thinner GaN channel layer improves 2DEG confinement because of the enhanced effectiveness of the AlN nucleation layer acting as a back-barrier. An excellent drain-induced barrier lowering of only 20 mV V^{-1} at a V_{DS} of 25 V and an outstanding critical electric field of 0.95 MV cm^{-1} are demonstrated. Good large-signal performance at 28 GHz with output power levels of 2.0 and 3.2 W mm^{-1} and associated power-added efficiencies of 56% and 40% are obtained at a V_{DS} of 15 and 25 V, respectively. These results demonstrate the potential of sub-100 nm gate length HEMTs on a buffer-free GaN-on-SiC heterostructure.

1. Introduction

GaN high electron mobility transistors (HEMTs) play an important role in applications requiring high power at high frequencies due to high electron mobility and velocity in combination with a large critical electric field. However, the performance is still limited by trapping effects and poor 2D electron gas (2DEG) confinement.[1–3] In conventional GaN HEMT structures grown on SiC or Si, the GaN buffer needs to be thick enough to minimize growth defects, caused by the lattice mismatch between the GaN and the substrates.[4,5] As-grown GaN buffer has a low resistivity, which requires deep acceptors doping, most commonly C or Fe, to ensure buffer insulation, high breakdown voltage, and reduced short channel effects.[6,7] However, the intentional acceptors also act as electron traps, contributing to DC–radio-frequency (RF) current dispersion.[1] To achieve good channel confinement in highly scaled HEMTs, the acceptor doping level has to be sufficiently high close to the channel, which leads to a further increase in trapping effects.[1,7,8] Another common approach is the introduction of a back-barrier, most commonly AlGaN or InGaN, which utilizes band structure engineering to improve 2DEG confinement.[9,10] However, acceptor dopants are still required to compensate for the unintentional background doping and mitigate parasitic channels beneath the back-barrier.[11,12]

To counter these limitations, the buffer-free concept of thin GaN channel epi-structure without thick Fe-/C-doped GaN buffer was proposed,[13,14] in which the AlN nucleation layer acts as a back-barrier.[14,15] However, the growth of such thin GaN channel with high structural quality and good 2DEG properties directly on the AlN nucleation layer with metal–organic chemical vapor deposition (MOCVD) is challenging. We have previously reported an electron mobility (μ) of 2030 cm^2 V^{-1} s^{-1}.[14,15] Similarly, Zhang et al.[16] and Narang et al.[17] have reported high μ's of 2238 and 1850 cm^2 V^{-1} s^{-1} with an MOCVD grown GaN channel thickness of 250 and 200 nm, respectively. For the highly down-scaled devices, further reduction of the GaN channel thickness is necessary to ensure desired 2DEG confinement.[11,15] However, a degradation of μ (1100 cm^2 V^{-1} s^{-1}) was reported with GaN channel thicknesses thinner than 200 nm due to poor structural quality.[18]

In this article, we demonstrate highly scaled GaN HEMTs fabricated on a QuanFINE heterostructure with reduced GaN channel thickness down to 150 nm. Apart from DC, pulsed-IV, and high-frequency small-signal characterizations, measurements of the large-signal microwave performance are demonstrated with active load-pull at 28 GHz.

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2. Experimental Section

Three AlGaN/GaN HEMT heterostructures with a thin GaN channel of 150, 200, and 250 nm (denoted as QF150, QF200, and QF250, respectively, in the following discussion) were grown on a 60 nm AlN nucleation layer with MOCVD by SweGaN AB.[13] The high structural quality of the thin GaN channel layers was confirmed by the full width at half maximum (FWHM) of the X-ray diffraction (XRD) rocking curve on the GaN (002) and (102) planes (**Table 1**). Further reduction of GaN channel thickness was under development to fulfill the desired GaN crystal structural quality with low FWHM. The barrier consists of a 1 nm AlN exclusion layer, 10 nm of AlGaN with 30% Al content, and a 2 nm GaN cap layer (**Figure 1**a). The 2DEG concentrations (n_s), μ, and sheet resistance (R_{sh}) were measured with contactless Hall (Lehighton) and Eddy current measurements (Table 1). The trend of decreasing 2DEG concentration with thinner GaN may due to the narrower quantum well, which potentially has less available energy states. This behavior had also been found in epi-structure with an additional back-barrier.[11,19] Moreover, these values showed that although the GaN layer was around 10 times thinner than conventional GaN buffers for AlGaN/GaN HEMTs on SiC, there was no apparent degradation of the 2DEG properties.[15] Technology computer aided design (TCAD) (Synopsys Sentaurus) was used to simulate the conduction band (E_c) and electron density (n_s) distribution for QF150, QF200, and QF250 (Figure 1b). The estimated n_s of QF150, QF200, and QF250 are 1.02, 1.06, and 1.08×10^{13} cm^{-2}, respectively, by integrating over the entire simulated depth. Indicatively, QF150 exhibited better electron confinement as a result of the larger slope of the conduction band.

For the HEMTs fabrication, a "passivation-first" process scheme was applied with an in situ NH_3 pretreatment, to reduce surface native oxide and minimize surface-related trapping effects,[20] followed by a deposition of 60 nm SiN passivation layer with low-pressure chemical vapor deposition. The device isolation was achieved through mesa etching with a depth of ≈120 nm below 2DEG. Recessed and Ta-based ohmic contacts produced contact resistances of ≈0.3 Ω mm as extracted from transmission line measurements for all samples.[21–23] HEMTs with gate lengths (L_g) of 40, 70, 100, 150, and 200 nm, a gate-source distance (L_{GS}) of 1 μm, gate-drain distances (L_{GD}) of 1 and 2.5 μm, and a gate width of 2×50 um were fabricated. The dimensions were verified with a scanning electron microscope. To reduce parasitic capacitance for high-frequency operation and allow for studies of trapping effects, there were no source-connected field-plate on these devices (Figure 1a).

Table 1. FWHM from XRD rocking curves and 2DEG properties of QF150, QF200, and QF250 before and after HEMT processing.

	QF150	QF200	QF250
GaN (002) ["]	72	83	60
GaN (102) ["]	312	340	315
2DEG properties before (and after) processing			
n_s [10^{13} cm^{-2}]	0.91 (1.00)	0.94 (1.01)	0.98 (1.05)
μ [cm^2 V^{-1} s^{-1}]	2210 (1970)	2150 (1940)	2110 (1870)
R_{sh} [Ω sq.$^{-1}$]	315 (317)	320 (318)	303 (318)

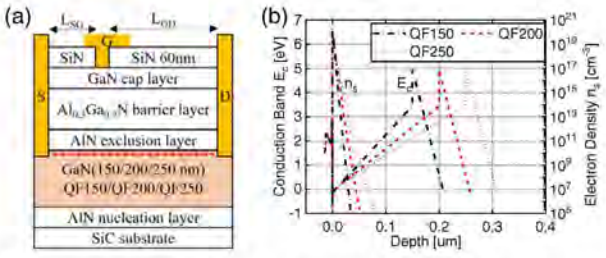

Figure 1. a) Cross section of the GaN HEMTs with standard field-plate gates on QuanFINE, b) simulated E_c and n_s of QF150, QF200, and QF250.

3. HEMT Results

3.1. Hall Characterization

The 2DEG properties were also measured on van der Pauw structures after processing (Table 1). There is no apparent sign of degradation of the 2DEG properties after processing. A small modification of 2DEG concentrations and electron mobilities may be the result of an additional compressive strain, which is induced by the SiN passivation layer.[24,25]

3.2. DC Characterization

The DC characteristics were measured on three randomly selected HEMTs of each L_g on each epi-structure with a parameter analyzer (Keysight B1500A). The HEMTs exhibit average source-drain currents (I_{DS}) above 1 A mm^{-1} at a gate-source voltage (V_{GS}) of 1 V. A higher I_{DS} for all HEMTs manufactured on QF250 can be explained by the higher n_s compared to QF200 and QF150 (**Figure 2**a). The highest extrinsic transconductance (g_m) of 500 mS mm^{-1} was measured for the devices with L_g of 70 nm on QF150. Large degradation of g_m was revealed on the devices with L_g of 40 nm, which is mainly due to short channel effects (Figure 2b,c).

Drain-induced barrier lowering (DIBL) was calculated from the following equation

$$DIBL = \frac{\left|V_{po}^{high} - V_{po}^{low}\right|}{\left|V_{DS}^{high} - V_{DS}^{low}\right|} \quad (1)$$

using the pinch-off voltage (V_{po}) at $V_{DS} = 1$ and 25 V with the pinch-off criteria $I_{DS} = 1$ mA mm^{-1}. Compared to conventional heterostructures for highly scaled device (**Table 2**), QF150 shows an outstanding 2DEG confinement with a DIBL of 20 mV V^{-1} for the HEMTs with an L_g of 70 nm (Figure 2c,d). Further reduction of GaN channel thickness (<150 nm) will further reduce the DIBL for the HEMTs with an L_g of 70 nm, which can be estimated from Figure 2c. QF200 and QF250 exhibit a higher DIBL of 54 and 157 mV V^{-1}, respectively (Figure 2c,e,f), which is in agreement with the trend of g_m. These results confirm a better 2DEG confinement on QF150 as indicated in Figure 1b.

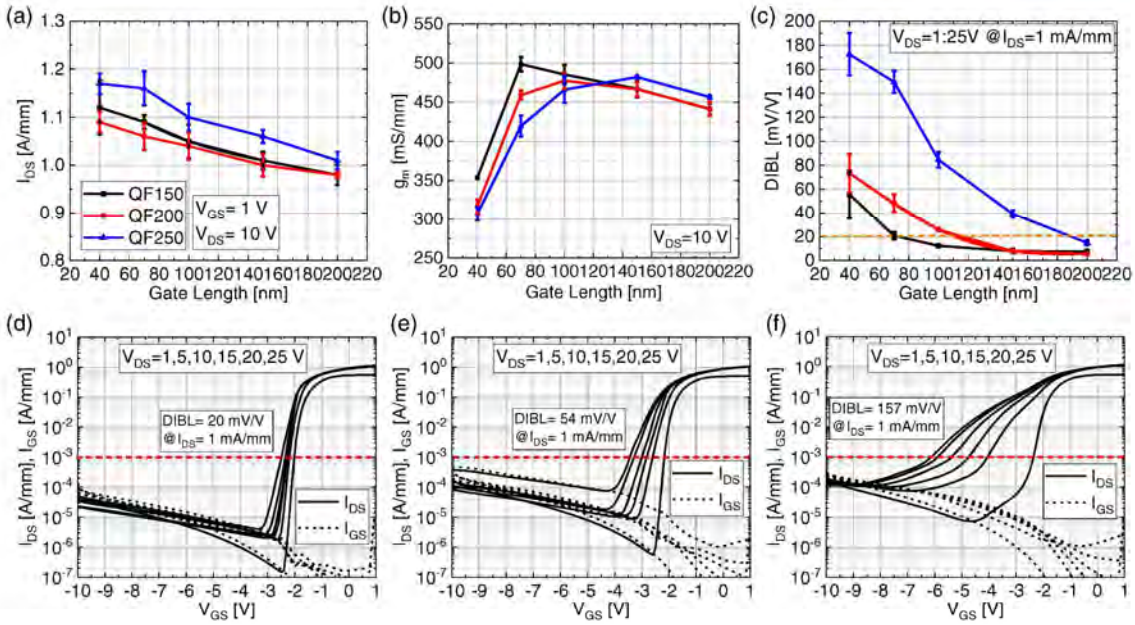

Figure 2. Average DC results on HEMTs with L_{GD} of 2.5 µm, a) I_{DS}, b) peak g_m, c) DIBL, and transfer characteristics of a typical HEMT with an L_g of 70 nm on d) QF150, e) QF200, and f) QF250.

The mesa isolation of each epi-structure was measured at separated pads of 15 µm at 200 V (**Table 3**). All samples show a similar mesa isolation resistance due to the similar remained epi-structure (GaN channel, AlN nucleation layer, and SiC substrate) after mesa recess etching.

The breakdown characteristics were measured on HEMTs with L_g of 40, 70, and 100 nm and L_{GD} of 1 µm on each epi-structure with the V_{GS} of −10 V and breakdown criterion of 1 mA mm^{-1}. This approach ensures identical depletion strength underneath the gate. A thinner GaN channel thickness and a larger L_g lead to a higher breakdown voltage (V_{BR}). An excellent critical electric field of 0.95 MV cm^{-1} was achieved on HEMT with an L_g of 100 nm on QF150. These results promote efficient power amplification with reduced L_{GD}.[30]

Table 2. Benchmark of DIBL in literature.

Barrier	Buffer	L_g [nm]	DIBL [mV V^{-1}]	References
AlGaN	QF150	70	20	This work
AlGaN	QF150	100	11	This work
AlGaN	Back-barrier	100	11	[26]
AlGaN	Proprietary thick buffer	150	2	[27]
AlN	C-doped thick buffer	120	131	[28]
AlN	Back-barrier	120	62	[28]
AlN	Back-barrier	140	39	[29]

Table 3. Mesa isolation resistance and breakdown performance of HEMTs with an L_g of 40, 70, and 100 nm with L_{GD} of 1 µm.

	QF150	QF200	QF250
Mesa isolation [10^9 Ω]	317	327	337
V_{BR}-L_g 40 nm [V]	67	50	37
V_{BR}-L_g 70 nm [V]	83	63	50
V_{BR}-L_g 100 nm [V]	95	70	52

3.3. Pulsed IV

The pulsed-IV characteristics at different quiescent biases were measured on three randomly selected devices with an L_g of 70 nm and L_{GD} of 1 µm on each epi-structure (**Figure 3**). The pulse width was 1 µs with a duty cycle of 0.001%. The quiescent bias points (V_{GSQ}, V_{DSQ}) were set at [(0, 0), (V_{po}−3, 0), (V_{po}−3, 20), and (V_{po}−3, 25) V], denoted as [Q_{ref}, Q_0, Q_{20}, and Q_{25}]. $I_{ds\text{-}knee}$ is defined at the knee where RF load-line is swinged of each I_{DS} curve, marked with black dots in Figure 3. Surface (Z_1) and buffer (Z_2)-related current collapse were calculated according to the following equations

$$Z_1[\%] = \left| \frac{I_{ds-knee}(Q_0) - I_{ds-knee}(Q_{ref})}{I_{ds-knee}(Q_{ref})} \right| \cdot 100 \quad (2)$$

$$Z_2[\%] = \left| \frac{I_{ds-knee}(Q_{20,25}) - I_{ds-knee}(Q_{ref})}{I_{ds-knee}(Q_{ref})} \right| \cdot 100 \quad (3)$$

QF200 shows the highest Z_1 and Z_2 dispersion (Figure 3d), and dynamic R_{on} degradation (**Table 4**) due to the lower structural quality (Table 1) compared to that of QF150 and QF250. This result indicates that high structure quality is critical for buffer-free heterostructure. Under a similar structure quality

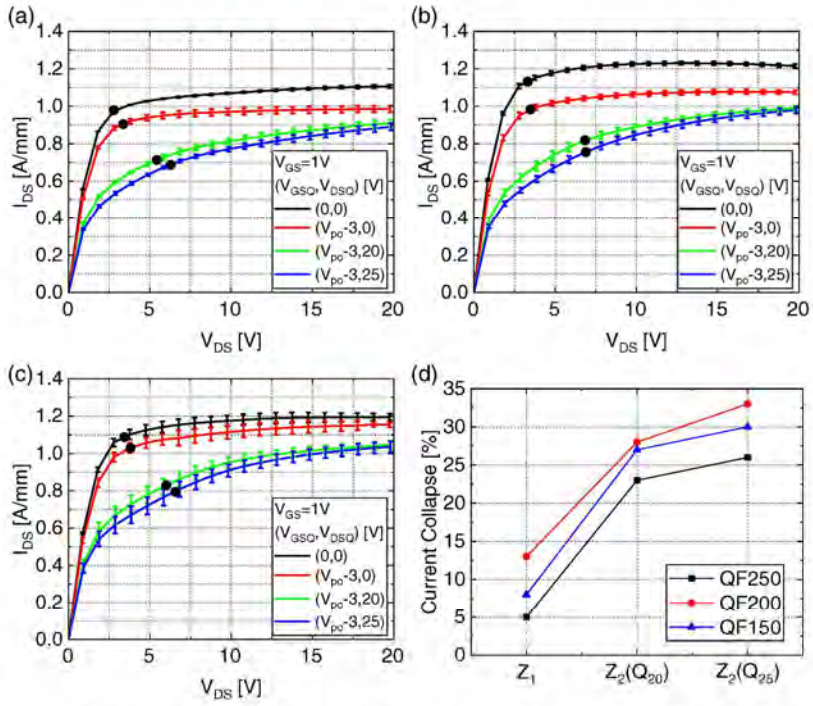

Figure 3. Pulse-IV measurements on a) QF150, b) QF200, and c) QF250. d) Summary of current collapse on each epi-structure.

Table 4. Extraction figure of merit from pulsed IV measurements.

	QF150	QF200	QF250
R_{on} (Q_{ref}) [Ω mm]	1.58	1.43	1.53
R_{on} (Q_{25}) [Ω mm]	2.73	2.61	2.37
Dynamic R_{on} [Increase %]	72	82	55

(Table 1), QF150 exhibits a higher Z_1 and Z_2 compared to QF250. Consistently, the dynamic R_{on} of QF150 is also higher than that of QF250 (Table 4). This phenomenon is likely caused by a thinner GaN channel thickness in QF150, which allows more traps to be filled easier at the interface of GaN/AlN nucleation layer (possibility of 2D hole gas)[31] or semi-insulating SiC substrate (long time constant traps such as Vanadium dopants or intrinsic point defects).[32,33] Higher trapping effects in QF150 can also be correlated to higher breakdown performance, since semi-insulating SiC substrate can be considered like a "high resistivity GaN buffer doped with acceptors in conventional high breakdown epi-structure for power HEMTs" in buffer-free heterostructure (Table 3).

3.4. S-Parameters

The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were extracted from 145 GHz s-parameters measurements (Anritsu ME7838A) on four randomly selected devices with an L_g of 70 nm and L_{GD} of 1 µm on each epi-structure. Average equivalent circuit parameters of small-signal model, including gate-drain (C_{gd}), gate-source (C_{gs}), drain-source (C_{ds}) capacitance, input resistance (R_i), output resistance (R_{ds}), and transconductance (g_m) were extracted on same devices by a direct extraction method (**Table 5**).[34] f_T/f_{max} are similar on all structures due to a simultaneous increase in C_{gs} and g_m. Without an advanced mushroom gate in this work, f_T/f_{max} is limited below 120 GHz due to a large parasitic capacitance. The higher C_{gs}, R_{ds},

Table 5. Small-Signal equivalent circuit parameters, f_T, f_{max}, and large-signal performance of HEMTs with an L_g of 70 nm.

	QF150	QF200	QF250
C_{gd} [fF]	7	7	8
R_i [Ω]	15	15	15
C_{gs} [fF]	109	103	95
R_{ds} [Ω]	470	435	401
C_{ds} [fF]	25	25	28
g_m [mS]	58	54	52
f_T [GHz]	86	76	74
f_{max} [GHz]	111	103	101
$P_{out,\ 3\,dB}$ [W mm^{-1}]	2.0	2.3	3.3
$P_{out,\ max}$ [W mm^{-1}]	2.8	2.6	3.6
Linear gain [dB]	13.8	10.9	7.7
PAE_{max} [%]	47	43	42
PAE @ $P_{out,\ max}$ [%]	44	42	38

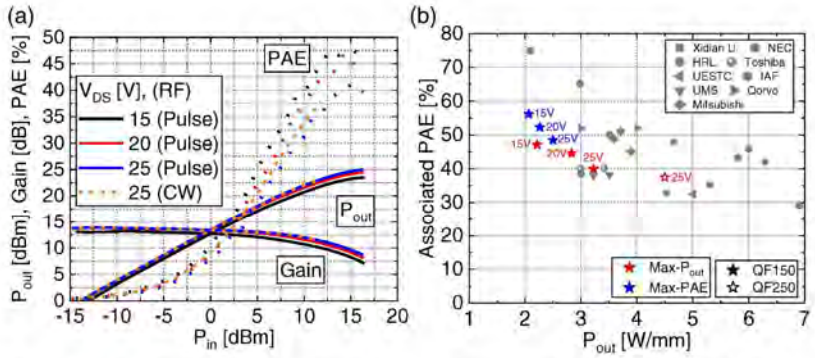

Figure 4. a) Power sweep at different V_{DS} on QF150. b) Benchmark of P_{out} and associated PAE with $Al_xGa_{(1-x)}N$/GaN-based devices ($x \leq 0.3$) with Schottky gate operated at 28–31 GHz.[38–47]

and g_m in QF150 can be correlated to better 2DEG confinement (Figure 1b and 2c).

3.5. High-Frequency Large Signal Performance

The load-pull measurements were performed on three randomly selected HEMTs on each epi-structure with L_g of 70 nm and L_{GD} of 1 µm at 28 GHz in an active load-pull system (MT2000) by Anteverta Maury.[35,36] The HEMTs were biased (unpulsed) at an $I_{DSQ} = 100\,mA\,mm^{-1}$ (class-AB). The power sweeps were performed both under continuous wave (CW) and pulsed conditions. The pulse width was 50 µs with a duty cycle of 10%. The CW measurements were limited to a maximum output power level of 24 dBm due to a limitation of power capability in the bias-tee. The RF performance of HEMTs showed no difference between CW- and pulse-RF modes up to an output power (P_{out}) of 23.5 dBm at $V_{DS} = 25$ V (**Figure 4a**), which might be due to an efficient heat spreading in QuanFINE structures.[37] The large signal performance is analyzed at $V_{DS} = 20$ V (Table 5) by comparing the ideal class-A $P_{out,max}$ defined as the following equation

$$P_{out,\,max} = \frac{(V_{DS,max} - V_{DS,knee}) \times (I_{DS,knee} - I_{DS,off})}{8} \quad (4)$$

where $V_{DS,max}$, $V_{DS,knee}$, $I_{DS,knee}$, and $I_{DS,off}$ are the voltages and currents at the knee- and off-region, respectively. The highest $P_{out,\,max}$ of $3.6\,W\,mm^{-1}$ was demonstrated on QF250, which can be correlated to higher I_{DS} (Figure 1a) and lower trapping effects (Figure 3d). QF150 and QF200 shows a lower $P_{out,\,max}$ of 2.8 and $2.6\,W\,mm^{-1}$, respectively. This is due to lower I_{DS} (Figure 1a) and higher trapping effects, which results in lower value of $I_{DS\text{-}knee}$. Due to a larger current collapse and knee walk-out on device without source-connected field plate, the impact of short channel effects on $V_{DS,max}$ and $I_{DS,\,off}$ is of less importance. The higher linear gain and power-added efficiency (PAE) on QF150 can be explained by higher g_m (Figure 1b) and lower DIBL (Figure 1c). In Figure 4a, good high-frequency performance with a linear gain of 14 dB, a P_{out} of 25 dBm ($3.2\,W\,mm^{-1}$), and an associated PAE of 40% were measured at 25 V. Reducing the V_{DS} to 15 V increases the peak PAE to 48%. A P_{out} of 3.2 and $4.8\,W\,mm^{-1}$ at $V_{DS} = 25$ V can be achieved on QF150 and QF250, respectively. A PAE of 56% with an associated P_{out} of $2\,W\,mm^{-1}$ at 15 V was achieved with tuning for maximum PAE on QF150. The buffer-free heterostructures were compared with conventional epi-structures (intentional acceptor dopants or additional back-barrier) at 28–31 GHz with various L_g (25–200 nm), and the load impedance was tuned for both maximum P_{out} and PAE (Figure 4b). Compared to Hughes Research Laboratories (HRL's) results ($L_g < 50$ nm), a higher PAE can be foreseen with advanced mushroom gate, shorter source-drain distance, and regrowth of n-GaN contacts. Compared to Xidian U's results with a higher P_{out} and similar PAE, optimization of surface passivation layer can further improve the P_{out}. Therefore, the benchmark results of the QuanFINE concept show high potential for high-frequency applications, especially of high-efficiency operations.

4. Conclusion

This study assessed the electron confinement properties in highly scaled AlGaN/GaN HEMTs on the buffer-free heterostructures with different undoped GaN channel thicknesses. Thin GaN channel with a thickness of 150 nm can be grown without degradation of the structural qualities and 2DEG properties. TCAD simulation, DIBL, and small-signal measurements show significant improvement of 2DEG confinement with a thin (150 nm) channel layer. This is the first demonstration that an excellent DIBL of $20\,mV\,V^{-1}$ at $V_{DS} = 25$ V on HEMTs with an L_g of 70 nm can be achieved on AlGaN/GaN epi-structures without intentional dopants or back-barrier. Moreover, QuanFINE with an outstanding critical electric field ($0.95\,MV\,cm^{-1}$) provides the possibility of reduced L_{GD}, resulting an efficient power amplification capability. With an improved 2DEG confinement, good large signal performance with higher gain and efficiency was demonstrated at 28 GHz. The benchmarking results confirm that the buffer-free GaN-on-SiC heterostructures with a thin GaN channel layer can be well suited for high-frequency applications.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

breakdown, GaN, HEMT, microwave, QuanFINE

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Paper G

Investigation and Mitigation of Trapping Mechanisms in Buffer-Free AlGaN/GaN HEMTs

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Investigation and Mitigation of Trapping Mechanisms in Buffer-Free AlGaN/GaN HEMTs

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***Abstract*—This study investigates a strategy to mitigate the trapping in buffer-free AlGaN/GaN HEMTs. A standard buffer-free AlGaN/GaN epi-structure is compared to a structure where the interface between the GaN channel and the AlN nucleation layer is doped with Si delta doping to engineer the band structure and to provide leakage path for trapped electrons. The epi-structures exhibit similar 2DEG properties (mobility and electron density) and crystal quality. Saturation currents of approximately 0.75 A/mm and transconductances of around 440 mS/mm are demonstrated on fabricated HEMTs. A lower buffer-related current collapse is demonstrated on the epi-structure with band structure engineering (20% compared to 27%). Drain current transient measurements indicate that the modified epi-structure effectively mitigates trap states with long time constants and improves the recovery speed of drain current. However, the devices on the novel epi-structure exhibits a larger drain-source leakage, suggesting a reduced buffer resistance, which result in a slightly higher DIBL (34 mV/V compared to 17 mV/V). These findings highlight the potential to mitigate trapping effects and facilitates improved performance of buffer-free AlGaN/GaN HEMTs under large-signal operation in microwave applications.**

***Index Terms*— QuanFINE, GaN HEMTs, Microwave, Trapping, Memory effects.**

I. Introduction

Gallium nitride high electron mobility transistors (GaN HEMTs) exhibit excellent properties for high-frequency applications with high power density due to their exceptional electron mobility, saturation velocity, and high critical electric field. However, the large-signal performance remains constrained by trapping phenomena, such as current collapse, degradation of dynamic on-resistance (R_{on}), and drain current memory effects. These trap states are predominantly found in the surface layers [1] and within the buffer layers [2].

Surface trap states, including native oxides and dangling bonds, can be mitigated through optimized surface pre-treatments and the application of passivation layers [3, 4]. In contrast, mitigating electron trapping in the buffer presents a more intricate challenge due to the inherent trade-off between trapping effects and electron confinement [2].

Unintentionally doped GaN buffers grown with Metal Organic Chemical Vapor Deposition (MOCVD), without intentional doping, exhibit n-type conductivity as a result of unintentional dopants, primarily oxygen on nitrogen sites (O_N) and silicon (Si) on gallium sites (Si_{Ga}) [5]. Therefore, intentional introduction of deep acceptors, such as iron (Fe) and carbon (C), is a common approach to achieve insulating properties [6, 7]. However, the incorporation of deep acceptors gives rise to the formation of electron traps, resulting in DC-RF current dispersion. Therefore, optimizing the doping profiles of Fe and C becomes essential [8, 9]. An alternative approach involves the incorporation of an additional AlGaN back-barrier to enhance 2DEG confinement. However, the introduction of a back-barrier introduces extra thermal resistance, which can degrade device performance [10] and also require optimization of the deep level doping [11].

We have previously demonstrated an innovative approach aimed at mitigating the aforementioned issues, which involves the complete removal of GaN buffers and back-barriers by the utilization of a transmorphically-grown AlN nucleation layer resulting in a high quality buffer-free epitaxial structure [12, 13]. This strategy results in the creation of a thin, undoped GaN channel sandwiched between the barrier and the nucleation layers, effectively forming a back-barrier enhancing the 2DEG confinement [14]. Despite the high structural quality and the absence of a doped GaN buffer, this buffer-free approach is not entirely free of trapping effects [12-14]. This occurrence may be attributed to a two-dimensional hole gas (2DHG) formation or defects due to lattice mismatch at the interface of GaN channel and the AlN nucleation layer [15-17], and the presence of trap states within the AlN nucleation layer [18, 19]. Furthermore, the semi-insulating SiC substrate, achieved by vanadium dopants or high-density point defects, may also present potential trapping location, given its proximity to the 2DEG channel [20, 21].

In this study, we investigate the trapping effects in two different buffer-free AlGaN/GaN HEMTs, a standard buffer-free (QF-A) epi-structure and the other one with a band-structure engineering interface between GaN channel and AlN nucleation layer (QF-B). HEMTs were fabricated on both HEMT structures and characterized. DC and pulsed-IV characterizations were complemented with drain current transient (DCT) measurements at varying temperatures and filling time durations to gain insights into the dynamic trapping and de-trapping behavior [22].

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II. Experimental

Two AlGaN/GaN HEMT epi-structures with a thin GaN channel of 250 nm (QF-A and QF-B), were grown on a 60 nm AlN nucleation layer using MOCVD by SweGaN AB (Fig. 1a) [13]. The barrier layers nominally comprise a 1 nm AlN exclusion layer, followed by 10 nm of AlGaN containing 30% Al content, and a 2 nm GaN cap layer. Compared to QF-A, QF-B features band structure engineering, incorporating a 2 nm-thick GaN layer with Si delta-doping to modify the Fermi level at the interface between the GaN and the AlN nucleation layer. The Si doping concentration is 3×10^{18} cm^{-3}, as measured by secondary ion mass spectrometry (SIMS). The structural quality of both epi-structures was characterized by the full width at half maximum (FWHM) of the X-ray diffraction (XRD) rocking curve on the (002) and (102) GaN planes (Table I). The slightly higher FWHM observed in QF-B can be attributed to modifications at the interface between the GaN channel and the AlN nucleation layer (due to the Si delta-doping in the GaN layer). The properties of the 2DEG, electron concentration (n_s) and electron mobility (μ, were determined using contactless Hall effect measurements (Lehighton) and Eddy current measurements (Table I). The slight reduction in μ observed in QF-B is primarily attributed to electron scattering resulting from the lower structural quality. TCAD (Synopsys Sentaurus) was used to simulate the conduction band (E_c) and valance band (E_v) for QF-A and QF-B (Fig. 1b). QF-A exhibited a peak in the valence band above the Fermi level, leading to the formation of a two-dimensional hole gas (2DHG). In contrast, the introduction of Si delta-doping at the interface between the GaN and AlN nucleation layers in QF-B resulted in a reduced slope of both the conduction band (E_c) and valence band (E_v). This modification led to a decrease in the 2DHG density from ~$2.5 \cdot 10^{13}$ to ~$8 \cdot 10^{12}$ cm^{-2} at the GaN/AlN interface in QF-B according to the simulation.

TABLE I
FWHM from XRD Rocking Curves and 2DEG Properties of QF-A and QF-B Before and After HEMT Processing.

	QF-A	QF-B
GaN (002) [arcsec]	122	216
GaN (102) [arcsec]	336	443
2DEG properties before (and after) processing		
n_s [10^{13}cm^{-2}]	1.06 (1.02)	1.07 (1.00)
μ [cm^2/Vs]	2057 (2002)	1966 (1911)
R_{sh} [Ω/sq.]	286 (306)	298 (327)

After the initial preparation of the samples, an in-situ NH_3 pretreatment was employed to minimize surface-related trapping effects followed by a 60 nm SiN passivation layer using low-pressure chemical vapor deposition (LPCVD) [3]. The isolation of the HEMTs was then implemented through mesa etching reaching approximately 120 nm below the 2DEG. A contact resistance of ≈0.3 Ω·mm, determined via transmission line measurements (TLM), was achieved on both epi-structures, through low annealing temperature Ta/Al/Ta recessed sidewall ohmic contacts [23]. The fabricated HEMTs featured a gate length (L_g) of 0.2 µm, a gate-source distance (L_{GS}) of 0.9 µm, a gate-drain distance (L_{GD}) of 2.2 µm, a field plate on the source side of 0.1 µm, a field plate on the drain side of 0.2 µm, and a total gate width (W_G) of 2×50 µm. No additional source-connected field-plate structures were utilized, since these may decrease the electron trapping effects that are to be characterized in this work (Fig. 1a). After the HEMT fabrication, the properties of the 2DEG were confirmed through Hall measurements on van der Pauw structures (Table I). A reduction in 2DEG n_s and μ was observed in both epi-structures, which could be attributed to an additional compressive strain (-200 to 0 MPa) induced by the Si-rich SiN passivation layer [24].

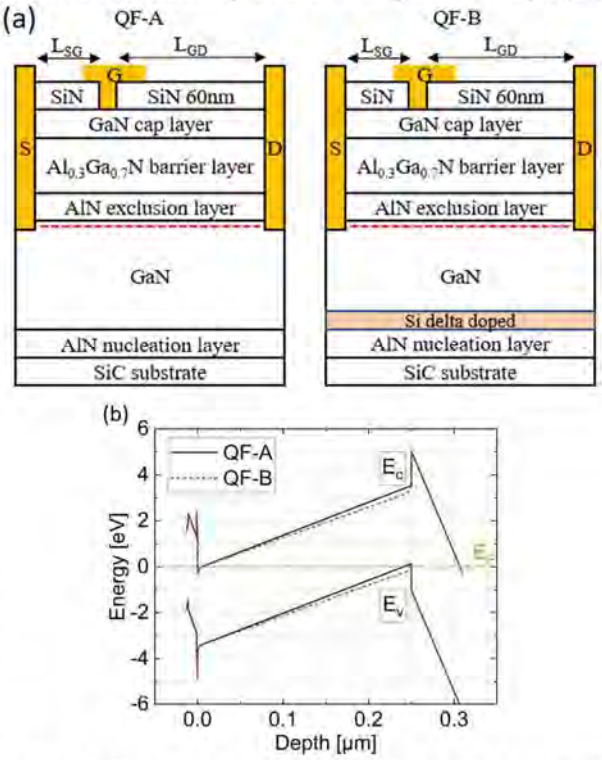

Fig. 1. (a) The concept of epi-structures in this work. (b) E_c and E_v of QF-A and QF-B.

III. Results

A. DC

The DC characteristics were evaluated by measuring three randomly selected HEMTs on each epi-structure using a parameter analyzer (Keysight B1500A) (Fig. 2 and Table II). No discernible kink effects were observed in the DC-IV characteristics of both epi-structures. Drain-source currents (I_{DS}) of 0.82 and 0.73 A/mm were measured at a gate-source voltage (V_{GS}) of 1 V, along with on-resistance (R_{on}) of 1.9 and 2.1 Ω·mm on QF-A and QF-B, respectively. The higher I_{DS} and lower R_{on} observed in QF-A can be partially attributed to the enhanced properties of the 2DEG and a threshold voltage (V_{TH}) shift of approximately 0.15 V. This V_{TH} shift may be the result of minor variations in the barrier thickness. A slightly higher g_m of 450 mS/mm in QF-A, compared to 423 mS/mm in QF-B, may be attributed to the higher mobility of the 2DEG (Table I), improved 2DEG confinement (Fig. 2e and 2f), reduced leakage currents, and enhanced pinch-off characteristics in the sub-threshold region. Short channel effects were assessed using the drain-induced barrier lowering DIBL = $\left|V_{po}^{high} - V_{po}^{low}\right| / \left|V_{DS}^{high} - V_{DS}^{low}\right|$, where the shift in the pinch-off voltage (V_{po}) at different drain-source voltages (V_{DS}^{low} = 1 V and V_{DS}^{high} = 25 V) are considered. The pinch-off criteria for this calculation were

set at an I_{DS} of 1 mA/mm. QF-A demonstrates better 2DEG confinement, with a DIBL of 17 mV/V compared to 34 mV/V for QF-B. Furthermore, the off-state leakage current in QF-B is one order of magnitude higher than that in QF-A (Table II). The mesa isolation measurements were performed on isolated contacts with a 15 µm separation and a bias voltage of 200 V. QF-B exhibits a three order of magnitudes lower mesa isolation resistance as compared to QF-A (Table II) [25]. The lower resistivity and higher off-state leakage are apparently due to the modification done in QF-B structure, indicating a non-optimum Si doping concentration and thickness.

TABLE II
SUMMARIZED AVERAGE DC PARAMETERS FOR QF-A AND QF-B.

	QF-A	QF-B
$I_{DS\text{-}max}$ [A/mm]	0.82	0.73
g_m [mS/mm]	450	423
V_{TH} [V]	-1.15	-1.00
DIBL [mV/V]	17	34
R_{on} [Ωmm]	1.92	2.06
Off-state leakage current I_{DS} [A/mm]	1E-5	1E-4
Mesa isolation resistance [10^9 Ω]	208	0.230

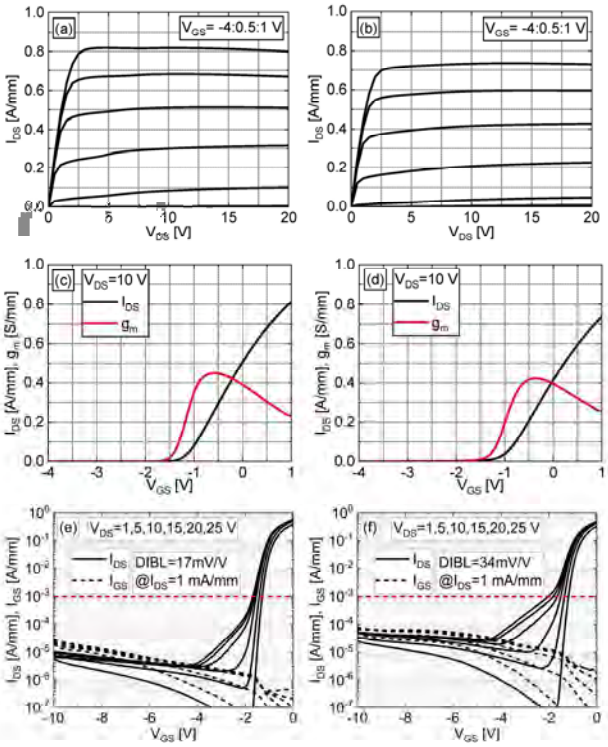

Fig. 2. DC I-V measurements on (a) QF-A and (b) QF-B. DC g_m measurements on (c) QF-A and (d) QF-B. Transfer characteristics in log scale on (e) QF-A and (f) QF-B.

B. Small Signal Measurements

The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were determined through s-parameter measurements (Anritsu ME7838A) up to 50 GHz and V_{DS} of 10, 15, 20, and 25 V conducted on three randomly selected HEMTs on epi-structures. A small-signal equivalent circuit model was extracted and averaged at the bias giving the highest f_{max} ([V_{GS}, V_{DS}] = [-0.9, 20] V) (Table III) [26]. A similar ratio between the g_m and C_{gs} tends to yield a similar f_T and f_{max}. The observed slight decreased in g_{ds} in QF-B can be correlated with the short channel effects discussed above.

TABLE III
THE f_T, f_{max}, AND SMALL-SIGNAL EQUIVALENT CIRCUIT PARAMETERS.

	QF-A	QF-B
f_T [GHz]	46	46
f_{max} [GHz]	105	100
C_{gd} [fF]	10	11
R_i [Ω]	7	6
C_{gs} [fF]	232	215
g_{ds} [Ω^{-1}]	0.82	0.75
C_{ds} [fF]	31	34
g_m [mS]	60	52

C. Pulsed-IV

Pulse-IV characteristics were acquired from three randomly selected HEMTs on each of the epi-structures, using the AMCAD AM3200 PIV system (Fig. 3). The measurement were performed with a pulse width of 1 µs with a duty cycle of 0.001%. Four different quiescent bias points (V_{GSQ}, V_{DSQ}) were considered: (0, 0), (V_{TH}-4, 0), (V_{TH}-4, 20), (V_{TH}-4, 40) V, referred to as Q_{ref}, Q_0, Q_{20}, and Q_{40}. To assess current collapse, two parameters were defined (equations 1 and 2): mainly surface-related current collapse (Z_1) and mainly buffer-related current collapse (Z_2):

$$Z_1[\%] = \left|\frac{I_{ds}(Q_0) - I_{ds}(Q_{ref})}{I_{ds}(Q_{ref})}\right| \cdot 100 \qquad (1)$$

$$Z_2[\%] = \left|\frac{I_{ds-knee}(Q_{20,40}) - I_{ds-knee}(Q_{ref})}{I_{ds-knee}(Q_{ref})}\right| \cdot 100 \qquad (2)$$

Both QF-A and QF-B HEMTs exhibit a comparable Z_1 of approximately 7 %, owing to the identical SiN passivation and barrier design. However, QF-A displays a higher Z_2 at 40 V of 27 %, in contrast to the 20 % observed in QF-B. These findings are consistently reflected in the dynamic R_{on} values of QF-B, which are smaller than those of QF-A (Table IV). These results highlight the advantages of QF-B, which effectively reduces buffer-related trapping effects.

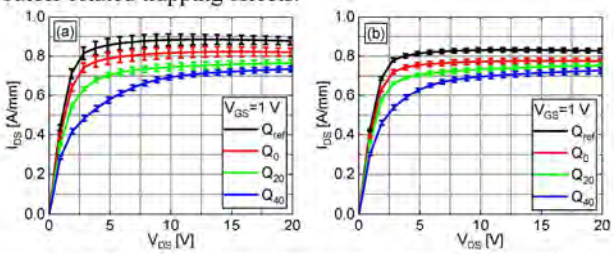

Fig. 3. Pulsed-IV measurements performed at different quiescent biases on (a) QF-A and (b) QF-B.

TABLE IV
EXTRACTED FIGURES OF MERIT FROM PULSED-IV MEASUREMENTS

	QF-A	QF-B
R_{on} (Q_{ref}) [Ω·mm]	2.06	2.14
R_{on} (Q_{40}) [Ω·mm]	3.28	3.07
R_{ON} [Increase %]	59.2	43.4
Z_1 [%]	7	7
Z_2 [%]	27	20

D. Drain Current Transient – Temperature

Drain current transient (DCT) measurements were performed on the same devices as the pulsed-IV measurements. In these DCT measurements, the devices were pulsed to the off-state with a bias of ([V_{GSQ}, V_{DSQ}] = [V_T-4, 40] V) for a filling time duration of 1 sec. Subsequently, the current recovery was monitored under an on-state bias setting of ([V_{GS}, V_{DS}] = [1, 7]

V) for 10 sec. The V_{DSQ} setting remained consistent with that employed in the pulsed-IV measurements, intended to activate a majority of traps. DCT measurements were conducted at four different temperatures (40, 60, 80, and 100 °C) (Fig. 4). Notably, QF-B demonstrated a smaller I_{DS} drop at 10^{-6} sec (compared to reference saturated I_{DS} at 10 sec) than QF-A (17% vs 11%). To extract the time constants associated with the recovery currents (as depicted in the inset of Fig. 4), the measured recovery I_{DS} were fitted using the stretched multiexponential function (equation 3):

$$I_{DS}(t) = I_{DS,final} - \sum_i^N A_i e^{-(\frac{t}{\tau_i})^{\beta_i}} \quad (3)$$

where the fitting parameters $I_{DS,final}$, N, A_i, τ_i, and β_i are the drain current at 10 s, number of traps, the amplitude of the trapping effect ($A_i > 0$: charge emission process, $A_i < 0$: charge capture process), trapping and de-trapping time constant, and the nonexponential stretching-factor, respectively. Once the τ_i was obtained, the Arrhenius plot was used to extract the activation energies (E_A) and the capture cross sections (σ) of the traps (Fig. 5 and Table V).

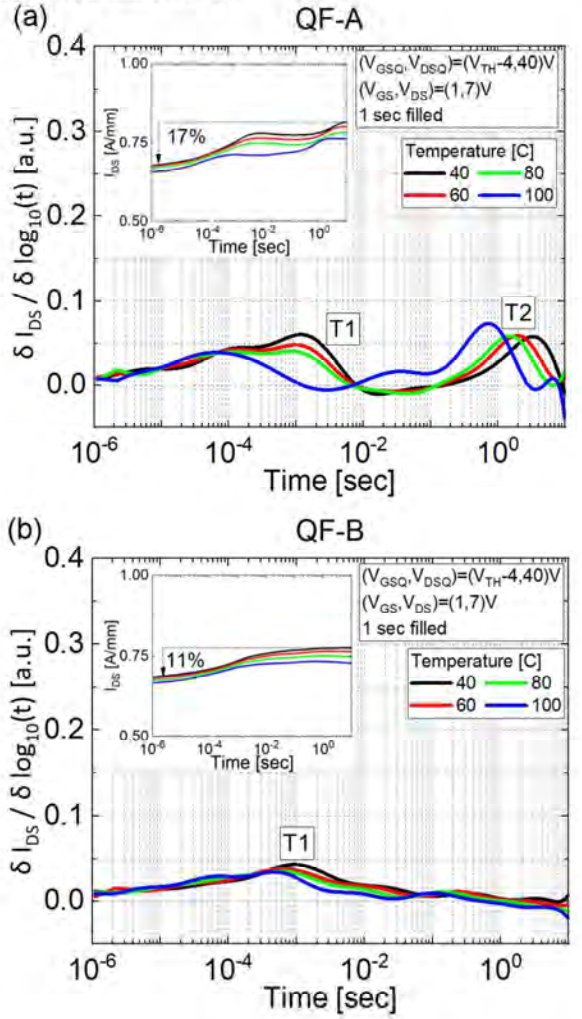

Fig. 4. Differential data (main figure) of the DCT measurements (inset) measured at different temperatures under the pinch off condition with V_{DS} of 40 V and 1 s filling time on (a) QF-A and (b) QF-B.

Two distinct traps, denoted as T1 and T2, were identified. T1 was shown in both epi-structures, while T2 was exclusively present in QF-A. A reduction in the amplitude of the T1 trap at higher temperatures was revealed for both QF-A and QF-B. This behavior indicate that T1 traps may result from threading dislocation [1]. Alternatively, this may indicate that the de-trapping processes are dominated by hopping [27] or tunneling [28] mechanisms. However, the T1 trap for QF-A exhibits a deviation at 100 °C (Fig. 5), resulting in non-Arrhenius behavior, which prevents the determination of activation energy. This phenomenon, as previously reported, can be attributed to a leakage process mediated by a defect band [29]. Trap T1 in QF-B revealed small activation energies (E_A) and β values, suggesting the formation of continuous trap energy levels. QF-B effectively mitigates trap T2, that exhibits a long time constant. The E_A associated with trap T2 demonstrates low thermal activation energy and a large time constant (1-10 seconds). This trap bears similarities to traps reported previously [22, 30-32]. Possible explanations for trap T2 include electron trap-assisted tunneling mechanisms [22], the presence of carbon or hydrogen impurities from trimethylgallium (TMGa) in C-doped epi-structure [9, 30], the charging and discharging between the 2DEG and buffer [31, 32], and the formation of 2DHG [15-17]. Another possible origin for the T2 trap could also be the threading dislocations due to lattice mismatch in epi-structure since the E_A and β are small, which indicates they are likely continuous trap energy states. By introducing the Si delta doping at the interface of GaN and AlN nucleation layer, it provide a lateral leakage path for a faster de-trapping mechanism [33, 34].

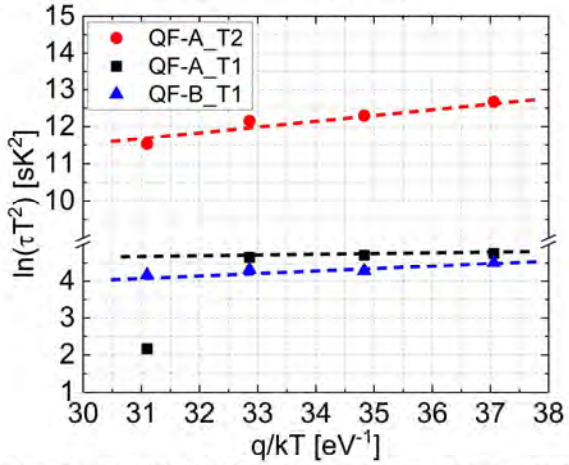

Fig. 5. Arrhenius plot of the identified energy levels in the temperature dependent DCT measurements.

TABLE V
EXTRACTED ACTIVE ENERGIES, CAPTURE CROSS SECTIONS, AND STRETCHING TERMS OF THE TRAPS FOUND IN FIG. 5

	QF-A T1	QF-B T1	QF-A T2
E_A [eV]	-	0.05	0.13
σ [cm²]	-	$1.9 \cdot 10^{-21}$	$1.3 \cdot 10^{-19}$
β	-	~0.5	~0.5

E. Drain Current Transient – Filling Time

DCT measurements were conducted with varying filling times on devices that were previously selected in the pulsed-IV

measurements. These measurements were performed at 25°C with filling times ranging from 100 µs to 10 sec, maintaining the same quiescent bias settings as described in Section III-D (Fig. 6).

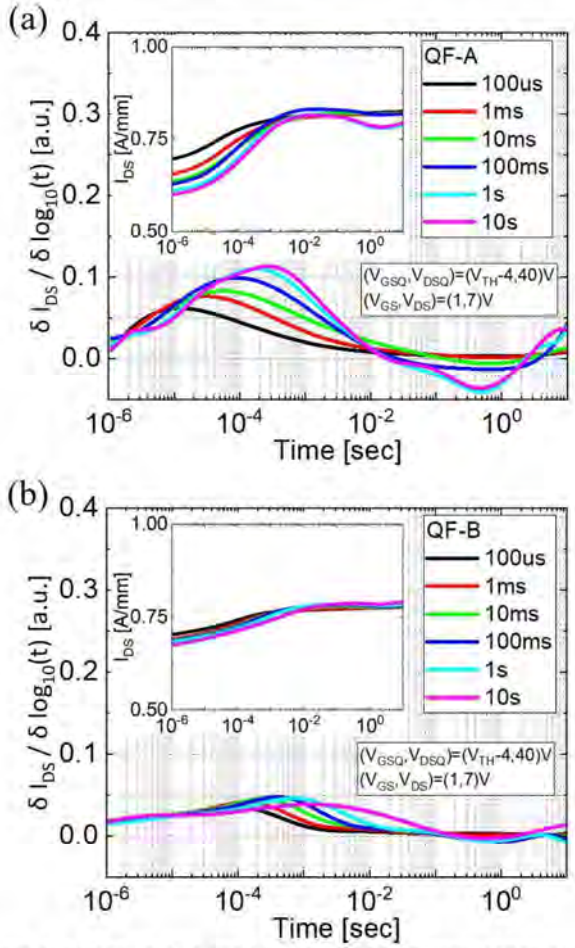

Fig. 6. Differential data (main figure) of the DCT measurements (inset) measured at different filling times under the pinch off condition with V_{DS} of 40 V at 25 °C on (a) QF-A and (b) QF-B.

An increased amplitude of T1 was found in QF-A for longer filling durations. Moreover, the T1 peaks for both epi-structures shifted toward longer time constants as the filling time increased. This behaviour suggest that traps are located at threading dislocations [12, 22]. Interestingly, the amplitude of T1 in QF-A saturated at filling times ranging from 1 s to 10 s, whereas in QF-B, this saturation occurred earlier, at a filling time of 100 ms. This suggests a relationship between the trap states, dislocations, and leakage path, where the design of QF-B appears to reduce trap states related to T1 by providing a leakage path, which may be correlated with both the Si delta doping GaN layer and lower crystal quality, that enhances the de-trapping process (Table I). With a small E_A close to 0 eV, tunnelling leakage is likely responsible for electron transport during the de-trapping procedure. For filling times longer than 1 s (T2 trap state in QF-A), a pattern of charging followed by discharging was evident at time constants around 0.1 to 1 s. This behavior may be attributed to the charging and discharging processes occurring between the 2DEG and buffer layers [31, 32]. Since the T2 trap in QF-B is fully suppressed by the Si doping, it indicates that the Si delta doping at the GaN/AlN interface could effectively facilitate the de-trapping procedure and/or reduce the formation of 2DHG. In the meanwhile, the un-optimized Si delta doping resulted in more leakage, higher DIBL and lower isolation property.

IV. Conclusion

This study investigates trapping effects in both standard QuanFINE and band-structure engineered QuanFINE with Si delta doping. Devices fabricated on both epi-structures exhibit similar I_{DS} and g_m. However, devices on band-structure engineered QuanFINE demonstrate a higher DIBL compared to that on standard QuanFINE. This difference can be primarily attributed to the lower GaN buffer resistivity and the band-structure engineering using Si delta doping. Furthermore, band-structure engineered QuanFINE showcases lower levels of buffer-related current collapse and smaller dynamic R_{on} degradation in contrast to standard QuanFINE. DCT characterization reveals that modified QuanFINE effectively mitigates the impact of long-time constant trap states (T2), specifically the one at 1 sec, while also reducing the amplitude of the trap state (T1) at 10^{-3} sec, which are mainly due to the controlled lateral leakage path that enhances the de-trapping process and the mitigation of 2DHG. In summary, these results highlight the potential of employing epi-design with further optimization of Si delta doping thickness and concentration in the growth of epi-structures for GaN HEMTs. This approach paves a way to minimize trapping effects and mitigate the long time constant trap state.

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