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A Ka-Band Doherty-Like Non-Load Modulated Power Amplifier

Edward Liu, *Graduate Student Member, IEEE,* Han Zhou *Member, IEEE,* Christian Fager *Fellow, IEEE,* and Hua Wang, *Fellow, IEEE*

***Abstract*—This article describes a three-way power amplifier (PA) topology that achieves broadband power back-off (PBO) efficiency enhancement without using active load modulation on the Main PA or supply modulation. This allows the PA to avoid the classic trade-off between load modulation and bandwidth that is typical among Doherty PAs. Unlike Doherty PAs, the proposed PA has both its voltage and current drive profiles reach a maximum at PBO, which causes the impedance of the Main PA to be constant across the entire input drive. This is achieved with a novel parallel-series output matching network (OMN) that primarily utilizes coupled-line baluns. A prototype is fabricated in the GlobalFoundries 45nm RFSOI and achieves a $\mathrm{P_{avg}}$ and $\mathrm{PAE_{avg}}$ of 6.45 - 12.61 dBm and 5.9 - 16.4% from 25 - 40 GHz, respectively. With a 200 MHz signal, $\mathrm{P_{avg}}$ and $\mathrm{PAE_{avg}}$ are 5.58 - 11.1 dBm and 4.8 - 13.3%, respectively.**

***Index Terms*—Load modulation, doherty, power amplifier (PA), broadband, CMOS, fifth generation (5G), frequency range 2 (FR2), power-added efficiency (PAE), power back-off (PBO), millimeter-wave (mm-wave).**

I. Introduction

MILLIMETER-wave (mm-wave) 5G promises multi-Gbps data rates by harnessing the vast spectral resources in frequency bands such as n257 - n261 (24.25 - 43.5 GHz) [1]. As seen in Fig. 1, different regions in the world are allocated different bands, highlighting the need for broadband RF front-ends. A broadband power amplifier (PA) that can cover multiple bands enables frequency-agile radio front-end deployment and reduces costs through increased re-usability [2], [3]. Furthermore, mm-wave communications rely on orthogonal frequency-division multiplexing (OFDM) to combat hostile environmental effects such as multipath fading [4]. However, OFDM drastically increases the peak-to-average power ratio (PAPR) of the RF signal, placing an extra burden on the PA. Since the PA must operate in PBO, the average efficiency when transmitting a high PAPR signal suffers. Therefore, one research trend is to develop architectures that are simultaneously broadband and efficient at PBO [5].

Doherty PAs are a popular choice for achieving PBO efficiency enhancement, but they usually suffer from narrow bandwidths caused by the required active load modulation and impedance inverting networks [6], [7], [8], [9], [10], [11], [12], [13], [14]. This problem is exacerbated with higher order Doherty PAs, as the required load modulation range and impedance transformation ratio is significantly larger [15], [16], [17], [18], [19]. Recently, main/auxiliary role-exchange has been explored as a bandwidth enhancement technique [20], [21], [22], [23]. However, one drawback in this technique is the large gain variation across frequency and the need for extra reconfiguration circuitry, which increases the complexity.

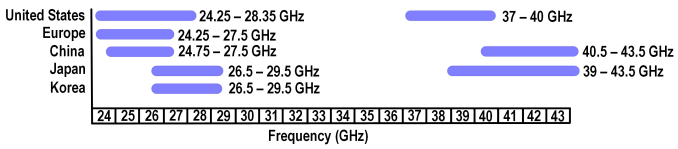

Fig. 1. 5G NR FR2 frequency allocation for different regions.

Another way of achieving broadband performance is to eliminate the need for load modulation entirely. One way of achieving this is with the sequential load modulated balanced amplifier [24], [25], [26], [27], [28], [29]. While most of the prior works are implemented at sub-6 GHz, recently this technique has also been demonstrated at Ka-band in CMOS [30]. However, the fractional bandwidth (FBW = $\frac{\mathrm{f_2-f_1}}{\mathrm{f_c}}$) of this design (15%) is much lower compared to the designs at sub-6 GHz, where FBWs of >100% have been demonstrated. This is possibly due to the extra output baluns needed to interface with the single-ended quadrature coupler, which also increases the loss of the output matching network.

The distributed efficient power amplifier (DEPA) architecture removes the load modulation and does not need a quadrature coupler [31]. However, the prototype DEPA PA in [31] uses six auxiliary amplifiers, which is not conducive to on-chip implementations and leads to large output combiner loss. Furthermore, the Main PA is furthest from the load, which results in a high combiner loss and lower PBO efficiency. A design that reduces the number of auxiliary amplifiers to four is presented in [32], achieving higher efficiency and output power, but with a reduced FBW of 38%, compared to the 71% of [31]. A new, Doherty-like architecture with no load modulation is presented in [33] uses two auxiliary amplifiers, but achieves a smaller FBW of 33%. In this spirit, an alternative architecture is explored that minimizes the number of auxiliary paths required, but also achieving the desired non-load modulated behavior over a wider bandwidth.

This article proposes a parallel-series architecture with two auxiliary paths that can achieve a FBW of 48%. As an

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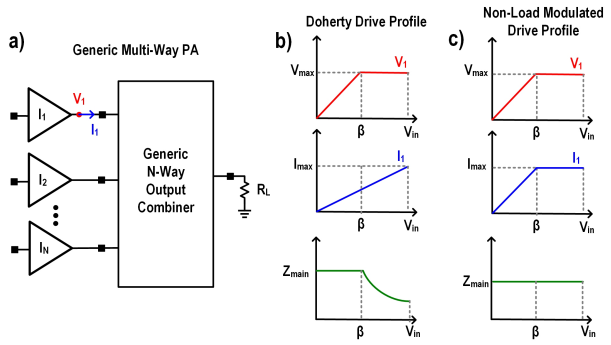

Fig. 2. (a) A generic schematic of a multi-way PA. (b) Voltage/Current drive profile of a Doherty PA. (c) Voltage/current drive profile of the proposed PA.

extension of [34], this article includes an expanded theoretical analysis of the proposed novel output combiner. The demonstrated PA, implemented in GlobalFoundries 45nm CMOS SOI technology, covers 25 - 40 GHz, which occupies the entire Ka-band and addresses four 5G FR2 bands (n257, n258, n260, and n261) without any tuning elements or main/auxiliary PA role-exchange. Section II describes the difference between the traditional Doherty current/voltage drive profile, and that of the proposed network. Section III introduces the circuit details of the PA. Section IV describes the measurement results and compares the performance with state-of-the-art CMOS PAs. Lastly, the conclusion is given in section V.

II. Non-Load Modulated Output Architecture

The current/voltage drive profiles of the proposed architecture and the traditional Doherty architecture is shown in Fig. 2. First, Fig. 2(a) describes a generic multi-way PA, and if this is designed as a Doherty PA then the current/voltage drive profile of the Main PA will look similar to Fig. 2(b). For a Doherty PA, the output voltage V_1 rises as the input drive increases, and is maximized at some back-off point β, leading to a high efficiency in the region from β to peak output power. It is important to note here that the current I_1 does not reach its maximum until the PA reaches its peak drive. Therefore, the impedance seen by the Main PA, Z_{main}, is modulated to a lower value in the high power region.

In contrast, the drive profile of the proposed PA is shown in Fig. 2(c). The key difference is that the current I_1 maximizes at β, which allows Z_{main} to remain independent of the input drive. In this design, β = 0.5. At the same time, the voltage swing is maximized at back-off, which ensures a high efficiency, just as in the case of a Doherty PA.

An example of a PA architecture that can achieve this drive profile is shown in Fig. 3. First, for a $\lambda/4$ transmission line, the voltage and current relationships at its terminals is given by

$$\begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & -jZ_o \\ -jY_o & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \tag{1}$$

where Z_o is the characteristic impedance of the line. With this information, the correct drive profile of the Main PA can be determined. Since the output is series combined, $I_o = I_B = I_C$, and $V_o = V_{a1} + V_C$. Additionally, both I_o and V_o increase linearly with input drive up to the peak point, as the PAs are modeled as ideal current sources. Then, both I_{a1} and I_{a2} only turn on in the high power region. This means that V_C, which is on the other side of TL_2, must follow I_{a2}. Then, V_{a1} can be determined as V_o - V_C. Lastly, I_m must follow V_{a1}, which means it reaches its maximum at β. Furthermore, I_A can be determined as I_B - I_{a1}. Since V_m must follow I_A, this means that V_m must also reach its maximum at β. Therefore, the drive profile of the Main PA is shown to behave as that of Fig. 2(c).

This output network can be further analyzed by dividing it into two operation regions, as shown in Fig. 4. The transmission lines TL_1 and TL_2 have values of R_{opt} and $\frac{R_{opt}}{2}$, respectively.

1) Low power region: In this region, only the Main PA is on. Since I_{a1} and I_{a2} are open circuited, the impedance presented to the Main PA Z_m can simply be determined directly as

$$Z_m = \frac{V_m}{I_m} = R_{opt} \tag{2}$$

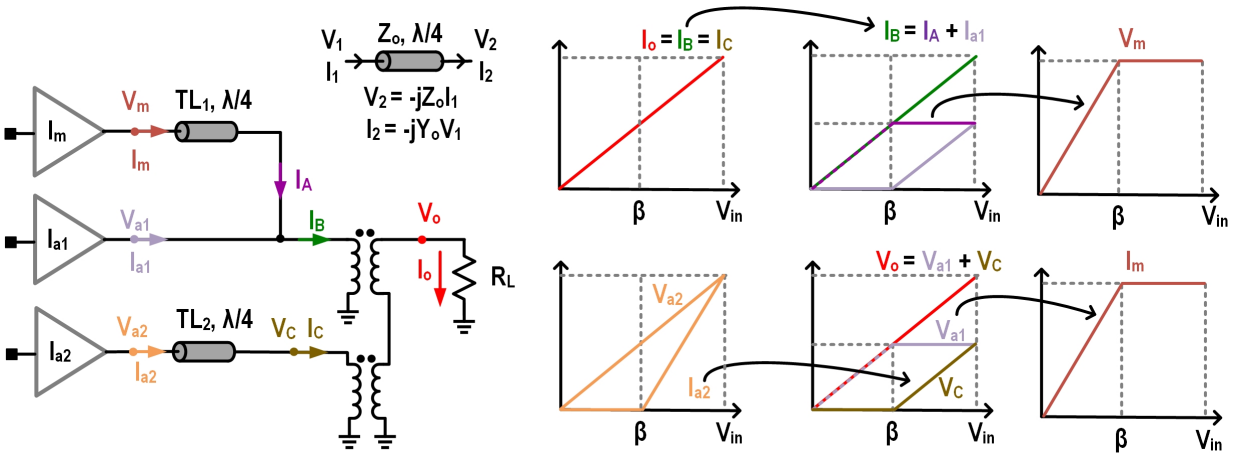

Fig. 3. Drive profile breakdown at different nodes in the output matching network.

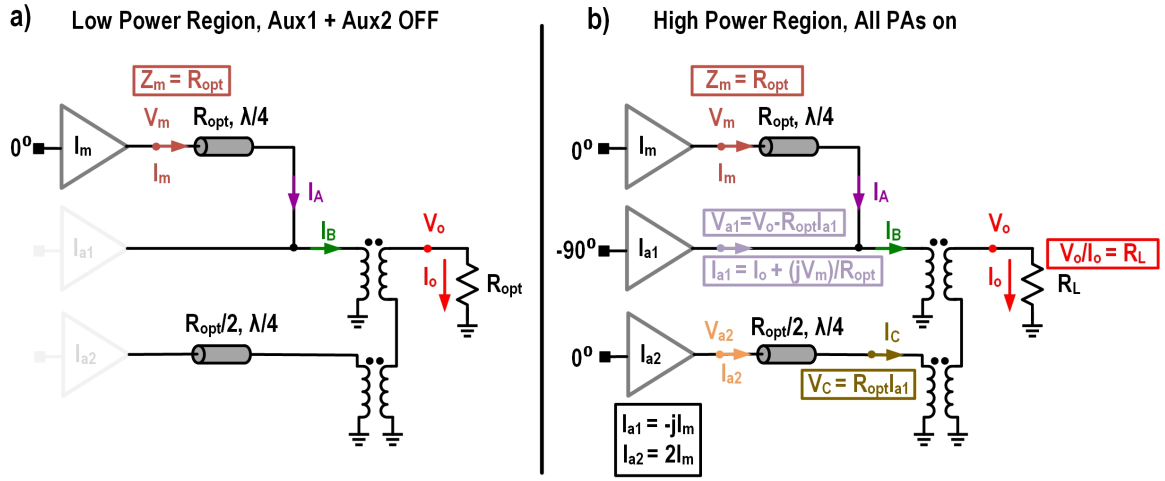

Fig. 4. (a) Low power region. (b) High power region. All PA paths are on, and the impedance Z_m is still R_{opt}.

2) High power region: At this point, both auxiliary paths (I_{a1} and I_{a2}) turn on, and the currents are sized as

$$I_{a1} = -jI_m \tag{3}$$

$$I_{a2} = 2I_m \tag{4}$$

Note that this is a key difference compared to higher-order Doherty PAs, where the auxiliary paths are turned on sequentially. At the same time the auxiliary paths turn on, the Main PA reaches voltage saturation, leading to an efficiency peak. By applying (1), the voltage at V_C and V_{a1} can be determined as

$$V_C = -j\frac{R_{opt}}{2}I_{a2} = R_{opt}I_{a1} \tag{5}$$

$$V_{a1} = V_o - R_{opt}I_{a1} \tag{6}$$

and the Main PA current I_m is calculated as

$$I_m = \frac{V_{a1}}{-jR_{opt}} = j(\frac{V_o}{R_{opt}} - I_{a1}) \tag{7}$$

Again by applying (1), I_{a1} can be determined in terms of V_m and I_o as

$$I_{a1} = I_o + \frac{j}{R_{opt}}V_m \tag{8}$$

Lastly, by combining (8) with (7) the impedance Z_m is calculated as

$$Z_m = \frac{V_m}{I_m} = R_{opt} \tag{9}$$

which is exactly the same as (2), confirming that in either low or high power region, the load of the Main PA is constant. The impedance seen by the auxiliary PAs at peak power can be derived in a similar way (see Appendix), and provided below as

$$Z_{a1} = R_{opt} \tag{10}$$

$$Z_{a2} = \frac{R_{opt}}{2} \tag{11}$$

Therefore, at peak power all PA paths are matched to their optimum load impedance. To summarize, the drive profiles for all three PA paths are shown in Fig. 5(a) - (b). The impedance seen by each PA is shown in Fig. 5(c), and the theoretical drain efficiency enhancement is shown in Fig. 5(d).

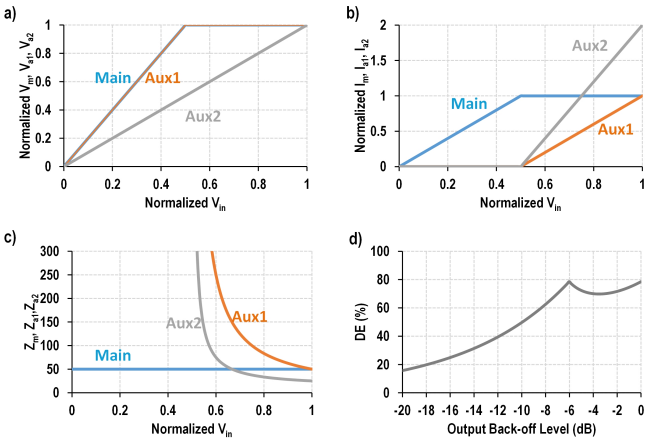

Fig. 5. (a) Voltage drive profile. (b) Current drive profile. (c) Non-load modulation behavior. (d) Ideal drain efficiency vs. power back-off level.

At this point, it is necessary to understand the bandwidth limitations imposed by the $\lambda/4$ lines. It can be shown that at PBO, the impedance seen by the main PA can be written as

$$Z_m = \frac{1 - j(\frac{1}{2}\cot(\theta) - \tan(\theta))}{\frac{3}{2} + j\tan(\theta)} \tag{12}$$

and the real and imaginary components can be determined as

$$\mathrm{Re}[Z_m] = R_{opt}\frac{1 + \tan^2(\theta)}{\frac{9}{4} + \tan^2(\theta)} \tag{13}$$

$$\mathrm{Imag}[Z_m] = R_{opt}\frac{-\frac{1}{2}(\frac{3}{2}\cot(\theta) - \tan(\theta))}{\frac{9}{4} + \tan^2(\theta)} \tag{14}$$

where θ is a frequency dependent parameter. This can be compared with a standard two-way Doherty that achieves load modulation from $2R_{opt} \rightarrow R_{opt}$. The normalized real part of the impedance is shown in Fig. 6(a), and the imaginary part is shown in Fig. 6(b). The real part of the impedance is

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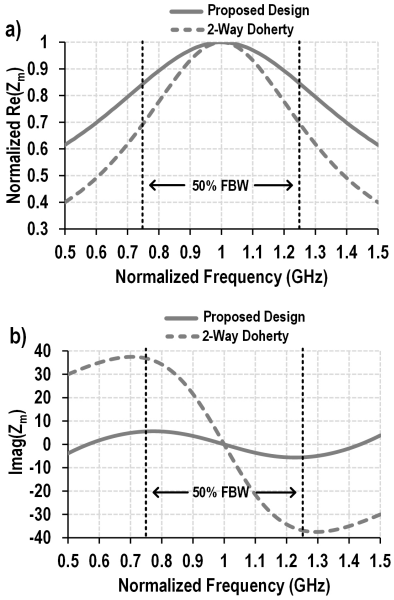

Fig. 6. (a) Normalized real part and (b) imaginary part of the impedance vs. frequency seen by the main PA at back-off of the proposed design compared to a standard two-way parallel Doherty.

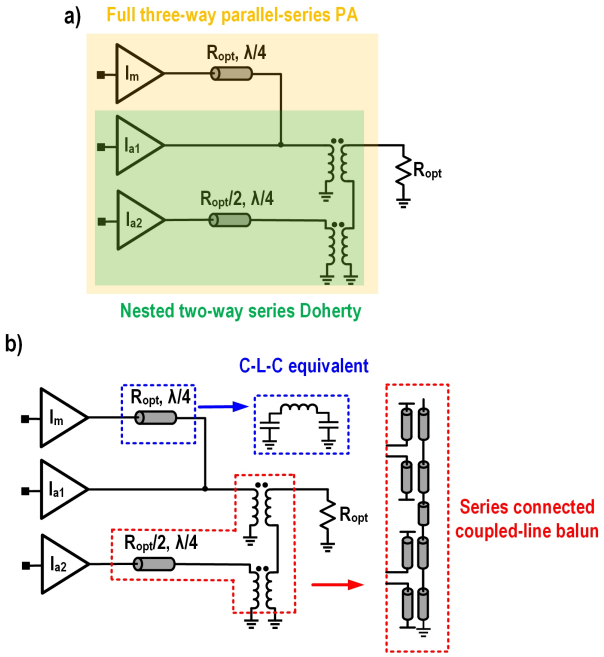

Fig. 7. (a) Full PA matching network, with sub series Doherty highlighted. (b) Converting ideal components to on chip equivalents.

normalized, since the Doherty PA performs load modulation whereas our design does not. Over a 50% FBW, our proposed network sees a decrease in the real part from the peak value to 0.85× of that. However, the standard two-way parallel Doherty sees a drop of 0.7×. This means that if R_{opt} = 50Ω, our network only sees a reduction from 50Ω → 42.5Ω whereas the Doherty network sees a reduction from 100Ω → 70Ω. Furthermore, over the same 50% FBW, the imaginary component of the impedance is also improved drastically. As shown in Fig. 6(b), the variation is reduced by over 6×. This is important because a large reactive impedance component will degrade the PA performance severely, and may in fact be the overall limiting factor.

As mm-wave CMOS PAs are usually implemented differentially, a few modifications to the architecture of Fig. 3 are needed. As shown in Fig. 7(a), the Aux1 and Aux2 paths comprise of a nested two-way series Doherty within the overall three-way parallel-series PA. This topology has been well studied in [35], and the broadband coupler balun-based approach can be easily adopted for this PA. These baluns absorb the PA output capacitance over a broad bandwidth, and allow for easy large signal matching and DC biasing. The λ/4 transmission line interfacing the Main PA can be realized as a lumped C-L-C network. This network can inherently absorb the PA output capacitance in its design, therefore only an extra inductor and capacitor is needed. The L and C values can be determined as

$$L = \frac{Z_o}{\omega} \tag{15}$$

$$C = \frac{1}{Z_o \omega} \tag{16}$$

Finally, one additional advantage of this output network is that despite needing three PA paths, only two baluns are required. The L-C network interfacing the main PA can be placed in the space between the two baluns. Therefore, the overall chip area can be minimized. It should be noted that the lumped element approximation of a λ/4 line will also limit the bandwidth of the output network, along with the transistor parasitic capacitance. However, these are limitations due to implementation, and not limitations inherent to the topology such as those illustrated in Fig. 6.

III. Circuit Implementation

The full circuit of the PA is shown in Fig. 8. The input signal is first split into three paths with proper phase shift by the input coupler. Each of the three paths consists of a common-source (CS) driver and a cascode PA stage. The Main:Aux1:Aux2 sizing ratio is 1:1:2. An adaptive biasing circuit is used to control the turn-on point of the Aux1 and Aux2 paths [21]. Lastly, the signals in each path are recombined through the output combiner. The next two subsections will describe the output matching network, input splitter, and adaptive biasing.

A. Output Network

As shown in Fig. 9(a), coupled-line baluns are used to interface with both Aux1 and Aux2 PAs [2]. The Main path is connected through a CLC-based transmission line, which is also used to absorb the output capacitance of the Main PA. The balun interfacing the Aux2 PA uses adjacent metal layers (M6 and M7) for high coupling, which is necessary to achieve a low odd-mode impedance Z_o (Fig. 9(b)). On the other hand, the balun interfacing the Aux1 PA requires a much larger Z_o, so non-adjacent metal layers (M6 and M8) are used.

Figure 10(a) shows that over the 25 - 40 GHz frequency range, Z_m is almost constant, confirming that this performance

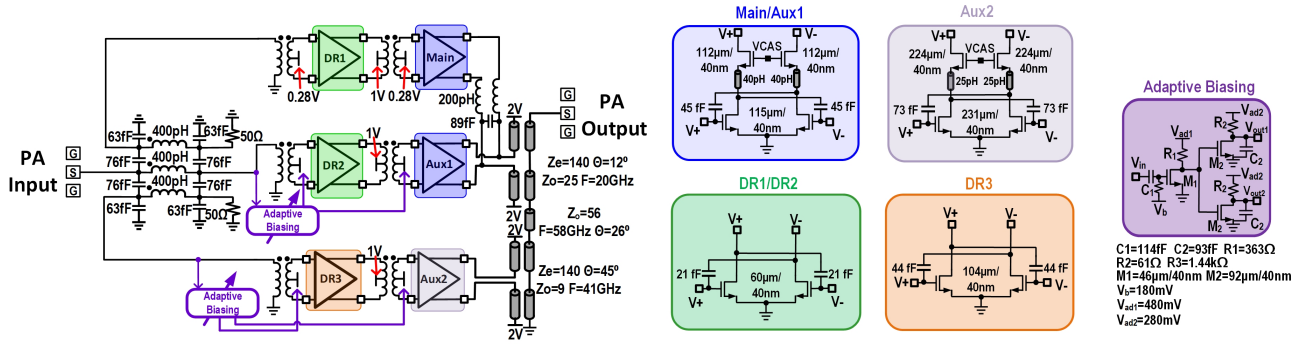

Fig. 8. Full schematic of the PA.

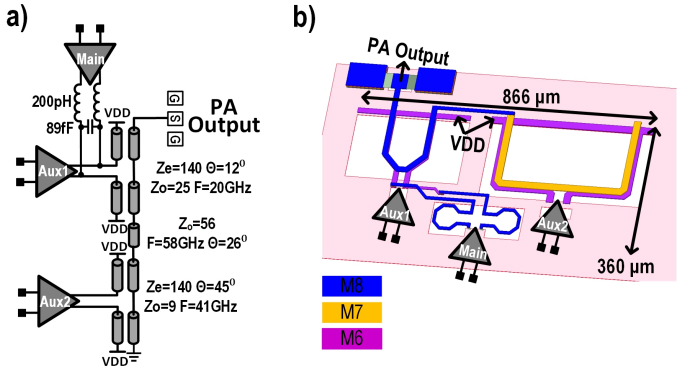

Fig. 9. (a) Schematic of the output network. (b) 3-D EM model.

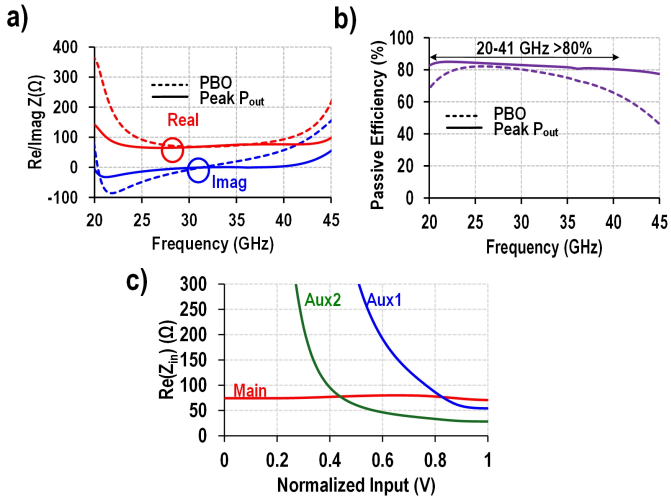

Fig. 10. (a) Impedance seen by the Main PA at back-off and peak power. (b) Passive efficiency. (c) Real part of the load impedance of the three PA paths over input drive at 33 GHz.

can be maintained over a large frequency range. The passive efficiency is >80% from 20 - 41 GHz at peak P_{out} and >60% at back-off as shown in Fig. 10(b). Lastly, Fig. 10(c) confirms that the real part of the Main PA impedance stays constant over the input drive. Furthermore, both auxiliary paths see an impedance close to their optimal values. Ideally, the Aux1 impedance should be equal to that of the Main at peak drive,

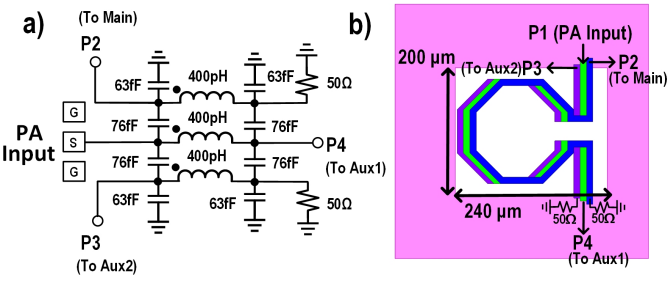

Fig. 11. (a) Schematic of the input splitter. (b) 3-D EM model.

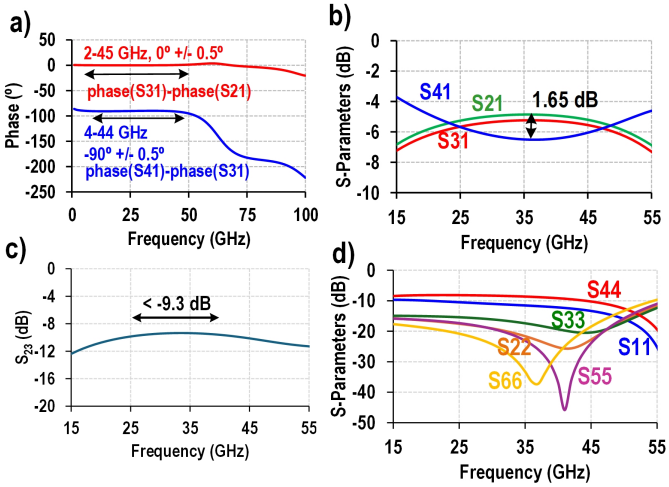

Fig. 12. (a) Simulated phase relationships between the different paths. (b) Simulated S21, S31 and S41. (c) Isolation between ports 2 and 3. (d) Input reflection parameters for all six ports.

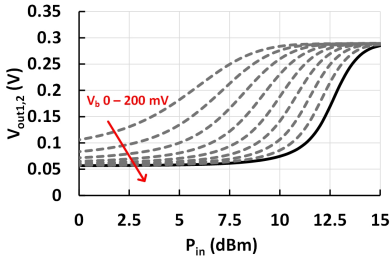

Fig. 13. Adaptive biasing ramp-up for different V_b values.

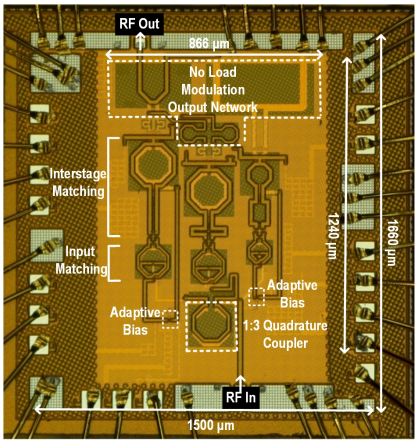

Fig. 14. Die photo of the PA.

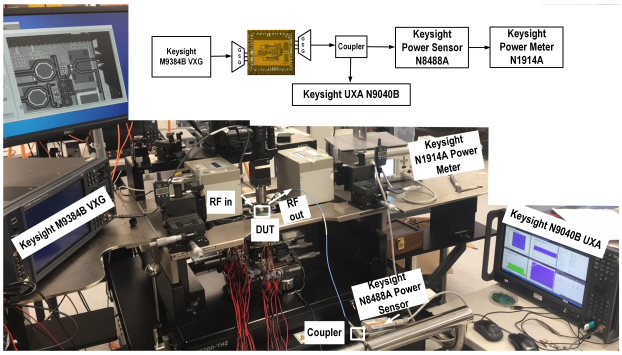

Fig. 15. Modulation measurement setup.

but in practice it is somewhat lower due to the nonidealities introduced by the EM simulated matching network.

B. Input Splitter

It is generally more difficult to design input splitting networks for three-way PAs compared to two-way PAs, especially those requiring a phase difference between the different paths and over a wide frequency range. This results in bulky networks involving multiple components, which increases the chip area. For example, the design in [17] utilizes a combination of a two-way Wilkinson divider and a single-ended quadrature hybrid. Similarly, [15] uses a Wilkinson divider, a quadrature hybrid, and additional 90° and phase compensation lines.

The transformer-based quadrature coupler design in [36] can be extended to support an extra coupled port, as shown in Fig. 11(a). This network uses three coupled inductors that can be overlayed, drastically reducing the total footprint (Fig. 11(b)) while simultaneously providing the correct phase relationships between the three PA paths as shown in Fig. 12(a). The total area required by the three coupled inductors is only 0.24mm $\times$ 0.2mm, which is about the same size as a single interstage matching transformer. The coupling between pairs of adjacent inductors is about k = 0.66. The phase difference between the Main and Aux2 is close to 0°, and the phase difference between the Aux1 and Aux2 (and Main) paths is -90°. This fulfills the phase requirement, as described in Fig. 4(b). Furthermore, the transmission parameters are shown in Fig. 12(b). Across the bandwidth, the power split between the three PA paths is relatively equal. Additionally, the isolation between the two coupled ports is shown in Fig. 12(c), and it is <-9.3 dB from 25 - 40 GHz. Lastly, Fig. 12(d) shows the input reflection parameters for all six ports, which are all <-10 dB in the bandwidth of interest, with the exception of S_{44}, which is <-8.1 dB.

C. Adaptive Biasing

Adaptive biasing is normally used in Doherty PAs to control the load modulation through the auxiliary path ramp-up. In this PA, it serves a similar function by keeping the Aux1 and Aux2 paths off, until the high power region, at which point the PAs are ramped up to class-AB biasing. By controlling the voltage V_b as shown in Fig. 13, the turn-on point of the Aux1/2 paths can be controlled. The adaptive biasing is applied to both the driver and the PA stage to ensure that there is no accidental turn-on of any path in the low power region. From simulations, the bandwidth of the adaptive bias circuit is approximately 2.2 GHz, which limits the modulation bandwidth to about 700 MHz when considering the AM bandwidth [37]. To improve the bandwidth of the adaptive biasing, techniques such as inductive peaking can be used [38], but may result in larger chip area.

IV. Measurements

The chip is fabricated in the GlobalFoundries 45RFSOI process, and the die photo is shown in Fig. 14. Measurements are conducted with RF probing and DC pads are wirebonded to a PCB. The modulation measurement setup is shown in Fig. 15. The modulated signal is generated by a M9384B VXG, and the amplified output is de-modulated by a N9040B UXA spectrum analyzer running 89600 Vector Signal Analysis (VSA) software. Output power is measured with a N1914A power meter and N8488A power sensor. The large signal continuous-wave (CW) setup is similar, with a Keysight E8267D replacing the VXG. The UXA is not used during CW tests.

A. Single Tone Measurements

Figure 16(a) and (b) shows the measured S-parameters and K-Δ stability factor, respectively. The S_{21} -3dB bandwidth is 25 - 41 GHz, demonstrating the broadband capabilities of this PA. The S_{11} is < -10 dB from 25 - 30 GHz and 35 - 50 GHz. From 30 - 35 GHz, the S_{11} is < -8.7 dB. The PA also demonstrates unconditional stability across the entire measurement frequency range, as shown in Fig. 16(b).

Figures 16(c) - (f) show the large signal CW measurements as a function of output power for different frequencies. Across the entire bandwidth, this PA demonstrates improved back-off efficiency, validating the broadband, PBO efficiency enhancement concept. A summary of the CW measurement results from 25 - 40 GHz is shown in Fig. 17. This PA achieves a power gain of 12 - 15 dB, an OP_{1dB} of 18.7 - 22.2 dBm and a PAE at the OP_{1dB} of 20.9 - 37.6%. The 9 dB PBO

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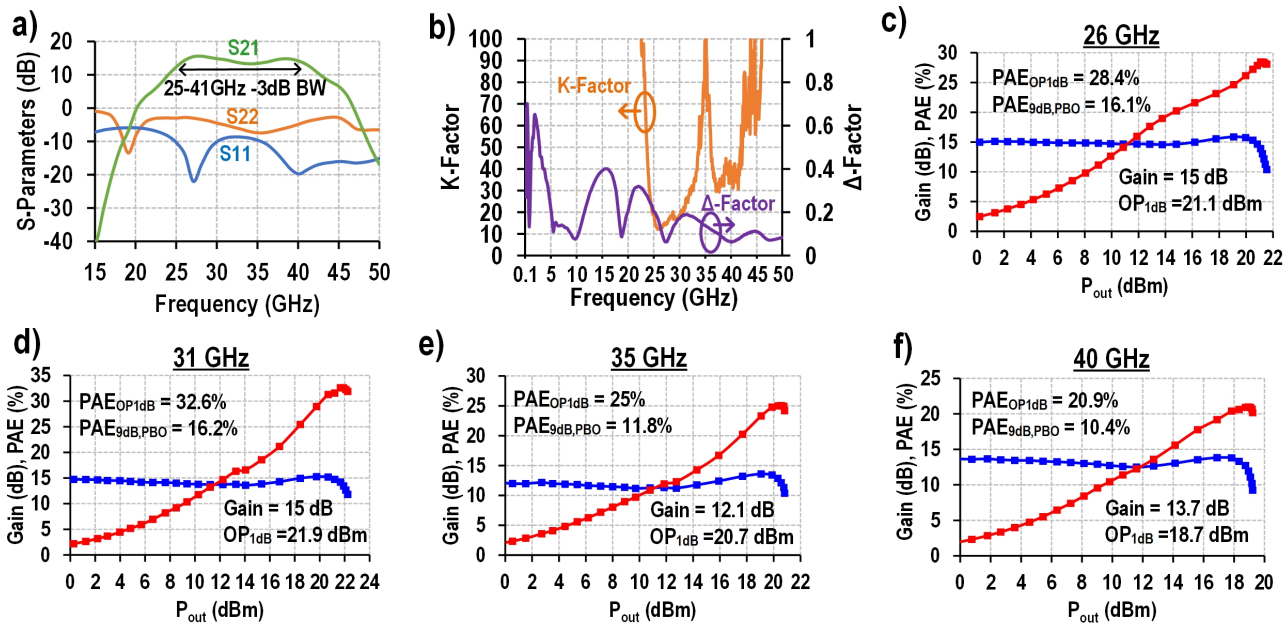

Fig. 16. Small signal measurements of (a) S-parameters and (b) stability. Large signal CW measurements at (c) 26 GHz, (d) 31 GHz, (e) 35 GHz, and (f) 40 GHz.

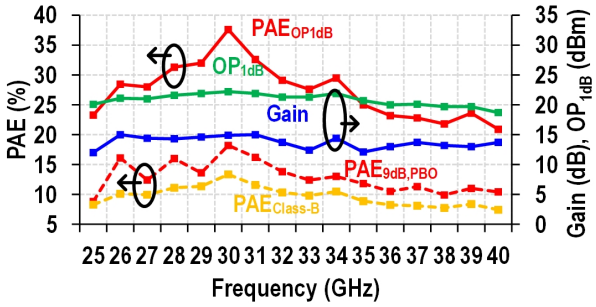

Fig. 17. Summary of CW measurement results from 25 - 40 GHz.

PAE is 8.8 - 18.2%. The PAE at 9dB PBO of hypothetical class-B PA with the same $\mathrm{PAE_{OP1dB}}$ is also plotted in yellow, demonstrating that the proposed design can achieve better PAE at PBO across frequency.

B. Modulation Measurements

The chip is tested with 5G NR FR2 64-QAM OFDM signals with 100 MHz and 200 MHz bandwidth. This signal has a PAPR of approximately 9.6 dB. Figure 18(a) shows the constellation and spectrum at different frequencies, and Fig. 18(b) shows the performance summary across frequency. With a 100 MHz signal and at an $\mathrm{EVM_{rms}}$ of -25 dB, the PA achieves an average $\mathrm{P_{out}}$ and PAE of 6.45 dBm - 12.61 dBm and 5.9% - 16.4% from 25 - 40 GHz. The best overall performance is achieved at 30 GHz, with a $\mathrm{PAE_{avg}}$ of 16% and a $\mathrm{P_{avg}}$ of 13.6 dBm. With a 200 MHz signal at the same $\mathrm{EVM_{rms}}$ and frequency range, the PA achieves an average $\mathrm{P_{out}}$ and PAE of 5.58 dBm - 11.1 dBm and 4.8% - 13.3%.

C. Discussion and Comparison

This PA is compared with other CMOS mm-wave PAs in Fig. 19. This PA achieves comparable modulation efficiency compared to the higher-order Doherty PAs ([17], [15], [19]) while at the same time achieving much higher bandwidth. Compared to [21], this design achieves a significant reduction in core area and has much higher gain flatness across frequency, although with a lower modulation efficiency. The work in [35] has a similar bandwidth but lower modulation efficiency, particularly in the n257 and n261 bands, and it has much larger gain variations. Overall, this PA achieves an exceptional balance between chip area, bandwidth, and efficiency compared to other designs in the same frequency range.

V. Conclusion

This article describes the design of PA that can achieve Doherty-like PBO efficiency enhancement without the need for load modulation. A prototype is designed in 45nm RFSOI CMOS, verifying its broadband, back-off efficiency enhancement capabilities. From 25 - 40 GHz, the PA demonstrates an $\mathrm{OP_{1dB}}$ of 18.7 - 22.2 dBm, a PAE of 20.9 - 37.6%, and a PAE at 9dB PBO of 8.8 - 18.2%. Lastly, the PA is characterized with modulated signals, confirming its efficiency enhancement capabilities.

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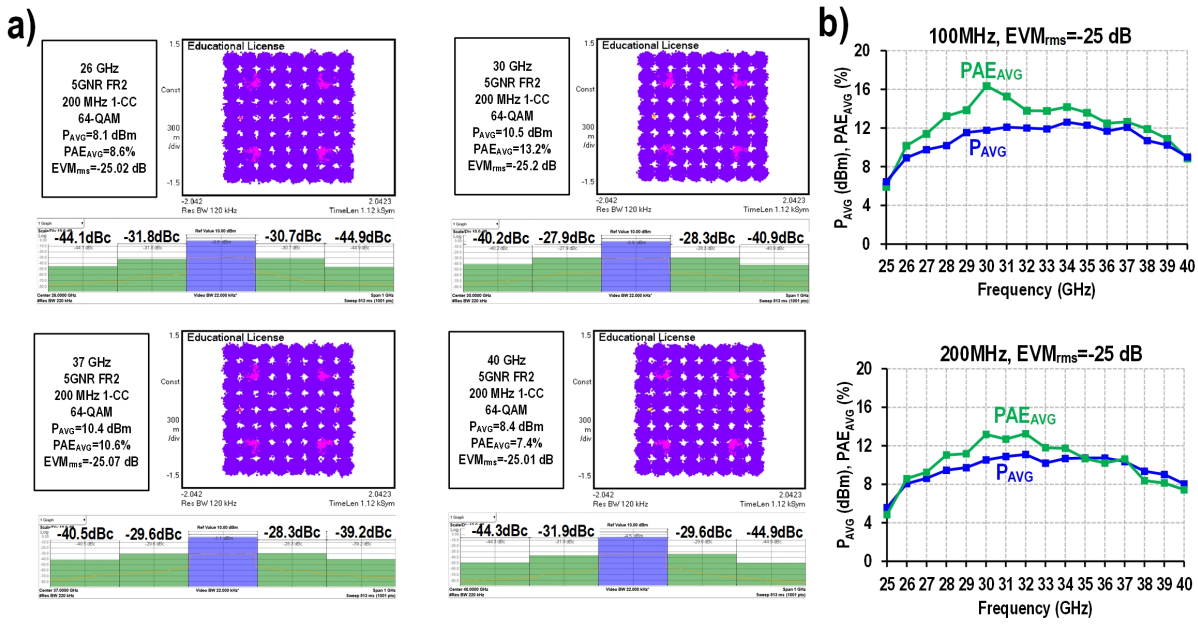

Fig. 18. (a) Constellation and spectrum across frequency and (b) modulation measurement summary across frequency at EVM_{rms} = -25 dB.

	This Work				[17]	[15]		[19]	[38]	[40]			[18]				[21]			
Technology	45nm SOI CMOS				55nm CMOS	40nm CMOS		40nm CMOS	45nm SOI CMOS	65nm CMOS			40nm CMOS				45nm SOI CMOS			
Architecture	3-Way Parallel-Series with No Main PA Load Modulation				Transformer-based 3-way Parallel -Series Doherty	Coupled-Inductor-based 3-Way Doherty		Digital Polar TX	Transformer-Based 4-Way Doherty	Broadband Doherty-Like Multi-Port			Balun-first 3-way Parallel Doherty PA				Coupler Based Parallel-Series Doherty			
Supply (V)	2				2.4	1.8		1	2	1.1			1.1				2			
-3dB S_{21} BW (GHz)	25-41 (48%)				25.9-32.6 (23%)	35.9-39.5 (10%)		24-31 (26%)	43.3-50.7 (15%)	N/A			23-28* (20%)				N/A			
Core Area (mm^2)	1.07				0.54	1.4		0.55[b]	0.81	1.35 (incl. pads)			0.77				1.55			
Freq (GHz)	26	30	37	40	28	38		29.5	47	28	37	39	26				26	33	38	40
Gain (dB)	14.5	14.9	13.7	13.7	16.1	15		N/A	17.1	15*	16*	17.5*	20				12*	15*	12*	13*
P_{SAT} (dBm)	21.4	22.6	20.2	19.1	25.5	18.9		18.7	24	19	19.6	19.2	20.7				23.5	24.1	22.8	22.7
OP_{1dB} (dBm)	21.1	22.2	20.1	18.7	24.3	18.4		N/A	23.7	19	16	18.1	19.5*				22.8	23.9	22.7	22.5
PAE_{1dB} (%)	28.4	37.6	22.8	20.9	24.4	23		36[c] (PAE_{max})	26.3	21.6	21.9	21.7	22*				27.6	38.2	26.8	26.2
PAE@9dB PBO (%)	16.1	18.2	11.3	10.4	18*	13.7**		26[c]*	18*	7*	13*	12*	7*				18*	29*	15*	12*
Modulation	5G NR FR2 1-CC 64-QAM OFDM				Single-Carrier 64-QAM	5G NR FR2 1-CC 64-QAM OFDM	5G NR FR2 2-CC 64-QAM OFDM	64-QAM OFDM (/w DPD)	5G NR FR2 1-CC 64-QAM OFDM	64-QAM OFDM			64-QAM OFDM				5G NR 1-CC 64-QAM		5G NR 1-CC 16-QAM	
PAPR (dB)	9.64				6	9.64	11.85	10.7	9.8	N/A			11.6				9.64		9.64	
Bandwidth(MHz)	100/200				250	100	100	300	2000	1000	2000		1000	800	400	200	100		400	
Freq. (GHz)	28	30	37	40	28	38		29.5	47	28	37	39	26				33		35	
EVM_{rms} (dB)	-25				-25.2	-25	-25.1	-27.58	-25	-22	-24	-23	-24	-24	-25	-27	-25		-20	
$Pout_{avg}$ (dBm)	10.2/9.5	11.8/10.5	12.1/10.0	9/8.04	17.7	11.3	10	7.9	14.1	7.5	9.8	9.1	9.4	9.8	9.4	9.3	14.3		16.6	
PAE_{avg} (%)	13.2/11	16.4/13.2	12.0/10.6	8.9/7.4	17.5	14.7	13.4	18[c]	13.7	5.1	10.2	8.5	15[c]	15[c]	14[c]	13[c]	25.2		26.4	

*Estimated from figures **9.6 dB PBO [c]Drain Efficiency [*]Excluding input balun [a]EVM normalized to peak signal [b]Core Area consisting of I/Q splitter, DPM, DPA, and SDC

Fig. 19. Comparison table.

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APPENDIX

The $\lambda/4$ transmission line expression (1) can be applied to determine V_{a1} as a function of I_m, which is

$$V_{a1} = -jR_{opt}I_m \tag{17}$$

Next, by applying (3) to (17) Z_{a1} is determined to be

$$Z_{a1} = R_{opt} \tag{18}$$

which is as expected, since both the Main and Aux1 PAs are the same size, and therefore should see the same optimum impedance at the peak power level. Next, since $I_C = I_o$ due to the series combiner, another application of (1) results in

$$-j\frac{2}{R_{opt}}V_{a2} = I_o \tag{19}$$

Furthermore, since $V_o = V_C + V_{a1}$, by combining (4), (5) and (17), V_o is calculated in terms of I_{a2} as

$$V_o = -jR_{opt}I_{a2} \tag{20}$$

substituting (20) into (19) and using the output boundary condition $V_o = I_oR_{opt}$ results in

$$Z_{a2} = \frac{V_{a2}}{I_{a2}} = \frac{R_{opt}}{2} \tag{21}$$

Again, this result is as expected, since the Aux2 PA is double the size of the Main / Aux1 PA, and therefore naturally requires an R_{opt} that is halved.

To derive the impedance seen by the main PA as a function of frequency at PBO, first we consider the schematic of Fig. 3 with both I_{a1} and I_{a1} set to 0. TL_2 is terminated with an open circuit, and therefore it introduces an impedance of $-jZ_o\cot(\theta)$ at the input of the lower transformer. Since the transformers are 1:1 ideal and connected in series, the impedance seen at the input of the upper transformer is $R_{opt} - j\frac{R_{opt}}{2}\cot(\theta)$. This because the same current flows through the load resistor and the impedance by TL_2, so their respective impedances are combined in series. Then, Z_{in} can be calculated as

$$Z_{in} = R_{opt}\frac{1 - j(\frac{1}{2}\cot(\theta) - \tan(\theta))}{\frac{3}{2} + j\tan(\theta)} \tag{22}$$

since the characteristic impedance is $Z_o = R_{opt}$ and the load impedance is $Z_L = R_{opt} - j\frac{R_{opt}}{2}\cot(\theta)$.

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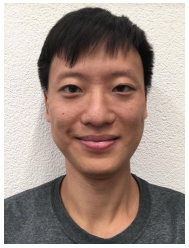

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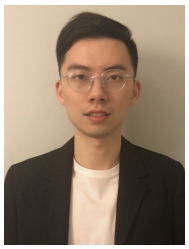

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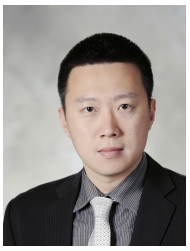

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