THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Design, Characterization and Modeling of GaN-based HEMTs for Low-Noise and Cryogenic Applications

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Abstract

Radio astronomy relies on detecting extremely weak signals and requires robust and rugged technologies, capable of preventing and withstand radio frequency interference (RFI). Low-noise amplifiers (LNAs) operating at cryogenic temperatures are key components in radio astronomy instrumentation. While LNAs based on advanced semiconductor technologies with limited power-handling capabilities have been widely used, gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) offer a promising alternative due to their high robusteness and excellent low-noise performance at room temperature. However, their low-noise behavior at cryogenic temperatures has remained largely unexplored.

This thesis investigates the potential of GaN-based HEMTs for cryogenic low-noise operation. The minimum noise temperature of GaN-HEMTs at 10 K was found to be in the range of 4–5 K (0.06–0.07 dB noise figure), which is comparable to other advanced technologies in the field. This was achieved through well-established experimental and modeling techniques, allowing for the characterization of noise contributions in GaN-HEMTs as a function of operating frequency, dissipated power, and total device periphery. The findings provide a foundation for designing future GaN-based LNAs that meet the requirements of cryogenic applications.

For the first time, GaN-HEMTs with superconducting niobium (Nb) gates were demonstrated. A comparative study with conventional gold (Au)-gated GaN-HEMTs revealed that superconducting Nb gates suppress the gate resistance dependence on gate width and length below Nb critical temperature ($T_c < 9.2$ K). However, self-heating effects were found to prevent the maintenance of Nb superconductivity at optimal noise-bias conditions, highlighting the need for further optimization of the device's heat dissipation capabilities.

GaN-based metal-insulator-semiconductor (MIS)-HEMTs with a silicon nitride (SiNx) gate dielectric were also examined at 4 K, demonstrating a minimum noise temperature of 8 K—comparable to their conventional HEMT counterparts under the same conditions. These results highlight the impact of the gate dielectric on the cryogenic small-signal and noise parameters of the device, suggesting that further reduction of gate leakage current through improved gate insulation could enable additional noise reduction.

The incorporation of gate field plates (FPs) was shown to improve device reliability by mitigating high-field and trapping effects, which become more pronounced at cryogenic temperatures. However, noise analysis of devices with and without FPs at 4 K revealed an overall detrimental impact of FPs, leading to at least a 35% noise degradation. This was attributed to increased parasitic capacitances, which reduced the cutoff frequency. Nonetheless, devices with FPs exhibited improved drain-source conductance, offering advantages for low-noise impedance matching.

Key words: Gallium Nitride (GaN), High Electron Mobility Transistor (HEMT), Cryogenic temperatures, high frequency, Low Noise Amplifier (LNA), Radio-astronomy, RFI.

List of Publications

Appended Papers

This thesis is based on the following papers:

[A] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "Noise Characterization and Modeling of GaN-HEMTs at Cryogenic Temperatures", IEEE Transactions for Transactions on Microwave Theory and Techniques, 2022. DOI: 10.1109/TMTT.2022.3226480.

[B] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Pavolotsky, A., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "GaN HEMT with superconducting Nb gates for low noise cryogenic applications", Physica Status Solidi A, 2022. DOI: 10.1002/pssa.202200468.

[C] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "A Cryogenic Scalable Small-Signal & Noise Model of GaN HEMTs", Proceedings of the 32nd IEEE International Symposium on Space Terahertz Technology (ISSTT), 2022. [online]: https://research.chalmers.se/publication/540402/file/540402_Fulltext.pdf.

[D] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "Comparison of the low noise performance of GaN HEMTs and MIS-HEMTs at cryogenic temperatures", 18th European Microwave Integrated Circuits Conference (EuMIC), Berlin, Germany, 2023. DOI: 10.23919/EuMIC58042.2023.10288670.

[E] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "Impact of the Gate Field Plates and Periphery on the Cryogenic Low-Noise Operation of GaN-HEMTs", 2025. Submitted.

[F] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Meledin, D., Sundin, E., Thorsell, M., Papamichail, A., Darakchieva, Rorsman, N., Joint, F., V., Belitsky, V. and Desmaris, V., "Cryogenic Trapping Effects in GaN-HEMTs: Influences of Fe-doped buffer and Field-Plates", 2025. Submitted.

Other Papers

The following publications are not appended at the end of the thesis due to overlapping content or due to content not related to the thesis:

[I] Mebarki, M.A., Ferrand-Drake Del Castillo, R., Pavolotsky, A., Meledin, D., Sundin, E., Thorsell, M., Rorsman, N., Belitsky, V. and Desmaris, V., "GaN HEMTs with superconducting Nb gates for cryogenic Low Noise applications", Compound Semiconductor Week (CSW), 2022, pp. 1-2.

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List of Abbreviations

2DEG	2-Dimensional Electron Gas
AlGaN	Aluminium Gallium Nitride
ALD	Atomic Lead Deposition
CT	Cryogenic Temperature
DSB	Double Side Band
ENR	Excess Noise Ratio
FET	Field Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
HEB	Hot Electron Bolometer
IF	Intermediate Frequency
InP	Indium Phosphide
LNA	Low Noise Amplifier
LPCVD	Low-Pressure Chemical Vapor Deposition
MIC	Microwave Integrated Circuit
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapor Deposition
PEALD	Plasma Enhanced Atomic Layer Deposited
PECVD	Plasma Enhanced Chemical Vapor Deposition
RFI	Radio Frequency Interference
RT	Room Temperature
SEM	Scanning Electron Microscope
Si	Silicon
SiGe	Silicon Germanium
SIS	Superconductor Insulator Superconductor
TCAD	Technology Computer Aided Design
VNA	Vector Network Analyzer

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1 Introduction

Advancements in instrumentation technology play a crucial role in driving scientific progress and discoveries. In radio astronomy, such developments enable scientists to extract increasingly precise and reliable data. This field focuses on observing distant cosmic objects and interstellar matter, with radio telescopes capturing faint electromagnetic signals emitted by astronomical sources. The detected signal intensity is typically very weak due to long-distance propagation and various attenuations mechanisms. As a result, highly sensitive instrumentation is essential. Sensitivity, defined as the minimum detectable signal variation in a radio-astronomy receiver, is primarily limited by noise. One fundamental constraint is the "sky-noise limit" an unavoidable background noise indistinguishable from the signal. However, electronic noise within the receiver itself can be minimized through technological advancements, thereby improving overall sensitivity.

Electronic noise refers to the spontaneous fluctuations of voltages or currents in a circuit. At a microscopic level, noise originates from the random motions of charge carriers and processes involving the charge carriers. One common metric to characterize noise is the equivalent noise temperature, given in Kelvins [K]. The concept of noise temperature derives from the analogy between an electrical noise source and blackbody radiation at an equivalent temperature $\mathrm{T_e}$, producing the same noise power over the same bandwidth. Hence, the equivalent noise temperature $\mathrm{T_e}$ is defined as:

$$\mathrm{T_e} = \frac{\mathrm{P_n}}{\mathrm{k_B B}} \tag{1}$$

Where $\mathrm{P_n}$ is the noise power, and B is the frequency-bandwidth. Thus, a lumped resistor presents an equivalent noise temperature equal to its physical temperature. An amplifier introduces its own intrinsic noise, which must be accounted for when evaluating system performance. To model this, an amplifier is typically represented as a noiseless device with a matched load having equivalent temperature that delivers the same noise power as measured at the amplifier output. The equivalent noise source, the matched load, is characterized by an equivalent noise temperature $\mathrm{T_e}$. The input noise source characterizes the amplifier's intrinsic noise contribution. Another common metric for characterizing noise is the noise figure (NF), expressed in decibels [dB]. The noise figure relates to the noise temperature by:

$$\mathrm{NF} = 10 \log_{10} \frac{\mathrm{T_e}}{\mathrm{T_0}} \tag{2}$$

Where $\mathrm{T_0}$ = 290 K, a reference noise temperature. The linear form of NF, known as the noise factor, represents the ratio of the signal-to-noise levels at the output and input.

To assess the impact of electronic noise on receiver performance, a common Figure of merit for evaluating radio receiver sensitivity of (S) is given by [1]:

$$\mathrm{S} \propto \frac{\mathrm{A_{eff}}}{\mathrm{T_{sys}}} \tag{3}$$

Here $\mathrm{T_{sys}}$ is the equivalent noise temperature of the system, $\mathrm{A_{eff}}$ is the effective signal-collection area, determined by the telescope dish antenna. According to equation (3), reducing the system's noise

Figure 1: Illustration of typical radio-astronomy receivers. (a): configuration used for frequencies up to around 116 GHz, (b): configuration used at f> 116 GHz.

temperature directly improves its sensitivity. Similarly, A_{eff} can be optimized by either increasing the size of the antenna or by forming receiver arrays, whose outputs can be combined into a single result.

Ultimately, the development of radio-astronomy receivers depends on continuous advances in low-noise technologies to push the limits of sensitivity and observational capability. Figures 1-a and 1-b show two common configurations of radio astronomy receivers. In both setups, the receiver consists of two main sections: the front-end and the back-end. The back-end processes the received signal, while the front-end is responsible for the initial signal reception and amplification. Thus, equation 3 mainly applies to the front-end to assess the system performance.

The front-end receiver consists of a chain of cascaded elements. The total noise contribution of such a system is calculated using the Friis equation:

$$T_{sys} = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + \cdots + \frac{T_n}{G_1 G_2 \ldots G_{n-1}} \quad (4)$$

Where T_i and G_i represents the noise temperature and gain of the i^{th} element in the cascade, respectively. The equation highlights that the noise contributions in the earliest stages of the receiver chain are most critical, particularly before the first Low Noise Amplifier (LNA), since the LNA's gain suppresses the impact of subsequent noise sources.

For detecting signals below ~116 GHz, the configuration in Figure 1-a is preferred, where the first LNA is placed immediately after the antenna. In contrast, for higher frequencies, the configuration in Figure 1-b is more common, where LNAs are placed after the mixer to handle intermediate frequency (IF) signals (< 20 GHz). These considerations drive efforts to optimize LNA noise performance and gain better understanding of its physical limitations.

To minimize thermal noise, radio-astronomy receivers operate at cryogenic temperatures (typically at 4 – 20 K) [2]. State-of-the art of cryogenic LNAs currently achieve noise levels of 3 to 5 times the fundamental quantum noise limit, defined as[1]: [3] $Q_L = hf/k_B$ For frequencies above 100 GHz and into the sub-THz range, the Figure 1-b configuration is dominant, as LNAs are not yet capable of operating at such high frequencies without excessive noise degradation. Instead, superconducting mixers, which can approach noise levels near the quantum limit ($\sim hf/k_B$) [4], are widely used. Two predominant superconducting mixer technologies are Superconductor–Insulator–Superconductor (SIS) mixers and Hot Electron Bolometers (HEBs). While offering superior noise-performance, SIS mixers are limited in frequency by superconducting material properties, with a typical cutoff near 0.7 THz for Niobium (Nb)-based SIS for example [5] [6]. On the other hand, HEBs, are theoretically not RF-frequency limited, but constrained by

[1]: In systems involving mixers operating in Double Side-Band (DSB) mode, the quantum limit of noise becomes $\frac{hf}{2k_B}$.

their IF bandwidth. Recent studies suggest that using GaN substrates can significantly improve IF bandwidth [7]. Therefore, in the long run, monolithic integration of cryogenic GaN-based IF LNAs with HEBs could enhance both the yield and performance of wideband, highly sensitive receivers.

Another critical factor in radio-astronomy receiver design is the dynamic range of signal detection. The configuration where LNAs occupy the front most position (Figure 1-a) provides a larger dynamic range and a wider IF bandwidth, since mixers have a more limited saturation power-level [2]. This allows for a more efficient mitigation of interference from unwanted signals, a phenomenon known as Radio-Frequency Interferences (RFI) [1], with excessively high-power signals that may be accidentally detected, posing a risk to receiver components. While state-of-the-art LNAs are typically based on III-V semiconductors, these materials exhibit limited dynamic range and low-power handling capabilities [8]. As a result, RFI can lead to a system failure or even permanent damage.

This challenge underscores the need for developing alternative LNA technologies that can simultaneously achieve low-noise performance while providing an enhanced robustness against RFI. In this regard, GaN emerges as a strong candidate, offering higher survivability under high-power condition compared to other semiconductors, while maintaining operation down to cryogenic temperatures.

Beyond radio astronomy, GaN-based LNAs also find applications in modern cryogenic systems that require high sensitivity, wideband operation and power robustness. Key applications include readout electronics for microwave kinetic inductance arrays [9] and quantum-computing systems [10].

1.1. HEMT technologies for low noise applications

Historically, Field-Effect Transistors (FETs) and parametric amplifiers were the technologies for low-noise amplification. However, the advent of High Electron Mobility Transistors (HEMTs) in 1979 marked a major breakthrough in the field [11]. In contrast to conventional transistors, HEMTs enabled high-speed charge transport. This translates to a higher gain and lower noise contribution at high frequencies. This was achieved using III-V compound semiconductors, with the first HEMTs based on Gallium Arsenide (GaAs). The key innovation in HEMTs was the spatial separation of ionized dopants from a conductive channel, forming a thin, highly dense electron confinement with high mobility: a triangular quantum well, also known as 2-D Electron Gas (2DEG). HEMT performance is determined by material properties and physical geometry. The second generation of HEMTs, based on Indium Phosphide (InP), enabled further improvements in low-noise performance, making them a preferred choice for many high-frequency applications.

In 1993, Gallium Nitride (GaN)-based HEMTs were first demonstrated [12]. GaN development was primarily motivated by its ability to sustain higher breakdown voltages, due to a wider energy bandgap (E_g), which is nearly three times larger than that of InP and GaAs. This inherent property enables superior high-power performance. Unlike III-V HEMTs, GaN-HEMTs do not require intentional doping, leading to key operational differences, which will be further discussed in chapter 2.

The microwave and low-noise performance of HEMTs is primarily determined by high channel conductivity and electron velocity. Channel conductivity depends on both the electron mobility and the 2DEG density (n_s). While GaAs and InP exhibit higher electron mobility than GaN, GaN-HEMTs compensate with a significantly larger electron density, with typical $n_s \sim 1 - 1.9 \times 10^{13}$ cm^{-2} against $0.2 - 0.4 \times 10^{12}$

cm^{-2} in their GaAs and InP counterparts. Thus, despite lower electron mobility, GaN-HEMTs achieve comparable conductivity due to their higher 2DEG density. Electron velocity, on the other hand, remains of the same order across these materials. Table 1 summarizes the key physical parameters at room temperature of commonly used semiconductors.

Table 1: Summary of the physical properties of Si, GaAs, InP and GaN bulk materials, at room temperature. The data were compiled from [8] [13]:

	SiGe	SiC	GaAs	InP	GaN
Electron mobility $[\mathrm{cm}^{-2}/\mathrm{Vs}]$	1500 – 2800	700	8500	5400	900 – 1100[2]
Electron saturation velocity $[\times 10^7\ \mathrm{cm/s}]$	0.1 – 1	2	1 - 1.3	1.9	1.5 – 2.3
Dielectric constant	14	9.7	12.9	12.5 – 14	8.9
Bandgap energy [eV]	0.94	0.945	1.41	1.35	3.49
Thermal conductivity $[\mathrm{W/cm-K}]$	1.5	3.5 - 4.5	0.5	0.7	1.3 – 1.5

Taking advantage of these properties, GaN has become a very promising material for high-frequency and high-power applications. Additionally, GaN-HEMTs can achieve excellent low-noise performance at room temperature, making them competitive with other LNAs technologies, while offering higher robustness and power handling capabilities, as recently reviewed in [14].

1.2. Cryogenically cooled HEMTs for low noise applications

The first cryogenic LNA based on the HEMT technology was specifically developed for a radio-astronomy receiver in 1985 [11]. A year after, this successful application led to the discovery of new interstellar molecules located ~400 light-years away [15].

The microwave low-noise performance of HEMTs improves at cryogenic temperatures primarily due to significant increase in electron mobility, enhancing charge transport and reducing contribution of the thermal noise due to an improved conductivity of metallic contacts and interconnects, minimizing parasitic resistance and losses. Moreover, a higher thermal conductivity allows for a denser circuit integration and reduces self-heating effects. Finally, superconductivity in Nb based devices, which occurs below ~9.2 K, further motivates the need for full cryogenic cooling in radio receivers.

Currently, state-of-the art cryogenic LNAs are based on Indium Phosphide (InP) [3]. GaAs-HEMTs, while slightly noisier, remain a costs-effective solution with broadband operation. Silicon-Germanium (SiGe)-based LNA can be used at cryogenic temperatures [16] too. In addition, superconducting parametric, and especially Traveling-wave-parametric amplifiers (TWPAs), were recently demonstrated with competitive noise performances at 4 K [17].

Cryogenic GaN-HEMT were shown exhibiting significantly improved electron mobility and 2DEG conductivity at low temperatures, [18] [19] [20]. However, determining the ultimate noise performance

[2]: In GaN-based HEMTs, 2DEG electron mobility is larger, typically ~1400 – 2000 cm^{-2}/Vs.

of cryogenic GaN-HEMTs requires detailed modeling and characterization of their microwave noise behavior at operational temperature. As further described in the next section, this thesis primarily addresses this part, so far lacking research efforts and information in the literature

1.3. Motivations and outline of the thesis

As discussed above, GaN-HEMTs combine high robustness with competitive low-noise characteristics, making them promising candidates for cryogenic applications, especially in radio-astronomy instrumentation and space applications. Using GaN-HEMTs in the first stage of front-end receivers could increase the power-dynamic range, reducing RFI-induced failure risks. Simultaneously, this may relax the need for extreme cooling, since cooling HEMTs below 10 - 15 K shows no major improvements in noise performance [21]. Furthermore, the integration of GaN-based IF-LNA may pave the way for a monolithic GaN HEMT integration with HEBs, taking advantage of their expanded RF bandwidth with a high-level of manufacturing repeatability and yield.

However, as the first step, the possibility of the GaN-HEMTs applications into low-noise and cryogenic instrumentation should be based on a prior characterization and modeling of their microwave and noise characteristics, power-consumption and frequency range of the intended applications. In a second step, the availability of noise model for cryogenic GaN-HEMTs, can be used to discriminate the limitation factors and design rules for their noise performance optimization at the same cryogenic temperatures.

This thesis investigates the cryogenic low-noise performance of GaN-HEMTs and approaches for its optimization. After the introductory chapter, the thesis is structured as follows:

- Chapter 2: Presents an overview of the physical principles defining the operation of GaN HEMTs. The cryogenic static and microwave characteristics of the technology are presented and analyzed.
- Chapter 3: Discusses charge trapping phenomena. Trapping effects in GaN-HEMTs at cryogenic temperatures are investigated, and design considerations for their mitigation are presented.
- Chapter 4: Provides an overview of existing technologies for cryogenic low-noise applications, their state of the art, and the added value of GaN-HEMTs in this field. After highlighting the need for accurate modeling of cryogenic noise behavior, physical and analytical approaches to achieve this task are presented.
- Chapter 5: Outlines the general procedure for measuring and extracting the noise characteristics of the device at cryogenic temperatures.
- Chapter 6: Presents a summary and analysis of the cryogenic noise model of GaN HEMTs. The model is used to investigate the potential benefits of minimizing noise sources in the device. This chapter also discusses the results of attempts to develop GaN-HEMTs with superconducting Nb gates. Additionally, the impact of incorporating gate field-plates and metal-insulator-semiconductor (MIS) structures are presented.
- Chapter 7: Summarizes the main conclusions and perspectives.

2 GaN-Based HEMTs Technology

GaN-based HEMTs are formed using III-Nitrides heterojunctions, with the upper barrier layer of a larger bandgap than the underlying GaN layer. The barrier is typically $Al_xGa_{1-x}N$ or $In_xAl_{1-x}N$, with different molecular fractions (x). The channel forms due to the conduction band discontinuity at the heterojunction interface, which can be described using Anderson's rules [22] [23]. The Fermi-level (E_F) aligns along the heterostructure, while the difference in electronic affinity between the materials creates a conduction band offset (ΔE_c) at the interface. Electronic affinity is a material constant, defined as the difference between E_c and the vacuum level. Since GaN has a lower electronic affinity than the barrier layer, the conduction band bends below the Fermi level on the GaN side of the interface. This results in the formation of a quantum well; a two-dimensional electron gas (2DEG), where charge carriers are confined and exhibit high mobility.

While doping is used to introduce carriers in other technologies, GaN-HEMTs do not require intentional doping. Instead, the accumulation of free carriers in the channel is obtained through intrinsic material polarization. In fact, spontaneous and piezo-electric types of polarization are inherently present in III-N materials.

In GaN, spontaneous polarization (P_{GaN}^{sp}) is due to the larger electronegativity of Nitrogen (N) compared to Gallium (Ga) atoms, with the asymmetry in the crystalline structure leading to an electric dipole moment along the growth direction. The orientation of spontaneous polarization determines whether the material is N-polar or Ga-face, depending on whether N or Ga atoms are present at the surface (Figure 2a). This thesis focuses on Ga-face GaN-based HEMTs, as they are the most commonly available, and, consequently, more technologically mature compared to N-polar [25] [22].

Piezoelectric polarization arises due to the lattice mismatch between GaN and the barrier layer, causing mechanical tensile strain in $Al_xGa_{1-x}N$ (P_{AlGaN}^{pz}) [8]. The relatively thick GaN layer is typically considered strain-free and, therefore, without piezoelectric polarization.

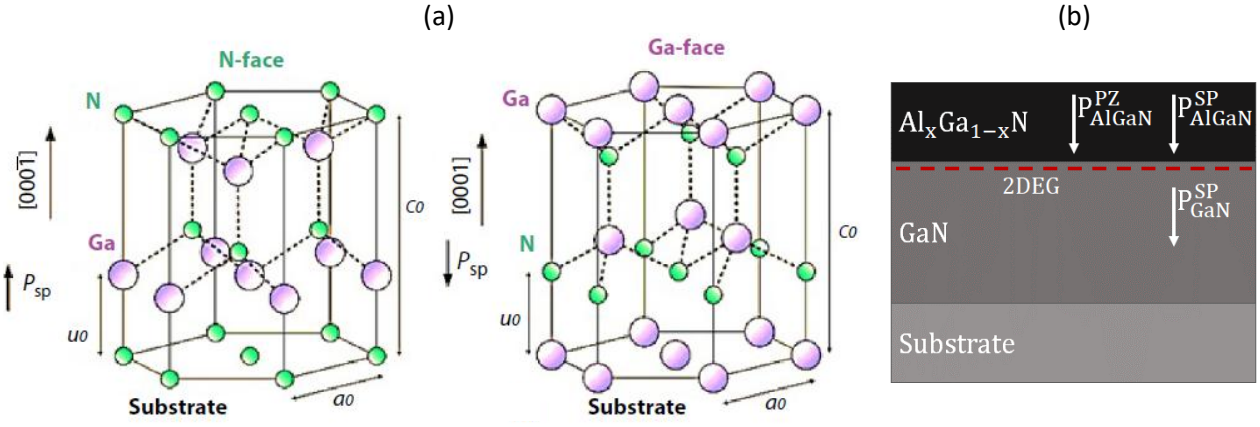

Figure 2: (a) Illustration of the lattice structure of GaN with Ga-face and N-face polarity. In Ga-face GaN, the spontaneous polarization vector points to the opposite direction of [0001] (c -axis)–after [24]. (b) illustration of (AlGaN/Ga-face GaN) heterojunction with the polarization-induced 2DEG in the GaN layer.

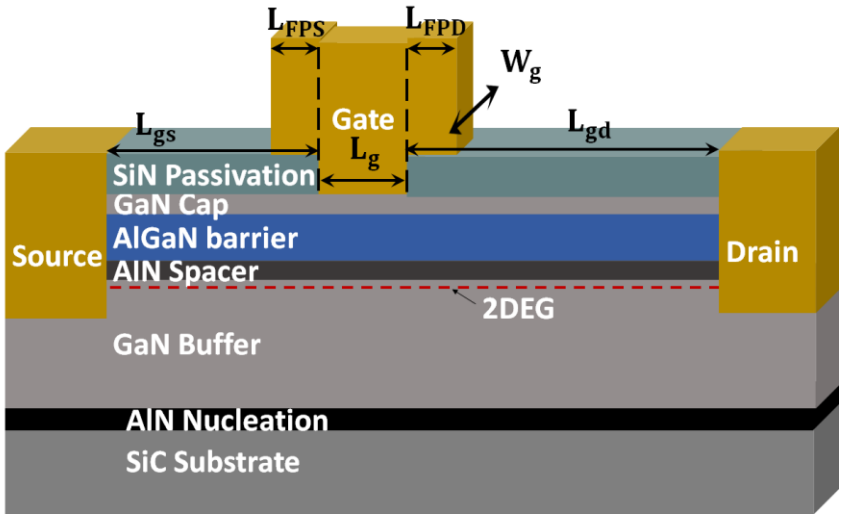

Figure 3: cross-section view of the epitaxial structure of the studied devices. The parameters L_g, W_g, L_{gs}, L_{gd}, L_{FPS} and L_{FPD} represent the gate length, gate width, gate-source distance, gate-drain distance, source field-plate length and drain field plate length, respectively.

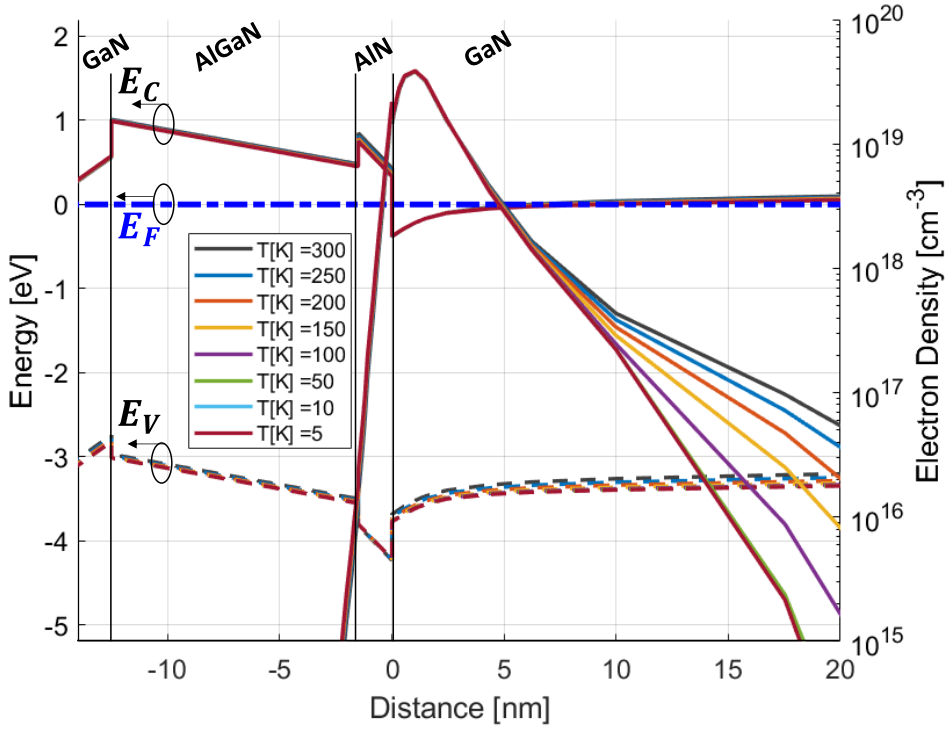

Figure 4: Spatial distribution at temperatures from 300 to 5 K along a vertical cutline from the cross-sectional view of the device of the electronic energy bands (left axis); the valence band (dashed lines) and the conduction band (solid lines), E_F (blue dashed lines), and the electron density (right axis, solid lines). The results were obtained using Sentaurus TCAD software.

The net polarization at the heterojunction interface is:

$$\sigma_p = P_{GaN}^{sp} - (P_{AlGaN}^{pz} + P_{AlGaN}^{pz}) \quad (5)$$

The 2DEG charge density (n_s) relates to σ_p and ΔE_c by [26]:

$$n_s \cong \frac{\sigma_p}{q} + \frac{\epsilon_0 \epsilon_b}{q^2 d_b}(\phi_b - \Delta E_c + \Delta) \quad (6)$$

Where d_b and ϵ_b are respectively the thickness and dielectric constant of the barrier layer, $\phi_b$is the Schottky barrier height of the gate contact and Δ is the penetration of the conduction band edge below E_F at the interface. The extraction of the spontaneous and piezoelectric polarization in III-Nitrides can be found in [27], based on linear interpolation from first-principles analysis.

While the inherent net polarization explains the accumulation of 2DEG carriers, their primary origin is ascribed to donor-like states present at the surface of the heterostructure, as introduced and commonly adopted from [28].

Typical 2DEG properties in cryogenic GaN-HEMTs are introduced in the following. A standard epitaxial structure is considered, similar to that of the devices studied in [A] and [B] (Figure 3). From top to bottom, these devices incorporate a GaN cap layer, $Al_{0.3}Ga_{0.7}N$ barrier, AlN spacer and a GaN buffer grown on AlN nucleation layer, on top of SiC substrate. Varying from the simple case introduced above, the addition of GaN cap layer has been shown to reduce the gate leakage and to improve high-voltage characteristics [29]. In addition, AlN spacer improves the 2DEG confinement by reducing its wave-function extension into the barrier [30]. A passivation layer is typically present at the surface, for protective purposes and to prevent surface-related trapping phenomena [31] [32].

Figure 4 presents the energy-band diagram and electron density under the gate, at different temperatures between 300 K and 5 K, calculated using physical simulations. Donor-like surface states were defined at the GaN-cap/passivation interface, as commonly adopted in the literature [33] [34]. These states were assigned a sheet density N_{SD} = 1 × 10^{14} cm^{-2} and energy level E_{SD} =0.2 eV, yielding 2DEG charge density n_s ~ 1·10^{13} cm^{-2} in line with experimental data reported in [B].

The obtained profiles highlight two main features:

1. First, no freeze-out of the carriers is observed down to cryogenic temperatures, unlike other semiconductor-doped technologies, for instance based on Silicon (Si), which may suffer from a dramatic drop of carrier density at low temperatures [35] [36]. Thus, this qualifies GaN-HEMTs for cryogenic operation.
2. Second, the carrier density presents a weak temperature-dependence, remaining nearly constant at low temperatures. This is in good agreement with experimental results reported for other GaN-based heterostructures [37] [38], highlighting the intrinsic structure stability within a wide range of temperatures.

The 2DEG sheet density and electron mobility can be experimentally obtained from Hall-effect measurements, using Van der Pauw structures [39]. Assuming unipolar charge transport and perfect confinement, i.e. no parallel buffer conduction, the channel sheet resistance (R_{sh}) relates to electron mobility (μ) and n_s by [39]:

$$R_{sh} = \frac{1}{q n_s \mu} \quad (7)$$

At room temperature (RT), n_s and μ are typically around 10^{13} cm^{-2} and 2000 cm^2/Vs respectively, as also found in [B]. The electron mobility is limited by scattering processes, affecting the carrier transport.

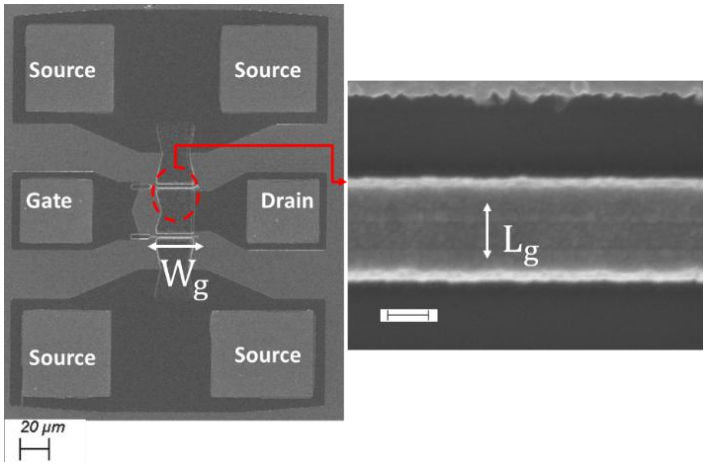

Figure 5: Scanning Electron Microscope (SEM) image of a fabricated device, the inset shows the gate finger is magnified. W_g and L_g refer to the width and length of the gate respectively. The sample presents a 2 x 25 µm gate periphery. From [B].

Thereby, reduced scattering enhances device high-frequency performance, and especially in terms of noise [40].

Cooling-down the device results in substantial reduction in phonon-related scatterings, reflecting lattice vibrations, otherwise dominating at room-temperatures in GaN-HEMTs [38]. In fact, at cryogenic temperature, GaN-based devices have been found mainly limited by a temperature-independent scattering due to interface-roughness [38] [41]. Consequently, electron mobility in different GaN-based heterostructures has been reported to increase by a factor of 5 – 7 at 4 K with respect to 300 K [19] [38].

2.1 Static operation

In the following, GaN-HEMTs featuring a two gate-fingers design are considered as shown in Figure 5. Figure 6 presents their typical DC characteristics at room temperature (RT) and cryogenic temperature (CT), of 295 K and 4 K respectively. Gate-source voltage (V_{GS}) modulates the channel electron density, while drain-source voltage (V_{DS}) drives the drain-source current (I_{DS}). Electrons accumulate in the channel even under no bias conditions. Increasing V_{DS}, I_{DS} rises linearly with electron velocity. The slope of this linear region defines the on-resistance, R_{on}, which is composed of the drain and source ohmic contact resistances, the access resistances and the channel resistance. The knee voltage (V_k) marks the saturation of electron velocity. In the saturation regime, I_{DS} is primarily controlled by channel density, which depends on V_{GS}. At fixed V_{DS}, the transconductance, g_m, characterizes the sensitivity of I_{DS} to the variation of V_{GS}:

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{8}$$

The output conductance is defined at fixed V_{GS} by:

$$g_{ds} = \frac{dI_{DS}}{dV_{DS}} \tag{9}$$

In the linear region of I_{DS} (V_{DS}), $g_{ds} = 1/R_{on}$. As will further be shown through the analysis of small-signal and noise model, design optimization for low-noise require minimizing both g_{ds} and R_{on}.

Applying V_{GS} below the threshold voltage, also called pinch-off voltage (V_{TH}), depletes the channel as the electrons are pushed away towards the substrate and no drain-current conduction is possible.

Upon cooling, a larger peak of the transconductance and a smaller on-resistance is typically observed, both are linked to increased electron velocity and mobility in the channel. The increase in electron mobility influences R_{on} through a lower channel resistance. Additionally, R_{on} improvement reflects the reduction in the ohmic and access resistances.

The transconductance is also influenced by the source access resistance, R_s, by:

$$g_m = \frac{g_{m-int}}{1 + R_s\, g_{m-int}} \tag{10}$$

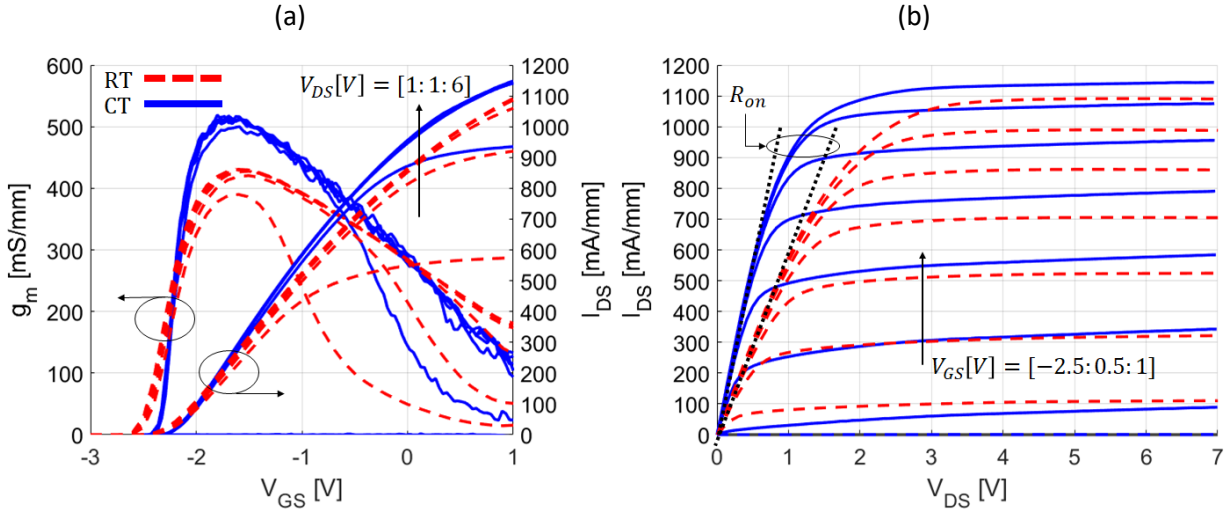

Figure 6 a) Variations of extrinsic transconductance, g_m, and the drain to source current, I_{DS}, with V_{GS}. b) I_{DS} (V_{DS}) curve at RT (dashed lines) and CT (continuous lines). Reproduced from [B].

where g_{m-int} denotes the intrinsic transconductance of the device. The intrinsic part of the device is defined as the region located beneath the gate contact. This distinction is further discussed the extraction of the small-signal model, in a later dedicated section. R_s is temperature-dependent, and in accordance with the variation of R_{on}, significantly decreases at CT, which also leads to improvement in the peak of the extrinsic g_m. The increase in the slope of g_m near the pinch-off also manifests the enhanced control of the gate over the channel, in line with the results from other cryogenic HEMT technologies [42] [3].

Considering the dominant impact of thermal noise in HEMTs, the reduction of the access resistances and the channel conductivity may contribute in large proportion to the improvement in high-frequency noise at CT. The increase in mobility and electron velocity leads normally to a larger maximum I_{DS}. However, charge trapping phenomena may lead to partial depletion of the channel at large V_{GS} and/or V_{DS}, resulting in degradations of electrical characteristics. Such anomalies were observed to be exacerbated at cryogenic temperatures in different HEMT technologies, and in paper [A], and are studied in chapter 3 in relation to trapping effects.

2.2 Small-signal operation and modeling

Although the transistor presents an inherently non-linear behaviour, its electrical response can be mathematically approximated to be linear upon input excitation around a fixed bias point. This principle defines the small-signal operation and is used to characterize the microwave properties of the device.

There are different approaches to describe the small-signal characteristics of the device [43]. Semi-empirical models are commonly used, as combining physical consistency with a relative simplicity. For these motivations, the results presented in this work were based on the approach proposed in [44].

Figure 7 shows the equivalent lumped model of the HEMT [44]. The model includes 17 elements. The subscripts g, s and d denote respectively the gate, source and drain. Arranged in a matrix form, the model

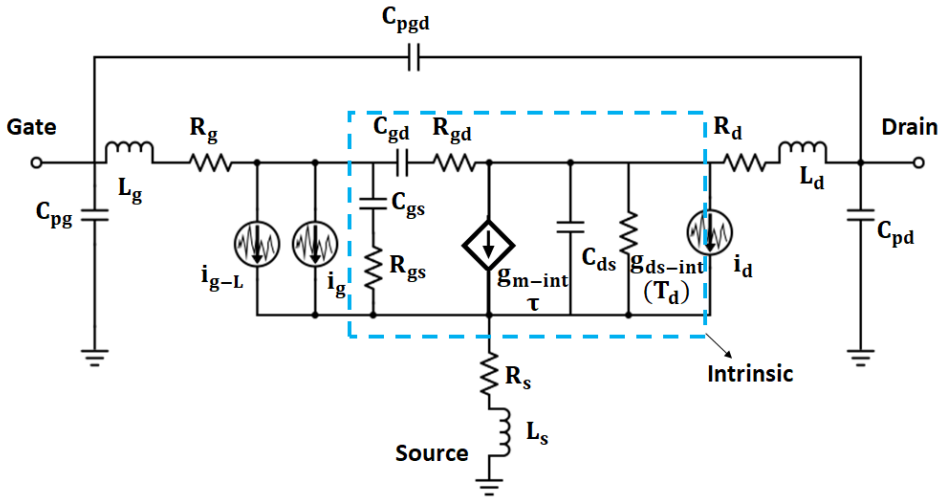

Figure 7: Equivalent small-signal model of the GaN HEMT [64]. The square with dashed-lines highlights the definition of the intrinsic device. The different current noise sources are illustrated; i_g, i_d, i_{g-L}, referring to those associated with the gate, drain and gate leakage.

is extracted by comparison to the measured S-matrix. The strategy for the extraction of these parameters relies on the distinction of an intrinsic part, which elements are bias-dependent. The remaining extrinsic elements are assumed bias-independent.

At V_{DS} = 0 V, the suppression of the voltage-current source (g_{m-int}) results in a simplified small-signal representation shown in Figure 8a, which is also called the cold-FET model. A more general representation can be found in [44] – Figure 2. For simplicity, the effect of the drain to source impedance is neglected in Figure 8a, considering full channel and sufficiently high-frequency conditions. The cold-FET model is typically used to extract the bias-independent elements, enabling the de-embedding of the intrinsic elements subsequently. For this purpose, the first task consists of removing the parasitic capacitances C_{pg}, C_{pd} and C_{pgd}, accounting for the coupling effects between the transistor and contact pads. These capacitances are obtained from the simplified circuit in Figure 8-b, which applies at bias conditions of $V_{GS} << V_{TH}$ and sufficiently low frequencies (usually <3 – 5 GHz), as these conditions allow neglecting the channel conductance, the series resistances and inductances. In this case, the Y-parameters are convenient to proceed with the extraction procedure of the parasitic capacitances, the following set of 3 equations is then obtained:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + C_{gsp} + C_{gdp}) \quad (11)$$

$$\mathrm{Im}(Y_{12}) = -j\omega(C_{gdp}) \quad (12)$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_{pd} + C_{dsp} + C_{gdp}) \quad (13)$$

Once the extrinsic capacitances de-embedded, the remaining bias-independent elements are conveniently extracted using the Z-matrix representation of the model in Figure 8-b. The parameters of the gate impedance are, first, extracted using an iterative procedure [44]. This was also detailed in [B].

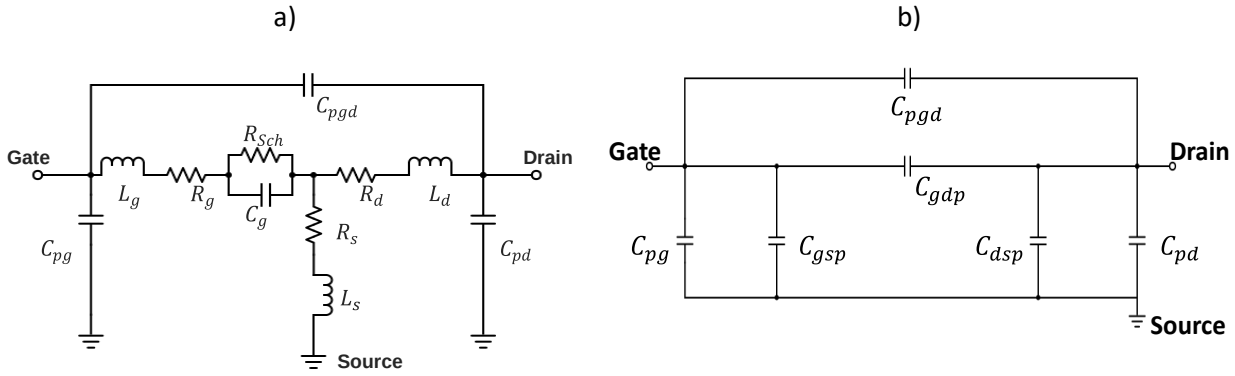

Figure 8: (a) Equivalent SSM at V_{DS} = 0 V b) Simplification of the model at $V_{GS} << V_{TH}$ and low frequency

The same applies to the source and drain resistances, which are obtained from the frequency-dependence of the Z-parameters.

Once the bias-independent element de-embedded, the intrinsic parameters from the model in Figure 7 are conveniently described using the Y-matrix as:

$$Y_{tot} = Y_{ext} + Y_{int} \tag{14}$$

Where Y_{tot}, Y_{ext} and Y_{int} are respectively the Y-matrix representations of the total, the extrinsic and intrinsic circuits. The fit of Y_{tot} to the Y-transform of the measured S-parameters, leads to the determination of the elements of Y_{int} as:

$$Y_{int} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{gs} + Y_{gd} & -Y_{gd} \\ -Y_{gd} - \dfrac{Im(Y_{gs})}{Y_{gs}^*} Y_{gm} & Y_{ds} + Y_{gd} \end{bmatrix} \tag{15}$$

Where:

$$Y_{gs} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{gs}} \tag{16}$$

$$Y_{gd} = \frac{j\omega C_{gs}}{1 + j\omega C_{gd} R_{gd}} \tag{17}$$

$$Y_{ds} = j\omega C_{ds} + g_{ds-int} \tag{18}$$

$$Y_{gm} = g_m e^{j(\frac{\pi}{2} - 2\pi f \tau)} \tag{19}$$

Figure 9 presents a comparison of typical measured and modelled S-parameters at a fixed bias point, V_{DS} = 5 V – V_{GS} = -1.1 V, at both RT and CT. This sample presents a total periphery of 2x25 µm. An excellent agreement of the model with the measurements over a large frequency range of 0.2 – 40 GHz is observed at both physical temperatures. Once a fitting of the model against measurements is achieved, the intrinsic

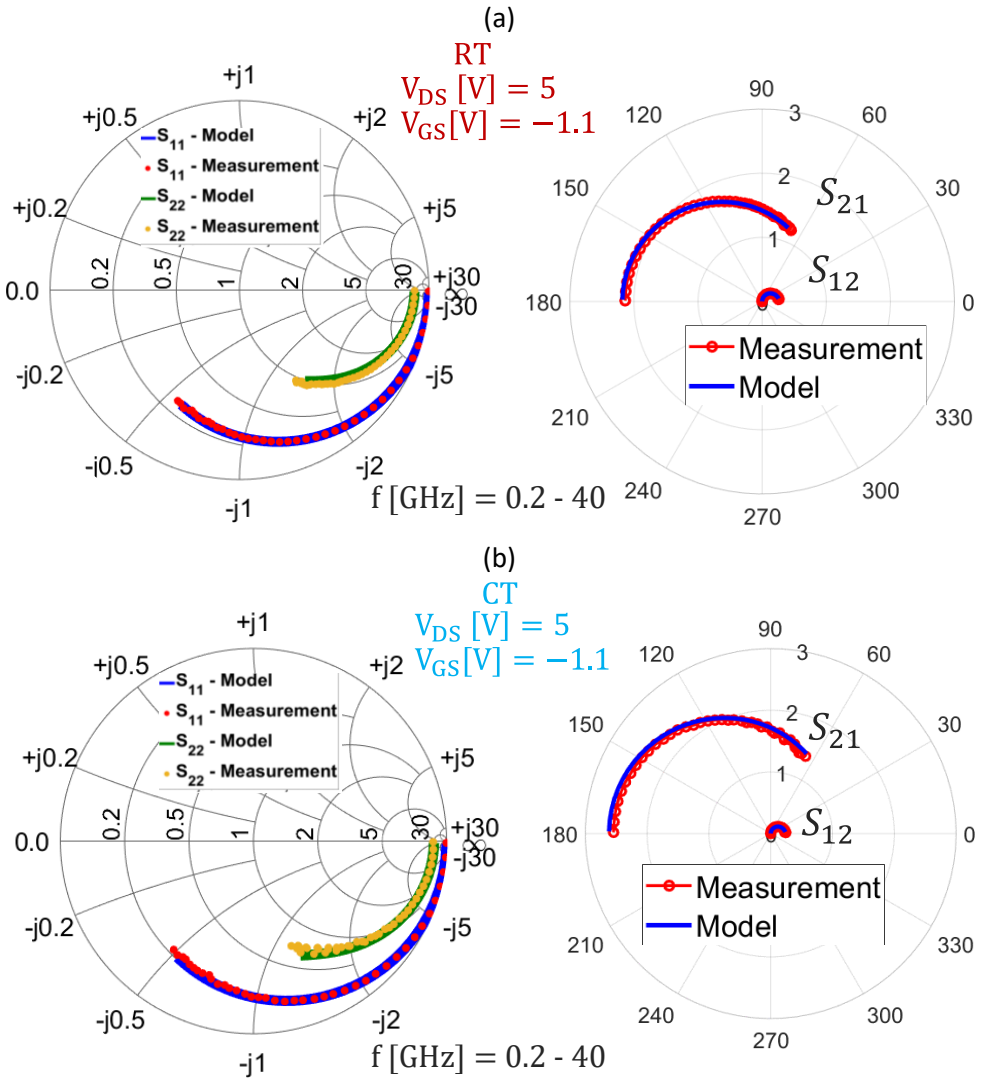

Figure 9: Comparison of typical measured and modelled S-parameters of a 2x25 µm device, at V_{DS} = 5 V and V_{GS} = -1.1 V over the frequency range 0.2 – 40 GHz at (a) RT (b) CT.

parameters can be determined from the frequency-dependence of the Y-transform of de-embedded S-parameters.

As one of the main parameters affecting noise performance, the intrinsic transconductance (g_{m-int}) was observed to increase significantly at CT. Additionally, a steeper slope of g_{m-int} after pinch-off is noted, indicating an enhancement of transport mechanisms in the channel and improved gate control over the channel due to device cooling (Figure 10a). The gate to source capacitance, C_{gs}, increases at CT as shown in Figure 10-b. The C_{gs}-I_{DS} characteristic is particularly temperature-sensitive, exhibiting a faster increase and earlier saturation at CT. The behavior of C_{gs} could be attributed to the temperature-dependent variation of material properties and carrier distribution, as previously observed in other III-V devices [45] [46]. The variation of C_{gd}, plotted in Figure 10c, is found to be less dependent on bias and temperature, suggesting relatively limited effects on noise performance. Together, these parameters determine the cut-off frequency, which is a key factor in the frequency dependence of noise performance. The intrinsic cut-off frequency, shown in Figure 10d, is defined by the equation:

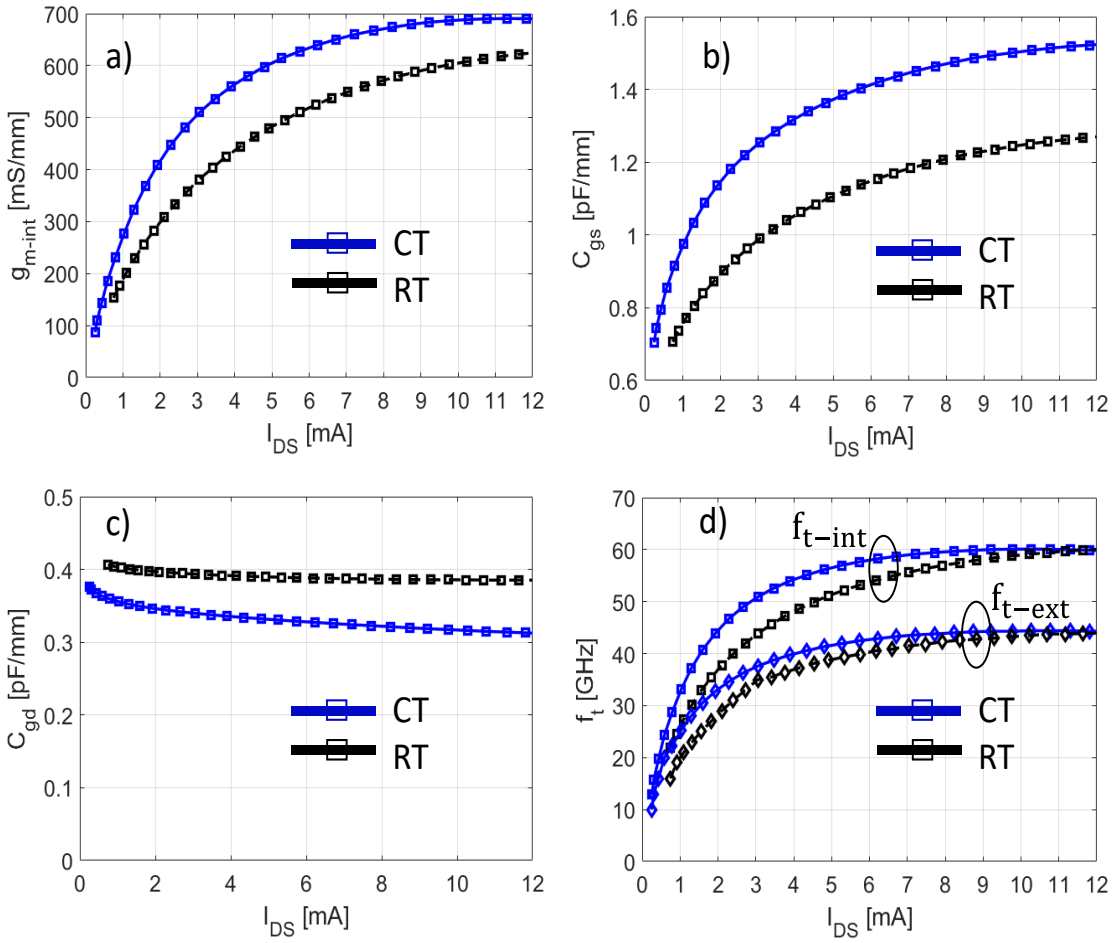

Figure 10: The current dependence at V_{DS}=5 V of the intrinsic small signal parameters at RT (black) and CT (blue). a) g_{m-int} b) C_{gs}, c) C_{gd} , d) f_t - reproduced from [A].

$$f_{t-int} = \frac{g_{m-int}}{2\pi(C_{gs} + C_{gd})} \tag{20}$$

An analytical approximation of the minimum noise temperature (T_{min}) relates to f_{t-int} by [47]:

$$T_{min} \sim 2\frac{f}{f_{t-int}}\sqrt{(R_s + R_g)T_g g_{ds-int}T_d} \tag{21}$$

Where T_d and T_g are the equivalent temperatures of the intrinsic drain- source and gate-source resistances, respectively. Equation 21 highlights the impacts of g_{m-int} and C_{gs}, through f_{t-int}, to which T_{min} exhibits direct proportionality.

The validity of the small-signal model can be verified using the following error function:

$$\epsilon_{ij}[\%] = 100 \times \frac{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}} - S_{ij_{modeled}}|}{\sum_{f_{min}}^{f_{max}} |S_{ij_{measured}}|} \tag{22}$$

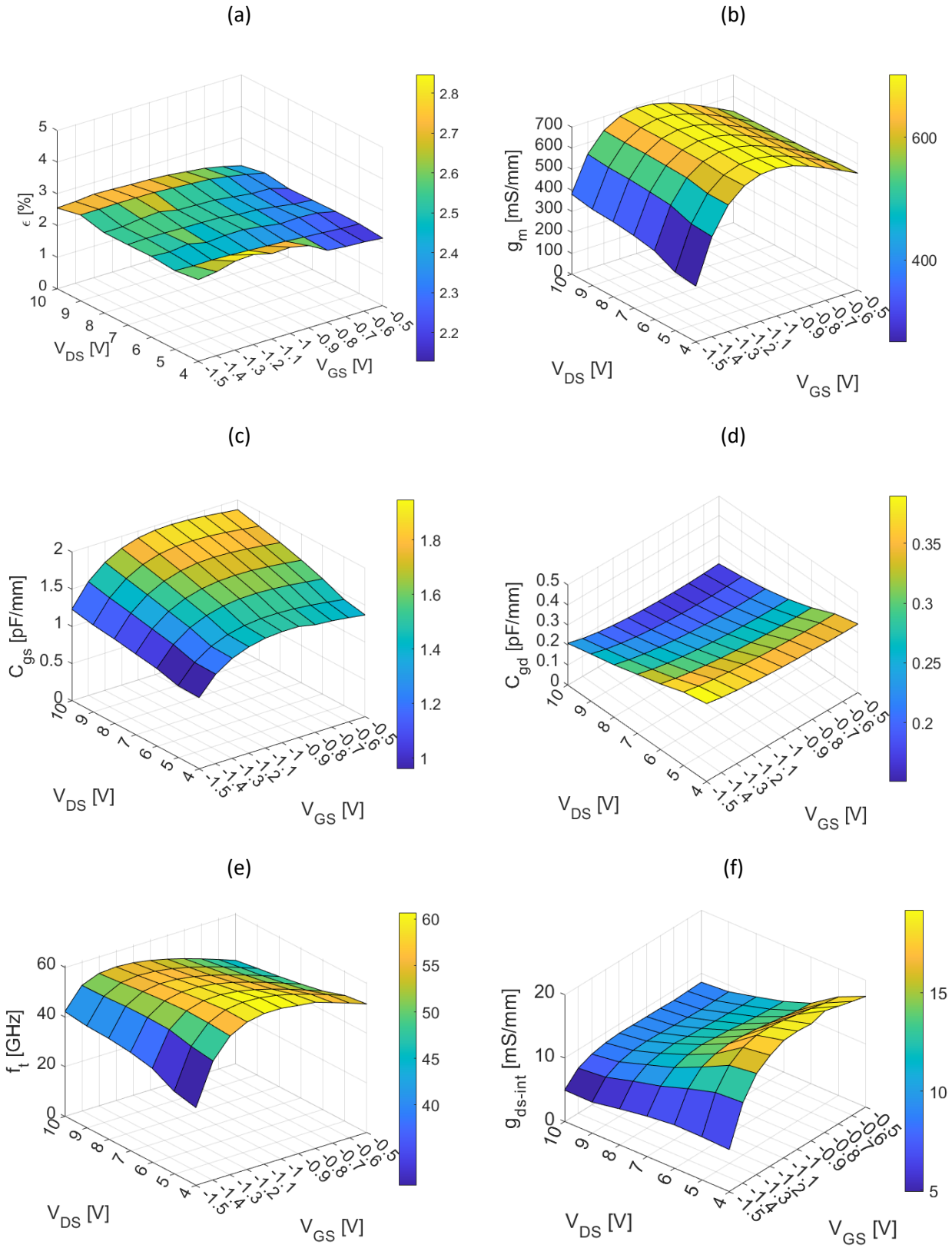

Figure 11: Bias-dependence, with respect to V_{DS} and V_{GS} of the parameters of the small-signal model at CT, reproduced from [A]: (a) The model error-function (b) g_{m-int} c) C_{gs}d) C_{gd} e) f_{t-int}f) g_{ds-int}.

where $S_{ij}{}_{measured}$ and $S_{ij}{}_{modeled}$ are respectively the measured and modelled S-parameters, i and j denote the port number, over the frequency range from f_{min} = 0.2 GHz to f_{max} = 40 GHz.

Figure 11a shows the variation of the error function as a dependence on the different bias points ranging from at V_{DS} = 4–10 V and V_{GS} = -1.5 – -0.5 V at CT, in the case of a 2x25 µm transistor studied in A. An average error in the range of 2 – 3 % was obtained in this case, which quantifies the accuracy of the model.

Additionally, the physical consistency of the model can be assessed by analyzing the variation of intrinsic parameters with both V_{DS} and V_{GS} (see Figures 11b–f). The variation of g_{m-int} exhibits only minor dependence on V_{DS}, reflecting the saturation of electron velocity (Figure 11b). C_{gs}, from a physical standpoint represents the parallel-plate capacitance formed between the 2DEG and the gate metal. As. V_{GS} becomes more negative, the channel depletes, resulting in C_{gs} to decrease near the pinch-off voltage due to the increased effective separation between the channel and the gate (Figure 11c). On the other hand, when the channel is present, increasing V_{DS} raises the electron velocity, increasing the probability of electrons approaching the barrier interface. This results in a reduced effective gate-channel distance. C_{gd} arises from the extension of the depletion region under the gate-drain region. Consequently, increasing the drain-to-source field leads to a decrease in C_{gd} (Figure 11d). Thus, the sum of C_{gs} and C_{gd} constitutes the total gate capacitance. Moreover, the gate capacitance also reflects the influence of field plate extensions from the gate metallization. Finally, g_{ds-int} reflects the channel conductivity and, as expected, saturates at high V_{DS} (Figure 11f).

2.3 Summary

This chapter provided an overview of the principles and electrical characteristics of GaN HEMTs, with a focus on their operation at cryogenic temperatures. The effects of various physical parameters on both static and small-signal performance were analyzed. A cryogenic small-signal model was extracted and validated across different bias conditions, laying the foundation for investigating the low-noise potential of these devices under the same temperature conditions in the following chapters.

3 Trapping mechanisms and cryogenic effects

Carrier trapping is a degradation mechanism that affects the electrical characteristics and device reliability. Although low-noise operation conditions typically minimize charge trapping, RF and noise instabilities in LNAs have been linked to charge trapping under eventual exposure to high bias or power stress. For instance, a study in [48] correlates trapping effects with gain and noise deterioration following exposure to power overloads. Other studies suggested a relationship between charge trapping and longer recovery times for RF and noise performances of LNAs subjected power stress [49] [50]. Trapping effects are primarily manifested by dynamic instabilities of the output characteristics under large V_{DS}/V_{GS} variations. Similar anomalies have been observed in cryogenic GaN HEMTs in [A] and [E], indicating enhanced trapping at low temperatures. Therefore, the characterization of trapping effects and analysing the dynamic behaviour of the device are essential to ensure an overall stable and reliable operation under cryogenic temperatures. Furthermore, a thorough analysis of the dynamic characteristics can help to discern the physical origins and locations of the traps. This, in turn, may guide the potential technological adjustments to prevent or reduce the impact of trapping.

Carrier trapping was observed across various HEMT technologies, since their early stages of development in the beginning of 1980s [51] [52]. In fact, trapping mechanisms are caused by defects at the atomic level, in the different layers and interfaces of the semiconductor devices. These defects consist of imperfections in the crystal lattice structure, that may be controlled or unintentional. Such defects relate, for instance, to the incorporation of dopants, presence of impurities, atom vacancies, dislocations… etc. An energy level E_T within the semiconductor bandgap is associated with these defects. When driven by the electric field, the electrons may be trapped at E_T. Hence, the term trap refers to defects, whose energy levels (E_T) are located between the edges of the valence and conduction bands. As depicted in Figure 12, the presence of a trap implies two possible periodic processes; carrier capture and emission. In HEMTs, the capture of electrons leads to the depletion of the 2DEG, which hinders its conductivity. Two types of traps are usually distinguished; (i) acceptor states, which are negatively charged when filled and otherwise neutral, and (ii) donor states, which are neutral when occupied and positively charged when empty.

In GaN devices, the existence of traps can relate to intrinsic defects, such as Gallium (Ga) vacancies and Nitrogen (N) interstitials. Additionally, impurities may unintentionally be incorporated, with their types and concentrations depending on the growth conditions. In GaN layers grown by MOCVD, such impurities especially involve Oxygen (O) and Silicon (Si) [53]. The latter act as donor states, affecting the semi-insulation character of the GaN buffer, leading to off-state leakage and short channel effects [54]. To address that, compensation doping in the buffer is commonly adopted using Carbon (C) or Iron (Fe), acting as acceptor states. However, intentional doping can also introduce traps in the buffer which can affect the device behaviour [55], as also shown in [F]. Moreover, donor-like states are present at the surface region and control the formation of the 2DEG (see chapter 2). To mitigate surface-related trapping, the incorporation of a passivation layer on top of the barrier has been proposed [31] [56]. However, later studies have shown that even with surface passivation, trapping may occur at the top surface or interfaces, under and near the gate metal [57].

Compared to other semiconductor technologies, GaN-based HEMTs are relatively more prone to trapping. In fact, GaN-based devices usually operate at large power loads and present large densities of defects. This is partly due to their emergence more than 15 years later than other semiconductor materials, implying a technological gap. Over the recent years, trapping effects in GaN HEMTs were significantly

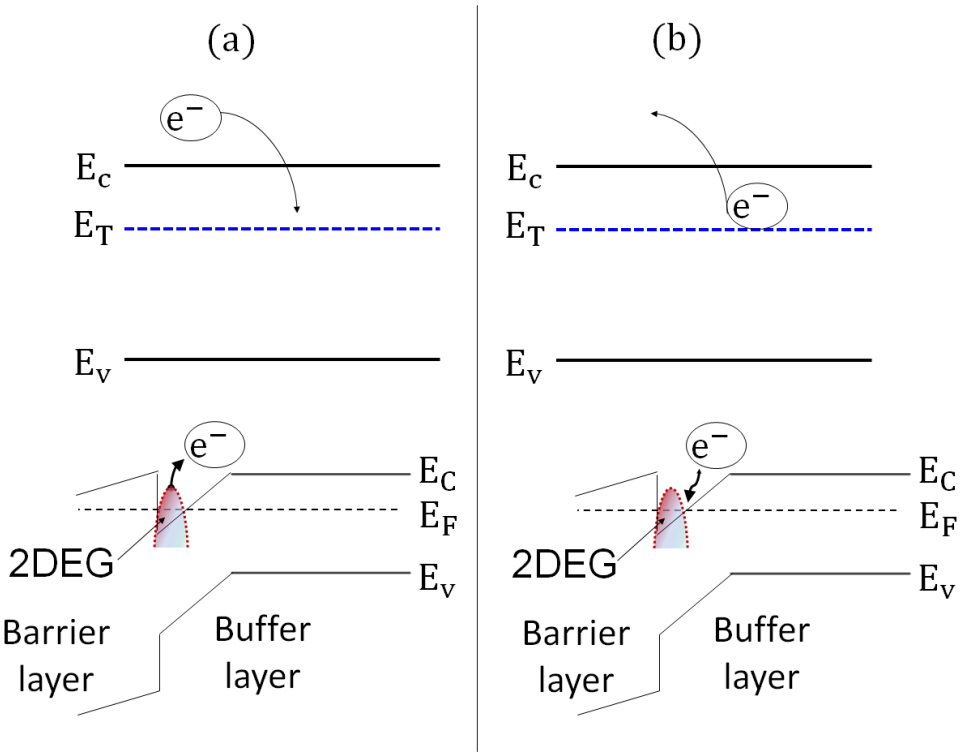

Figure 12: Schematic representation of the (de)-trapping processes of an electron from 2DEG by an acceptor trap state, determined by the energy level E_T. (a) Capture: under applied field, the electrons are trapped at E_T. (b) Emission: the field is switched-off, the trapped electron is released after return to thermodynamic equilibrium

reduced through optimized epitaxial designs and improved processing techniques [58]. Trapping in GaN-HEMTs under high temperature conditions has been extensively studied [59].

However, there are only few studies concerning trapping characteristics at low temperatures. In a study limited to 77 K, GaN HEMTs demonstrated enhanced trapping upon cooling down [60]. GaN MISHEMTs operating at 120 K exhibited large instabilities of the threshold voltage due to trapping at the surface of AlGaN barrier in [61]. Additionally, dynamic degradations of the output conductance in GaN-HEMTs at 100 K was linked to fluorine-based surface-treatment, which activated traps beneath the gate metal [62]. Moreover, trapping at cryogenic temperatures in GaN HEMTs was highlighted through low-frequency noise characterization in [63]. In [F], trapping effects in GaN-HEMTs were studied at cryogenic temperature down to 4.2 K, revealing increasing impacts of buffer-doping and gate design at low temperatures, enhanced by the slow-down of the emission rate of trapped electrons.

This chapter aims to provide an overview of the methods employed for the characterization of trapping mechanisms and effects, applied to the investigation of trapping behaviour in GaN HEMTs at cryogenic temperatures. The next sections present the principles and implementation of pulsed I-V tests and Drain Current Transient Spectroscopy. Based on established techniques, various cryogenic trapping mechanisms are identified and their effects quantified. Finally, the impact of different technological parameters is studied, aiming at further discerning the causes of trapping and possible solutions for its minimization.

3.1 Trapping Characterization

Different characterization techniques of trapping effects in HEMTs were proposed in the literature, based on the variation of metrics affected by trapping [64]. For instance, low-frequency noise [65], frequency-

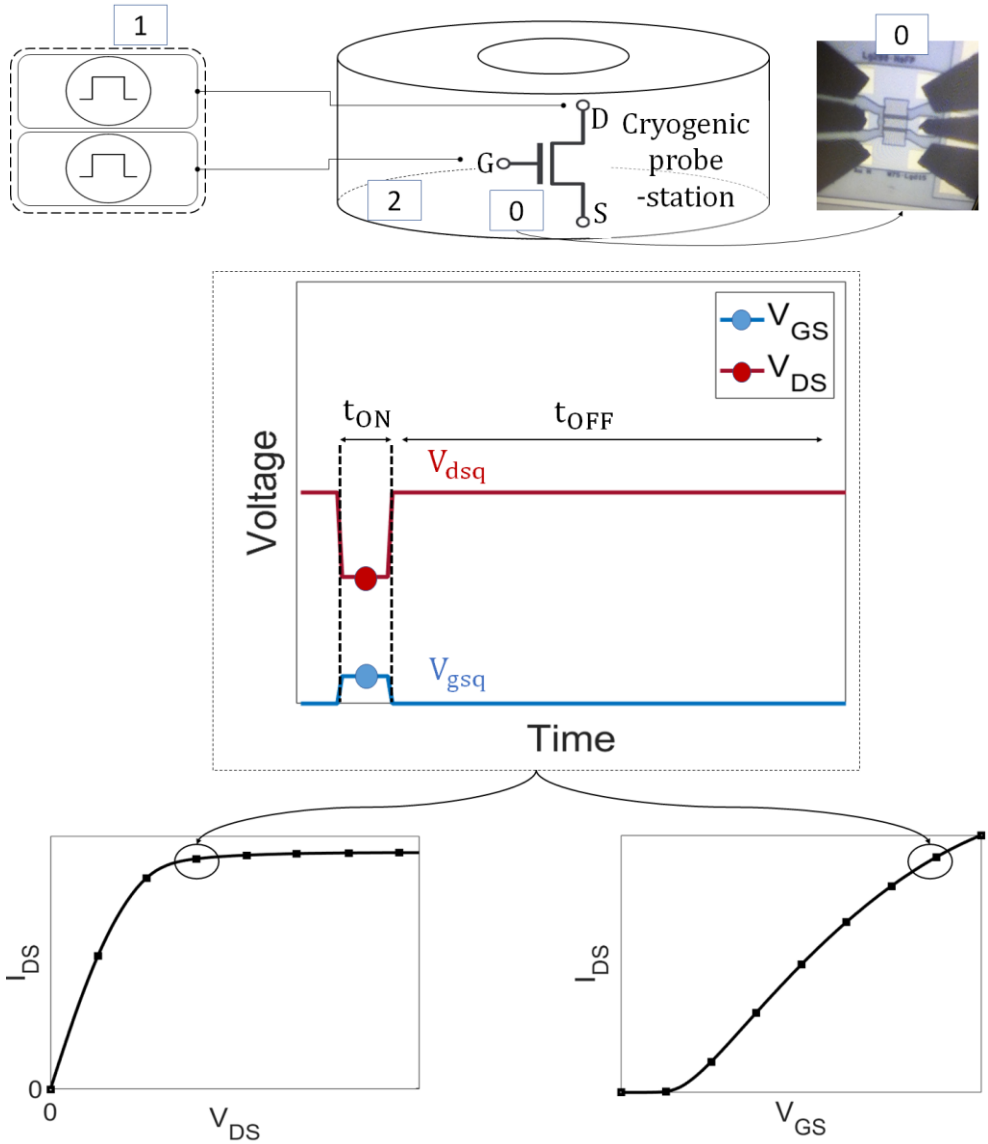

Figure 13 Upper part: schematic of the pulsed tests setup. A microscopic image of the device taken through the cryostat window in the cryogenic probe station is shown at the right (0). Pulsed voltages are applied using the AMCAD 3200 system (1). The temperature of the helium-cooled cryostat is controlled via an integrated heating system (2), from 4.2 – 295 K. Bottom part: Illustrative diagram of double pulsed I-V measurements. The gate and drain pulses are synchronously applied. The test begins with a quiescent state (V_{gsq}, V_{dsq}), for a duration t_{off}, followed by the on-state bias (V_{GS}, V_{DS}) for t_{on}. These steps are iterated to obtain the I_{DS}-V_{DS}/V_{GS} sweep curves.

dispersion of transconductance [66] as well as optical methods [67] can be used to probe the trapping activity. However, these techniques may require specific setups and instrumentation. For practical and reliable technology qualification at early stages after fabrication, on-wafer methods based on transient current measurements have been developed [68].

Based on this approach, two main methods are commonly employed and can be complementary to each other. First, the double pulsed I-V method is shown to relate transient characteristics to gate or drain-dependent trapping, allowing to quantify their effects [69]. Additionally, analysing the variation of these characteristics can provide insights into the location of traps [70]. Second, Drain Current Transient Spectroscopy (DCTS) provides the time-dependence of trapping processes [71]. This information enables

the retrieval of the defect energy levels and the identification of specific traps signatures. The principles and use of these two methods are presented in the next sections.

3.1.1 Double-Pulsed I-V

Double pulsed current-voltage (I-V) measurements are widely used to characterize the dynamic behaviour of HEMTs [68] [71]. Figures 13 presents a schematic representation of the double pulsed I-V acquisition. During these tests, the transient I_{DS} is collected as a function of both the pulsed V_{DS} and V_{GS}– hence the term "double pulse". The measurements are preceded by a quiescent-stress state (Q_i), defined by specific drain and gate voltages (V_{dsq}, V_{gsq}), that can promote carrier trapping. The full pulsed curve (I_{DS}-V_{DS}, V_{GS}) is thereafter obtained by iterating the procedure, with a short duty cycle that limits the self-heating effects. This approach enables the investigation of (de-) trapping processes by analysing the dynamic response of the device in terms of I_{DS}, R_{on}, V_{TH} and g_m. These measurements were employed at low temperatures, down to 4.2 K, to assess the impact of trapping mechanisms in GaN-based HEMTs under cryogenic conditions, as discussed in [F].

Typically, the methodology of these measurements relies on 3 quiescent configurations [72] [69]:

i) Reference test, Q_{ref}, of V_{dsq}= V_{gsq}= 0 V
ii) Gate voltage switching tests, Q_0, with V_{dsq} [V] = 0 and V_{gsq}<< V_{TH}
iii) Drain voltage switching tests, Q_N, with V_{dsq} [V]= N; N >0 and V_{gsq}<< V_{TH}

By comparing gate-lag and drain-lag tests to reference measurements, current reduction due to trapping controlled by either gate- or drain-fields can be distinguished respectively. The resulting relative current degradation is further referred to current collapse, while other terms are used for the same phenomenon in the literature such as current slump [72], given by:

$$Current\ Collapse = \frac{I_{DS}(Q_N) - I_{DS}(Q_{ref})}{I_{DS}(Q_{ref})} \quad (23)$$

The dynamic variation of on-resistance, noted ΔR_{on}, is calculated using a similar relationship between the Q_{ref} and Q_N measurements.

Gate-lag and drain-lag were commonly associated with surface- and buffer-related traps, respectively [72]. Therefore, identifying the field involved in the trapping can provide information on the location of the traps. As an illustrative example, a case study from [F] with rectangular gate and intentionally Fe-doped GaN buffer is considered here. The results in Figure 14b from the pulsed I-V measurements were performed at 295 K (RT) and 4.2 K (CT). Current collapse due to gate-lag is observed at both temperatures, indicating trapping at the surface region. Moreover, the gate-lag increases by a factor of more than 3 at CT, suggesting a larger density of trapped electrons compared to RT. Drain-lag is also observed with increasing V_{dsq}, pointing to the presence and activation of acceptor traps in the buffer. The drain-lag also increases at CT, showing a larger occupancy of these traps at low temperatures. The acceptor-like traps in this case were ascribed to Fe-doping in buffer, a conclusion further supported by DCTS measurements in [F].

In addition to the electric field, (de)-trapping dynamics can be promoted by light illumination. Conducting the pulsed measurements under different lighting conditions can be used to evaluate the recovery of the current conduction, trap occupancy of trap characteristics [73]. In GaN devices, variation in the pulsed

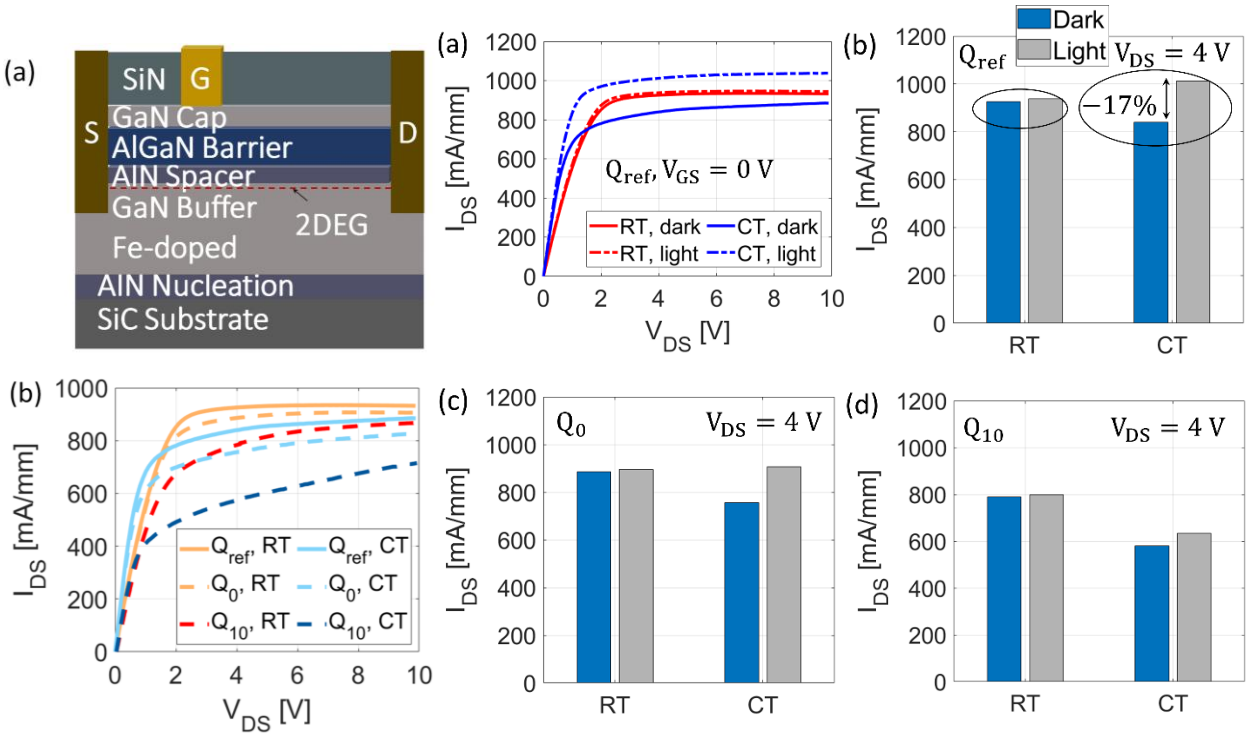

Figure 14: (a) Epitaxial structure of the device with rectangular gate and Fe-doped buffer. (b) Pulsed characteristics $I_{DS}(V_{DS})$ of the Fe-doped device without field-plates, at quiescent states, at RT and C, shown in shades of orange and blue, respectively. Reproduced from [F].

Figure 15: (a) $I_{DS}(V_{DS})$ at V_{GS} = 0 V, at Q_{ref}, in the dark (solid) and under illumination (dashed), at RT (red) and CT (blue). (b–d) Comparison of I_{DS} at V_{DS} = 4 V under the same conditions, at different quiescent states: (b) Q_{ref}, (c) Q_0 and (d) Q_{10}. Reproduced from [F].

characteristics under different wavelengths was shown to provide insights into the existence, the location and energy of the traps [74] [75]. Moreover, light illumination can serve as a useful tool at cryogenic temperatures to discriminate trapping effects. This is especially relevant at low temperatures when (de)-trapping tend to slow-down. For similar purposes, light exposure has been employed in the context of cryogenic measurements with GaAs and InP HEMTs [76] [77] [78]. In the case study from [F], cryogenic trapping effects in GaN HEMTs were also investigated using light illumination covering half of the GaN energy bandgap (~1.6 – 3 eV). As shown in Figure 15, light illumination had negligible influence on the RT characteristics, confirming limited trapping activity under these conditions. However, at CT, the maximum current reacted to illumination even without the involvement of electric field from the quiescent state. Light exposure mitigated trapping effects, leading to an increase in the maximum current at CT, enabled by enhanced electron mobility. On the other hand, the incident photons from the illumination influence the number of trapped carriers by facilitating the discharge of traps. This, in turn, modulates the number of electrons in the 2DEG, resulting in a stronger recovery of I_{DS}. These results suggest that the existent traps are more likely located at shallow energy levels, closer to the conduction band. The overall increasing in trapping activity at cryogenic temperatures is in qualitative agreement with reports on the cryogenic trapping effects in GaAs and InP-based HEMTs [79] [80], with comparable responses to light illumination observed in GaN HEMTs at other temperatures [75] [60].

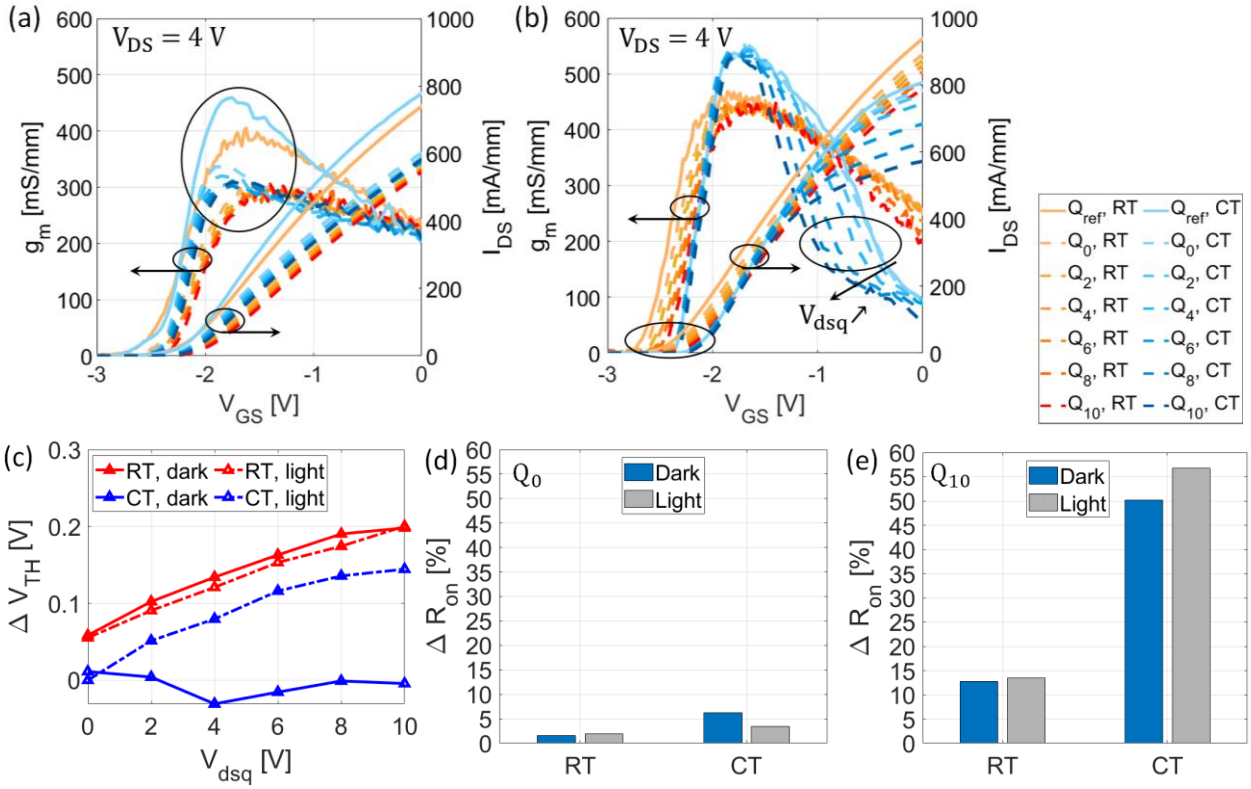

Figure 16: Pulsed I_{DS}, g_m (V_{GS}), at V_{DS} = 4, measured at different quiescent states (Q_0 – Q_{10}), at RT (dashed, graded orange) and CT (dashed, graded blue). Reference curves are shown as solid lines. (a) Example showing a drop in peak g_m, following Q_0. Reproduced from [F], for the case of the device with undoped buffer. (b) Example showing g_m degradation at high V_{GS}, increasing with V_{dsq}. (c) Variation of V_{TH} with V_{dsq} at V_{DS} = 4 V, at RT (red) and CT (blue), in the dark (solid) and under illumination (dashed). (d) Comparison of ΔR_{on}, at RT and CT, in the dark (blue) and under illumination (grey), at Q_0. (e) Same as (d) but for Q_{10}. The results shown in (b), (c), (d) and (e) are reproduced from |F], for the case of the device with Fe-doped buffer and without field-plates (FPs).

The analysis of the pulsed gate-dependent characteristics can also help to further identify the location of traps, particularly through the dynamic variations of the pinch-off voltage (V_{TH}) and transconductance (g_m) [81].

From the examples of V_{GS}-dependent pulsed characteristics shown in Figure 16, a positive shift in the pinch-off voltage is observed upon cooling-down, even in absence of quiescent stress. While a similar behaviour was also observed in other technologies and ascribed to improved 2DEG confinement [82], it may also indicate a higher density of captured carriers under the gate at CT. In which case, a lower level of the gate-field is required to deplete the 2DEG. At CT, V_{TH} is less sensitive to V_{dsq} in the dark. However, upon light exposure, V_{TH} increases with V_{dsq} in a similar trend as at RT. This could be due to an enhanced sensitivity to the electric field under illumination, with a higher initial density of free electrons in these conditions. In any case, the positive shift of V_{TH} supports the prior conclusion on the presence and filling of acceptor states under the gate, and particularly in the buffer due to the influence of Fe-doping [71].

The variation in the pulsed g_m may result from two trapping mechanisms, depending on which V_{GS}-region is most impacted. A reduced peak of g_m suggests trapping in the gate-source region, while a drop at large V_{GS} indicates trapping in the gate-drain side [81]. Figure 16a shows an example where the peak of g_m drops following a gate-lag test, indicating surface-trapping in the gate-source region. In the studied case earlier above, the peak of g_m exhibited negligible variation across the different quiescent states, at

both RT and CT (Figure 16b). However, at large V_{GS}, increasing V_{dsq}led to substantial drop of g_m at CT. Thus, this can be attributed to the enhancement of the peak of electric field on the drain side of the gate at higher V_{DS}, leading to an increased trapping in the gate-drain region. Consequently, the drain access resistance increases. As a result, the on-resistance is also significantly degraded at high V_{dsq}as shown in Figure 16d. Compared to RT, the degradation of R_{on} becomes ~3 times larger at CT, and this ratio rises up to 4 and 4.2 after Q_{10} in the dark and under light, respectively. This further highlights the temperature-dependence of the charge capture and emission processes. These properties are further examined in the next section using DCTS measurements.

3.1.2 Drain Current Transient Spectroscopy

While pulsed I-V tests allow quantification of trapping effects, additional time-dependent measurements are necessary to fully understand the trapping dynamics and the properties of the involved traps and processes. For this purpose, two electrical approaches, based on transient spectroscopy are commonly employed. The first method relies on capacitance measurements [83]. However, as transistor's dimensions continue to scale down, the resulting reduction in capacitances makes their direct measurement increasingly difficult [84] [85]. Alternatively, current-based techniques known as Drain Current (or -Level) Transient Spectroscopy (DCTS or DLTS) are used [68] [71]. DCTS relies on the same setup as double pulsed I-V tests, recording the time dependence of I_{DS} following the switching from a quiescent stress. Thereby, this technique provides the time constants of the carrier emission/capture processes. Furthermore, by performing DCTS at multiple temperatures, the traps can be characterized in terms of activation energy and cross-section. Ultimately, these measurements provide signatures of the traps, offering insights into their location and origins. In the following, the principles of this method and its implementation to investigate the trapping characteristics at cryogenic temperatures.

The relation between the dynamic response of the device and the capture and emission periods, governed by the trap characteristics, can be analysed based on the Shockley-Read-Hall (SRH) theory [40]. Considering a trap state, denoted by the subscript i, the probability of carrier emission is inversely proportional to its time constant ($1/\tau_i$). Upon the filling of the trap, the time constant for the release (emission) of trapped carriers relates to the characteristics of the trap by:

$$\tau_i = \frac{1}{\langle v_e \rangle N_c \sigma_i} exp\left(\frac{E_i}{kT}\right) \tag{24}$$

E_i and σ_i represent the activation energy and cross-section of the trap respectively. E_i is defined as the energy difference between the trap (defect) level and the bottom edge of the conduction band. Emission of electrons requires an external energy input, which can be supplied through either applied bias, light exposure or combination of both.
v_e is the average velocity of the electrons, and N_c represents the density of states in the conduction band, both are temperature-dependent:

$$\langle v_e \rangle = \sqrt{\frac{3kT}{m^*}} \tag{25}$$

$$N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{26}$$

Where m^* is the electron effective mass. Equation 24 indicates that the emission time of trapped carriers follows an exponential law with temperature. The emission is manifested by the recovery of I_{DS}, that is τ_i

marks the exponential increase of I_{DS}. This highlights the importance of performing DCTS measurements at varying temperatures, by tracking the variation of I_{DS} with time and temperature. In other words, one can retrieve the characteristics of the trap using the obtained variation of τ_i across a set of known temperatures. In fact, plugging equations 25 and 26 into 24, the latter transforms into:

$$ln(\tau_i T^2) = E_i \left(\frac{1}{kT}\right) + ln\left(\frac{h^3}{2(2\pi)^{\frac{3}{2}}\sqrt{3}m_e k^2 \sigma_i}\right) \quad (27)$$

Equation 27 now allows the extraction of E_i and σ_i from the slope and y-intercept, respectively, of the resulting Arrhenius plot ($ln(\tau_i T^2)$ vs. $(1/kT)$). Thus, through this equation, measuring the de-trapping time constants (τ_i) at different temperatures, the characteristics of the traps (E_i and σ_i) can be determined.

Previous studies have shown that inaccuracies in estimating the actual temperature of the device can lead to misleading interpretations of DCTS results [86]. Due to self-heating during on-state operation, the effective temperature of the device may differ from that of the cryogenic plate or the chuck temperature. Therefore, the effective temperature (T_{eff}) is considered by accounting for the thermal contribution from the self-heating of the device:

$$T_{eff} = T + R_{th}(I_{DS}V_{DS})/W_g \quad (28)$$

Here R_{th} is gate-width-normalized thermal resistance, which depends on the material properties, the epitaxial structure and geometry. In GaN HEMTs with similar epitaxial properties and dimensions, R_{th} has been reported to be in the order of 5 – 10 K·mm/W at 300 K [87] [88]. However, R_{th} presents a temperature-dependence with a reverse bell-shaped variation, improving by nearly up to an order of magnitude at low temperatures, with a minimum occurring in the temperatures range of ~ 40 – 80 K. [89]. This behavior was attributed to competitive thermal scattering processes, whose temperature dependences yield similar levels of R_{th} at 4.2 K and 300 K. Therefore, the effective temperature of the device presents an uncertainty, depending on R_{th}, the chuck temperature and I_{DS}.

3.1.3 Investigation of cryogenic trapping characteristics

To exemplify, DCTS results with quiescent conditions at Q_{10} are presented, as this condition resulted with the largest dispersions at cryogenic temperature in the previous section.

Figure 17 shows examples of the time evolution of the drain current, following a quiescent state Q_{10}, measured at physical temperatures of 45 – 85 K. Electrons capture hinders the current conduction, as promoted by quiescent stress, while the subsequent emission of trapped electrons leads to current recovery. Although taking the first derivative of I_{DS} (t) could provide indications about the de-trapping events, systematic noise in the measured data complicates such analysis. Moreover, multiple de-trapping phases may be involved, making it challenging to distinguish individual kinetics. To address that, a common approach for analyzing the measured transient data involves modeling the time-dependence of I_{DS} (t). To do that, different methods are proposed in the literature, including linear polynomial fitting and exponential fitting techniques [90] [68]. A comparative study of these methods in [71] highlighted an advantageous reliability of the model based on stretched multi-exponential fitting. Also, the latter is widely adopted in the literature to study similar technologies [87] [88]. For these reasons, stretched multi-exponential fitting model was employed in this thesis to facilitate the interpretation of the DCTS results

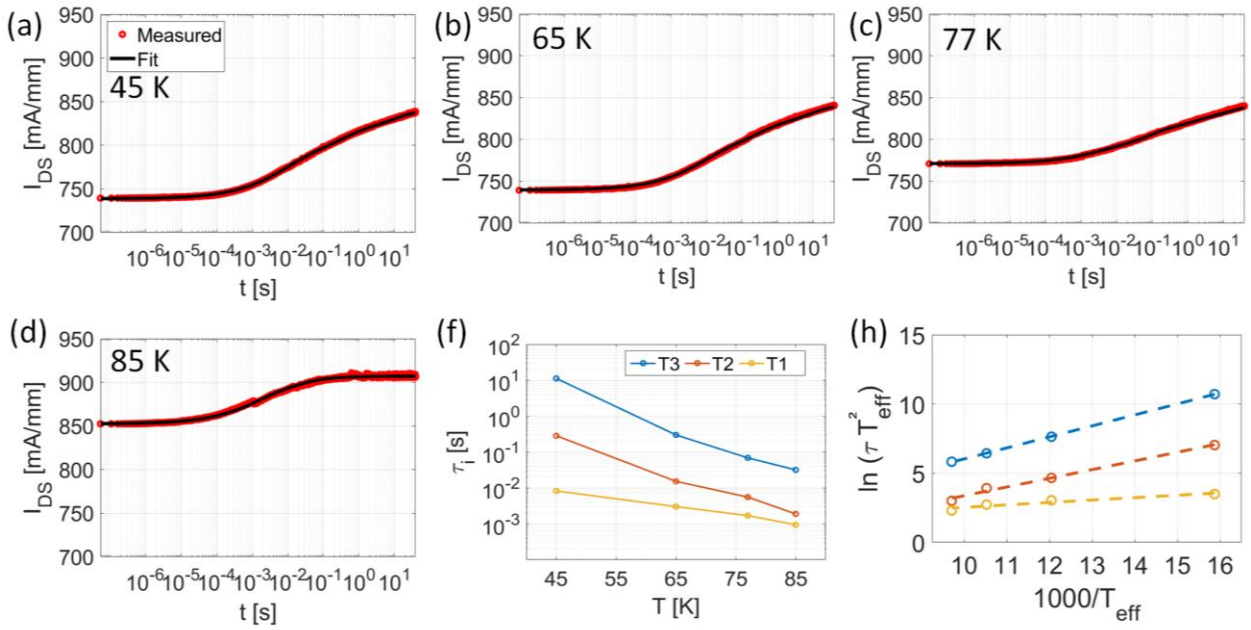

Figure 17: Results of DCTS measurements for the device with Fe-doped buffer and without FP. (a–d) Comparison of the measured and fitted I_{DS} transients at V_{DS}=4 V, at Q_{10}, at T = 45, 65, 77 and 85 K respectively. (e): Temperature dependence of time-constants of the emission time constants of the traps. (f): Extracted Arrhenius plot, showing ln (τT^2) vs. 1000/T. The slope of the curve indicates the activation energy the trap, while the y-intercept relates to the cross-section.

and was also applied in [F] to investigate the cryogenic trapping characteristics in GaN HEMTs. The model expresses I_{DS} (t) in relation to the emission time constant (τ_i) by the expression:

$$I_{DS}(t) = I_{DS,max} - \sum_{i=1-N} \alpha_i \, e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \tag{29}$$

With N the total number of characterized traps. α_i is the amplitude of recovered current over the emission phase and β_i is the stretching factor. The parameter β can also relate to the origin and location of the trap. For instance, a low β is typically associated with surface-related mechanisms such as hopping and tunneling [91].

In Figure 17, the measured and fitted I_{DS}(t) curves are compared at different cryogenic temperatures (45 – 85 K). The fit captures the evolution of I_{DS}(t) over the entire measured period, demonstrating the ability of this method to extract the emission time constants. Figure 17 also shows an example of extracted Arrhenius plot from the data presented in [F]. In this case, 3 traps (T1, T2, T3) were identified, with their characteristics summarized in Table 1 from [F].

All extracted traps present an increase in τ_i, demonstrating a significant slow-down in the emission rate of trapped electrons at low temperatures. This behavior explains the enhanced degradation of trapping effects over fixed time window at cryogenic temperature. Such a trend is predicted by the SRH theory, and is consistent with observations reported in other technologies [80] [60]. Nevertheless, trap T1 presents the weakest temperature-dependence and the lowest β factor (0.5), suggesting the contributions of non-thermionic process, such as hopping or tunneling, which are likely to occur at the surface region [87]. Furthermore, the energy activation of T1 (0.17 eV) falls within the same range of

surface-related traps reported in the literature [91]. Therefore, this may also explain the gate-lag effects in the previous section and which are attributed to surface trapping.

The DCTS results further confirm the influence of Fe-doping on the buffer-related trapping effects, revealing its exacerbation at cryogenic temperatures caused by the reduction in the associated emission rate. Indeed, the energy level of T2 (0.63 eV) aligns with that of the acceptor states stemming from Iron (Fe)-doping of the GaN buffer [85] [71], consistent with DCTS results from other GaN devices grown by MOCVD reported in [70]. Furthermore, the extracted activation energy of T2 is in close agreement with Fe-influenced traps in GaN observed using optical methods in [92]. In addition, the activation energy of T3 (0.79 eV) can be attributed to the intrinsic defects in GaN, such as effects of N interstitials or Ga vacancies [93]. However, due to temperature variation, T3 signature may also correspond to other Fe-related traps in the buffer [70].

Noteworthy, whereas the interpretation of the DCTS results relies on table-based identification of traps from data found in the literature, most of these were obtained at high temperatures due to a research gap around the cryogenic trapping effects in GaN HEMTs. However, due to the temperature-dependence of the energy bandgap [94], trap energy states may shift at low temperatures. In fact, the temperature dependence of the GaN bandgap is given by:

$$E_g(T) = E_{g,0} + \frac{aT^2}{b+T} \tag{30}$$

Where $E_{g,0}$ = 3.495 eV is the bandgap energy at T= 0 K, a and b are empirical parameters that were experimentally determined in [95]. The energy bandgap of GaN was estimated to increase by 0.07 – 0.08 eV within the studied temperature range (4 – 85 K) relative to its value at 300 K, based on the data found in [95]. Therefore, this quantifies an additional uncertainty in the interpretation of the results of the activation energy of the traps at cryogenic temperatures.

3.2 Exploring the impact of technological parameters on trapping effects

The methods and techniques presented above can help the technologists and designers in developing optimized structures and layouts, able to prevent or overcome trapping-related limitations. For this purpose, different technological solutions were elaborated in the literature [96]. For instance, the mitigation of surface-related trapping has been investigated using different passivation techniques and materials such as SiN_x, SiO_xN_y and SiO_2 [31, 56] [97]. To reduce the impact of buffer-doping responsible for trapping, back-barriers to the channel electrons were proposed by introducing an additional layer below the 2DEG. Such schemes were obtained using different materials with large bandgap such as InGaN [98] and AlGaN [88]. For the same purpose, field-engineering have been demonstrated using structures with graded-polarization profiles [99] [100].

However, prior to processing optimization, more precise insights can be gained by systematically including or excluding specific technological factors to either promote or mitigate particular trapping effects. This approach has been employed to further pinpoint the location of trapping mechanisms in GaN HEMTs at cryogenic, based on the results reported in [F]. Through comparative studies of devices with different buffer and gate structures, the next two sections deal with the influences of and the incorporation of extended gate field-plates at the surface, and the absence of doping in the buffer.

3.2.1 Gate field-plates

Gate field-plates (FPs) were originally employed with GaAs MESFETs and HEMTs to mitigate the charging of surface traps by modulating the electric field distribution, thereby enhancing high-voltage performances [101]. The integration of FPs into GaN HEMTs has been shown to improve the power performance, mitigate reliability issues and increase the breakdown voltage [102].

The design of FP primarily aims to achieve a more uniform electric field distribution near the gate, and especially along the direction of the 2DEG confinement and around the drain-edge of the gate where the peak field typically occurs. Since traps charging is driven by the injection of electrons through the applied electric field, reducing the peak field can prevent the trapping of the 2DEG carriers [103]. Figure 18 illustrates the modulation of the lateral electric field (along the x-axis) by the gate FP, using TCAD simulations of structures with the same epitaxy and dimensions of the case study from the previous section (Figure 19a). The electric field distributions in devices with and without FP are compared at V_{DS}= 10 V, at different depth below the channel junction (5 – 50 nm). When the FP is included, the 0.2-µm gate extends symmetrically by 0.2 µm towards the source and drain. For a device without FP, the electric field shows a single peak at the drain edge of the gate. In contrast, with FP, the field distribution presents two distinct peaks, both of which are of reduced amplitude compared to the single peak without FP.

Based on the results reported in [F], a comparison of the unstressed tests shows no signs of unstable saturation as in the case without FP, leading to a larger maximum I_{DS}at CT than at RT (Figure 19a). This underscores a stronger impact of FPs at cryogenic temperatures in mitigating trapping, whose effects would otherwise counteract the improvement in carrier transport within the 2DEG upon cooling, as also evidenced by the enhancements in R_{on} and g_m (Figure 19b). Compared to the case without FP, the gate-lag and its aggravation at cryogenic temperatures are substantially reduced when the field-plates are included. The degradation of the dynamic on-resistance (ΔR_{on}) is also prevented by up to a factor of 3.9 at Q_{10} (Figure 19c). Consequently, g_m remains nearly insensitive to off-state stress. This demonstrates

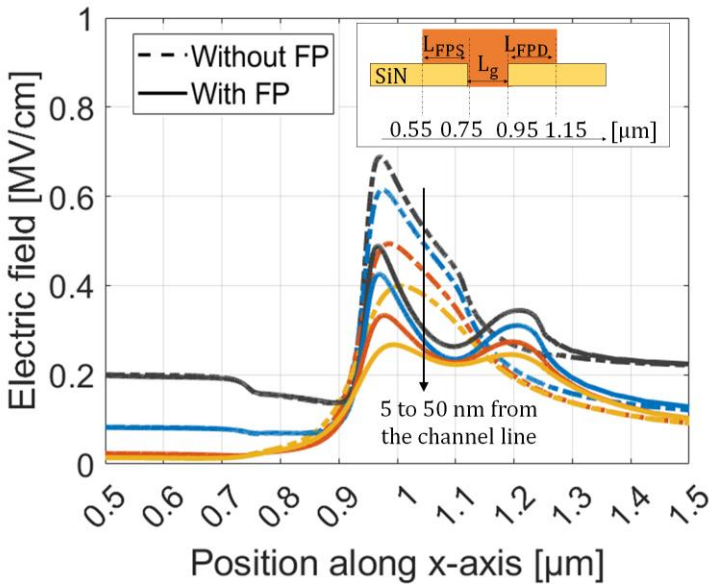

Figure 18: Comparison of the spatial distributions of the lateral electric field obtained from TCAD, at 5, 10, 25 and 50 nm below the channel junction, in the case of a device with (solid lines) and without gate field plates (dashed lines). The inset shows the position and dimensions of the gate, including the field-plates.

that

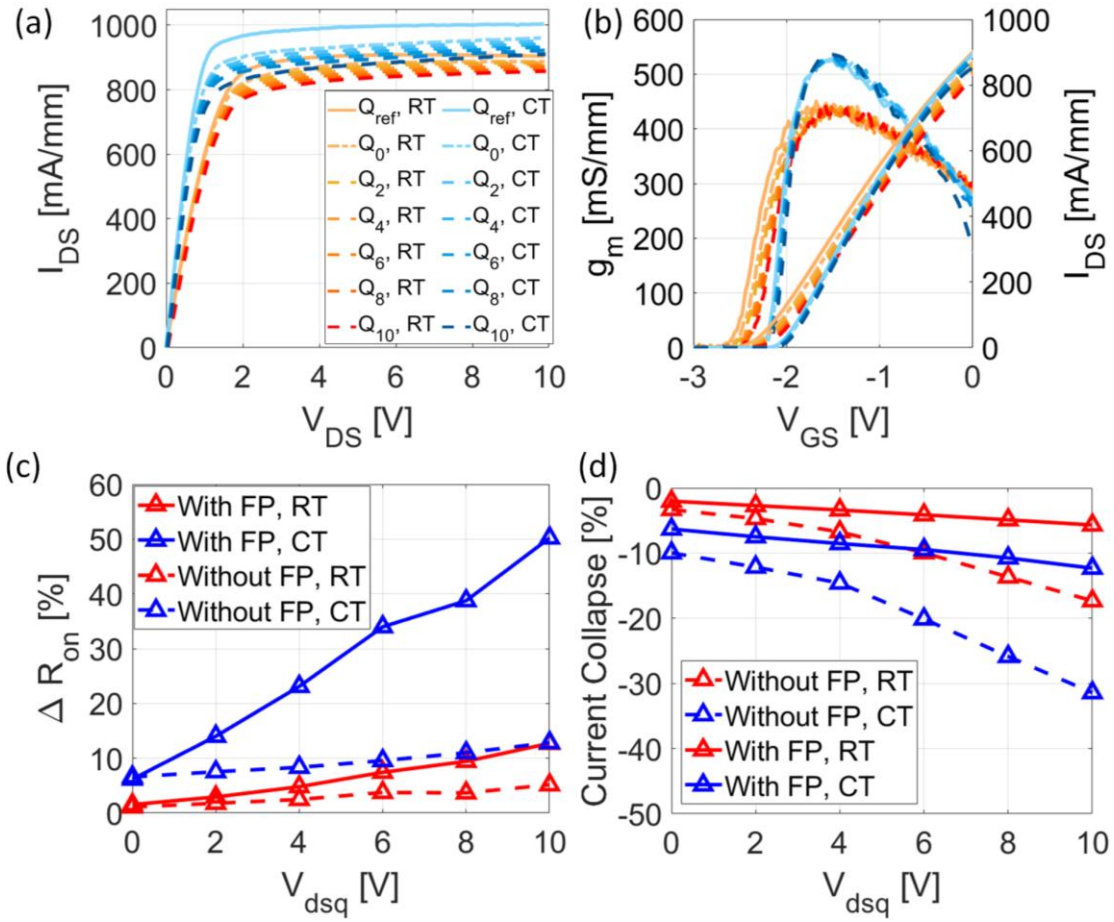

Figure 19: (a) Pulsed I_{DS}-V_{DS} characteristics of the devices with gate field-plates, at RT and CT at different quiescent states. (b) Variation of the pulsed I_{DS} and g_m with V_{GS}, of the same device under the same conditions. Comparison of the variation with V_{dsq} of the at RT (red) and CT (blue) in the devices with (solid lines) and without FP (dashed lines) of (c) dynamic $\Delta R_{on,}$ and (d) the current collapse ratio. Reproduced from [F].

FP effectively suppresses trapping at the surface and in the access regions, though its influence on electric field, similar to its action as at RT, but with more pronounced impact at cryogenic temperatures.

The field-plates also prevent buffer-related trapping. By modulating the vertical expansion of the electric field below the channel, the FP influences the density of trapped carriers in the buffer [104]. As depicted with TCAD in Figure 18, the FP limits the penetration depth of the electric field into the buffer, reducing the probability of carriers capture by lowering the free electrons density in the buffer where Fe-related acceptor traps are more likely to be present. In fact, based on the results from [F], the FP reduces drain-lag by a factor of 2 and up to 2.6 at RT and CT, respectively. Furthermore, at CT, the FP reduces the sensitivity of current collapse to V_{dsq} by up to 18% as indicated by the slope of the measured data in Figure 19d. Thus, the FP-influence on the electric field gains more importance at low temperatures as the mobility of electrons increases, and the emission rate of captured electrons is reduced. However, it is important to note that the integration of a FP can degrade the low-noise performance at cryogenic temperatures due to increased parasitic capacitive effects, as shown in [E]. Therefore, while these results demonstrate a strong potential of minimizing the cryogenic trapping effects in GaN HEMTs using FP, further optimization of this type of gate design may be necessary to enable a better compliance with the requirements of high-frequency and low-noise cryogenic applications. This aspect is discussed in more detail in a dedicated section in this thesis.

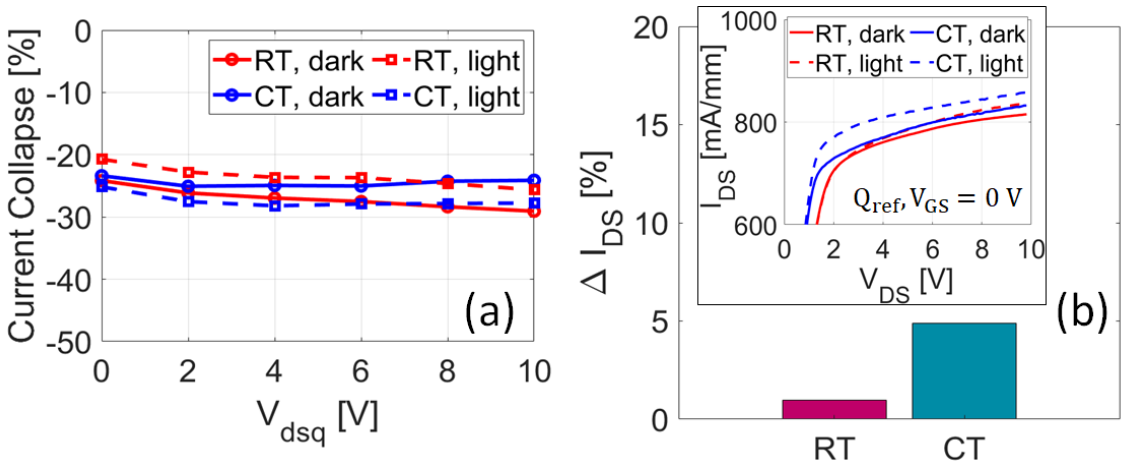

Figure 20: Variation of the current collapse with V_{dsq} in the device without Fe-doping in the buffer, at RT (red) and CT (blue), in the dark (solid) and under illumination (dashed). (b): Relative variation of maximum I_{DS} (V_{GS} = 0), at RT and CT, due to light illumination with respect to respective measurements in the dark. The inset shows the reference measurements of the saturation current the same conditions.

3.2.2 GaN-buffer without Fe doping

The results from the previous section indicate that the intentional Fe-doping in the GaN buffer is associated with electron trapping, with these effects significantly increasing upon cooling-down to cryogenic temperatures. While the introduction of acceptor states aims to enhance the power performance at high frequencies [4], these results raise the question of whether removing intentional doping offers a better trade-off for cryogenic applications.

To investigate this, a similar epitaxial structure to that shown in Figure 20a was studied, but without intentional doping in the buffer. Cryogenic pulsed measurements from [F] reveal that undoped devices present no drain-dependent current collapse at 4.2 K (Figure 20a). This univocally demonstrates that buffer-related trapping is suppressed in the absence of Fe-doping at cryogenic temperatures. Prior reports suggest that the ~0.5 – 0.6 eV traps in GaN at RT and higher temperatures, also observed above in doped structures through cryogenic DCTS, may originate from intrinsic defects, with their concentration and activation attributed to Fe-doping [34]. Therefore, the results in [F], confirm that the activation of traps in GaN buffers at deep cryogenic temperatures is prevented in absence of intentional doping. However, gate-lag is still observed at both RT and CT, indicating the activation of surface-related traps. As shown in the inset of Figure 20b, the subsistence of carrier trapping at CT was verified using light illumination, leading to a slight increase of I_{DS} (~ +5% and +2%, at CT and RT respectively), even in absence of quiescent stress. Nonetheless, cooling-down to 4.2 K does not affect significantly the extent of trapping, suggesting that this mechanism is unlikely to be controlled by thermal processes. Instead, trap-assisted tunneling of electrons or hopping can explain this behavior, as these processes are prominent at the surface and in the vicinity of the gate [91].

3.3 Summary

In this chapter, the trapping of carriers was studied and shown to cause dynamic degradations in the electrical characteristics of the GaN HEMTs depending on bias and temperatures conditions. The impact of this phenomenon on the cryogenic performance was quantitatively evaluated using the pulsed I-V technique, revealing an overall increase of trapping effects at low temperatures.

The analysis of the pulsed characteristics provided evidence of trap activation at the surface region and in the buffer layer. Using Drain Current Transient Spectroscopy, the characteristics of these traps were further identified, with their signatures determined in terms of activation energy and cross-section. The results highlighted the predominant influence of Fe-doping in the GaN buffer, along with other intrinsic defects and surface-related trapping.

Different technological factors were found to influence these phenomena. First, the integration of gate field-plates mitigated trapping effects associated with both surface and buffer regions, with an increasingly pronounced impact at low temperatures. Second, eliminating the intentional incorporation of Fe doping in the buffer effectively suppressed buffer-related trapping, thereby reducing the overall trapping effects at cryogenic temperatures. This work provides insights regarding the device engineering of GaN HEMTs to minimize trapping effects at cryogenic temperatures. In particular, reducing the buffer doping and optimizing the gate design with field-plates are promising strategies for improving device performance and reliability in such conditions.

4 Low noise amplification at cryogenic temperatures: state-of-the-art and modeling approaches

LNAs are typically implemented as a cascade of multiple stages. As illustrated in Figure 21, each LNA stage consists of an input matching network, a transistor device, and an output matching network. The design of these matching networks ensures optimal noise temperature while simultaneously enabling microwave gain and stable operation. The expressions for gain and stability, found in [105] (equations 3.2.4 and 3.3.19–20 respectively), depend on the HEMT scattering parameters and the impedances shown by the matching networks. Increasing the number of LNA stages results in a higher total gain. According to Friis's formula for cascaded systems (equation (4), from chapter 1), the noise performance of the first stage has the most significant impact on the total noise temperature. Therefore, prior noise modeling of the HEMT is critical for estimating its noise temperature and identifying the parameters that minimize it. The noise performance at both the system and device levels, along with the impact of various physical parameters, is discussed later in this chapter.

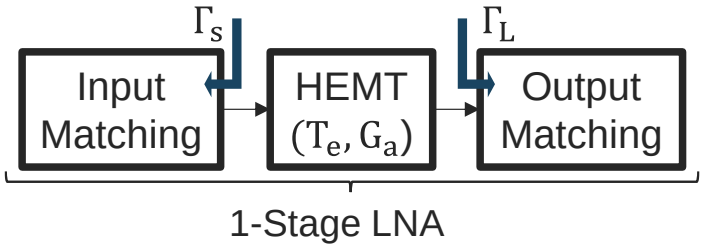

Figure 21: Schematic block illustration of a single stage LNA. Γ_s and Γ_L are respectively the source and load reflection coefficients from the input- and output- networks.

A record of average noise temperature of 1.4 K in the range of 4 to 8 GHz was reported using InP HEMTs at the physical temperatures of 4 to 15 K [106] [107]. The frequency-bandwidth is mainly influenced by the matching networks design. Cascade of multiple stages can also enhance the bandwidth. However, to maximize the flatness of the LNAs' frequency response, the design of individual stages is usually made for a slightly higher noise temperature than the lowest possible. From that perspective, as studied in [C], the choice of the transistor-size determines the impact of possible deviations from the optimum-noise matching. In terms of wideband operation, a fractional bandwidth of up to around 190 % was reported using InP HEMTs [108]. Most recently, advanced InP-HEMTs technology achieved a state-of-the-art 4 K noise temperature over the entire 2 to 18 GHz band [109].

The maximum frequency of operation is strongly impacted by the gate length, as the cut-off frequency is inversely proportional to L_g. Hence, HEMTs development for low-noise applications at high-frequencies was focused on L_g-downscaling over the past years. InP-HEMTs with 25 nm gate length were reported to operate up to 670 GHz with 15 – 25 dB gain and 400 K noise temperature at 25 K physical temperature [110], while InGaAs mHEMTs with 50-nm gate length were shown outperforming their InP counterparts in the 67-116 GHz band [111].

A high-power dynamic range prevents failure risks due to interferences and power overloads. The dynamic range of LNAs refers to the difference between the power levels for maximum linearity and minimum detection. The maximum power linearity is usually characterized in terms of the power level for 1-dB compression, noted P1dB. Material properties and epitaxial design determine maximum linearity, with

GaN-HEMTs particularly advantageous in this regard as introduced earlier. Additionally, P1dB is influenced by bias conditions, imposing additional constraints on achieving simultaneous low-power dissipation [112]. Dynamic range and power-handling capabilities are often overlooked or not reported for cryogenic LNAs. Among the few available examples, state-of the art cryogenic InP-based LNAs optimized for IF bandwidth achieved input P1dB of -43 dBm, but with a relatively high-power consumption of 18 mW. In contrast, InP LNAs with the lowest reported power consumption (0.1 mW) exhibited a tenfold lower P1dB (-53 dB) at 4 – 6 GHz and 4 K. SiGe-LNAs were reported achieving higher power-handling capabilities, with recently reported input P1dB of -28 dBm at 6 GHz at 3.7 K [113]. While the design of GaN-based HEMTs for low-noise cryogenic operation is still under investigation, available data suggest significantly higher power-handling. For instance, GaN-based LNAs were shown at 243 K to sustain an input P1dB around 20 dBm at 2 GHz [114].

Low power consumption is critical for cryogenic applications, as cooling power at cryogenic temperatures is usually limited and the presence of a "hot" element would warm up nearby components. The power consumption of InP-HEMTs is also the most competitive among semiconductor technologies, with a recent record of 0.1 mW of 3-stages LNAs, achieving an average 2.6 K noise and 22 dB gain in the 4 – 6 GHz range [115].

Another challenging aspect in cryogenic-LNAs design concerns the input reflections. High return losses usually arise from trade-offs between wideband and optimum noise-matching, leading to restrictions on the input standing-wave-ratios (SWR). For instance, in [116], the LNAs specifically designed for radio-astronomy applications presented an average S_{11} as high as -3.7 dB in the 4 – 12 GHz band. A high input return loss may affect the overall receiver performance, and especially mixers as directly connected to LNAs [117]. To address this challenge, one possible solution implies using input isolator. However, this might lead to further noise degradation and mechanical and size restrictions. Another solution may rely on a balanced amplifier design, as demonstrated in [118].

The assembly and integration of LNAs for cryogenic applications is usually achieved through either Microwave Integrated Circuits (MICs) or Monolithic MICs (MMICs). MICs rely on surface-mount components, manually assembled and interconnected via bond-wires [119]. MMICs emerged following the development of advanced fabrication processes, relying on the integration of all components onto a single substrate [108]. While MMICs offer high levels of integration, repeatability, and yield, achieving optimal noise performance can be challenging due to limited tuning flexibility. In contrast, MICs allow for tuning and selection of individual components to achieve optimal overall performance, making them the preferred choice for applications with ultra-low noise requirements [2].

4.1 GaN-based HEMTs for low-noise amplification – State-of-the-art

For low-noise applications, GaN-HEMTs technology present a unique combination of high-frequency, low-noise and high-power performance. At room temperature, one of the most illustrative results of such combination were reported in 2008 [114]. These LNAs, based on AlGaN/GaN HEMTs on SiC substrates with 0.2-µm gate length, achieved an average noise temperature of 35 K at RT within a bandwidth of 2 – 8 GHz. The the gate-length scaling of GaN-HEMTs also enabled excellent low-noise at high frequency. For instance, GaN-HEMTs with L_g = 0.1 µm achieved 28 – 84 K at room temperature in the 22-30 GHz band in [120]. Using 70 nm gate-length, 63-101 GHz operation was recently reported with 21 – 24 dB and an average noise temperature of 259 K [121], yet about twice higher than state of the art based on InP in the

same range. However, GaN-based LNAs, usually require a power consumption about an order of magnitude higher than their counterparts based on the III-V materials. This is because, as initially designed for high-power operation, the best intrinsic features of GaN-HEMTs at high frequencies are usually obtained at higher biasing conditions. Nevertheless, in [122], lateral downscaling was demonstrated to be effective in reducing DC dissipated power of GaN-HEMTs with 0.15-µm gate-length under low-noise operating conditions. Most recently, aggressive downscaling of both the gate-length and source-drain distance to sub-100 nm were achieved, demonstrating significant technological advances and leading to an improvement in both noise performance and power dissipation [123]. For example, GaN-HEMTs with a 20 nm gate length and 100 nm source-drain distance were demonstrated in [124], achieving power consumption of 1.6 – 27.3 mW per stage with a noise performance of ~101 – 175 K (NF ~ 1.3 – 2 dB) and 24 dB gain in the 30 – 39.2 GHz band. These results were then directly comparable to room temperature state-of-the-art based on other technologies. Notably, these improvements were also partly due to the combined optimization of ohmic contacts and vertical epitaxy, both contributing to enhanced noise and gain performances at high frequencies. Simultaneously, these devices maintained their superior high-power potential, with breakdown voltages still around 2.5 times higher than those of GaAs and InP technologies.

In 2008, based on room temperature design from [114], GaN-based LNAs with 0.2-µm gate length were tested at modestly low temperature of 243 K (-30 C°) in [125], revealing an impressive reduction with a noise temperature level below 13.7 K (< 0.2 dB) at 2 – 8 GHz. Compared to RT results, the average noise performance improved by a factor of ~4. However, noise measurements were shown challenging under these conditions, resulting in large variations across the measured band. Nevertheless, power performances of this technology remained nearly constant upon cooling, with a linear output power of 32.8 dBm (~2 W). In 2019, commercial GaN-LNAs were experimentally tested for the first time at cryogenic temperatures of about 10 K [20]; a noise improvement by a factor of ~10 was then reported. temperature conditions. However, these amplifiers were initially designed for room-temperature operations and high-power applications, meaning that noise matching was not included for low-temperature conditions. Hence, the design of an appropriate matching network for cryogenic LNAs must be based on a prior model of GaN-HEMTs at the same temperature.

Cryogenic GaN-HEMTs noise performance of were investigated in this thesis, with the first noise model for length reported in [A]. This model demonstrated an average best noise temperature of 4.1 K over the 4.5–6.5 GHz range at a physical temperature of ~10 K. These results will be further discussed in Chapter 6.

Figure 22 provides an overview of the state-of-the-art cryogenic HEMTs reviewed in this chapter. The noise performance of GaN-HEMTs at cryogenic temperatures is shown to be at least four times higher than that of their counterparts based on other technologies, highlighting the potential for further improvement through device optimization. To this end, analysing their noise model may provide insights into the influence of key technological parameters, as discussed in a dedicated chapter. III-V materials dominate at different frequency ranges. Besides InP, GaAs pHEMTs exhibit a higher level of technological maturity due to their earlier development. However, their noise performance is generally inferior to that of InP HEMTs [2]. Among the best results, an average noise temperature of 5 K with 25 dB gain over 4 – 8 GHz at the physical temperature of 12 K was reported in [126].

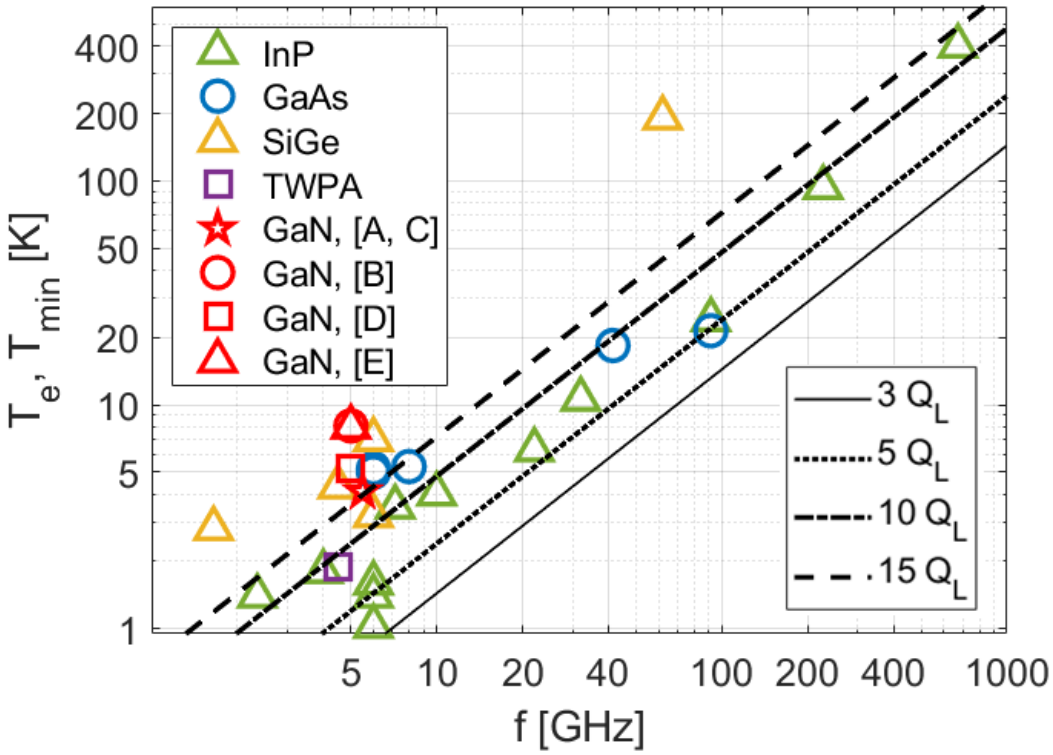

Figure 22: Summary of the state-of-the art of cryogenic HEMTs, the plot shows the average best noise temperature at cryogenic temperatures of 4 – 20 K achieved at center frequency from the reviewed literature.

Silicon (Si)-based technologies cannot operate at cryogenic temperatures due freeze-out of the carriers [35]. However, this is enabled with incorporation of Germanium (Ge) to Si in Heterojunction-Bipolar-Transistors (HBT). SiGe LNAs were shown particularly attractive in terms of low power consumption, with 4 – 8 GHz LNAs demonstrated at 0.3 mW in 2016 [16], that has been since then outperformed by InP-HEMTs [127] [115].

Among superconducting parametric amplifiers, recent advancements in traveling wave parametric amplifiers (TWPAs) resulted in low-noise and efficient power consumption similar to InP-HEMTs. Recent reports demonstrated a noise performance of 1.9 K at 4 K and 3.5 – 5.5 GHz with 0.1 mW power consumption [17]. However, these technologies exhibit a fundamental drawback in terms of power-dynamic range, with P1dB typically below -90 dBm [128]. Additionally, their gain generally remains below 20 dB, with a bandwidth of only few gigahertz [129].

4.2 Sources of noise in HEMTs

The noise behavior in FETs was for the first time theoretically studied in [130]. At microwave frequencies, two main physical origins of noise in HEMTs can be distinguished: thermal noise and shot noise. However, at low frequencies (<1GHz), the noise performance can be limited by other mechanisms, called Flicker noise or 1/f noise, as generally exhibiting a inverse proportionality to the frequency of operation. Low-frequency is especially influenced by charge trapping as affecting the channel carrier density [131]. However, these phenomena are not treated in this work, as focused on high-frequency noise behavior.

4.2.1 Thermal noise

Thermal noise originates in HEMTs from the random scattering of the charge carriers in the 2DEG channel. This noise mechanism results in random fluctuations in the number of carriers in the channel due to their scattering with the lattice. Additionally, due to the capacitive coupling between the channel and the gate, an induced noise of the same origin appears at the gate. As a result, the gate and channel noises are correlated.

At thermal equilibrium, the current and voltage noise associated with an ohmic resistor (R) are given by [131]:

$$< i_n^2 > = \frac{4\, k_B T}{R} B \tag{31}$$

$$< v_n^2 > = 4 k_B T R B \tag{32}$$

Where T is the physical temperature. The noise voltage and current are expressed in terms of their variance due to the statistical nature of thermal noise. These formulas can be used to account for the thermal noise associated with the equivalent resistors in the HEMT small-signal model, providing the foundation for noise modeling.

4.2.2 Shot noise

Shot noise arises from the discrete nature of charge carriers participating in current conduction. For shot noise to occur, charge carriers must cross a potential barrier [131]. In HEMTs, the conduction of leakage current through the Schottky gate leads to an associated shot noise, which is expressed as a function of the DC current, I_{DC}, by:

$$< i_{shot}^2 > = 2\, q\, I_{DC}\, B \tag{24}$$

The barrier-crossing condition is generally considered unfulfilled in the 2DEG channel [130]. However, for very short gate lengths (<0.1 μm), the origin of channel noise has been linked to shot noise suppression, suggesting a possible deviation from conventional noise mechanisms [132].

4.3 Noise modeling

From the circuit design perspective, the noise temperature of the transistor depends on the source impedance, $Z_s = R_s + jX_s$, as [133] [47]:

$$T_e = T_{min} + R_n G_{opt} T_0 \frac{\left|Z_S - Z_{opt}\right|^2}{R_s R_{opt}} \tag{33}$$

where T_{min}[K], is the minimum noise temperature; $Z_{opt} = R_{opt}[\Omega] + jX_{opt}[\Omega]$ is the optimum impedance and its equivalent admittance: $Y_{opt} = G_{opt}[S] + jB_{opt}[S]$, R_n [Ω] the noise resistance and T_0 = 290 K the standard temperature. This equation defines a set of four noise parameters (NPs):

$\{R_{opt}, X_{opt}, T_{min}, R_n\}$ that describe the transistor noise contribution to any circuit. Through Equation (33), providing $Z_s = Z_{opt}$ enables best noise performances, as leading to $T_e = T_{min}$. Thus, the design of the input matching network determines the noise contribution of the transistor in a single-stage configuration similar to that shown in Figure 21. R_n characterizes the sensitivity towards deviations from the optimum impedances.

In order to relate the four noise parameters to the small-signal parameters of the device, and the associated sources of noise, the circuit-theory of noisy linear two-ports can be used, based on findings in [134] [135]. To this end, the noise correlation matrix introduced, analogous to the scattering matrix (S-parameters) dealing with deterministic signals, as illustrated in Figure 23.

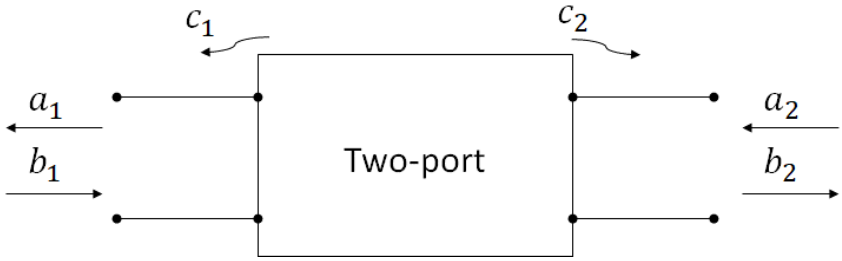

Figure 23: Illustration of the noise waves associated with a linear two-ports device.

The definition of the S-parameters relates to the input waves, a_1 and a_2, to the output waves, b_1 and b_2. By analogy, the two-port's noise can be treated as waves, noted c_1 and c_2, which emanate from the input and output, respectively. This definition combined with that of S-parameters leads to the linear matrix representation:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} + \begin{bmatrix} c_1 \\ c_2 \end{bmatrix} \tag{34}$$

Here c_1 and c_2 are correlated, as they originate from the same source: the intrinsic two-port.

A physical interpretation of this representation in the time domain is that the noise sources, c_1 and c_2, correspond to the noise self- and cross-power spectral densities. In the frequency domain, these quantities correspond to the auto- and cross-correlation functions, obtained by Fourier transform [136].

By arranging the noise sources, c_1 and c_2, and their correlation terms in a matrix form, the noise correlation matrix is obtained as:

$$C_s = \begin{bmatrix} c_{11} & c_{12} \\ c_{21} & c_{22} \end{bmatrix} = \overline{\begin{bmatrix} c_1 \\ c_2 \end{bmatrix} \begin{bmatrix} c_1 \\ c_2 \end{bmatrix}^+} = \begin{bmatrix} \overline{|c_1|^2} & \overline{c_1 c_2^*} \\ \overline{c_1^* c_2} & \overline{|c_2|^2} \end{bmatrix} \tag{35}$$

where the superscript "+" denotes the conjugate transpose operation, and "*" represents the complex conjugate. Equation (35) thus defines the noise correlation matrix of the two-port network.

A useful expression for C_s, relates, c_1 and c_2 to the physical temperature and the S-parameters by:

$$C_s = k_B T(I - SS^+) \tag{36}$$

Where I is the identity matrix. Additionally, two-port noise representation in admittance, impedance and chain forms of C_s can be obtained using appropriation transformations, provided in Table 1 in [136]. Figure 24 illustrates these equivalent two-port representations and the corresponding arrangements of input and output noise sources resulting from these transformations. Based on these properties, the rules for accounting for different types of two-port interconnections are obtained using equations 5 – 7 in [136].

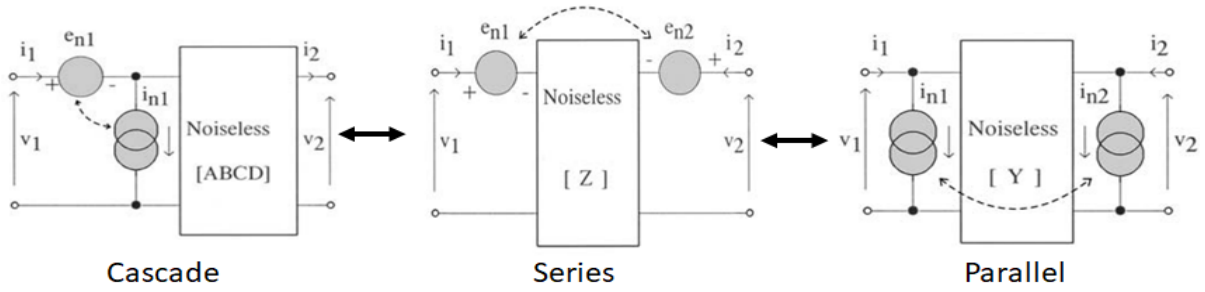

Figure 24: Illustration of the equivalent representations of a linear noisy 2-ports, based on ABCD, Z and Y-matrices – from [137].

For practical purposes, the chain (ABCD) representation is particularly useful, as it aligns with the general definition of equivalent input noise temperature. In this framework, the noisy two-port is modeled as a noiseless device with correlated noise sources connected at its input. Obtained This representation is therefore well-suited for extracting the four noise parameters introduced earlier:

$$C_A = \begin{bmatrix} C_{A11} & C_{A12} \\ C_{A21} & C_{A22} \end{bmatrix} = \begin{bmatrix} R_n & \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}^*} \\ \frac{T_{min}}{2T_0} - \frac{R_n}{Z_{opt}} & R_n |Y_{opt}|^2 \end{bmatrix} \quad (37)$$

Equation (37) is derived from equation (36) through the appropriate transformation. Thus, this formulation enables the extraction of the two-port's noise parameters when the physical temperature and S-parameters are known.

However, in the case of HEMTs, the effective temperature of the intrinsic device differs from the ambient temperature due to their active nature. As a result, the temperature in equation (36) cannot be obtained directly. Consequently, the four noise parameters of a HEMT are most commonly obtained using semi-empirical methods. Among the most established of these methods, the Pospieszalski noise model method has been widely implemented for the reliable modeling of various HEMT technologies at cryogenic temperatures, as in [47] [138] and in [A – E], and is introduced in the next section.

4.4 Pospiezalski's noise model

The Pospieszalski noise model has been proposed following a prior theoretical work by Van der Ziel in 1962 [130]. Channel thermal noise was then identified as the main noise mechanism in FETs, at frequencies beyond which 1/f noise can neglected. Upon the assumption of thermal noise origin, in the Pospieszalski model, each resistive element in the equivalent electrical model contribute to the total noise temperature of the device. Thus, the full estimation of the device noise contribution depends on the effective temperatures of the resistances in the lumped equivalent model. In addition, the noise

temperature values of the equivalent lumped elements which are not part of the intrinsic device are fairly approximated to be at the ambient temperature. The drain-to-source resistance, on other hand, is directly exposed to the self-heating from the drain power dissipation. The equivalent drain noise temperature is then noted T_d. In the Pospieszalski model T_d, is treated a fitting parameter, that can be obtained from single noise measurements. This is together with the intrinsic gate noise temperature, T_g which is usually tends to the same value as the ambient temperature [47] [139]. To comply with the fundamental thermal noise origin, T_d and T_g are frequency-independent.

To relate T_d and T_g to the HEMT noise parameters, the admittance form of C_s can be convenient, resulting in the representation shown in Figure 7 from chapter 2. In this case, the gate and the drain nodes are assigned noise current sources $\overline{i_g}$ and $\overline{i_d}$ respectively, in shunt with the noiseless device. Both current noise sources are correlated through the factor:

$$C = \frac{\langle i_g^* i_d \rangle}{\sqrt{\langle i^2{}_g \rangle \langle i^2{}_d \rangle}} \tag{38}$$

C reflects the capacitive coupling between the gate and the channel. The admittance form of the noise correlation matrix of the intrinsic device, C_{Y-int}, is then expressed [140]:

$$C_{Y-int} = \begin{bmatrix} \langle i_g^2 \rangle & \langle i_g i_d^* \rangle \\ \langle i_g^* i_d \rangle & \langle i_d^2 \rangle \end{bmatrix} \tag{39}$$

Since C_{Y-int} is related to the S-parameters of the devices, by means of equation (36) and the corresponding transformation matrix, it can be expressed as function of the equivalent small signal parameters and their assigned equivalent temperatures:

$$C_{Y-int} = \begin{bmatrix} T_g(R_{gs}|Y_{gs}|^2 + R_{gd}|Y_{gd}|^2) & T_g\left(R_{gs}|Y_{gm}|^* + R_{gd}|Y_{gd}|^2\right) + T_d g_{ds-int} \\ T_g(R_{gs}|Y_{gm}| + R_{gd}|Y_{gd}|^2) + T_d g_{ds-int} & T_d g_{ds-int} + T_g R_{gs}|Y_{gm}|^2 + T_g R_{gd}|Y_{gd}|^2 \end{bmatrix} \tag{40}$$

On the other hand, since the admittance and chain representations are equivalent, the NPs are directly derived from C_{Y-int} through equation (36) after applying the corresponding matrix transformation. Thus, the retrieval of the small signal model, in addition to T_d and T_g, leads to the extraction of the full noise model of the device through its 4NPs.

In fact, one notes that the intrinsic noise behavior of the device can also be fully described using the set of 4 parameters introduced in equation (39): $< i_g >$, $< i_d >$ and the real and imaginary parts of the correlation factor C. These parameters provide a direct insight on the frequency- and bias-dependences of the noise behavior at the discrete level of the device. This is in contrast to the set of 4NPs from equation (20), which are mainly indicative on the noise behavior at the macroscopic or the system level. Thus, the analysis of the parameters in equation (39) is useful from the perspective of the physical interpretation of the device's noise model.

4.4.1 Physical interpretation

Considering the example of the first cryogenic noise model of the GaN-HEMTs, from the experimental data presented in [A], Figure 25a–d show the frequency- and bias-dependences of $< i_g >$, $< i_d >$ and C

at the physical temperature of T ~ 10 K. A strong dependence of $< i_d >$ with respect to I_{DS} is observed. $< i_d >$ mostly reflects the bias-dependence of T_d. The latter increases proportionally to the drain power dissipation, leading to the channel self-heating (Figure 25d). $< i_d >$ is almost frequency-independent. This is consistent with the negligible effect of C_{gd} as observed in the previous chapter. $< i_g >$ presents a weak bias-dependence, it becomes relatively sensitive to I_{DS} for current levels higher than around 20% of the saturation level of the drain current. This might be linked to the increase of the ambient temperature due to the self-heating of the transistor. $< i_g >$ increases linearly with the frequency, resulting from the effect of C_{gs} on the input impedance of the transistor. This is also reflecting the fact that the noise appearing at the gate is induced from the channel through the capacitive effect, represented by C_{gs}. The variation of C tends to be frequency-independent. Also, C shows a negligible effect of its real part with respect to the imaginary one. One can reasonably consider that this correlation factor between the gate and the channel noise sources is purely imaginary. This is in line with the conclusions obtained from the theoretical works [141] [142]. Thus, in this case, the intrinsic noise model can be simplified to three parameters by excluding the real part of C.

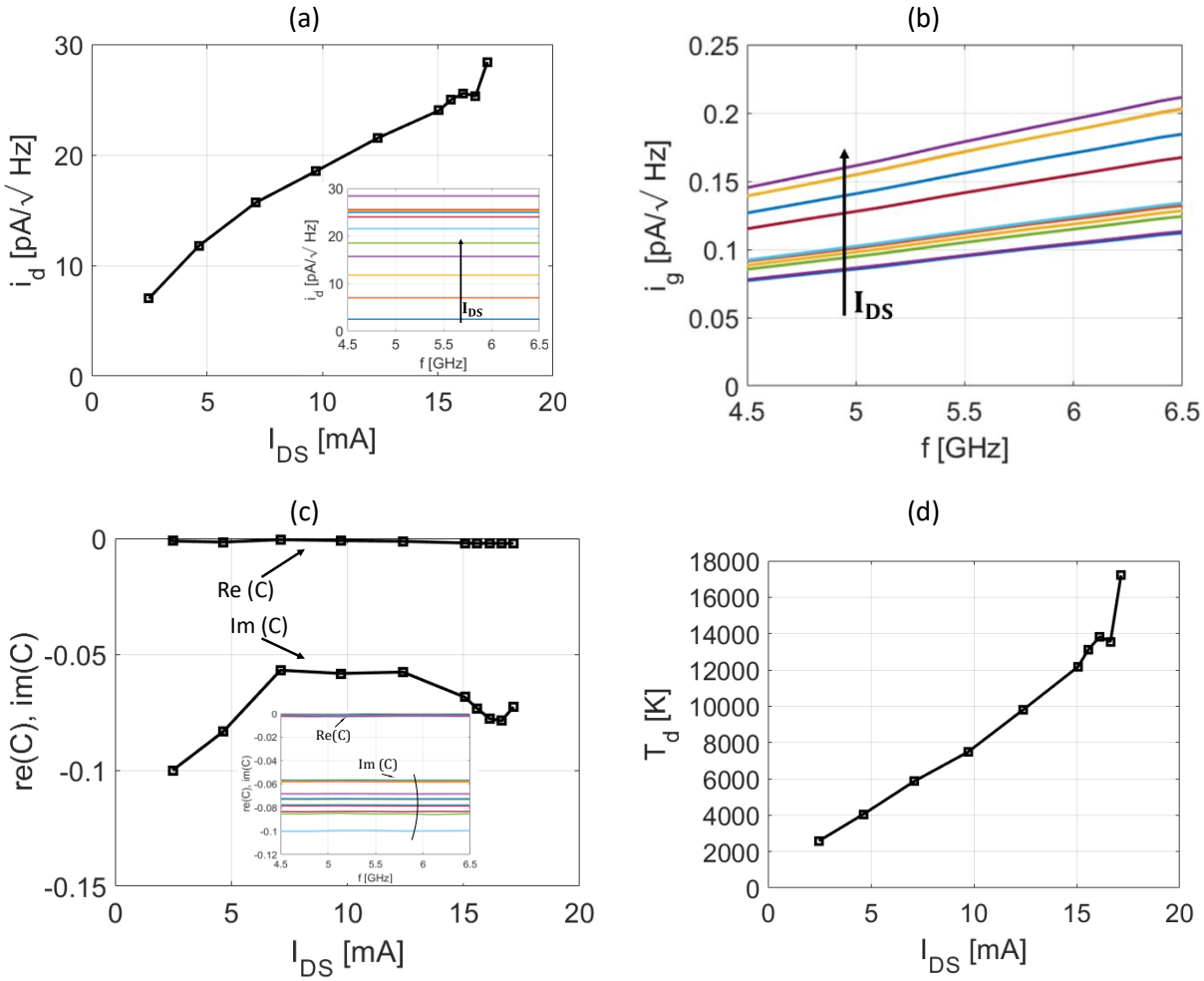

Figure 25: Extraction of the intrinsic noise sources of a GaN-HEMT at a cryogenic temperature of ~10 K, as studied in [A]. (a) Bias-dependence of $< i_d >$ at f= 6 GHz, the inset shows its frequency-dependence. (b) frequency-dependence of $< i_g >$ at I_{DS} within the same range in Figure 25a. (c) Bias-dependence of C at f = 6 GHz, the inset shows the frequency-dependence. (e) bias dependence of the frequency-independent parameter T_d.

4.4.2 Physical validation

The physical validity of the extracted Pospieszalski noise model can be verified through the condition on the Lange parameter defied as $N = R_n G_{opt}$, introduced in [143] and [47]:

$$1 \leq \frac{4NT_0}{T_{min}} \leq 2 \tag{41}$$

The left-hand side of the expression is consequence of the non-variant nature of N and T_{min} under lossless impedance transformation, while the second side is a property that was found specific to HEMTs and HBTs devices [143]. Considering the intrinsic transistor, which noise contribution is denoted $T_{min-int}$, this condition is found to be satisfied over both the entire studied frequency and bias ranges as shown in Figure 26.

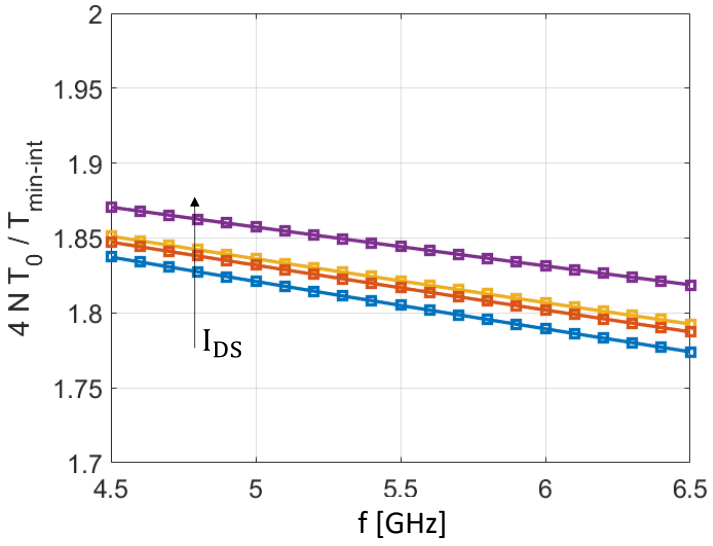

Figure 26: Variation of $\frac{4NT_0}{T_{min-int}}$ with frequency at cryogenic temperatures, at $I_{DS}[mA] = 2.5 - 10$, V_{DS} = 5 V – from [A].

4.5 Summary

This chapter reviewed state of the art cryogenic HEMTs technologies for low-noise applications at cryogenic temperatures, showing a strong potential of GaN-based HEMTs through the combination of excellent low-noise and high-power capabilities. Noise modeling techniques have been presented, and applied to the case of cryogenic GaN-HEMTs using Pospieszalski noise model, allowing for consistent physical verification of the results.

5 Microwave Noise Measurements & techniques at cryogenic temperatures

This chapter discusses the noise characterization techniques, applied to cryogenic GaN-HEMTs. A general procedure to this end is presented, involving a specific test setup and a de-embedding routine. Finally, the validity and the uncertainty of the measurements and de-embedding processes are verified using a reference LNA.

5.1 Y-factor method

Microwave noise measurements are commonly obtained using the Y-Factor approach, relying on two distinct levels of noise powers, or equivalently two different physical temperatures, shown at the input of the device under test (DUT). The DUT is assumed in the linear power regime, implying that any variation in the measured output noise power relates to a change in the input noise power. Hence, the Y-Factor (Y) is defined based on two distinct input states and their corresponding output noise power, providing information on both the equivalent noise temperature and available gain of the transistor.

Different techniques can be used to deliver the required couple of known input powers [126] [144]. For the following discussion, a noise-diode is considered. From the off-state and on-state of the noise diode, the noise powers P_c and P_h, and their noise temperatures T_c and T_h, are respectively shown at the input of the DUT. The terms cold and hot are also used to refer to the off and on-states of the noise diode respectively, hence the subscripts c and h. The Y-Factor is then defined as:

$$Y = \frac{P_h}{P_c} \tag{42}$$

At the output of the noise source, the noise temperature relates to the noise power through the ratio:

$$T_{h,c} = \frac{P_{h,c}}{B\, k_B} \tag{43}$$

In order to specify T_h with respect to T_c, a parameter called the Excess-Noise-Ratio (ENR) is introduced and expressed in a linear scale as:

$$ENR = \frac{T_h - T_c}{T_0} \tag{44}$$

The DUT presents an available gain, noted G_a. From the general definition of the concept of noise temperature, the noise power at the output of the DUT results from the amplification of its equivalent noise temperature, T_e, and that delivered by the noise diode. It is expressed as:

$$P_{h,c} = B k_B G_a (T_{h,c} + T_e) \tag{45}$$

Hence, using the Y-factor definition and solving for T_e, the equivalent noise temperature of the DUT is:

$$T_e = \frac{T_h - T_c Y}{Y - 1} \tag{46}$$

Similarly, the available gain derived from (36) is:

$$G_a = \frac{P_h - P_c}{Bk_B(T_h - T_c)} \tag{47}$$

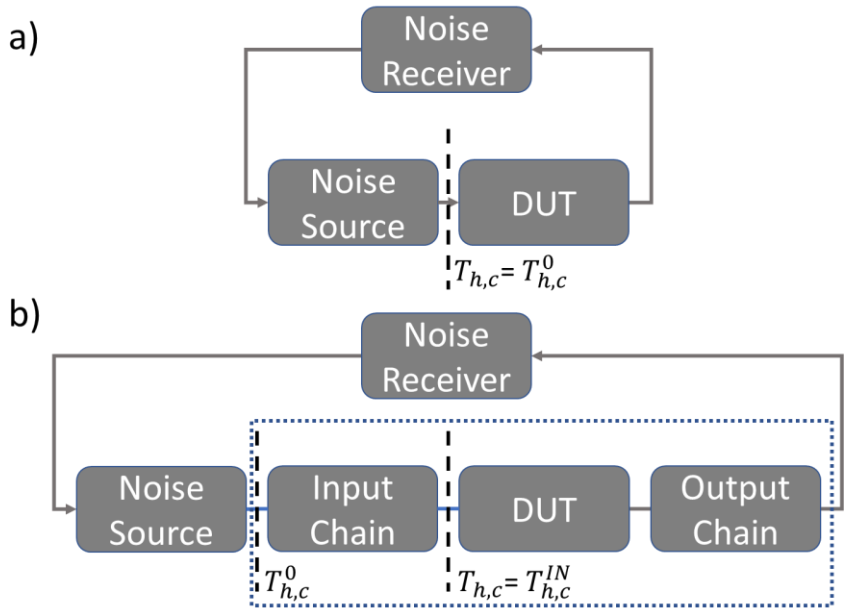

Figure 27: Illustration of the typical setup for the noise measurement in the case; a) a noise source directly connected to the noise receiver b) involving input and chains interfacing the DUT to the noise receiver, corresponding to the cryogenic measurements.

Equations (43) – (47) can be straightforwardly applied in the case of a DUT directly connected to the noise source. However, in practice and especially for the measurements in a cryogenic environment, a chain of components is used to interface the noise source with the DUT as illustrated in Figure 27. These components are usually passive and introduce different losses which, therefore, alter the expressions of T_h and T_c effectively presented at the input of the DUT. In this case, the latter parameters are noted $T^{IN}_{h,c}$. This is in order to distinguish the hot and cold temperatures delivered by the noise-diode which from now on are noted $T^0_{h,c}$.

As to provide a general expression of the resultant extraction in such scheme, it is considered a passive input pad at a known physical temperature T_{a-IN}, presenting insertion losses noted L_{IN} =1/G_{a-IN} , with G_{a-IN} its available power gain. Using the same reasoning as for equation (43), the noise power at the output of the input chain,.i.e., at the input of the DUT is expressed:

$$P^{IN}_{h,c} = kB\left[\frac{T^0_{h,c}}{L_{IN}} + \frac{T_{e-IN}}{L_{IN}}\right] \tag{48}$$

$$P_{h,c}^{IN} = kB\left[\frac{T_{h,c}^{0}}{L_{IN}} + T_{a-IN}\left(1 - \frac{1}{L_{IN}}\right)\right] \quad (49)$$

Here T_{e-IN} is the equivalent noise temperature of the input chain. In equation (49), it was introduced the definition relating the equivalent noise temperature to the physical temperature and the insertion losses:

$$T_{e-IN} = T_{a-IN}\left(1 - \frac{1}{L_{IN}}\right) \quad (50)$$

Thus, plugging in equation (43), it is obtained:

$$T_{h,c}^{IN} = \frac{T_{h,c}^{0}}{L_{IN}} + T_{a-IN}\left(1 - \frac{1}{L_{IN}}\right) \quad (51)$$

Then, to extract the noise temperature of the DUT, equation (51) must be plugged into equation (46) using $T_{h,c} = T_{h,c}^{IN}$.

5.2 Cryogenic noise measurements – Specifications and challenges

T_e tends to substantially reduce at cryogenic temperatures. Thus, from the analysis of the equations extracted in the previous section, the impact of the input chain ($T_{h,c}$) is further emphasized in such conditions. Thus, in a cryogenic environment, one needs to particularly consider the specific conditions of the input chain from both the microwave and the thermal points of view. In fact, the cryogenic measurements present a number of challenges that condition both the structure of the characterization setups and the procedures to obtain the noise data.

First, compared to the noise measurements at RT, a major difference is the substantial larger time that the cryogenic measurements require. This is mainly due to the time needed for the cooling cycles, which typically take 7 – 8 hours. Second, from the microwave perspective, two main challenges can be identified. The first concerns the noise source impedance which may differ when switching from its off to on states. This impacts the frequency-dependence of the resulting noise temperature [145]. This is because the estimation of the frequency-dependent losses and gains, including that of the DUT, depend on the source impedance. The second concern is the estimation of the S-parameters at the cryogenic temperatures, since the insertion losses are calculated from the scattering parameters (S-parameters). Note that in the case of the cryogenic on-wafer measurements of the HEMT, a cryogenic calibration-substrate is usually available and is used with a coplanar probes-station embedded into a cryogenic system. However, this is not the case for the coaxial-based setups. This may impact, in particular, the estimation of the insertion losses from the input chain. Thus, a calibrated Vector Network Analyzer (VNA) is required to measure the respective S-parameters. A usual calibration at any physical temperature requires the measurements of 3 to 4 known standards. However, at cryogenic temperatures, such a 2-ports' procedure would require at least 42 hours in our conditions. This is because no mechanical manipulation of the setup is possible once the system is cooled down. Over this required time for such a method of calibration, the possible drifts of the VNA operation may lead to multiple errors from each of the calibration standards' measurements. Besides, a measurement using a RT calibration may no longer be valid at cryogenic temperature (CT). This is due to the variation of the physical properties and geometry of the setup connections with the

temperature (thermal contraction and conductivity changes), leading to an equivalent shift in the reference planes and hindering a proper de-embedding of the data.

Finally, a concern from the thermal point of view arises from the fact that not all the elements of the measurement setup are at the same physical temperature. It implies that the interconnects, typically made of coaxial cables, are subjects to a thermal gradient. Consequently, the estimation of the respective noise temperature is affected by the propagated uncertainty of its assigned physical temperature.

Addressing this set of challenges, a variety of non-trivial strategies were proposed in the literature to accurately extract the noise parameters of HEMTs [145] [144]. The choice of an appropriate method should simultaneously serve the practicality, the time consumption and the accuracy of the measurements. For this purpose, the cold-attenuator (CA) method offers several advantages [145]. The practicality of this method at cryogenic temperature is facilitated by the fact that only one noise source and a microwave attenuation are required. This is contrasting with other methods requiring, for instance, the use of input impedances-tuner [146], mechanical switches [147] or adapted heating systems [126] which are difficult and time-consuming to implement in a cryogenic setup. Furthermore, once the S-parameters of the different parts of the setup are available, the noise measurements are obtained over only one cooling cycle using the CA method. This is also advantageous time-wise.

The method primarily addresses the errors related to the input chain. This is achieved by placing an attenuator in front of the DUT. The losses of the attenuator are significantly larger than those of the other elements of the setup. Since the attenuator is placed at a fixed and uniformly distributed cryogenic temperature, which can then be monitored using a thermal sensor, its noise contribution is determined with a higher accuracy than the other input elements. Hence, the accuracy of $T_{h,c}$ is improved since the contribution of the cryogenic attenuator dominates in the expressions of T_{e-IN} and L_{IN}. In fact, considering now the presence of the attenuator, the expression of $T_{h,c}$ =$T_{h,c}^{IN'}$ at the input of the DUT becomes:

$$T_{h,c}^{IN'} = \frac{T_{h,c}^{0}}{L_{IC}L_{CA}} + \frac{T_{a-IC}(L_{IC}-1)}{L_{IC}L_{CA}} + T_{a-CA}(1-\frac{1}{L_{CA}}) \quad (52)$$

Where L_{IC} and L_{CA} refer to the losses of the input cable and the cryogenic attenuator, correspondingly, while T_{a-IC} and T_{a-CA} are their respective physical temperature values. It can be seen from equation (52) that, when L_{CA} is large enough, all the terms tend to be insignificant with respect to the last term which is only dependent on the temperature and losses of the CA. This way, the impact of the thermal gradient over the input cable is reduced proportionally to L_{CA}. The same also applies to the impact of the possible changes in the noise-source impedance when switched from its on to off states.

5.3 Experimental cryogenic setup for noise characterization

Figure 28 presents a typical schematic overview of a cryogenic setup for the microwave noise measurements. This setup was, for instance, employed in [A], where further description of its different parts is provided.

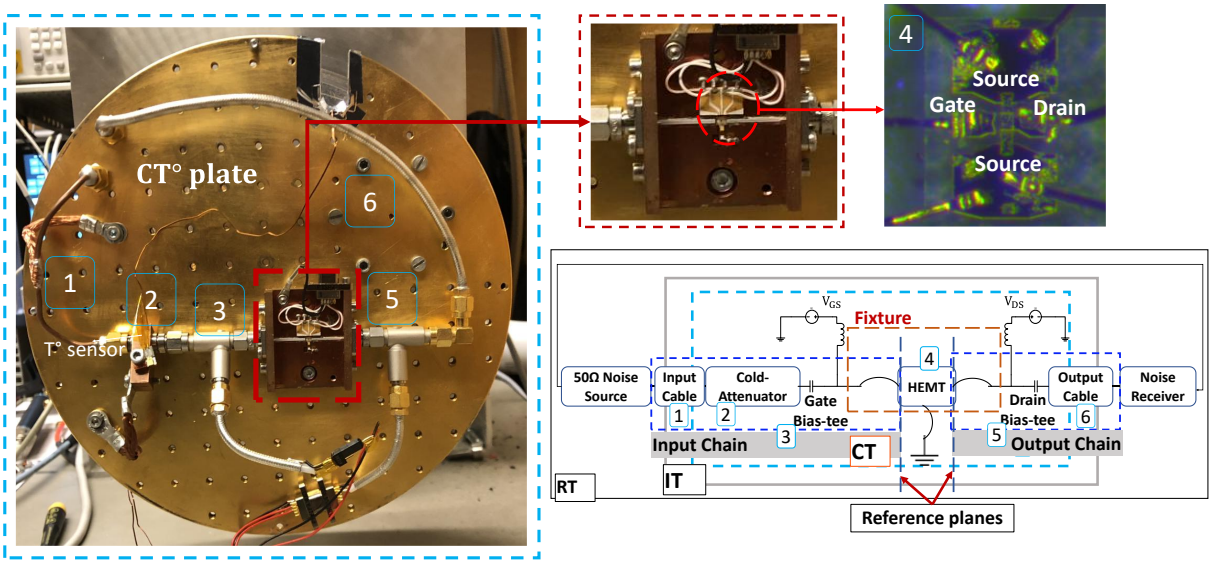

Figure 28 Image of the cryogenic noise measurements setup (left) with the corresponding block schematic (right). The image was mirrored to facilitate the readability of the schematic from left to right. In the top right is shown a microscopic top-view image of the transistor with the interconnecting bond wires, as mounted on fixture for the noise measurements. IT refers to the physical temperature of the cryostat stage interfacing the RT to the CT parts of the system. Reproduced from [A]

Such a setup relies on the implementation of the CA method. The system consists of a commercial 50 Ω noise-diode source placed at RT, the cryostat where the cryogenic system is embedded and includes coaxial cables, the 20-dB cold-attenuator, the bias-circuits and the fixture where the HEMT is mounted. The noise data are collected by the noise receiver, consisting of a spectrum analyzer and preamplifier, via an output coaxial cable. The cryostat has different stages, ensuring the transition from RT to the to the lowest cryogenic physical temperature, noted CT. The latter corresponds to the stage where the DUT is placed. A typical CT is around 10 K [A]. Further cooling can be provided, down to 4 K, as was the case in [B].

As discussed earlier, the CA method addresses the thermal gradient through the coaxial cables. In practice, for accurate implementation of the method, a calibrated thermal sensor is directly clamped to the 20 dB CA. Therefore, knowing the exact temperature of the attenuator helps in the de-embedding of the device noise temperature [148] [A]. In addition, in order to limit the thermal variation between the two ends of the stainless coaxial cables, with relatively low thermal conductivity.

The copper (Cu) fixture (Figure 28) hosting the HEMT acts a thermal sink for the transistor. The fixture, providing good thermal conductivity, consists of the input and output microstrip lines through which the transistor is electrically connected with Gold (Au)-based bond wires. A thin (5 mil) Alumina substrate is used for the microstrip lines.

The noise receiver block includes, for low-gain measurements, a preamplifier LNA in front of the spectrum analyzer to increase the signal-to-noise ratio. An electrical isolator in front can be used to limit the impact of the output impedance shown by the measured system on the noise temperature of the preamplifier [78]. The Friis formula is then used to subtract the noise contribution of the noise receiver block from the total measured noise temperature, before the extraction of the DUT noise temperature.

5.4 De-embedding of the cryogenic noise measurements

The de-embedding procedure of the cryogenic noise measurements addresses the challenges described in section 4.2.

For the following discussion, referring to Figure 28, the input chain includes: the input coaxial cable, the cryogenic attenuator, the gate bias-tee and the input microstrip line placed on the fixture. Also, the output chain is defined as including: the output microstrip line, the drain bias-tee and the output coaxial cable. T_{e-IN} and T_{e-OUT} , G_{a-IN} and G_{a-OUT} are respectively the resultant noise temperature and the available gain of the input and output chains. Hence, T_{e-DUT}, the noise temperature of the DUT is expressed:

$$T_{e-DUT} = G_{a-IN}\left[T_{e-sys} - \left(T_{e-IN} + \frac{T_{e-OUT}}{G_{a-IN}G_{a-DUT}}\right)\right] \quad (53)$$

To solve the equation (53), both the physical temperature and the available gain of each of the elements composing the input and the output chains must be known.

As discussed earlier, over the input coaxial cable the physical temperature is not uniformly distributed. Assuming a linear distribution, it is treated as in thermal equilibrium at an average between RT and CT noted T_{a-IC}. Considering the dominating impact of the CA, this same practice is commonly adopted with this type of measurements as reported in [144]. As mentioned earlier, the physical temperature of the CA, T_{a-CA}, is measured using a cryogenic thermal sensor. The CA and the fixture can be approximated to be at the same thermal equilibrium. Then, T_{e-IN} is expressed using the Friis formula as:

$$T_{e-IN} = T_{a-IC}(L_{IC} - 1) + T_{a-CA}L_{IC}[(L_{CA} - 1) + (L_{FI} - 1)\,L_{CA}] \quad (54)$$

Here the subscript "FI" refers to the input of the fixture, including the bias circuit, the microstrip line and the gate bond wire.

Similarly, T_{e-OUT} is:

$$T_{e-OUT} = T_{a-CA}(L_{FO} - 1) + T_{a-IC}(L_{OC} - 1)L_{FO} \quad (55)$$

The subscript "OC" denotes the output cable, and "FO" refers to the output of the fixture, including the bias circuit, the microstrip line and the drain bond wire. Both the gate and drain interconnecting bonding-wires from the microstrip lines on the fixture to the transistor had to be de-embedded simultaneously with the other fixture elements, so they were not considered as part of the DUT. Since a set of 4 bond wires was used in parallel to connect the source pad to the ground, provided by the coper-wall of the fixture, the total source inductance is negligible and was accounted as part of the DUT.

The estimation of the available gains, and correspondingly the losses and the noise temperature of the passive elements, depends on the S-parameters measured using a VNA. At CT, a correction of the VNA calibration must be performed, as discussed earlier. In order to tackle this challenge, the following procedure was used.

It is based on the reasoning that the equivalent cryogenic effects, with respect to the RT calibration, can be treated as a virtual adaptor that is added at CT with respect to the RT reference planes. Also, it assumed that no additional mismatches are caused by the cooling-down at the frequencies of interest (< 8 GHz). Thus, a standard Short-Open-Load-Thru (SOLT) calibration is first performed at the desired reference planes at RT. Then, a 1-port measurement of a known reflective standard, a short which impedance, Γ_{L}, is measured at RT and CT [149]. Thus, considering the S-matrix of the virtual 2-ports which accounts for the cryogenic effects, as:

$$\mathrm{S_V} = \begin{bmatrix} \mathrm{S_{11-V}} & \mathrm{S_{12-V}} \\ \mathrm{S_{21-V}} & \mathrm{S_{22-V}} \end{bmatrix} \tag{56}$$

The passivity implies $\mathrm{S_{12-V}} = \mathrm{S_{21-V}}$. Its input reflection obtained from the 1-port measurement writes as:

$$\Gamma_{\mathrm{IN-V}} = \mathrm{S_{11-V}} + \frac{\mathrm{S_{12-V}^2}\,\Gamma_{\mathrm{L}}}{1 - \mathrm{S_{22-V}}\Gamma_{\mathrm{L}}} \tag{57}$$

The assumption of the mismatch errors' absence leads to $\mathrm{S_{11-V}} = \mathrm{S_{22-V}} = 0$. Then, the insertion loss from the cryogenic effects is:

$$\mathrm{S_{12-V}} = \sqrt{\frac{\Gamma_{\mathrm{IN-V}}}{\Gamma_{\mathrm{L}}}} \tag{58}$$

In the ideal case $\Gamma_{\mathrm{L}} = 1$, and $\mathrm{S_{12-V}}$ is directly obtained from the 1-port measurement. The same is applied at each of the 2-ports termination that requires the correction, during the same cooling cycle. This cryogenic calibration method was previously applied in [149]. In [144], the use of the "fixture removal" tool available only in the modern VNAs was suggested. This function relies on the same reasoning as that of the procedure described above.

However, an additional step is required for the extraction of the S-parameters of the coaxial cables. As they are embedded in the system and bent to fit the cryostat setup, they cannot be measured directly. Thus, the first step consists of performing and saving a SOLT calibration at the external end of the coaxial cable at RT. Then, at the opposite end of the cable located in the CT stage of the cryostat, the standards are measured and used to de-embed their S-parameters at RT. The cryogenic effects can be afterwards corrected using the aforementioned procedure.

Alternatively, it was for instance suggested in [145] to perform a single measurement of the lines connected back to back. Half of the total measured insertion loss is then assigned to each cable. Since a perfect symmetry of the setup is assumed, additional considerations concerning the measurements setup would be in this case required. Once the losses from the cables determined, the losses of the cold-attenuator could be also similarly extracted based on the same assumption. In the next section, the results

from this latter method applied to a reference LNA will be compared to those from the procedure describe above.

Once the S-parameters of the input cable, the attenuator and output cables are determined, the rest of the measurement system can be de-embedded from the total S-parameters measurements using matrices transformations. Moreover, the S-parameters of the transistors are obtained from on-wafer measurements in a cryogenic probe station, before mounting the fixture. While the bias circuits can be measured separately, the S-matrix of and the fixture elements can be accurately modelled using an EM simulator knowing their respective dimensions and physical parameters. These latter were tuned within 20 % of their nominal values, selecting the best fit result against multiple measurements with the transistor at different bias points.

To illustrate the result of the noise de-embedding procedure, the measured noise temperature from a similar sample as studied in [A] is presented in Figure 29 and compared to the simulated curves. These data were obtained at CT ~ 10 K. An excellent agreement of the measured and simulated data is obtained, at the different tested bias points and over the entire frequency range.

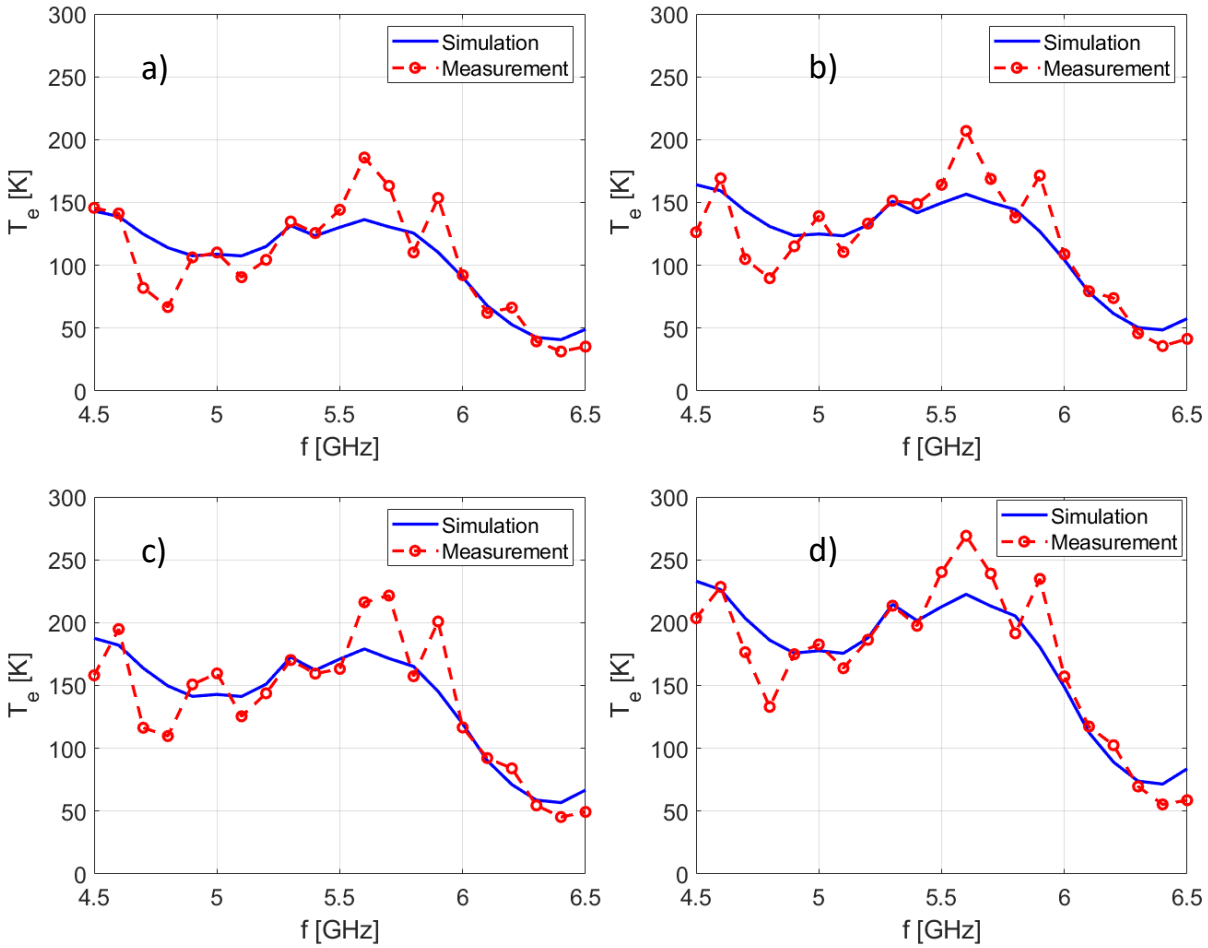

Figure 29: Comparison of the frequency-dependence of the modelled noise temperature (in blue) and the measured noise temperature (in red) of the DUT on-fixture, at V_{DS} [V] = 5 at different V_{GS} levels. a) V_{GS} [V] = -1.4, b) V_{GS} [V] = -1.3, c) V_{GS} [V] = -1.2, d) V_{GS} [V] = -1.1.

5.5 Measurements verification and uncertainty analysis

In order to gain insight into the validity of the cryogenic noise measurements, the de-embedding procedure introduced above and the confidence range in the estimation of the DUT noise temperature, a calibrated LNA of similar technology as reported in [150] was characterized as a reference, as shown in Figure 30. Hence in this section this LNA is referred to the as the Device Under Test (DUT). The reference LNA was measured in two different setups, noted setup # 1 and setup #2. The method relying on the gain measurements to estimate the losses of the different input and output chains was compared to the procedure based on the S-parameters measurements, both described earlier. The former method is referred to as method #1, while the de-embedding based on the measured S-matrices is referred to as method #2. Also, the measurements of the LNA gain using the noise figure meter (NFM) were compared to those using the VNA in setup #1.

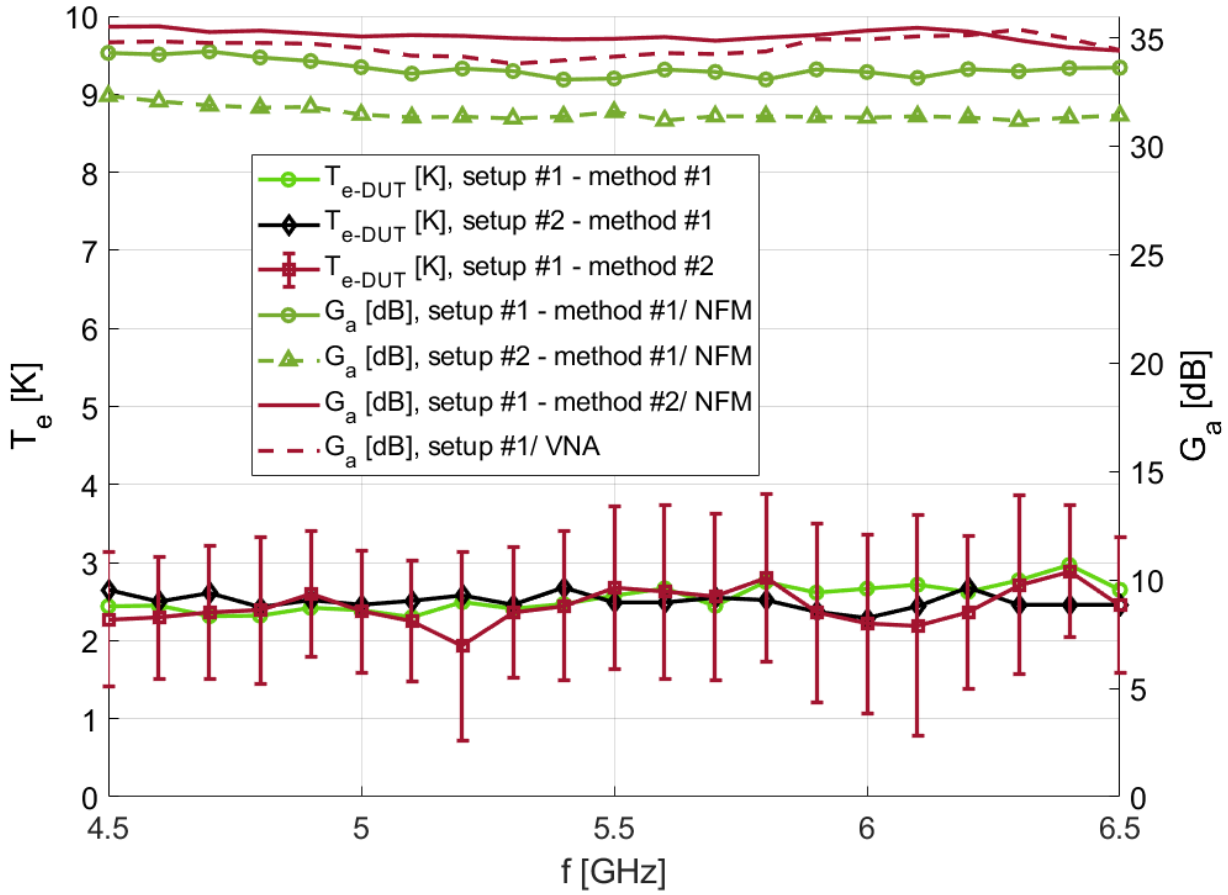

Figure 30: Comparison of the results of the calibrated LNA measured at ~ 10 K. The error bars are providing the RSS uncertainty of the noise temperature measured at each frequency point.

After its cooling to around 10 K, the noise temperature of the LNA, here denoted T_{e-DUT}, was de-embedded using the procedure described earlier. An overall good agreement is observed between the different data, demonstrating the efficiency of the calibration and de-embedding procedure. It simultaneously supports the repeatability of the results that can be obtained using the CA method, despite the use of different instrumentations calibrated at different places and times.

A quantitative estimation of the uncertainties around the noise temperature can be obtained through a sensitivity analysis of the different sources of errors. In the case of the measurements presented in Figure 30, a summary of the considered sources of errors is provided in table 2. The total uncertainty on the noise temperature of the DUT resulting from the sum of all the sources of errors, averaged over the entire considered frequency range of the noise characterization, is around ± 1.5 K. This uncertainty estimation is comparable with those obtained by other groups and published works. Note that the uncertainty estimation is usually presented in a root of the sum of squares (RSS) form, under the assumption that all the considered sources of error are uncorrelated, which corresponds in our case to ±0.8 K. For instance, a total (and RSS) uncertainties of ±1.3 K (±0.6 K), ±2.3 K (± 1.2 K), ±1.4 K (±0.7 K RSS) were reported in respectively [145], [106] and [126] .

Table 2: Summary of the uncertainty analysis of the results in Figure 30.

Source of error	Tolerance	Average resultant error in T_e [K]
Noise diode ENR	±0.15 dB	± 0.6
Noise diode temperature sensor	±1 K	± 0.02
Cryogenic temperature	± 12 mK	± 0.012
Input chain mismatch losses	±0.2 dB	± 0.6
Y-Factor	±0.02 dB	± 0.24
		± 1.45

The mismatch errors ascribed to the input chain, are usually ignored [106], [126] due to the difficulty surrounding their de-embedding and estimation. Also, an uncertainty on the physical temperature of the cryogenic attenuator that adds to that specified for its dedicated temperature sensor, was pointed out in [106]. This latter relates to the potential gradient of temperature between the outer conductor and the core resistive parts of the cold attenuator. It was considered ± 0.5 K in [106] using a similar cold attenuator-based setup. Adding this possible contribution to the initial analysis leads to a total uncertainty of ± 1.9 K (± 1 K RSS).

6 Noise Performance of GaN HEMT at cryogenic temperature

This chapter presents the microwave noise performance and analysis of GaN HEMTs at physical temperatures of 4–10 K, based on the results from [A]–[E].

Considering the case of a sample with a gate-periphery of L_g[µm] × N_f × W_g[µm] = 0.2×2×25, Figures 31a and b present the minimum noise temperature (T_{min}) and associated gain (Ga) at RT and CT, based on the results from [A]. The best T_{min} at CT was determined to be ~4.1 ± 0.5 K, averaged at 4.5 – 6.5 GHz measured band. Notably, this represents one of the first reported cryogenic noise performances of GaN HEMTs in the literature, highlighting the promising potential of this technology for cryogenic low-noise applications.

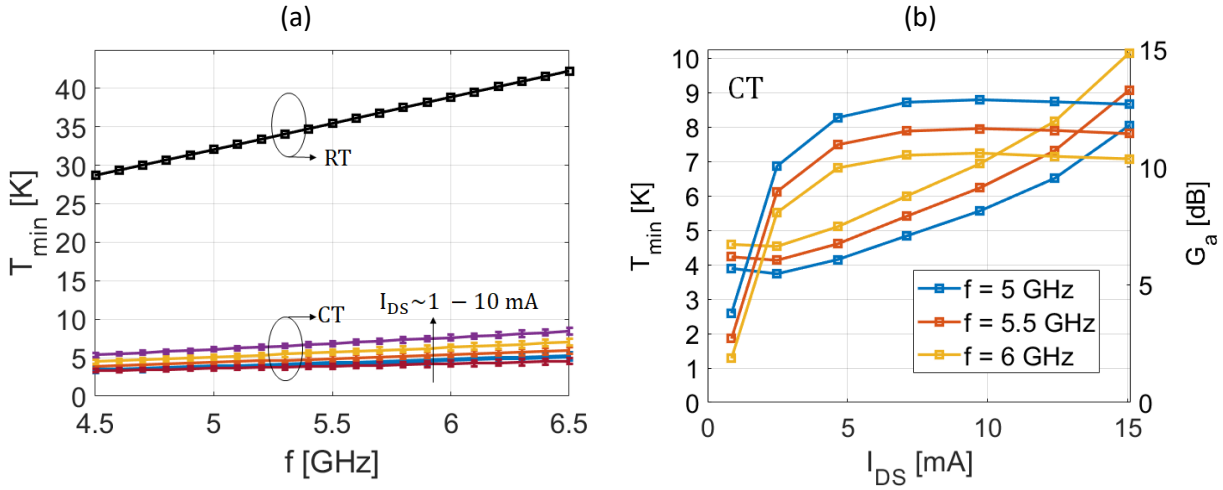

Figure 31: (a) Frequency-dependence of T_{min} at RT and CT. (b) Bias-dependence of the extracted T_{min} and the associated gain G_a at CT, at f [GHz] = 5 – 5.5 – 6 at V_{DS} = 5 V. Reproduced from [A].

Comparing the results at RT and CT, T_{min} is significantly reduced by a factor of ~7.6. The corresponding noise model aligns with the conclusions drawn from the DC and small-signal characterization in Chapter 2. Specifically, the reduction in access resistances, along with an increase in transconductance, accounts for the observed improvements, as detailed in [A]. The temperature dependence of the noise model in GaN HEMTs was found to be consistent with studies on other technologies, such as GaAs and InP HEMTs [46] [151].

Referring to the current status of existing technologies presented earlier, the noise performance of GaN-HEMT at cryogenic temperatures compares to other technologies, particularly those based on GaAs [2]. Nevertheless, the best T_{min} at cryogenic temperatures is higher by at least a factor of 4 than InP-HEMTs noise performance at the same frequencies. Also, this was achieved at a power consumption of approximately 12.5 mW, which is about an order of magnitude higher than the lowest power dissipation (~0.1 mW) obtained with technologies based on InP [115] and SiGe [16]. However, it is important to note that no prior optimization for cryogenic low-noise operation was conducted for the devices studied here. In contrast, other technologies were subject to multiple iterations and investigations on the structural optimization over at the past decades.

Furthermore, the analysis of the noise model can provide insights into the impact of potential technological improvements, as proposed in [A] and [E]. In fact, the gate and source resistances are the among most important contributors, as positioned prior to the gain stage of the transistor, represented by g_{m-int}. The gate resistance is primarily determined by its metallization. In [B], the impact on noise performance of the gate resistance was studied, along with its mitigation feasibility using a superconducting Nb-based gate metallization. This aspect is further discussed in a later section.

The contribution to the minimum noise temperature of the access resistances was of the order of at least 1 K, increasing with frequency and bias conditions (referring to Figure 11 in [A]). The source resistance is linked to two factors. The first is partially embedded in the semiconductor region, extending down to the channel, and is therefore dependent on the epitaxial properties and 2DEG confinement. The second factor concerns the resistivity of the ohmic contact, which was approximately R_c ~ 0.3 – 0.4 Ω·mm as estimated from TLM measurements at RT. The ohmic contact resistance usually present a weak-temperature-dependence [42]. In this case, the ohmic contact resistance here is about 10 times larger than usually obtained in state-of-the-art technologies, with typical values of 0.03 and 0.04 Ω·mm reported for InP-based HEMTs at RT and CT [108]. Consequently, this aspect of the transistor could present one of the main bottlenecks for future optimization.

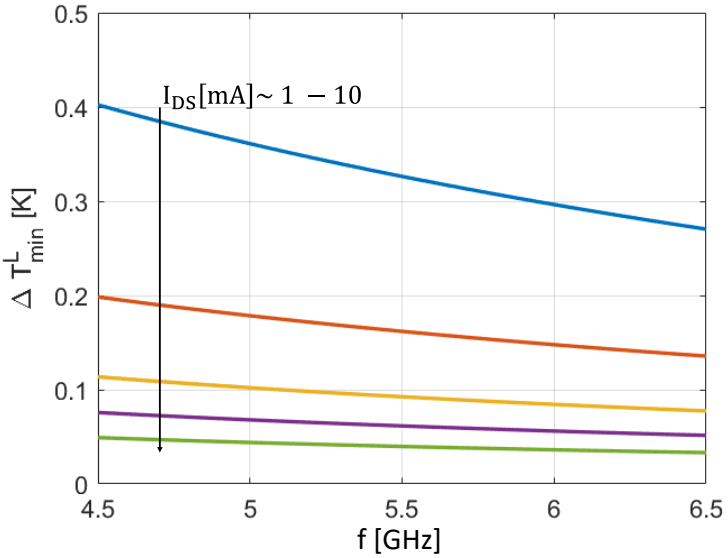

Figure 32: The frequency-dependence of the effects of the gate leakage on T_{min} at CT – Reproduced from [A].

Additionally, the noise the gate leakage current contributes with a shot-noise current source, following the proposed approach in [47]. The gate leakage was found to contribute by up to 4 % at the average best minimum noise temperature. However, the proportion of this contribution increases at low frequencies as shown in Figure 32, which is consistent with the principles introduced in [152]. This finding may also guide the design of cryogenic LNAs based on this technology model, particularly to meet the requirements for wideband operation, including coverage of relatively low frequencies.

6.1 Impact of gate-width dependence

From the perspective of LNA design, the availability of the noise model for different sizes of the transistor can help meeting the applications requirements and facilitate reaching design trade-offs has driven

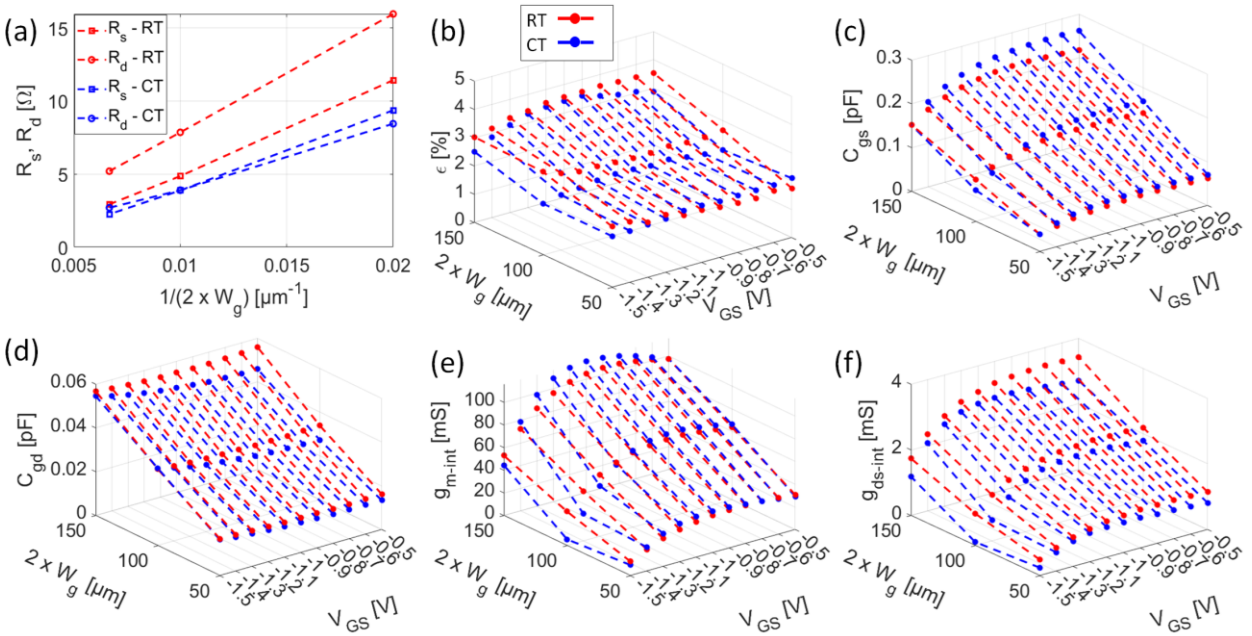

Figure 33: Gate-width dependence of the equivalent small-signal model parameters at RT (red) and CT (blue); (a) R_s and R_s . (b) model error ϵ, (c) C_{gs} (d) C_{gd}(d) $g_{m-int}$and (e) g_{ds-int} . Reproduced from [C].

multiple efforts in the literature to propose scalable models for different HEMT technologies [153] [154]. Moreover, the scalability of the noise models can help to assess the repeatability and validity of the noise characterization.

Considering the same technology presented in the previous section, and based on the results in [A] and [C], the variation of the main equivalent small-signal model parameters is shown in Figure 33. As expected, the model exhibits excellent physical consistency, with errors relative to the measured data ranging from 2% to 4% for all tested gate widths. The drain and source access resistances (R_s and R_d) are inversely proportional to the gate-width. As further analyzed in the next section, the gate resistance scales in the opposite direction relative to the access resistances, resulting in a counterbalancing effect from the noise model perspective. The difference between R_s and R_d tend to cancel at CT, reflecting the dominant effect of the ohmic contacts compared to the contributions from the semiconductor-embedded regions, as also shown in [E]. The intrinsic capacitances increase linearly with gate width, impacting the optimum noise matching through the device input impedance. The same trend applies to the intrinsic transconductance and output conductance, leading to counterbalancing effects on the variation of the minimum noise model with gate width.

Figure 34 present the variation of the four noise parameters with the gate-width (W_g) a CT. In Figure 34a, the variation of T_{min} with power-dissipation ($P_{DS} = V_{DS} \cdot I_{DS}$) demonstrates two main features. First, T_{min} appears weakly to nearly unsensitive to gate-width variation within the studied range of 50 to 150 µm. This is due to mutually counterbalanced effects from the gate-width dependence of the small-signal model, and T_d being independent of W_g, in line with the findings reported in [154] and in [E]. Second, the resulting optimal minimum noise temperature at CT converged to similar values in the range of 4 – 5 K for all the tested samples with the different gate-widths. On the other hand, the normalized drain current,

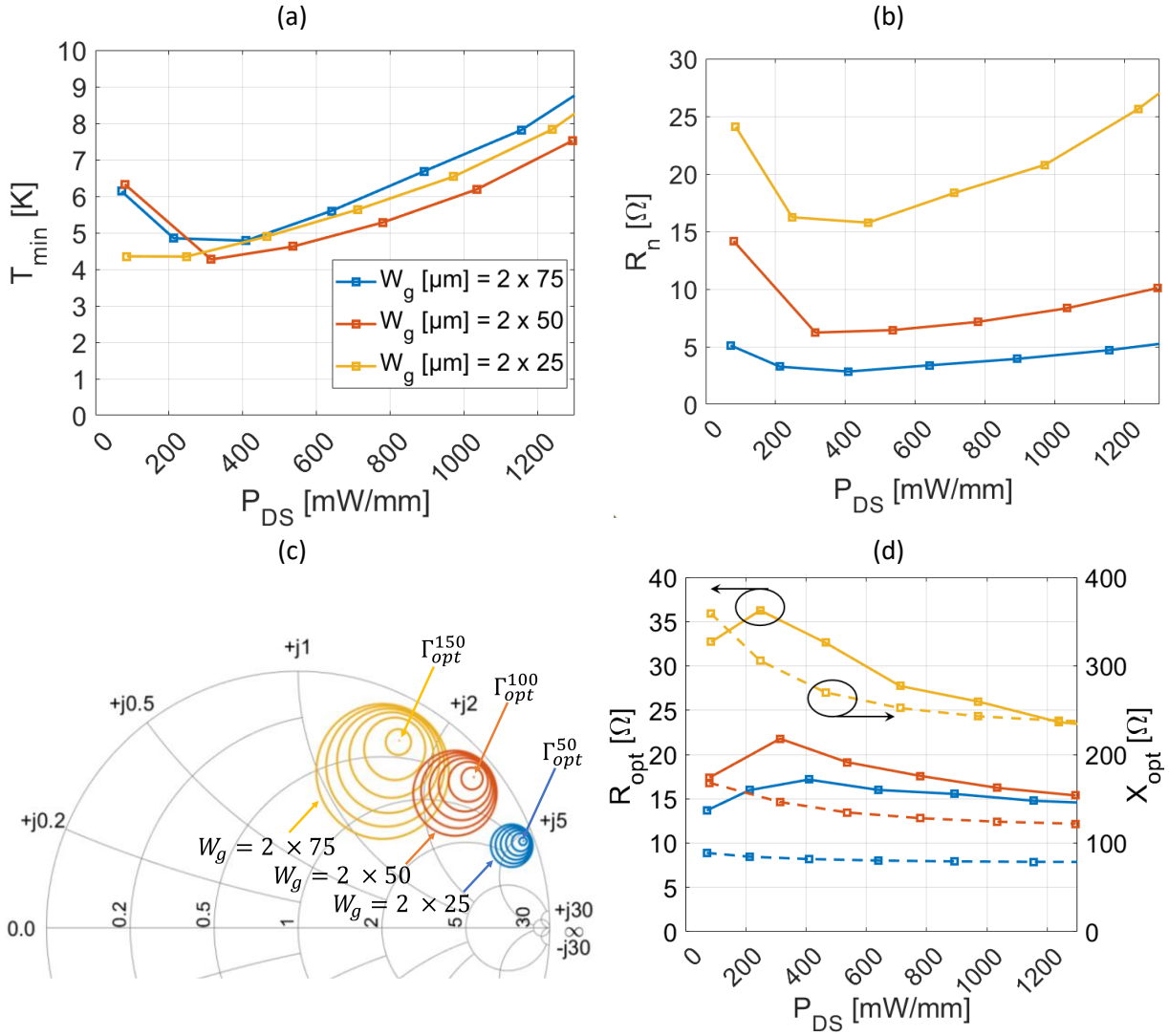

Figure 34: Variations as a function of power dissipated for different gate widths: 2x25 um (light orange), 2x50 um (dark orange) and 2x75 um (blue). (a) T_{min}. (b) R_n. (c) Constant circles of noise temperatures T_e [K] = 5:1:10, at f = 6 GHz and power dissipation of ~0.5 W/mm. (d) R_{opt} (left-axis) and X_{opt} (right axis). Reproduced from [C].

I_{opt}, at which optimal T_{min} is obtained is found to scale by approximately the same factor as the total gate-width. Therefore, the choice of the transistor's size from the studied range of W_g has limited effects on the noise contribution, while affecting the power consumption.

The noise resistance, R_n was found to be the most sensitive noise parameter to the total gate width, exhibiting a consistent decrease as W_g increases. This is mainly due to a linear increase of the transconductance with W_g, as R_n features an inverse squared dependence on g_{m-int} [155]. It should be noted, however, that R_n is also linearly dependent to g_{ds-int}, which increases with W_g. Due to these effects, it was suggested in [156] the existence of a threshold W_g above which R_n reaches a sufficiently low level that cannot be further improved by increasing the total gate width.

A low R_n is desirable from the perspective of LNA design, as it minimizes noise degradation when the noise-matching impedance deviates from Γ_{opt}. Therefore, within the studied range of total gate widths, the largest tested W_g (150 µm) was found to be the most suitable, as allowing for more flexibility in designing the matching networks.

The plot of the constant noise temperature circles in the Smith Chart (Figure 34c) provides useful insights onto the different options for the optimum noise-matching of the devices, with a broad noise circle facilitating simultaneous design trade-offs at a fixed frequency. The radius of the noise circle mainly depends on T_{min} and the magnitude of the optimum input reflection coefficient ($|\Gamma_{opt}|$). At a fixed current density, since T_{min} is weakly varying with W_g, the radius of the constant noise circle follows the same gate-width dependence as the optimum impedance. More specifically, a low imaginary part of the optimum impedance has been shown promoting increased the noise-circles radius in [154]. As shown in Figure 34b, increasing W_g,leads to reduced X_{opt} as inversely proportional to C_{gs}, which increases with W_g,. Hence, broader noise circles are obtained when increasing W_g. This feature supports the interpretation of the observed reduction of R_n with the width as a reduced sensitivity towards possible impedance mismatches. Nevertheless, a device with a larger total gate width drives more current and power dissipation, which becomes further critical when considering the design of LNAs with multiple stages.

6.2 Towards cryogenic GaN-HEMTs with superconducting gates

The impact of the gate resistance on the microwave and noise performances has been extensively studied in the literature [157] [158], and highlighted for cryogenic GaN-HEMTs in [A], [B] and [E]. Furthermore, in the previous section, the influences of the gate impedance and its gate width-dependence on the optimum impedance, noise resistance, and consequently the low-noise matching of the transistor, were experimentally demonstrated. Based on these observations, the introduction of a superconducting gate electrode could be expected to provide two major benefits: first, the thermal noise source associated with the gate would be mitigated, as the sheet resistance of the superconducting metallization approaches zero; second, the scaling of the gate resistance with the gate dimensions and geometry would also be eliminated.

Exploring these properties, the impact of integrating Nb-based superconducting gates in cryogenic GaN-HEMTs was investigated in [B]. For reference, devices with identical structures and dimensions but with Au-gates were simultaneously tested under the same conditions.

Using devices with single gate-finger design (Figure 35a), four-probe measurements can be used to examine the gate superconductivity (Figure 35b). In this case, the DC-measured end-to-end gate resistance is denoted as R_{g-ee}, to distinguish it from R_g in the small-signal model. R_{g-ee} and R_g compare by a factor of 1/3, accounting for the distributed effects over the active region at high-frequency operation [158].

In [B], R_{g-ee} measurements were reported for devices with different gate lengths, ranging from 0.5 µm to 0.15 µm. As shown in Figure 36, the results revealed a superconducting transition in the Nb-gates at a critical temperature T_c~9.2±0.5 K. The extracted sheet resistance of the Au-gate at room temperature (RT) and cryogenic temperature (CT) were approximately 3.5 nΩ·m/square and 0.5 nΩ·m/square,

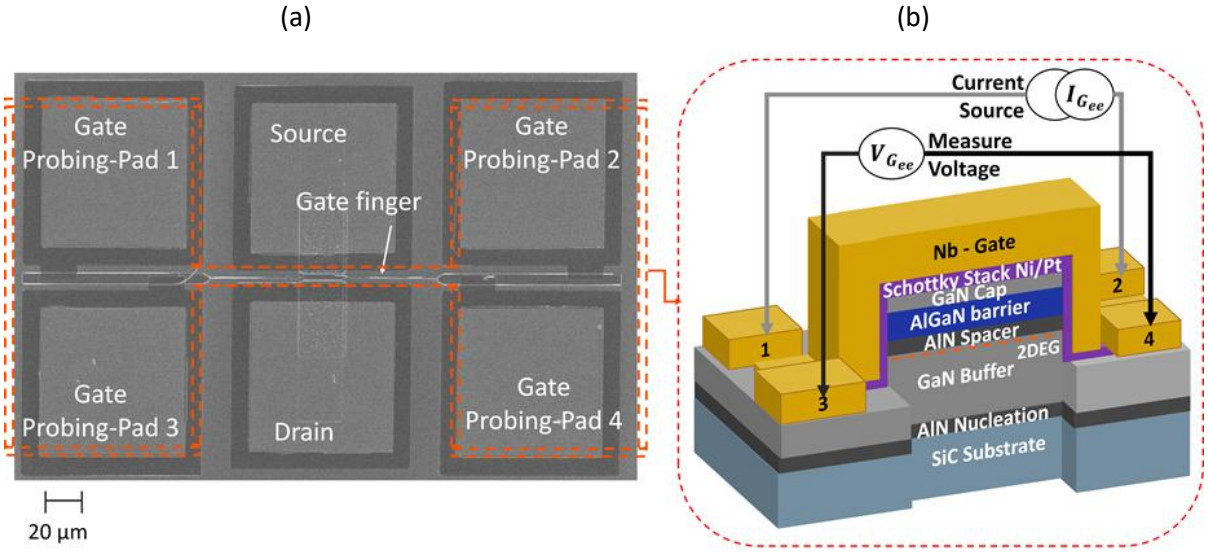

Figure 35: (a) SEM picture of a device featuring 1-finger gate, incorporating four gate probing pads, as designed for the DC end-to-end gate resistance measurements. (b) Schematic cross-section view of the gate finger, with illustration of the setup used for the end-to-end measurement of the gate resistance: a current is forced through one pair of the gate probing pads, while the second pair is used to measure the voltage drop across the gate finger.

respectively. This substantial reduction in sheet resistance with decreasing temperature for the Au metallization also highlights the benefit on noise performance when cooling the device.

The gate superconductivity was also verified using the small-signal-model obtained from S-parameters measurements, in transistors with two gate-fingers, following the procedure detailed in [B]. As shown in Figure 37, the extracted gate resistance in Nb-gated devices was minimized, compared to their Au-gated counterparts, indicating the impact of superconductivity. This conclusion was also verified to hold true independently of the gate-width. Hence, superconducting Nb-gates removes the consideration of the impact of gate resistance and its scalability when selecting a transistor size that best fits the application requirements. The average gate resistance with Nb was 0.4 – 0.5 Ω independently of the gate-width within a margin of error as discussed in [B]. In this case, the remaining part in the calculated $\mathrm{R_g}$ is attributed to the probing path of the gate electrode, as the absence of gate length scaling of the devices with Nb-gate confirms their stable and repeatable transition to a superconducting state. On the other hand, and as expected, $\mathrm{R_g}$ increased linearly with the gate-width in Au-gated transistors.

Analyzing the bias-dependence of $\mathrm{R_g}$, the onset of the forward Schottky gate conduction at $\mathrm{V_{F-C}}$ was found to correlate with the superconductivity breakdown of the Nb-gates. As a result, a sudden rise in $\mathrm{R_g}$ was observed at $\mathrm{V_{GS} > V_{F-C}}$, marking the transition to the normal state in Nb-gates, independent of their gate width. Conversely, no significant change in $\mathrm{R_g}$ of Au-gated transistors with was observed under these conditions, which further supports the causality effect of the gate leakage current on Nb-superconductivity. This behavior can be explained by a critical current for Nb-superconductivity, analogous to the effect of T_c, which was supplied and exceeded through the Schottky gate current at $\mathrm{V_{GS} > V_{F-C}}$ [159].

Nevertheless, comparing the results of noise characterization at 4 K from [B], GaN HEMTs with Au-gates outperformed their counterparts with Nb-gates. At the optimum-noise bias point, GaN-HEMTs with Nb-

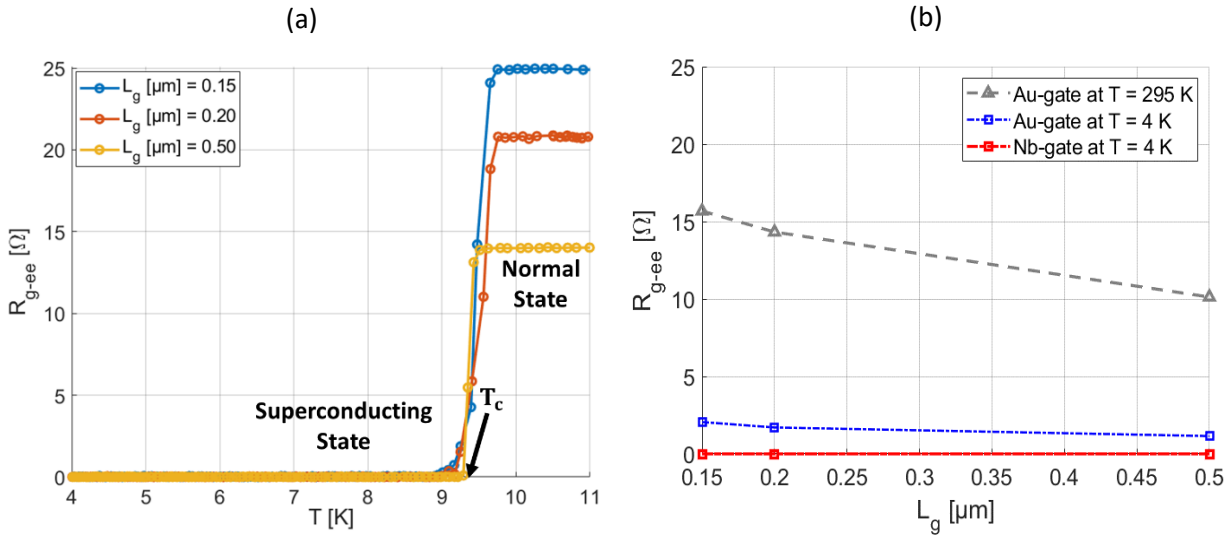

Figure 36: Results of the measured temperature of the end-to-end gate resistances ($R_{g\text{-}ee}$) with temperature, reproduced from [B]. (a) Variation of $R_{g\text{-}ee}$ in Nb-gated device with the cryogenic temperature down to 4 K. (b) Variation of $R_{g\text{-}ee}$ with L_g in the case of the Au-gated and Nb-gated devices.

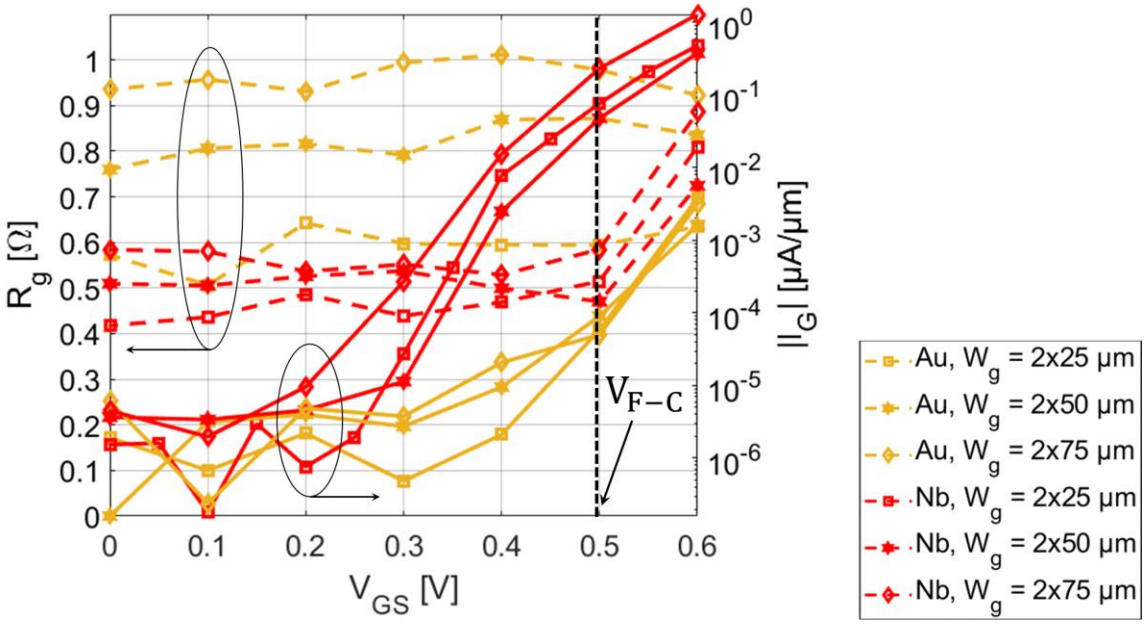

Figure 37: The gate-bias dependence of R_g (left axis) as calculated from the small-signal model and I_G (right axis), in Au-gated (in orange) and Nb-gated (in red) transistors. The markers square, hexagonal and diamond refer respectively to the unit gate widths of 25, 50 and 75 μm. At V_{GS} ~ V_{F-C}, I_G reaches a current density of ~ 0.1 μA/μm which coincides with a sudden significant rise of R_g.

gates presented T_{min} about 5 K higher than Au-gated devices, where $T_{min}$was around 8 K at 5 GHz (Figure 38a). This difference is linked to the transition in Nb-gates to normal-state. Indeed, under these bias conditions, superconductivity breakdown occurred under the influence of power dissipation from the channel. This was verified using four probes measurements at on-state operation conditions as shown in Figure 38b.

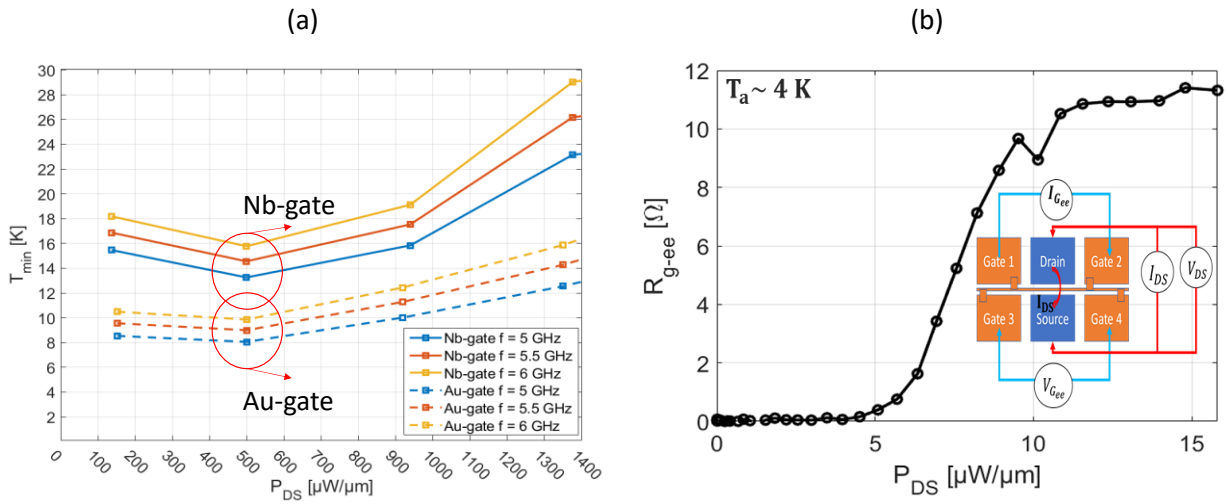

Figure 38: (a) Comparison of calculated T_{min} vs. the dissipated power, $P_{DS} = V_{DS} \times I_{DS}$, at CT in GaN-HEMTs with Au and Nb-gates at f [GHz] = 5 – 5.5 - 6. (b) Variation of the end-to-end gate resistance of the Nb-gate with the channel power dissipation, at temperature T_a ~ 4 K. The inset shows a schematic representation of the test structure with the 4-points configuration, used to measure the end-to-end gate resistance while varying the drain to source bias. Reproduced from [B]

In the normal-state, R_g of the Nb-gates becomes 3 times higher than in Au-gates, which explains the difference in noise performance under optimal low-noise bias conditions. In this case, the break of superconductivity can be ascribed to self-heating effects from the channel, leading to increase in physical temperature locally beyond T_c ~ 9.2 K, despite the temperature of the cryogenic chamber maintained around 4 K. This might indicate that the thermal impedance of the device allows such a gradient. Thus, practical use of GaN-HEMTs with superconducting Nb-gates for low-noise applications is conditioned by further enhancement of the heat-sinking capabilities in the future.

Besides, it should be noted that the comparison of the results of the Au-gated transistors from this section with those presented in [A] reveals an important role of the gate capacitive coupling of the channel noise. Indeed, these transistors present a difference in the gate field-plates dimensions; L_{FPS} and L_{FPD} were respectively 50 % and 25 % shorter in [A]. This difference affects the gate capacitance, and consequently the cut-off frequency of the devices. The latter has a significant impact on T_{min}, further discussed in a later dedicated section.

6.3 Impact of MIS-gate structures

Metal Insulator Semiconductor (MIS)-HEMTs are obtained by introducing a dielectric layer between the gate metal and the semiconductor barrier. The MIS structure reduces the probability for the gate- current leakage through the barrier, thereby improving the device reliability. Preventing the gate-current leakage can suppress the associated shot-noise source, which contribution increases with low frequencies and constraints the design of broadband LNAs as studied in different works [160] [161]. The gate leakage was also identified among the limitations for the noise performance of cryogenic GaN-HEMTs in [A]. Furthermore, LNAs based on MIS-HEMTs can offer a better level of linearity compared to HEMTs. This is due to a larger gate-voltage range for on-state operation, as typically manifested by the transconductance exhibiting a flatter and broader V_{GS}-dependent profile [162]. As introduced in chapter 1, linearity is an important feature to prevent the failure of systems prone to interferences such as in radars and radio-astronomy instrumentation. Hence, the development of MIS-HEMTs also contribute to reinforce the advantage of the GaN-HEMTs technology over other materials in terms of robustness and survivability.

The impacts of MIS structure on the electrical performances largely depend on the type of gate dielectric and deposition techniques. Various gate dielectrics were investigated in the literature, such as SiO_2 [163], Al_2O_3 [164], HfO_2 [165], SiN [166] and SiNx [167]. GaN MIS-HEMTs with ALD-deposited Al_2O_3 gate dielectric of 0.25 µm gate-length exhibited a noise performance of 1 dB at 10 GHz, with a cut-off frequency of 40 GHz [168], with the same technology demonstrated to feature a superior linearity than its conventional-HEMTs counterpart [169]. Using PEALD-SiN gate dielectric, better minimum noise performance at 10 GHz

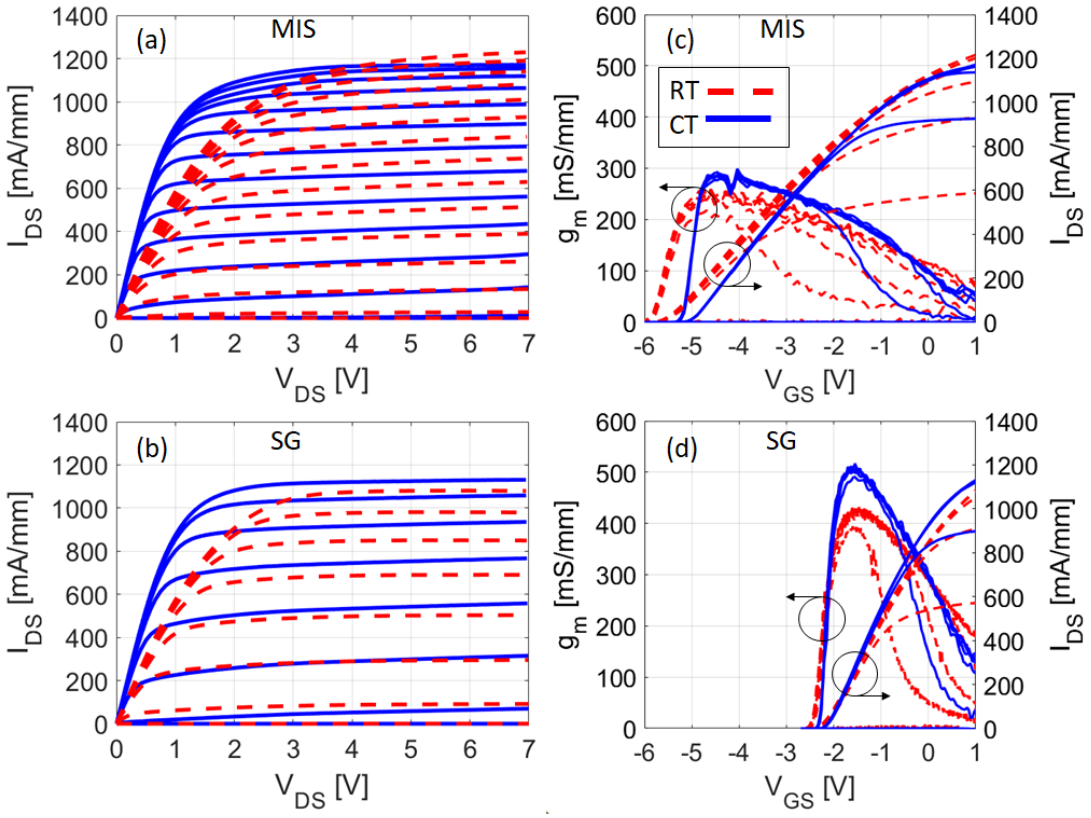

Figure 39: DC characteristics of the MIS- (top) and SG- (bottom) HEMTs with 2x25 µm gate-width, at RT (red, dashed lines) and CT (blue, solid lines), (a) – (b): I_{DS}-V_{DS} curves at V_{GS} = -2.5 V to 1 V, with 0.5 V steps. (c) – (d): V_{GS}-dependence of I_{DS} and g_m, at V_{DS} from 1 to 7 V. Reproduced from [D].

of 0.18 dB was more recently reported in [170] for a LNA based on 0.25-µm gate-length. The integration of the MIS-structure to N-polar GaN devices was also revealed of promising potential for high-frequency and low-noise applications, with high cut-off frequencies of > 140 GHz obtained using 80-nm gate length with SiNx gate dielectric in [171], and other reports on highly-linear LNAs with a noise performance of ≤1.9 dB up to 30 GHz [172]. However, the cryogenic performance of GaN-based MIS-HEMTs at cryogenic temperatures were hardly investigated. DC and low-frequency noise characteristics measured at 4.2 K were recently studied in [173], concluding on overall improvement of carrier velocity and mobility of the GaN MIS-HEMTs upon cooling. Whereas in [174], high-frequency characteristics down to 16 K were investigated, showing improvements in the cut-off frequency at decreased temperatures with a relative saturation below 100 K. However, high-frequency noise data were first reported in [D]. In [D], a comparison of microwave and noise characteristics of GaN MIS-HEMTs and Schottky-gated (SG) GaN-HEMTs with identical epitaxy and layout at 4.2 K. In this case, the MIS structure was obtained by LPCD Si-rich SiNx, with 0.2-µm gate length.

The DC characteristics of the MIS-HEMTs and SG-HEMT are presented in Figure 39. Compared to the SG-HEMT, the MIS-HEMT presents a larger maximum I_{DS}. In addition, the MIS-HEMTs feature a substantially broader V_{GS}-profile gm, highlighting their superior linearity. Nevertheless, the MIS-HEMTs present a larger pinch-off voltage and lower transconductance, both due to a larger gate-channel distance.

R_{on} and g_m improve in both types of devices upon cooling, due to the increase in electron mobility and velocity. However, in contrast to the SG-HEMT, the MIS-HEMT experiences more severe sings of trapping at CT, as manifested by a degradation of I_{DS} at high V_{GS}. In addition, a more significant shift of the pinch-off voltage is observed upon cooling of the MIS-HEMT (~ +0.4 V against +0.1 V for the SG device). The aggravation of trapping at CT can be related to the slowing-down of de-trapping mechanisms, in connection with the findings from [F]. Similar anomalies were also recently reported for other GaN MIS-HEMTs at low temperatures and ascribed to trapping activities around the gate dielectric [175] [61]. In fact, these results highlight a key challenge inherent to the MIS-structures and gate dielectrics, as the quality of their interfaces and intrinsic defects has a significant influence on the device performance [176].

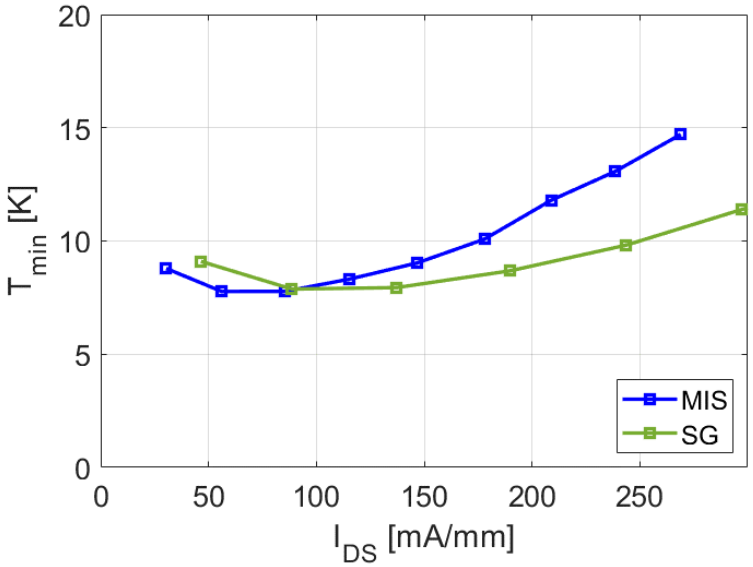

Figure 40: I_{DS}-dependence of average T_{min} in the frequency range of 3 – 7 GHz at V_{DS} = 4 V, of the SG and MIS-HEMTs shown in green and blue respectively, from [D].

An average minimum noise temperature of around 8 K in the 3 – 7 GHz range was achieved in both SG- and MIS-HEMTs at CT (Figure 40). However, of T_{min} of the MIS-HEMT presents a larger degradation with increasing of I_{DS}. This variation is closely related to the current-dependence of the intrinsic cut-off frequency, controlled by the intrinsic transconductance and gate capacitance.

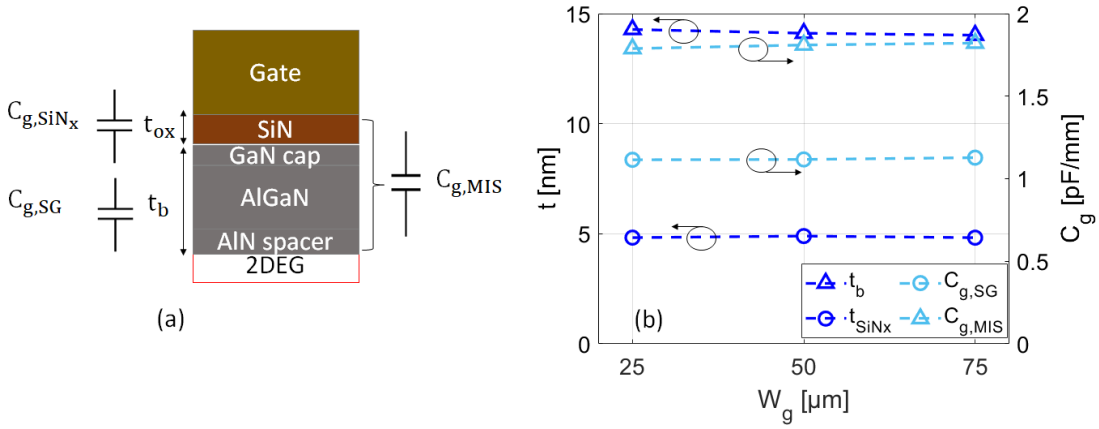

Figure 41: (a): illustration of the equivalent capacitances in the MIS-HEMT. $C_{g,SG}$ is common to both devices SG and MIS-HEMTs. (b): On the left y-axis: extracted thicknesses of the SiN_x gate dielectric (dark blue circles) and the SG barrier (dark blue triangles). Right y-axis: the equivalent gate capacitances from the small-signal model, at V_{DS} = 0 V at CT, of SG and (light blue triangles) and MIS-HEMTs (dark blue circles). The results are verified for 3 different unit gate-widths of 25, 50 and 75 µm.

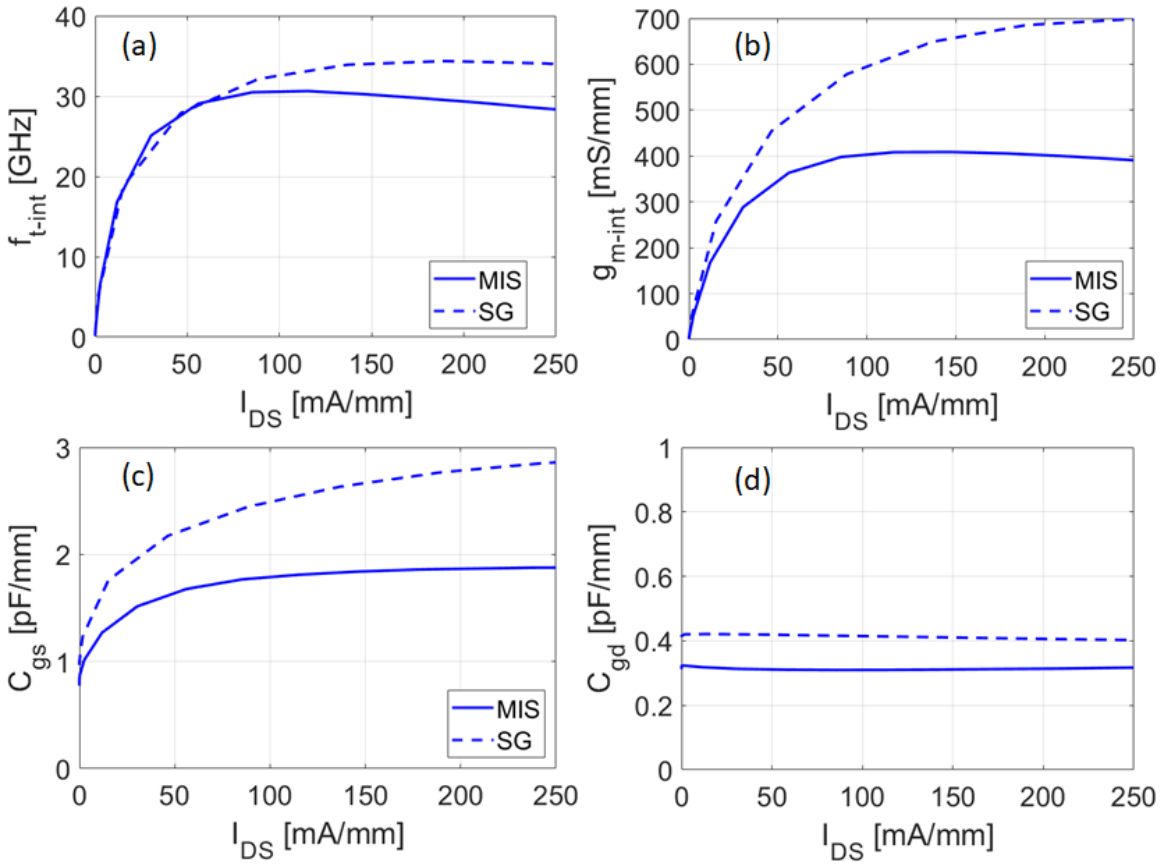

Figure 42: I_{DS}-dependence at V_{DS} = 4 V of the intrinsic small-signal parameters influencing f_{t-int} at CT, in the 2x25 µm HEMTs with MIS (solid lines) and Schottky (dashed lines) gates: (a): f_{t-int}, (b): g_{m-int} , (c) $C_{gs,}$ (d) C_{gd}. Reproduced from [D].

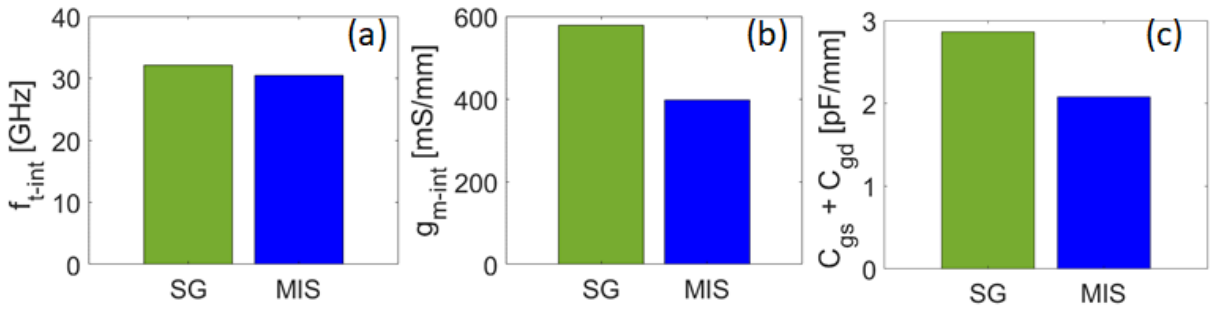

Figure 43: Comparison of the intrinsic small-signal parameters influencing $f_{t\text{-}int}$ at the optimum-noise bias point, in the 2x25 µm MIS- and SG-HEMTs, represented in blue and green respectively. (a): $f_{t\text{-}int}$. (b): $g_{m\text{-}int}$ and (c) C_{gs}+C_{gd}

The insertion of a gate dielectric layer reduces the total gate capacitance by introducing an additional series capacitance, along with the semiconductor barrier capacitance, which represents the coupling with the 2DEG under the gate. The series MIS capacitance relates to the thickness and dielectric constant of the passivation layer:

$$C_{g,\ SiN_x} = \frac{A_g \epsilon_{SiN_x}}{t_{SiN_x}} \tag{59}$$

Where A_g is the effective area of the gate region. Similarly, the barrier capacitance ($C_{g,\ SG}$) relates to its dielectric constant and thickness t_b. Note that, in this case, t_b implicitly accounts for the sum of the $Al_{0.3}Ga_{0.7}N$ barrier, the GaN cap and AlN spacer layers. The contribution of the two latter is neglected in these formulations for simplicity. Hence, a lower gate capacitance in the MIS-HEMTs ($C_{g,\ MIS}$) is obtained as:

$$C_{g,\ MIS} = \frac{1}{\frac{1}{C_{g,SG}} + \frac{1}{C_{g,SiN_x}}} \tag{60}$$

These formulations can be used consistently to verify the thicknesses of t_b and t_{SiN_x}, using the gate capacitances obtained from the cold-FET small-signal model [177]. To exemplify, SG and MIS devices with rectangular gates were selected, as the contribution of the FPs would otherwise lead to a more complex analysis. Their effective gate-length was adjusted to 0.28 µm to account for fringing effects [178]. The dielectric constant of SiNx and the barrier are around 2.4 and 10.3, from [179] and [180] respectively. The resulting values align accurately with the nominal values on the mask with t_b ~ 14 nm and t_{SiN_x}~5 nm, as shown in Figure 41 based on data of 3 different sizes for each type of devices.

Through the same capacitive effects, the transconductance in the MIS-HEMT is also reduced accordingly, as shown in Figures 42a–d. Resulting from these effects, the MIS-HEMT presented a peak of f_{t-int} at CT around 30 GHz, about 5 GHz lower than the SG-HEMT. However, at the optimum bias point (I_{DS}~85 mA/mm), the differences in g_{m-int} and gate capacitances are nearly canceled as shown in Figures 43a–c. Consequently, due to a steeper increase of $g_{m-int}$with I_{DS} than C_{gs}, f_{t-int} in both devices converge to similar levels (Figure 43a).

Further increasing I_{DS}, g_{m-int} of the SG-HEMT becomes sufficiently large to compensate for the higher C_{gs} and C_{gd} compared to the MIS-HEMT, resulting in a higher f_{t-int}. Consequently, the noise temperature of MIS-HEMTs experiences a more significant drop at high I_{DS}, as T_{min} is linearly dependent to f_{t-int}.

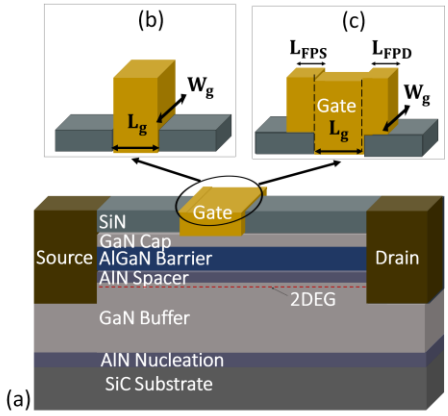

Figure 44: Epitaxial structure (a), and gate designs of the devices without (b) and with field-plates (c). The gate-length (L_g), the length of source and drain field-plates (L_{FPS}, L_{FPD}) and gate-finger width (W_g) were 0.2, 0.2, 0.2.

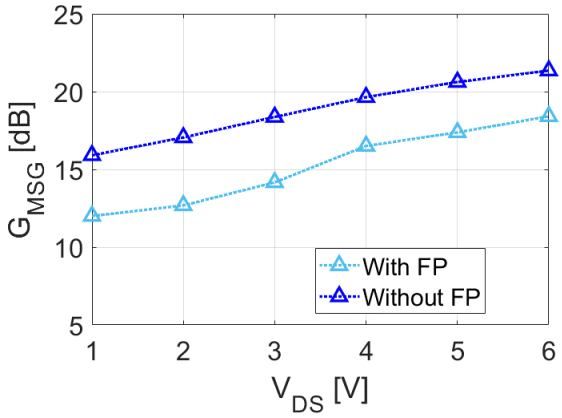

Figure 45: Variation of the maximum stable gain (G_{MSG}) at 5 GHz with V_{DS} at 4.2 K, in the 2x50 µm device with (light blue) and without field-plates (dark blue).

Nevertheless, the behavior of the g_{m-int}/C_{gs} ratio, that is of f_{t-int}, at low I_{DS} is promising from the perspective of design optimization for low-noise operation. Indeed, using the same epitaxy, further improvement in the gate leakage in the MIS structure is expected to result in a better noise performance at the same low current conditions.

6.4 Impact of gate field-plates

The integration of field plates (FPs) played a major role in advancing GaN HEMTs for high-frequency power applications, enabling an advantageous power density by more than an order of magnitude over alternative materials [181]. This is due to the FPs' ability to alleviate high-field issues by reshaping the electric field profile. In the context of low-noise applications, high-field effects are also increasingly underscored as their impact is amplified by the continuous down-scaling of the gate length and lateral dimensions [54]. Hence, to improve reliability and robustness, LNAs based on GaN-HEMTs with various field-plate structures were proposed in the literature [182]. In addition, incorporating field-plates in GaN-based LNAs increases their robustness against power and bias overloads, as reviewed in [183]. Furthermore, GaN HEMTs with optimized design for low-noise operation were shown to benefit from reduced short-channel-length effects through the integration of FPs [184].

In terms of noise performance, the field-plates reduce the thermal noise associated with the gate electrode by increasing its cross-section. However, the FP gate-metallization introduces additional detrimental parasitic capacitances. In fact, the FP capacitance reduces the cut-off frequency, leading to a degraded noise performance. Nevertheless, as shown in [185], an overall noise performance may result from a trade-off between the reduction of the gate resistance (R_g) and increased gate capacitances (C_{gs} and C_{gd}). Studies on GaAs and InP HEMTs have also concluded that the benefits from using laterally extended gates may exceed their detrimental effects in short-channel devices [157]. However, R_g may benefit from a simultaneous reduction through an appropriate layout design, involving a short periphery and/or multiple gate-fingers, in addition to processing advances [156]. On the other hand, mitigating the FPs' capacitances may be especially challenging as the FP length exert a simultaneous control over both the associated field-modulation and RF parasitic effects [186] [187]. The parasitic drawback of the FPs can

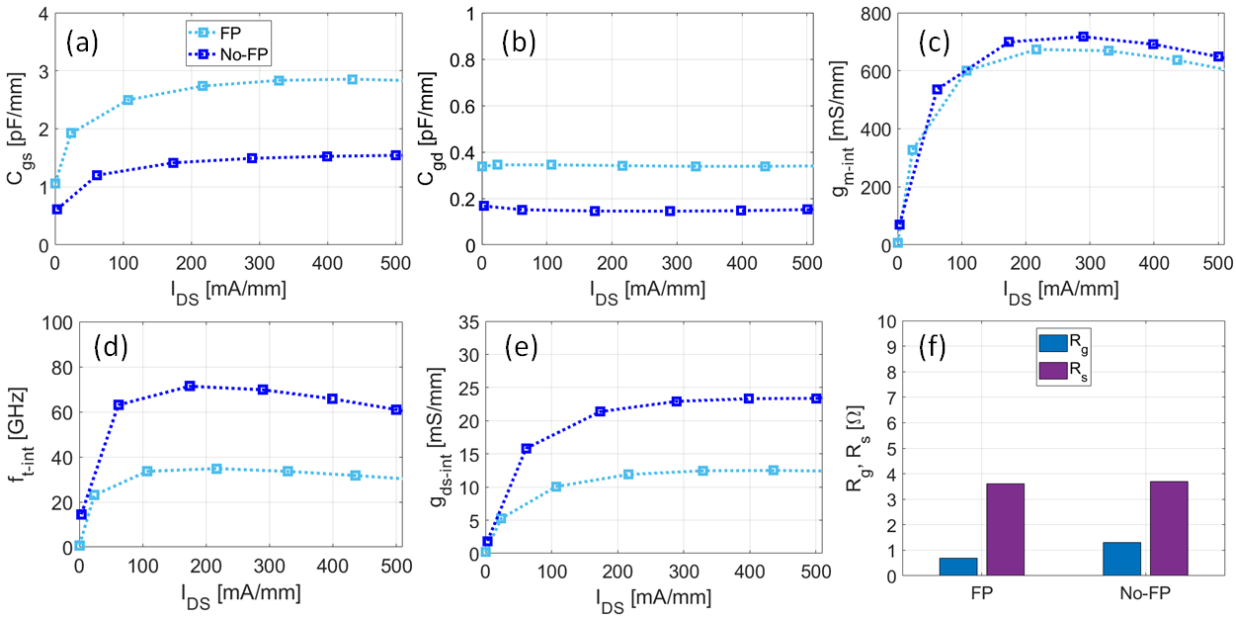

Figure 46: I_{DS}-dependence of the small-signal parameters at V_{DS} = 4 V at CT in the devices with FP (light blue) and without FP (dark blue). (a) C_{gs} (b) C_{gd}, (c) $g_{m\text{-}int}$, (d) $f_{t\text{-}int}$, (e) $g_{ds\text{-}int}$, (f) R_g and R_s.

also be compensated by a simultaneous lateral scaling and the optimization of access regions as demonstrated in [188]. LNAs based on similar technologies using 0.15 µm gate-length exhibited a noise temperature (noise figure) of 66 K (0.89) dB at 10 GHz in [189], with a peak cut-off frequency of 50 – 60 GHz at room temperature. To achieve the same goal at higher frequencies, a more advanced gate design may involve a large aspect ratio between the lateral and vertical dimensions of the gate, further referred to as mushroom- or T-gates [190]. Using T-gates with reduced lateral dimensions, the cut-off frequency of 162 GHz and 225 GHz using gate-lengths of 110 and 55 nm, respectively in [190], and exceeded 400 GHz in [191]. Combination of optimized gate geometry with lateral extensions, scaled with adapted vertical engineering, provided a better control of parasitic effects [192] [193]. Using such configurations with 50-nm gate-length, a noise performance of 35.4 K (0.5 dB) at 30 GHz at room temperature was achieved in [194].

However, such complex optimizations may rely on a prior analysis of the parasitic effects at the same temperature of intended applications. From this perspective, the cryogenic behaviour of the gate parasitic effects in GaN HEMTs, based on the design illustrated in Figure 44, were analysed at cryogenic temperatures in [E].

Figure 45 compares the V_{DS}-dependence of the maximum stable gain (G_{MSG}) at 5 GHz at 4.2 K. In both devices, G_{MSG} increases rapidly up to V_{DS} = 4 V, which marks a relative saturation of the electron velocity. Due to this behavior, the following analysis is focused at V_{DS} = 4 V, as larger V_{DS} would increase thermal effects with no major improvements of gain and noise. The devices without FP present about 3 dB advantage, independently of the gate-width. Thus, this is quantifying the impact of the FPs' parasitic effects on the gain. The origin of this impact is confirmed by a nearly doubling of C_{gs} and C_{gd}, at their saturation levels, in presence of the FPs (Figure 46). The similarity in the increase ratios of C_{gs} and C_{gd} compared to the case without FP relates to L_{FPD} and L_{FPS} extending by the same distance, equal to L_g. The FPs add to C_{gs} and C_{gd} from the non-FP situation a parallel contribution, which is essentially controlled by L_{FPD} and L_{FPS}. In both types of devices, C_{gs} exhibits a similar I_{DS}-dependent increase, pointing to a comparable 2DEG modulation effect by the gate, consistent with their identical epitaxial

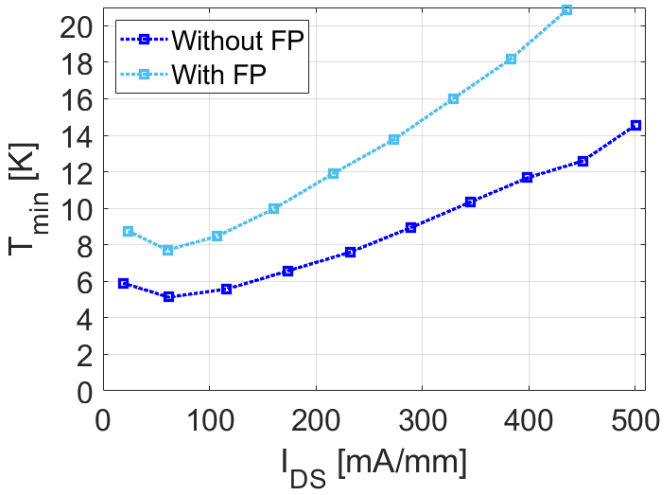

Figure 47: I_{DS}-dependence of T_{min} at 4.2 K at 5 GHz in the 2x50 µm devices with and without FP, represented in light and dark blue respectively.

properties. This is further confirmed by the variation of g_{m-int}, presenting similar shape of the curves at all I_{DS} levels with slightly reduced peak with FP. While this difference was only about 5 % and can be due to processing yield and modeling effects, other reports suggested that the larger effective gate-length in field-plated devices can result in a reduction of their g_{m-int} amplitude [186] [195].

Figure 47 compares the variation T_{min} of the devices with and without FP, with I_{DS} at V_{DS} = 4 V at 5 GHz. At the optimum bias point, T_{min} increases by ratio of 1.5 in presence of FP, evolving from 7.7 K (0.11 dB) to 5.1 K (0.08 dB) with and without FP, respectively. This suggests competing influences on T_{min} of the small signal parameters impacted by the FPs. T_{min} is primarily impacted by the intrinsic cut-off frequency (f_{t-int}), through the effect of C_{gs} and C_{gd}, as T_{min}, can be approximated by:

$$T_{min} \simeq \frac{2f}{f_{t-int}} \sqrt{g_{ds-int} T_d R_t T_g} \qquad (61)$$

Where $R_t = R_g + R_s + R_{gs}$. The peaks of f_{t-int} were around 35 and 71 GHz with and without FP respectively, resulting from the same decrease ratio with FP of C_{gs} and C_{gd}. Hence, T_{min} was also affected by approximately the same ratio. On the other hand, the FP reduces the gate resistance by 45%, passing from 7 to 13 Ω/mm at CT. This translates to 16 % worsening of T_{min} in absence of FP, as shown in [E]. However, in both devices with and without FP, R_g represented respectively 65 to 80 % of R_s. The latter is unaffected by the FPs. Hence, from the noise perspective, the effect of R_s dominates over R_g. In [E], this analysis was extended to other values of total gate-widths (W_g) of ± 50 µm. In these cases, R_g and R_s scale in opposite directions as shown earlier in this thesis. Hence, the larger the gate-width, the detrimental impact of R_g in absence of FP is more emphasized, as R_g increases and R_s decreases. However, R_g remained lower than R_s even for the largest tested W_g of 150 µm, indicating that the total benefit of reducing R_g could not compensate for the impact of FP on C_{gs} and C_{gd}in any of these cases.

Another parameter impacted by the inclusion of the FPs is g_{ds-int}, found to decrease by nearly the same ratio as the increase of C_{gs} and C_{gd}. The larger g_{ds-int} in absence of FP may relate to larger trapping or injection of the channel electrons, otherwise prevented by the FP mitigation of the electric field as introduced in chapter 3. This behavior might also reflect a larger effective length in presence of FP, leading

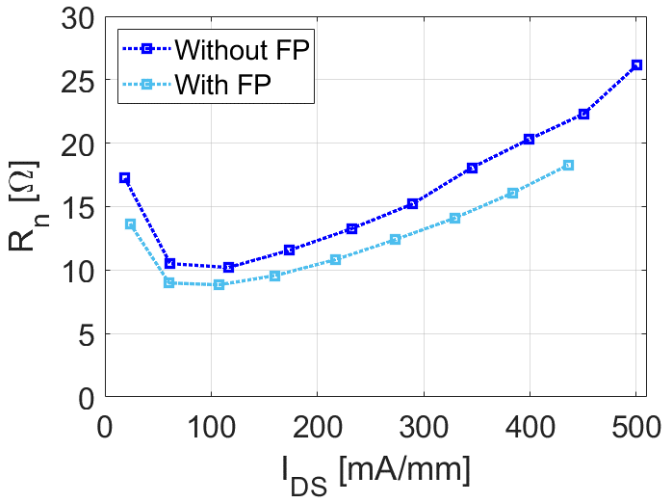

Figure 48: I_{DS}-dependence of R_n at 4.2 K at 5 GHz in the 2x50 µm devices with and without FP, represented in light and dark blue respectively.

to less punch-through effects which are typically observed with short channel length (also referred to by short channel effects) [196]. The latter are also manifested by a stronger dependence of the pinch-off voltage to V_{DS}, which was observed in the cryogenic GaN-HEMTs without FP in [E]. Hence, at the same bias conditions, the FP devices are less likely to experience charge trapping or short channel effects. A lower g_{ds-int} in presence of FP is beneficial from the microwave noise perspective, as contributing by the same weight as the sum of R_g+ R_s. However, a more in-depth analysis in [E] revealed that the advantage of g_{ds-int} in field-plated devices is counterbalanced by a simultaneous increase of T_d. In fact, the product $T_d \cdot g_{ds-int}$ accounts for the 2DEG's equivalent noise temperature [197]. The larger T_d in presence of FP is an undirect consequence of the larger gate capacitance, leading to a larger coupling between the thermal noise sources from the channel and the gate. Consequently, based on the analysis in [E], the net advantage for the device with FP from the reduction of g_{ds-int} is of only 7 % after subtracting the detrimental increase of T_d. Nevertheless, a reduced $T_d \cdot g_{ds-int}$ product suggests an enhanced 2DEG confinement, as pointed in studies on HEMTs based on other materials [198]. Therefore, these results predict a more prominent impact of the use of FP with further gate-length reduction, as generally leading to more pronounced short-channel effects that can affect g_{ds-int} and the 2DEG confinement [199].

Another noise parameter impacted by g_{ds-int} is the noise resistance (R_n). Figure 48 compares the I_{DS}-dependences of R_n with and without FP, showing a small advantage for the device with FP at all tested bias conditions. In fact, a first approximation of R_n relates to the small-signal parameters and T_d by the relationship:

$$R_n \simeq \frac{T_g R_t}{T_0} + \frac{T_d g_{ds-int}}{T_0} \frac{\left(1 + \left(2\pi f\, C_{gs} R_t\right)^2\right)}{g_m^2} \qquad (62)$$

At frequencies around 5 GHz, the term $1+(2\pi f\, C_{gs} R_t)^2$ tends to 1. Hence, the effects of R_t and the product $T_d \cdot g_{ds-int}$ are dominating in this situation. Therefore, the same analysis above on the FP impacts on T_{min} applies to the parameters involved in this equation. The slight advantage in R_n for the device with FP results essentially from the net decrease of $T_d \cdot g_{ds-int}$, as the product $T_g \cdot R_t$ is further insignificant at such low physical temperatures. Previous works highlighted the role of the device geometry in optimizing R_n, through a careful selection of the gate dimensions to achieve a trade-off between the contributions

of R_t and the g_{ds-int}/g_{m-int}^2 ratio [200]. The latter parameter can also be addressed through a proper optimization of the vertical epitaxial properties and dimensions, to enhance g_{m-int} and improve the 2DEG confinement [201]. The enhancement in the design of broadband LNAs at cryogenic temperatures through reduced R_n was showcased in various reports based on different technologies, as in [202] and [203]. Hence, the results from [E] highlight a positive impact of the FPs on the optimization of R_n at cryogenic temperatures.

7 Conclusions and future work

This thesis investigated the potential of GaN-HEMTs technology for low-noise applications at cryogenic temperatures. Improvements in noise performance of GaN-HEMTs upon cooling have been demonstrated to be comparable to state-of-the-art technologies, through well-established characterization and modeling techniques., These findings pave the way for harnessing GaN-HEMTs' superior robustness with further low-noise optimization.

For this purpose, the impact of key design parameters on the microwave noise behavior of cryogenic GaN HEMTs have been analyzed; including gate geometry, total periphery, lateral extension with field-plates and Metal-Insulator-Semiconductor (MIS) gate structures. Notably, the integration of superconducting-niobium gates has been demonstrated for the first time. Additionally, the effects of charge trapping on device stability and reliability at cryogenic temperatures have been studied, revealing an enhanced impact upon cooling, and informing design strategies to mitigate these phenomena.

AlGaN/GaN HEMTs with 0.2-µm gate-length exhibited a up to tenfold reduction in minimum noise temperature (T_{min}) upon cooling from room temperature to 4 – 10 K, achieving a best performance of 4 – 5 K at 5 GHz. These results, verified across multiple samples with varying gate peripheries are within a factor of four of the state of the art, suggesting further improvements through refinements in device layout and epitaxial design. Based on S-parameters and noise measurements at cryogenic temperatures, a model was developed to describe the frequency and bias dependence of cryogenic microwave noise behavior. Furthermore, the model also featured consistent scalability with gate width, providing a basis for designing GaN-based LNAs that meet transistor size-related requirements. Analysis of the noise model indicates that noise improvement is mainly due to increased transconductance, reflecting enhanced electron transport and reduced scattering in the channel, as well as reduced thermal noise from gate and source resistances. However, the source resistance exhibited a stronger impact than the gate resistance within the range of 50 to 150 µm total periphery. Despite significant reduction upon cooling, gate leakage was also found to contribute to shot noise.

To mitigate thermal noise associated with gate resistance, superconducting niobium-based gates has been demonstrated below the critical temperature of T_c~9.2 K using both DC and S-parameters measurements. Under these conditions, gate resistance was suppressed across various gate geometries and peripheries, regardless of gate geometry or periphery, with various gate lengths ranging from 0.5 to 0.15 µm. This demonstrates that the typical increase in gate resistance observed with lateral downscaling in gold-based gate metallization, can be effectively mitigated with this approach. However, under on-state operating conditions, superconductivity in the Nb gate was suppressed before reaching the optimal low-noise bias point, leading to significant noise degradation as the Nb gate resistance exceeded that of Au-based gates. This effect is attributed to power dissipation from the channel, which heats the gate, as observed through DC measurements under on-state conditions on dedicated test structures. These findings highlight the need for further investigation of thermal mitigation techniques and superconducting materials with higher critical temperatures to enhance noise reduction through gate resistance suppression.

The impact of MIS structures on microwave and noise characteristics at cryogenic temperatures was investigated by incorporating a thin SiN_x layer between the gate and the GaN cap layer. While MIS-HEMTs exhibited a lower peak cutoff frequency than their Schottky-gated counterparts, T_{min} remained unaffected

under optimal low-noise bias conditions. This behavior was attributed to the counterbalancing effects of the MIS structure on gate capacitance and transconductance at low I_{DS}. However, no significant improvement in gate leakage current was observed, suggesting potential for further noise reduction at low frequencies. These results indicate that MIS structures could benefit broadband low-noise design, provided that gate leakage is further minimized.

Field plates were found to introduce a parasitic contribution to gate capacitance, which had a more detrimental impact on cryogenic noise performance than their beneficial effects on gate resistance and drain-source conductance. As a result, the cutoff frequency was nearly halved, with peaks at 35 GHz and 71 GHz for devices with and without field plates, respectively. At 4 K and 5 GHz, GaN HEMTs with field-plates exhibited at least 35% higher T_{min} compared to their counterparts without field-plates. However, they also demonstrated lower noise resistance due to reduced drain-source conductance, which was attributed to mitigated high-field effects and a larger effective gate length. While field plates can be advantageous for broadband LNA design, further optimization, such as by adopting a T-gate design, is needed to mitigate their parasitic effects.

Charge trapping was identified as a key in the degradation of current at cryogenic temperatures, particularly at high V_{GS} and V_{DS}. Transient cryogenic measurements and comparison with undoped devices confirmed a substantial influence of Fe-doping in the buffer. Notably, gate field-plates mitigated charge trapping effects, suggesting that minimal doping incorporation, combined with an optimized gate field-plates design, could ensure a more reliable and stable operation at cryogenic temperatures.

In addition to noise reduction, minimizing power consumption will be a key challenge in the future, as cryogenic applications typically have stringent power budgets [204]. At low-noise bias conditions, the power dissipation of the cryogenic GaN-HEMTs investigated in this work was an order of magnitude higher than the state-of-the-art based on III-V technologies [115]. Future efforts to address this issue could involve more aggressive reduction of the source-to-drain distance, as demonstrated at room temperature in previous studies [122] [205]. This approach decreases the on-resistance, allowing saturation to be reached at lower levels of V_{DS}. Simultaneously, lateral downscaling can minimize the access resistances, especially on the source side, which has been identified as critical for achieving lower minimum noise temperatures, as shown in [A] and [E]. Another way to reduce the source resistance may involve the re-growth of heavily n-doped GaN [206]. This has been shown to significantly reduce the resistivity of ohmic contacts, achieving values as low as 0.05 Ω.mm at room temperature in [207], nearly an order of magnitude lower than current process and approaching contact resistances typical of III-V materials [108].

The field-plates capacitance can be minimized by adapting a T-gate design, adjusting the height of the gate and its lateral extension [193]. Additionally, minimizing the passivation thickness may also help to reduce the parasitic gate capacitance, but might be achieved at the cost of enhanced trapping [208]. Downscaling of the gate length further reduces gate capacitance and improves the transconductance, leading to higher cut-off frequencies and lower minimum noise temperatures. However, this may also exacerbate short-channel effects, which can be mitigated by reducing the gate-to-channel distance via gate recessing or a thinner barrier layer [209].

As gate-length and lateral dimensions are further reduced, superconducting gates could play an increasingly significant role in noise performance. However, the break of superconductivity due to self-heating from the channel calls for further improvement of the thermal conductivity of the epitaxial structure to increase the critical power dissipation threshold. Alternative superconducting materials with

higher critical temperature such as NbN with T_c up to 16 K [210], could provide a solution by maintaining low gate resistance under lower noise bias conditions. Moreover, the lattice structure of GaN has been demonstrated to facilitate high-quality integration of NbN [211]. Additionally, integrating superconducting gates to MIS-HEMTs with reduced gate leakage current may further reduce the probability of superconductivity breakdown as discussed in [B]. Other techniques for mitigating gate leakage, including the use of alternative dielectric materials, have recently been explored [212] [170], their cryogenic behavior worth further investigation in the future.

To address charge trapping due to buffer doping, one possible solution is the incorporation of a back-barrier layer beneath the channel [88]. However, this approach has also been shown to affect the heat dissipation [213]. Another alternative may involve a buffer-free design, recently proposed to reduce trapping effects [214]. In this configuration, the nucleation layer acts as a back-barrier to a relatively thin GaN channel layer. Moreover, this design has demonstrated high mobility at room temperature (>2200 cm^{-2}/Vs) [215], which can contribute to noise reduction at cryogenic temperatures.

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