Thesis for the Degree of Doctor of Philosophy

Novel Approaches for Thermal and Electrical Characterization of GaN HEMTs

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Abstract

The evaluation of microwave components requires detailed knowledge of different performance aspects, and component models must be extracted from highly accurate characteristics. However, heating and trapping effects in active components create multifaceted characteristics with complex behavior. This creates major measurement challenges and can cause established measurement methods to yield inaccurate and inadequate information. This thesis outlines solutions to problems faced in the characterization of GaN-based devices and circuits by introducing new measurement techniques capable of capturing complex characteristics and mitigating distortion due to trapping effects.

A new method to perform the I_{ds}-V_{ds} characterization is shown, which minimizes trap-related memory effects by controlling the ordering of the bias points in the sweep. This allows extracting rudimentary IV properties, and facilitates studying the effects of trapping and heating separately. In addition, a method for electric-based thermal evaluation of GaN semiconductor technologies is outlined, where trap-related distortion in the thermal resistance is suppressed, which facilitates the comparison of thermal properties of different devices. A method to electrically characterize the lateral heat spread is also introduced, by utilizing the HEMT temperature characteristics to design a thermal sensor suitable for integration into GaN MMICs. This enables the use of standard electrical test equipment to measure lateral thermal coupling in packaged circuits. Thermal compensation is explored using a new biasing technique to compensate for thermal performance degradation in an LNA, in which the gate- and drain-voltage dependencies of the RF performance are utilized to maintain a constant gain as the temperature increases. Lastly, GaN HEMT breakdown measurements and characteristics are examined, and a method for RF breakdown characterization is introduced. This allows studying the breakdown at different signal conditions, and comparisons show that the breakdown voltage increases with frequency, which demonstrates the need to evaluate devices under application-relevant conditions. Overall, the proposed methods in this thesis enable more comprehensive and accurate assessments of thermal and electrical device properties, which is crucial in the development of new devices and circuits.

Keywords: AlGaN/GaN, breakdown, characterization, HEMT, measurement, thermal coupling, thermal effects, thermal resistance, trapping effects

List of Publications

Appended Publications

This thesis is based on the content in the following papers:

[A] J. Bremer, N. Rorsman, and M. Thorsell, "Method for Suppressing Trap-Related Memory Effects in IV Characterizations of GaN HEMTs," *IEEE 36th International Conference on Microelectronic Test Structures*, Edinburgh, United Kingdom, April, 2024.

[B] J. Bremer, D. Chen, A. Malko, M. Madel, N. Rorsman, S. Gunnarsson, K. Andersson, T. Nilsson, P. Raad, P. Komarov, T. Sandy, and M. Thorsell, "Electric-Based Thermal Characterization of GaN Technologies Affected by Trapping Effects," *IEEE Transactions on Electron Devices*, vol. 67, no. 5, pp. 1952-1958, May, 2020.

[C] J. Bremer, J. Bergsten, L. Hanning, T. Nilsson, N. Rorsman, S. Gustafsson A. M. Eriksson, and M. Thorsell, "Analysis of Lateral Thermal Coupling for GaN MMIC Technologies," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 10, pp. 4430-4438, October, 2018.

[D] J. Bremer, L. Hanning, N. Rorsman, and M. Thorsell, "Compensation of Performance Degradation Due to Thermal Effects in GaN LNA Using Dynamic Bias," *48th European Microwave Conference*, Madrid, Spain, Sept., 2018.

[E] J. Bremer, B. Hult, N. Rorsman, and M. Thorsell, "Static and Dynamic Breakdown Characteristics of Microwave GaN HEMTs," *to be submitted to IEEE Transactions on Electron Devices*, 2025.

Other Publications

The content of the following papers partially overlaps with the appended papers or is out of the scope of this thesis.

[a] L. Hanning, J. Bremer, M. Ström, N. Billström, T. Eriksson, and M. Thorsell, "Optimizing the Signal-to-Noise and Distortion Ratio of a GaN LNA using Dynamic Bias," *91st ARFTG Microwave Measurement Conference*, Philadelphia, PA, USA, June, 2018.

[b] T. Kristensen, T. M. J. Nilsson, A. Divinyi, J. Bremer, and M. Thorsell, "Numerical Modeling of Dynamic Thermal Coupling in GaN HEMTs Calibrated by Transient Measurements," *IEEE Transactions on Electron Devices*, vol. 71, no. 12, pp. 7343-7349, Dec. 2024.

[c] T. Kristensen, T. M. J. Nilsson, A. Divinyi, J. Bremer and M. Thorsell, "Dynamic Thermal Coupling in GaN MMIC Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 1, pp. 38-44, Jan. 2025.

Abbreviations & Notations

AlGaN	Aluminium gallium nitride
AlN	Aluminium nitride
BV	Breakdown voltage
CTE	Coefficient of thermal expansion
DUT	Device under test
FET	Field-effect transistor
GaN	Gallium nitride
GaAs	Gallium arsenide
GRT	Gate resistance thermometry
HEMT	High electron mobility transistor
LNA	Low noise amplifier
MTTF	Mean time-to-failure
MMIC	Monolithic microwave integrated circuit
NF	Noise figure
OIP3	Output third order intercept point
P1dB	1 dB compression point
RF	Radio frequency
SiC	Silicon Carbide
SMU	Source measurement unit
TIM	Thermal interface material
TBR	Thermal boundary resistance
TR	Thermoreflectance
TCAD	Technology computer-aided design
TB	Thin buffer
2DEG	Two-dimensional electron gas
BV_{ds}	Drain-source breakdown voltage
α	Thermal coefficient
L	Contact separation
W	Device width
μ	Electron mobility
C_{th}	Thermal capacitance
E	Electric field
G_{ii}	Carrier generation rate due to impact ionization
I	Current
I_{d}	Drain current
I_{g}	Gate current
I_{s}	Source current

I_{ds}	Drain-source current
$I_{\mathrm{ds,max}}$	Maximum drain-source current
n_{s}	Electron density
P	Power dissipation
R_{on}	On-resistance
R_{th}	Thermal resistance
R	Differential resistance
R_{in}	Differential input resistance
R_{pd}	Drain protection resistor
T_{ck}	Thermal chuck temperature
T_{c}	Average channel temperature
t_{d}	Propagation delay
t_{dm}	Measurement delay time
V	Voltage
V_{gs}	Gate-source voltage
V_{ds}	Drain-source voltage
$V_{\mathrm{ds,max}}$	Maximum drain-source voltage
$V_{\mathrm{gs,max}}$	Maximum gate-source voltage
$V_{\mathrm{gs,min}}$	Minimum gate-source voltage
V_{d}	Drain voltage
V_{po}	Pinch-off voltage
V_{dg}	Drain-gate voltage
V_{knee}	Knee voltage
$Y_{\mathrm{in}}^{\mathrm{e}}$	Extrinsic input admittance
$Y_{\mathrm{in}}^{\mathrm{i}}$	Intrinsic input admittance
Z_{th}	Thermal impedance
Z_{in}	Input impedance

Contents

Chapter 1

Introduction

Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) is a transistor technology that possesses many of the intrinsic properties necessary to fabricate high-performance electronic circuits at a broad range of frequencies. As a result, GaN technology is today increasingly used in industry sectors such as defense, aerospace, telecom infrastructure, and power electronics, to meet the increasing performance demands on the applications in these sectors.

Power electronic applications such as switching converters need to be efficient, have high power handling capability, and must be manufacturable at a low cost. Applications such as power supplies also need to be able to operate safely over a long period of time. A high switching frequency enables the use of smaller transformers and filter components, which reduces the size, weight, and cost of converters. However, a higher switching frequency increases the switching losses and transistors with high switching speeds are therefore attractive. In addition, the transistor needs a high breakdown voltage and low on-resistance to meet the requirements on efficiency and voltage conversion.

In wireless communication systems, the demands on capacity, data rate, latency, and reduced power consumption are constantly increasing. To achieve multi-gigabit per second speeds and ultra-low latency, mobile operators must improve the performance of the systems through investments in spectrum acquisitioning, network infrastructure, and transmission technologies. The system performance is largely determined by the equivalent isotropic radiated power (EIRP) of base stations. A higher EIRP needs to be achieved without increasing the non-radiated power, which put high demands on the semiconductor technologies used for the power amplifiers in the transmitters. In 5G systems, multiple-input multiple-output (MIMO) technology is used to increase performance and capacity, and the size of the MIMO antenna arrays strongly influences the cost for base stations. To further increase the system capacity, a higher bandwidth is needed, which makes it necessary to design the systems at higher mm-wave frequencies. Advanced 5G systems are designed to operate at frequencies up to 86 GHz and future systems, including backhaul infrastructure, will possibly operate in the sub-THz region [1, 2].

In the defense sector, systems often require highly reliable and rugged components with RF output power levels in the order of kilowatts. The complex communication environment requires complex modulation schemes and

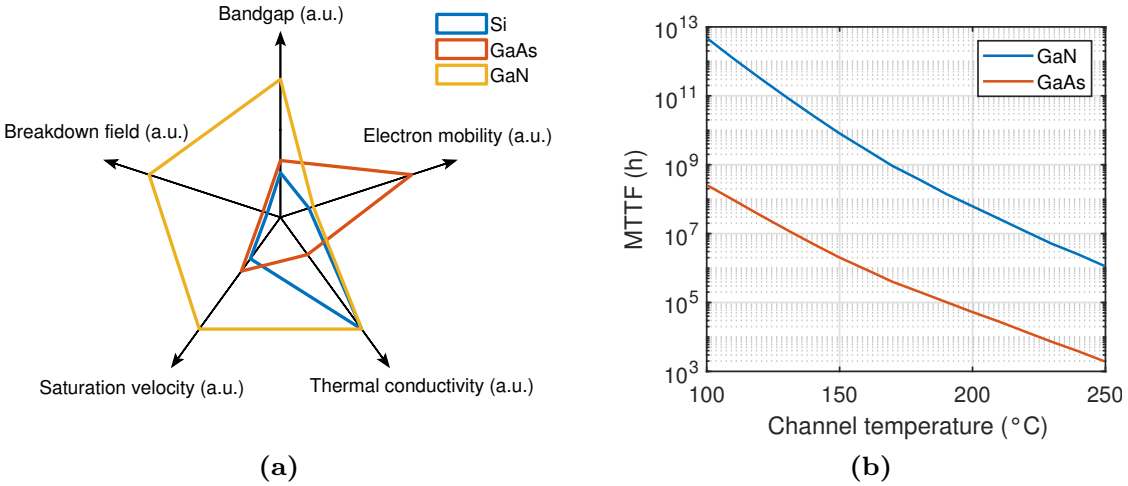
transmissions occur over multiple channels over a wide spectrum, creating a need for wideband components. Several applications migrate away from traveling wave tube amplifiers to solid-state power amplifiers due to the advantages in voltage power supply requirements, noise figures, energy costs, availability, and instant-on capability. In radars, actively electronically scanned array (AESA) architectures are increasingly used as an alternative to more traditional mechanical-based systems. AESA systems require high power, small form factors, and need to be able to operate reliably at high temperatures. The requirements on size, weight, power, and cost are high in air and space-based systems, where the space and load capacity is limited. Receivers need high sensitivity, to detect weak signals but must also be robust to withstand large input signals without losing any sense/detection capabilities. The RF output power needs to be maximized to increase the range as well as to improve the capability to detect objects with small electric signatures. The requirements are similar for electronic warfare systems such as radar warners and jammer systems, which must be functional in harsh electromagnetic environments, as well as be small and light to be portable and integrable. Satellite communication systems share many of the requirements of defense applications. In these systems, demands for smaller satellites, portables, and mobile satcom devices drives the need for more compact, lightweight components with lower power consumption. Furthermore, high output power and wide bandwidth is needed to transmit large amounts of data over the long distances associated with satellite communication.

For any industry application, high reliability is desirable since it translates to a long application lifetime and the ability of the application to function at elevated temperatures for shorter times. All applications therefore strive for semiconductors with higher reliability, better heat removal, and higher efficiency, which reduces the temperature as well as the cost for operating the application. To meet the challenges in the different industry sectors, microwave and power electronics continuously need to be developed. In this context, the beneficial intrinsic properties of GaN HEMTs can be utilized.

Implications of Intrinsic GaN HEMT Properties

The advantages of GaN HEMTs stem from the large bandgap of GaN (3.4 eV) as well as the ability of GaN to form heterostructures with high electron mobility ($> 2000\,\mathrm{cm^2/Vs}$), large electron sheet density ($> 1 \times 10^{13}\,\mathrm{cm^2}$), and high electron velocity ($2 \times 10^7\,\mathrm{cm/s}$). A comparison of transistor material properties is shown in Fig. 1.1a, where the area of the polygon is a measure of the performance of the technology. The area of GaN is significantly larger than e.g. Si, meaning GaN can be used to fabricate circuits with higher performance.

The large bandgap enables a high breakdown voltage, which makes it possible to fabricate devices that can operate at high voltages. This increases the device robustness, enables large voltage handling, and increases circuit efficiency since the current in conductors can be reduced. In addition, the high electron mobility and large sheet density enable a high current density and a low on-resistance. As a result, GaN devices are attractive for power electronics since the devices can achieve low on-resistance ($< 4.5\,\mathrm{m\Omega cm^2}$) for breakdown voltages up to 2 kV [3].



(a) **(b)**

Figure 1.1: (a): comparison of device material properties. **(b)**: typical MTTF versus channel temperature for GaN and GaAs-based devices.

The high current density and primarily the large bandgap make it possible for GaN devices to output high power densities. As a result, the devices and circuits can be made smaller. The array-size in wireless base stations as well as the form factor in defense and other commercial applications can therefore be reduced to save cost and weight. A higher power density also enables smaller losses in power combining circuits since more compact networks can be used due to the need of fewer and smaller devices. Furthermore, the power density enables more flexibility to control the port impedances of the device, which enables the design of matching networks with lower loss. Reduced losses lead to a higher efficiency, reliability, gain, and power for GaN-based circuits.

An additional benefit of high power density is the possibility to reduce the parasitic capacitances of the HEMTs since the capacitances scale with the size of the device. The parasitic capacitances degrade the high-frequency performance of the device and GaN-based HEMTs therefore exhibit less degradation at higher frequencies. Furthermore, the high electron velocity of GaN HEMTs is a key factor that enables high frequency performance, and f_{T} and f_{max} values over 400 GHz have been demonstrated [4]. As a result, GaN HEMT can output high power density (3 W/mm) at operating frequencies up to 100 GHz [5]. This enables the design of microwave circuits with larger bandwidth that can be used to design wideband radars and communication systems with higher capacity. The high frequency also translates to fast switching speeds, which can be utilized for power electronic applications.

The reliability of GaN transistors rank among the highest of all semiconductors, and the mean time-to-failure (MTTF) is several orders of magnitude higher than e.g. GaAs, as shown in Fig. 1.1b. As a result, GaN HEMTs are able to operate at higher device temperatures, which means that several times higher voltages and currents are supported. Since the higher power density of GaN HEMTs naturally leads to higher device temperatures, the higher temperature tolerance is a key feature that enables the performance of GaN HEMTs.

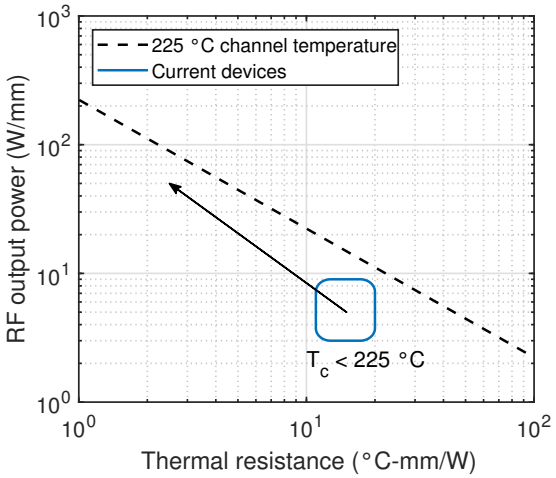


Figure 1.2: RF output power versus thermal resistance for a fixed channel temperature. The rectangle indicates the output power and thermal resistance of currently available devices.

Thermal Limitations

To be able to continue to meet the increasing industry demands, efforts are made to further improve the performance of GaN HEMTs, whose full potential is still far from realized. GaN technology therefore remains an active research area, where the focus is on increasing power density, efficiency, and linearity through progress in both material science and device design. The power density is a key enabling factor for many applications, and the current power density of GaN HEMTs is significantly lower than predicted theoretical limits as well as power levels that have been demonstrated with short pulses on small devices (40 W/mm) [6]. In practice, such power levels cannot be realized in sustained operation today due to the excessive waste heat that would be generated in the device. The waste heat is a result of the DC-to-RF conversion efficiency which is less than unity. The dissipated power elevates the channel temperature, resulting in rapid transistor performance and lifetime degradation, as shown in Fig. 1.1b. The channel temperature increases with increasing power density, and a typical requirement for commercial devices is a lifetime of at least 10^6 hours, meaning the channel temperature cannot exceed approximately 225 °C. As a result, commercial monolithic microwave integrated circuit (MMIC) technologies are limited to power densities between 5 and 10 W/mm [7]. Attempting to operate the devices at 40 W/mm under real-world waveforms conditions, would result in unacceptably high channel temperature, which would lead to a lifetime reduction of five orders of magnitude [8]. The power density of GaN HEMTs today is therefore thermally limited to levels approximately ten times lower than what is known to be attainable. To increase the output power while maintaining a sustainable channel temperature, the thermal resistance must be reduced. Fig. 1.2 shows the power density as a function of thermal resistance at 225 °C. The approximate power levels and thermal resistance of current GaN devices is indicated by the rectangle. The arrow shows that in order to increase the power density ten times with a temperature below 225 °C, the thermal resistance must be reduced by approximately a factor eight. Efforts are therefore made to reduce the thermal resistance by the implementation and improvement of remote and integrated cooling techniques.

Thesis Motivation and Outline

In the development of new semiconductor devices, measurement methodology is crucial since measurement results is the basis on which conclusions about material and device designs are drawn. The work to increase e.g. the power density involves efforts to increase the current density and breakdown voltage coupled with efforts to lower the thermal resistance and increase the efficiency. In the work to achieve this, modifications to the device design are made and key measurements are used to assess the alterations in regard to the thermal and electrical properties of the device. It is thus imperative that the measurement methods are capable of providing accurate and extensive characteristics. However, new semiconductor technologies create new measurement-challenges, and methods must therefore continuously be developed and adapted. The characterization of GaN-based devices is associated with a number of challenges that can make performance evaluations complicated. Key challenges and needs related to measurements can be summarized as follows. (i) Electron trapping create electrical memory effects that can distort rudimentary IV characteristics and electric-based thermal characteristics. Trapping effects and thermal effects are coupled and their interdependencies make it difficult to separately observe properties such as self-heating effects. (ii) Due to the limitations of optical-based thermal measurements, there are few techniques to reliably measure the lateral thermal coupling in GaN circuits. Furthermore, electric-based techniques are needed to evaluate solutions to disperse the heat in fully enclosed circuits, and the need to assess thermal coupling increases as the size of circuits decreases at higher frequencies. (iii) The power density is limited by the breakdown voltage, which is normally determined using DC measurements. However, the DC breakdown voltage does not necessarily represent the actual voltage limitation of the device during large-signal operation, where the maximum voltage is only applied for a short time. Furthermore, GaN devices inherently lacks the ability to be driven in the breakdown region [9], which makes it challenging to compare different breakdown results.

This thesis presents techniques for improved thermal and electrical characterization of GaN HEMTs. The methods have been developed to capture complex characteristics and to mitigate distortion due to trapping effects, which facilitates the evaluation of new GaN devices. Chapter 2 covers fundamentals aspects of GaN devices and briefly describes the device structure, functionality, and its inherent dispersive properties. Chapter 3 is dedicated to electrical characterization under trap-dispersive conditions, and methods are introduced to obtain distortion-free IV and thermal characteristics in the presence of trapping effects. In chapter 4, a method to characterize the lateral thermal coupling is presented as well as a biasing technique for GaN MMICs, which compensates for the RF performance loss due to thermal effects. In chapter 5, the static breakdown characteristics of GaN HEMTs are studied and methods to perform dynamic breakdown measurements are outlined. The different breakdown characteristics are subsequently compared and the influence of the buffer thickness on the breakdown measurement is examined.

Chapter 2

Key Aspects of GaN HEMT Technology

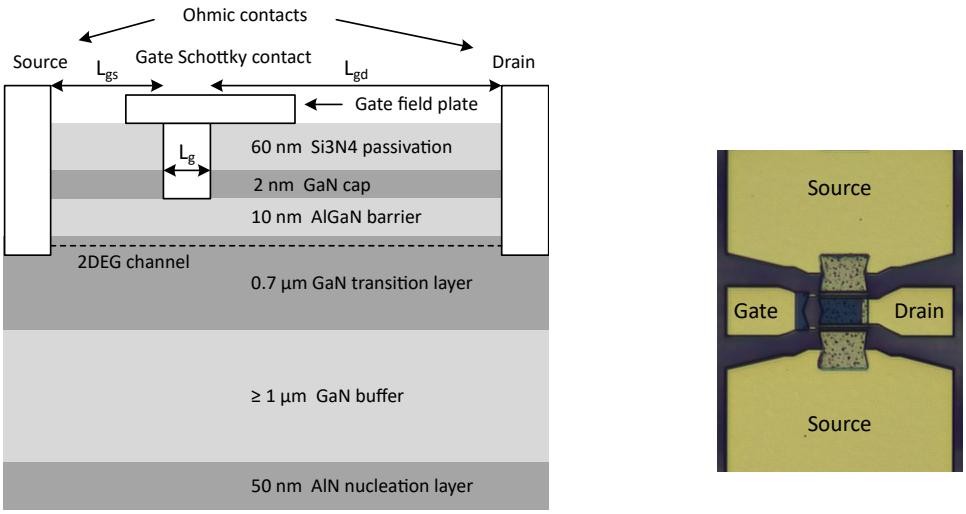
The purpose of this chapter is to briefly describe key aspects of GaN HEMT technology for RF applications, to make the research discussed in subsequent chapters more comprehensible. A more detailed description of GaN-based devices and their functionality can be found in e.g. [10, 11]. The GaN HEMT is a compound semiconductor technology, which is based on a heterojunction that is formed by the growth of a GaN layer and a III-nitride barrier layer. The first HEMT based on an AlGaN/GaN heterojunction was reported in the 90s [12], and it showed the potential of heterostructures designed with wide bandgap materials. Since then, efforts have been made to fully realize the potential of GaN-based devices.

2.1 Device Structure and Functionality

A schematic cross section of a basic microwave GaN HEMT is shown in Fig. 2.1a (not to scale). The HEMT is created by growing semiconductor materials in a layer structure, and by incorporating metal contacts and dielectrics in a device processing step. The different layers materials and their typical thickness are depicted in Fig. 2.1a. Although all GaN-based devices share a common core structure, the layer arrangement and dimensions are designed differently to enhance different device properties. In this case, the shown dimensions are indicative of the typical size of each layer, and the device features a generic design, which resembles the design of the evaluated devices in this thesis. The different parts of the device serve different purposes to create the desired device functionality. In the following sections, the purpose and challenges for each part are described briefly.

AlGaN Barrier and 2DEG

The GaN buffer and AlGaN barrier form the heterojunction where the channel is created, which enables the core functionality of HEMTs. All III-N materials are polarized due to the difference in electronegativity between the elements in the compounds. The polarization fields point downwards in the structure, and



(a) **(b)**

Figure 2.1: (a): schematic cross section of a basic microwave GaN HEMT. **(b)**: top view of a basic microwave GaN HEMT with coplanar layout.

the fields bend the energy bands, which are formed into a quantum well at the junction. The field strength is higher in the AlGaN compared to GaN, resulting in a net positive polarization charge at the AlGaN/GaN interface. This attracts electrons from donor-like surface states on the the AlGaN surface, which form a two-dimensional electron gas (2DEG) in the well at the AlGaN/GaN junction. To form the 2DEG, a minimal barrier thickness is required and the barrier bandgap needs to be wider than the bandgap of the GaN layer [13]. The electron density (n_s) in the 2DEG depends on the polarization charge and therefore on the barrier Al content. Increasing the thickness and/or the Al concentration in the AlGaN barrier increases n_s. However, the lattice constant of the AlGaN barrier is generally not matched to GaN, and the barrier is therefore subjected to strain, which increases with the Al mole fraction. The strain increases the probability of dislocations and partial relaxation, which reduces the reliability of the device. This limits the maximum Al content in the AlGaN layer to values ranging from 15 to 30 %, and the thickness is normally around 10 nm.

In HEMTs, the carrier electrons are spatially separated from the donor atoms. This reduces the electron scattering due to collisions between particles, which translates to a higher carrier mobility for HEMTs compared to other types of FETs. Furthermore, in contrast to HEMTs based on GaAs, GaN HEMTs do not require n-doping in the barrier for the 2DEG to be created.

Surface Layers and GaN Buffer

A thin GaN cap layer around 2 nm is normally included on top of the barrier layer to protect the surface of the barrier from oxidization during fabrication. Since the electrons in the 2DEG originates from the barrier surface, it is sensitive to changes in the surface potential. The GaN cap layer can therefore slightly impact the maximum drain current as well as the gate leakage. To reduce channel modulations via the surface potential, a surface passivation layer is deposited to passivate the trap states. The most used and studied

passivation layer for GaN HEMTs is silicon nitride, SiN_x [14, 15].

The main purpose of the GaN buffer layer is to decrease the number of defects in the channel region and provide a flat surface where the barrier layer can be grown. Therefore, the GaN buffer normally needs to be more than 1 µm. To mitigate short channel effects, the buffer should be designed to have high electric isolation as well as to confine the electrons to the channel. Several buffer design topologies can be used for this purpose, including transition layers with different doping profiles and materials. For microwave devices, the buffer is normally iron doped to increase the isolation whereas carbon is normally used for power devices. The main challenge is to introduce design changes without inadvertently impact other performance aspect of the device. Both the carbon and iron reduce current leakage but these elements also introduce acceptor-like trap states, which cause dispersion in the device.

Substrate and Nucleation Layer

The largest part of the device is the substrate underneath the buffer and nucleation layer. The substrate strongly influences the device reliability since it is the main medium through which heat flows away from the channel. The substrate should have high thermal conductivity to cool the device as much as possible, and it should ideally have a matched lattice constant to minimize the induced strain on the buffer. While SiC is the most common substrate for GaN MMIC technologies, GaN, AlN, and diamond are attractive alternatives since e.g. GaN would enable growing buffers with lower dislocation densities. Diamond has superior thermal conductivity but it would introduce a large mismatch in terms of lattice constant and coefficient of thermal expansion. The effective permittivitty is largely set by the substrate properties, which are crucial for the performance at microwave frequencies.

To reduce the lattice mismatch and to promote two-dimensional growth of the GaN buffer, a nucleation layer is generally grown on the substrate, which is lattice matched to the buffer. For SiC substrates, AlN is mostly used, and due to the SiC-AlN lattice mismatch, the crystal quality is inherently low in the nucleation layer. This contributes to that the nucleation layer acts as a thermal barrier [16], which therefore reduces the heat flow from the channel to the substrate.

Ohmic and Schottky Contacts

The source, drain and gate contacts are indicated in Fig. 2.1a. The HEMT uses ohmic and Schottky type contacts to get access to and control the current in the channel. The source and drain should enable efficient injection and extraction of current, and minimal contact resistance to the channel is thus desirable. Ohmic contacts are therefore used, which have low contact resistance and promote a linear current flow between the contact and channel. The purpose of the gate is to control the flow of current between the two ohmic contacts while minimizing current flow through the gate. A Schottky contact is therefore used, which exhibits a non-linear IV characteristic, that allows current to flow predominantly in one direction. This allows for high reverse voltages on the gate, which is necessary to influence the flow of current in the channel. Control of the current in the 2DEG is done with the field effect where a voltage is

applied to the gate terminal, which results in band bending underneath the gate contact. A sufficiently negative voltage raises the the quantum well above the fermi level, which depletes the 2DEG of charge carriers, effectively closing the channel.

Device layout

The layout of the device includes the dimensions and arrangement of the contacts, field plates, and access conductors to the HEMT. The layout strongly influences the device properties and performance, including thermal, frequency, and breakdown characteristics. Scaling down the device is generally necessary to improve the high frequency performance. However, a more compact device often leads to a higher operating temperature, lower breakdown voltage, and larger performance-deteriorating short-channel effects. The parasitics are also affected when the separation between electrodes, as well as geometry of contacts and conductors, are changed. Additionally, a reduction of e.g. L_{gd} lowers the breakdown voltage due to the ensuing higher electric field between the drain and gate. A field plate is normally connected to the source and extended towards the drain to reduce the electric field and therefore increase the breakdown voltage. The device in Fig. 2.1a features a gate field plate, which is a simpler form of field plate that is connected to the gate.

GaN HEMTs normally feature several gate contacts connected in parallel (known as gate fingers), to increase the current and utilize chip area more efficiently. Furthermore, the devices often feature a co-planar design, where the signal and ground conductors are in the same plane, which enhances the RF performance due to reduced parasitics and better characteristic impedance control. Fig. 2.1b shows a coplanar 2x50 µm device intended for tests and development, and the same kind of device was used for the studies in paper [A,E].

To enable the design of complete circuits, and to design test structures used to evaluate HEMT technologies, devices without the gate contact are often required. This type of device is essentially a HEMT with a constantly open channel, and it is refereed to as gateless device/ungated HEMT, GaN resistor or mesa resistor, depending on the method to electrically isolate the device. In paper [B,C], the properties of gateless devices are exploited to investigate lateral heat coupling in GaN MMIC technology and to suppress trap-related distortion in thermal resistance extractions.

Basic Functionality

The basic functionality of HEMTs can be understood by the their basic IV characteristics. Considering only the drift current, which is much larger than the diffusion current in GaN devices, the drain current can be expressed as [10]

$$I_{\mathrm{ds}} = q n_{\mathrm{s}}(x) W v_{\mathrm{d}}(x), \tag{2.1}$$

where q is the electron charge, n_{s} is the charge carrier density in the channel, W is the width of transistor, and $v_{\mathrm{d}}(x)$ is the electron drift velocity at the horizontal position x in the channel. To derive accurate expressions of (2.1) in terms of physical parameters of the device as well as the gate-source voltage

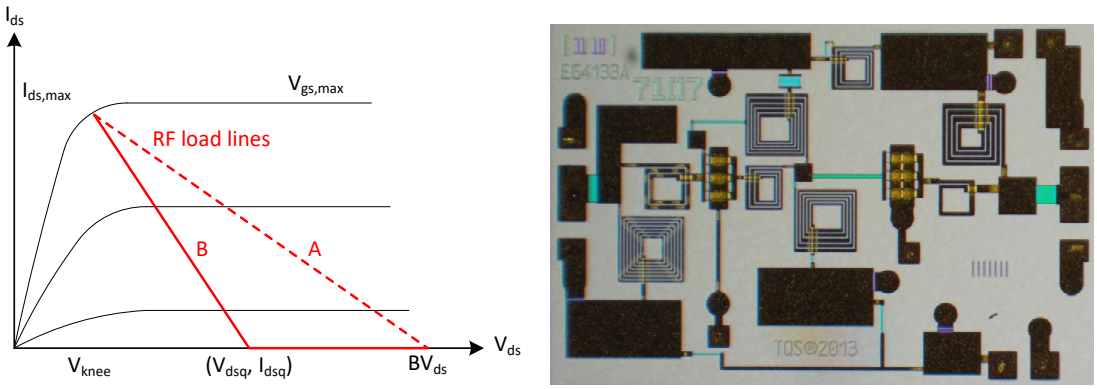


Figure 2.2: **(a)**: GaN HEMT I_{ds}-V_{ds} characteristics. The red lines show RF load lines associated with a class A (dashed) and B (solid) bias. **(b)**: LNA MMIC featuring two GaN HEMTs connected in cascade.

(V_{gs}) and drain-source voltage (V_{ds}) can become complex due to the inclusion of detailed physics of the device. Accurate expressions of $v_{\mathrm{d}}(x)$ and $n_{\mathrm{s}}(x)$ for GaN-based HEMTs are needed, and several publications have been made on this topic [17]. However, by using simplified expressions for $v_{\mathrm{d}}(x)$ and $n_{\mathrm{s}}(x)$, basic functionality can be studied. First, Si-like velocity-field characteristics can be assumed, meaning $v(x) = \mu E(x)/(1 + \mu E(x)/v_{\mathrm{sat}})$, where v_{sat} is the saturation velocity, μ is the electron mobility, and $E(x)$ is the electric field. It can be further assumed that $n_{\mathrm{s}}(x) = \varepsilon_2/(qd)\,[V_{\mathrm{gs}} - V_{\mathrm{off}} - V(x)]$, where ε_2 is the dielectric constant in the AlGaN barrier, d is the barrier thickness, and V_{off} is the threshold voltage under ideal conditions. Inserting these expressions in (2.1), and integrating over the gate length yields the following expression for the drain current:

$$I_{\mathrm{ds}} = \frac{1}{1 + \mu V_{\mathrm{ds}}/v_{\mathrm{sat}} L_{\mathrm{g}}} \left\{ \frac{\mu W}{L_{\mathrm{g}}} \frac{\varepsilon_2}{d} \left[(V_{\mathrm{gs}} - V_{\mathrm{off}}) V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2} \right] \right\}. \tag{2.2}$$

The I_{ds}-V_{ds} characteristics obtained by evaluating (2.2) for different V_{gs} are shown in Fig. 2.2a (solid lines). At low V_{ds} the slope at the maximum gate-source voltage ($V_{\mathrm{gs,max}}$) is high meaning the on-resistance (R_{on}) of the HEMT is small. Conversely, at sufficiently low V_{gs} the output resistance approaches infinity. The red line in Fig. 2.2a shows the current when the HEMT is biased at (V_{dsq}, I_{dsq}), and a large AC signal is applied to the gate. The small gate voltage causes a large current and voltage modulation on the HEMT output, and this signal gain can be used to fabricate amplifier circuits at high frequencies, including MMIC amplifiers. An example of such a circuit is shown in Fig. 2.2b, which shows the MMIC amplifier used for the study in paper [D]. In the circuit, two HEMTs are connected in cascade, and additional circuitry for e.g. biasing surround the HEMTs, which enable the functionality of the amplifier.

In amplifier applications, the current and voltage follow the RF load line (A or B in Fig. 2.2a), and the slope of the line is determined by the impedance of the load connected to the HEMT output. For power amplifiers, the load should be selected to maximize the swing in the characteristics to maximize the output power. Amplifiers are classified by their conduction angle, which indicates the fraction of the signal period during which the transistor conducts.

For a class A amplifier, the HEMT is always on (360 °conduction angle), and this is achieved by biasing the device so the channel conducts throughout the entire cycle. For this class of operation, the maximum output power of the HEMT is given by

$$P_{\max} = \frac{I_{\mathrm{ds,max}}(BV_{\mathrm{ds}} - V_{\mathrm{knee}})}{8}, \tag{2.3}$$

where $I_{\mathrm{ds,max}}$ is the maximum drain current, BV_{ds} is the drain-source breakdown voltage, and V_{knee} is the knee voltage, as indicated in Fig. 2.2a. Although the breakdown can occur at on- or off-state V_{gs}, the off-state breakdown voltage has the most direct effect on the power limits of a device since the maximum voltage for the most commonly used amplifier classes is reached while the HEMT is in a pinch-off condition. The output power can be increased by increasing either $I_{\mathrm{ds,max}}$ or BV_{ds}. Increased $I_{\mathrm{ds,max}}$ decreases the optimal output impedance, and a higher current can be achieved by simply increasing the gate periphery. On the other hand, a high BV_{ds} increases the optimal output impedance, which can be utilized to design for a maximum output power at an output impedance closer to 50 Ω. This enables to design a simpler and more efficient matching network with large bandwidth, which facilitates the design of wide band amplifiers. Thus, increasing $P_{\max}$ by increasing BV_{ds} is advantageous and it is possible due to the large bandgap of GaN.

2.2 Dispersive Effects

There are several physical mechanisms in GaN HEMTs that can cause dispersion, which is broadly defined as undesired variations in electrical characteristics as a function of bias conditions, operating timescales, or signal properties such as frequency. Self-heating and electron trapping are prevalent and create major challenges in the development of GaN HEMTs. In the following sections, self-heating, electron trapping, and the effects of these dispersion sources are briefly discussed.

Self-heating Effects

Self-heating is caused by the conversion of electric power in the device into heat. The dissipated power increases the device temperature, which causes thermal effects such as a reduction of the current. n_{s} in (2.1) is relatively stable versus temperature although a small decrease at higher temperatures has been observed [18]. The primary reason for a reduced current is the reduction in v_{d} due to decreased electron mobility at higher channel temperatures (T_{c}) since generally $v_{\mathrm{d}} = v_{\mathrm{d}}(\mu(E, T_{\mathrm{c}}), E)$. The mobility is determined by different scattering mechanisms, and there are numerous scattering mechanisms occurring in different types of semiconductors. The scattering mechanisms in 2DEG systems are optical and acoustic phonon scattering (lattice vibrations), alloy scattering, remote ionized impurity scattering, residual screened impurity scattering (background or intentionally doped channel impurities), and interface roughness scattering. At temperatures higher than room temperature, polar optical phonon scattering is the dominant mechanism [19, 20], which causes the mobility to decrease significantly with increasing temperature. The temperature increase due to self-heating can be expressed in the frequency

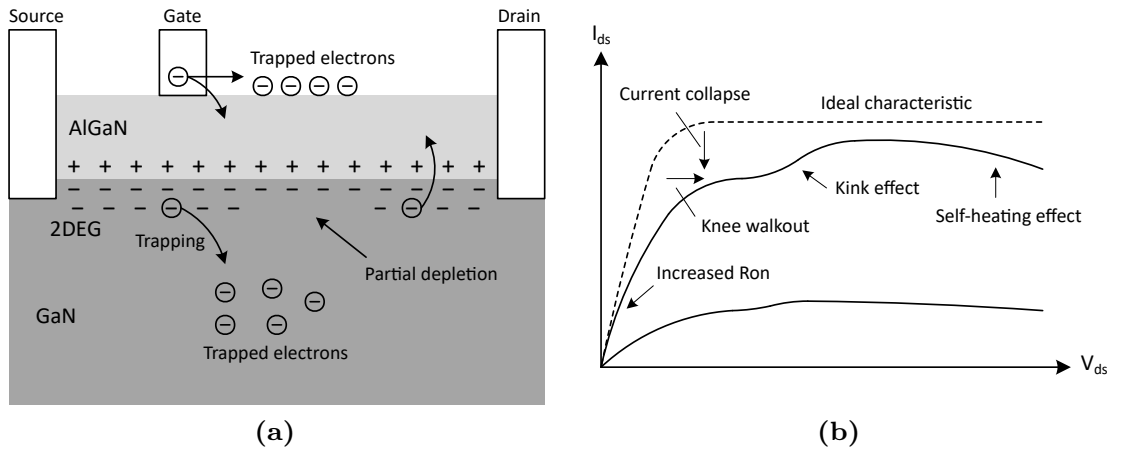


Figure 2.3: (a): illustration of the trapping and build-up of trap charge in a GaN HEMT. **(b)**: illustration of trapping and self-heating effects in the I_{ds}-V_{ds} characteristics of a GaN HEMT.

domain as a function of the power dissipation and the thermal properties of the device according to

$$T_{\mathrm{c}}(\omega) = P(\omega)Z_{\mathrm{th}}(\omega) + T_{\mathrm{a}}, \tag{2.4}$$

where P is the power dissipation and T_{a} is the ambient temperature. $Z_{\mathrm{th}}(\omega)$ is the thermal impedance, which represents the thermal properties of the device. $Z_{\mathrm{th}}(\omega)$ is comprised of a thermal resistance (R_{th}), which quantifies the ability of the device to conduct heat from the channel region to the surrounding environment, and a thermal capacitance (C_{th}), which represents the ability of the device to store heat. The thermal impedance is often modeled as a parallel RC, Foster or Cauer RC network [21]. The latter is used to better approximate the distributed nature of heat transfer through several materials. An implication of these models is that the self-heating is frequency-dependent, and can be constant above a certain frequency and vary according to e.g. the envelope of modulated signals. At low frequency, T_{c} increases with P, causing μ to decrease with P, and the current in the I_{ds}-V_{ds} characteristic therefore decreases at higher power dissipation levels, as shown in Fig. 2.3b. The effects of self-heating generally involve a deterioration of the electric characteristics of the transistor and circuit where the device is used. The noise power increases at higher temperatures, and the reduced current reduces the RF power and the gain. Furthermore, the S-parameters depend on temperature, and the temperature variations can degrade the functionality and effectiveness of circuitry connected to the device.

Electron Trapping Effects

The effects of trapping range from localized charge accumulation to degradation of electrical performance. Trap-states are created by crystal defects in semiconductors, which can be divided into point defects and extended defects. Point defects are places where an atom is missing or is irregularly placed in the lattice and the following types of point defects exist: Foreign substitutional (e.g. dopant atom), foreign interstitial (e.g. oxygen in silicon), self-interstitial,

and vacancy defects. Extended defects include line defects (groups of atoms in irregular position), planar defects (two-dimensional interface defects such as grain boundaries), and volume defects (e.g. regions with several missing atoms). The different crystal defects and associated trap-states are found at various locations in GaN HEMTs. At the surface, trap states are formed due to the termination of the bulk crystal structure. Furthermore, more trap states are present at/around interfaces because of the lattice mismatching, which leads to a higher strain and therefore larger amount of defects at such regions. The effects of trapping are typically caused by the following traps: surface traps, bulk traps in the AlGaN barrier, interface traps at the AlGaN/GaN interface, bulk traps in the GaN buffer, interface traps at the transition from the GaN buffer to the AlN nucleation layer, and traps in the substrate.

The different trap states are characterized by their energy level, capture cross section (probability to capture an electron) as well as their emission and capture and time constants. Deep-level traps have energies far down in the band-gap and therefore exhibit long emission time constants. Most trap time constants are temperature-dependent and can create severe memory effects in GaN HEMTs. In general, the trapping leads to deterioration of the electric characteristics, which reduces and limits the performance of the device in terms of e.g. output power, noise, and efficiency. This can be understood by the illustration of trapping effects in Fig. 2.3. In Fig. 2.3a, it can be observed that electrons from the gate are captured by surface traps, which is equivalent to negatively charging up an imaginary gate (referred to as virtual gate). This partially depletes the channel underneath of electrons and creates a second barrier along the channel, leading to reduced current. When a high V_{ds} is applied, the electrons in the conducting channel are rapidly accelerated, and can gain enough kinetic energy to be injected into an adjacent regions such as the buffer. The electrons can subsequently become trapped in the buffer, as shown in Fig. 2.3a, and the build-up of negative charge in the buffer depletes the channel region, which reduces the current further. The effects of trapping on the I_{ds}-V_{ds} characteristics are shown in Fig. 2.3b. Compared to the ideal IV curve, the non-ideal curve has a higher on-resistance and a collapse of the current in the knee region can be observed. Furthermore, V_{knee} is seen to increase, which directly reduces the power in eq. (2.3). The kink in the curve above the knee is a hysteretic instability of the drain current in FETs, which is caused by trapping effects, although several trap-based explanations for this effect can be found in the literature [11].

Chapter 3

Measurement-Based Mitigation of Trap-Effects

IV measurements are the most fundamental measurements used to evaluate the performance of transistor technologies. The measurements provide basic information of the device including R_{on}, $I_{\mathrm{ds,max}}$, and pinch-off voltage (V_{po}), as well as figures of merits for short-channel effects such as DIBL (drain-induced barrier lowering) and SS (subthreshold swing). Furthermore, the IV characteristics can be used to analyze the thermal properties of the device due to the coupling between the electric power and the device heating. The IV data is also essential for the extraction of a HEMT model, which enables simulations in MMIC design, where the properties predicted by the model are used to design circuitry surrounding the transistor.

To ensure that the IV data can be used for the different purposes as intended, the IV measurements should ideally meet certain requirements. The characterization process and setup fixture should not affect the measurement result. Furthermore, it is desirable to be able to fully control all types of current-affecting factors (such as voltage, temperature, and trapping) in IV measurements since this would enable to evaluate e.g. the effects of self-heating and trapping separately. An example of a temperature-controlled characterization is pulsed IV, where the influence of self-heating on the resulting characteristic is controlled by the pulse timing.

However, trapping effects in GaN devices make it difficult to carry out the ideal characterizations. In general, the IV characteristics are always sensitive to parameters influencing the trapping and de-trapping, including the bias voltage, stimulus timing, and the temperature. Furthermore, the self-heating and trapping effects are interdependent, which further complicates isolating the influence of self-heating in an IV characteristic, making it difficult to perform a thermal analysis. Additionally, the wide range of trap time constants cause IV characteristics to be affected by short- and long-term memory effects. As a result, IV characteristics may vary over time, and all parts of a characteristic depend on measurement settings such as the maximum voltage and the stimulus timing in measurement sweeps. It can therefore be difficult to repeat measurement results, and obtained characteristics may be strongly dependent on specific settings.

In this chapter, the impact of trap-related effects on IV characteristics is demonstrated, and measurement methods to mitigate distortion of IV and electric-based thermal characteristics are introduced. A new method to perform the I_{ds}-V_{ds} characterization is shown, which minimizes the influence of trap-related memory effects on the measurement result. The method yields a rudimentary IV characteristic suitable for the extraction of basic device properties. Additionally, a methodology to extract the thermal resistance of GaN devices using electric measurements is introduced, where trap-related effects are circumvented to prevent distortion of the results. This is useful when the thermal properties of different GaN samples are compared since the distortion due to trapping effects can vary significantly between different technologies.

3.1 Trapping Effects in IV Characteristics

Trapping effects in IV characteristics are commonly studied using pulsed IV measurements, where e.g. deep buffer trapping and surface trapping can be induced by controlling the quiescent bias and the pulse timing. Another method is presented in [22], where dynamic load-lines measured in the MHz range are used to reconstruct the equivalent of pulsed IV curves. In this case, the trapping is controlled by the frequency and the maximum V_{ds} reached in the dynamic voltage swing. The main advantage is that the characterization (and subsequent model extraction) is performed under conditions better resembling the intended transistor operation.

However, even when trapping effects are not deliberately induced, GaN HEMTs are affected by trapping so that the transistor performance depends on signal frequency and recently applied maximum voltages [22]. Trap-related memory effects in IV characteristics can be observed using bi-directional I_{ds} versus V_{ds} sweeps, as demonstrated in paper [A]. The results of three consecutive sweeps with increasing maximum drain-source voltage ($V_{ds,max}$) are shown in Fig. 3.1a, and the visible hysteresis is a distinct manifestation of a memory effect. Although hysteresis can be observed for all three voltage settings, it increases significantly when the maximum voltage in the sweep is increased. It can be further noted that the forward sweep for $V_{ds,max} = 15\,\text{V}$ overlaps with the reverse sweep of $V_{ds,max} = 7\,\text{V}$, showing that the 15 V measurement starts with the memory state left by the previous sweep. Thus, each measurement starts with a different initial memory state in the device, which makes comparisons of the results of different IV measurements on GaN HEMTs complicated.

For sweeps to higher voltages, the trap-related kink effect (chapter 2.2) can often be observed in the I_{ds}-V_{ds} characteristics [23] in addition to other memory effects. The kink anomaly is most visible in characteristics measured with a slow V_{ds} sweep, and it can be seen between 5 and 15 V in Fig. 3.1b, where several I_{ds}-V_{ds} characteristics of a GaN HEMT are shown. From these cases, it can be concluded that the kink effect becomes apparent when $V_{ds,max}$ is increased beyond 15 V. Furthermore, it can be noted that the entire IV characteristic deteriorates with increasing $V_{ds,max}$ predominantly due to the kink effect. For example, $I_{ds,max}$ is seen to be notably lower and V_{knee} is seen to be slightly higher at 30 V compared to $V_{ds,max} = 15\,\text{V}$. It can be further concluded that the shape of the obtained characteristics are bound to the selected $V_{ds,max}$, which

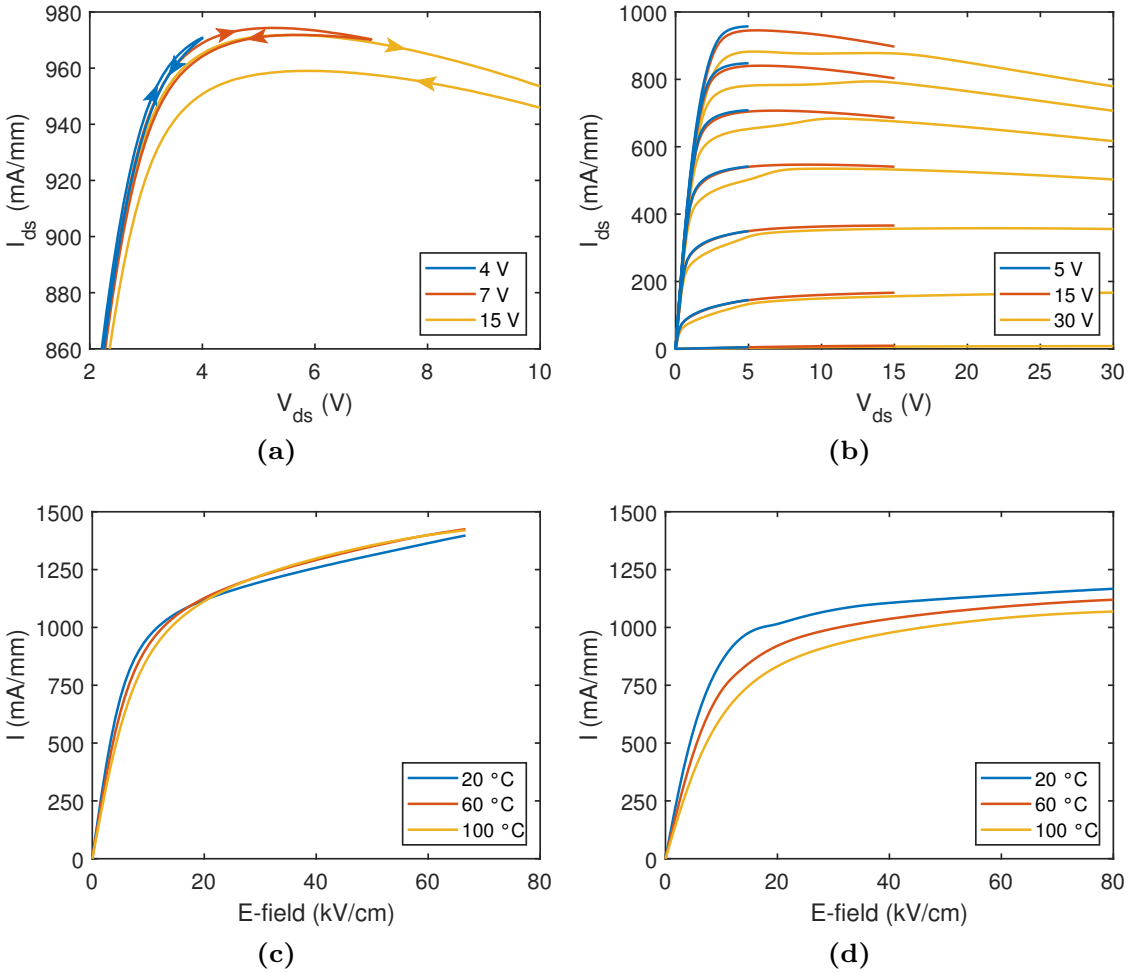


Figure 3.1: **(a)**: consecutive bi-directional IV sweeps, with increasing $V_{\mathrm{ds,max}}$ (4 to 15 V). **(b)**: I_{ds}-V_{ds} characteristics with increasing $V_{\mathrm{ds,max}}$ (5 to 30 V). **(c)**-**(d)**: current versus approximate E-field for two different GaN technologies.

makes it difficult to compare characteristics that have not been measured using the same settings. The extent to which basic properties of the characteristics are influenced by the specific voltage limits is also difficult to assess from a single measurement.

The electrical device properties are temperature dependent, and IV measurements at different ambient temperatures (chuck temperature in this work) is the obvious method to evaluate the thermal behavior of the device. However, the manner and way in which self-heating and trapping affect the current is different; self-heating affects the current due to the temperature dependence in v_{d}, whereas the charging and discharging of traps primarily modulate the current via n_{s}. The trapping and de-trapping of electrons strongly depends on the electric field [24], but the de-trapping is also heavily influenced by the temperature, which depends on the dissipated power. Hence, the self-heating and trapping effects are interdependent. Furthermore, these effects can affect the current in the opposite direction, which can be understood at e.g. higher temperatures, where v_{d} is decreased while increased de-trapping can cause n_{s} to increase. This is demonstrated in Fig. 3.1c & Fig. 3.1d, where the current (I) versus the approximated homogeneous electric field (E-field) of gateless devices is shown at three different chuck temperatures (T_{ck}). The figures show IV

characteristics of two different GaN HEMT technologies, and it can be seen in Fig. 3.1c that the current is first decreasing with temperature up to 15 kV/cm, after which the current temperature coefficient (dI/dT_{ck}) is inverted due to de-trapping effects. In contrast, the characteristics of the other GaN technology in Fig. 3.1d exhibits a negative temperature coefficient up to 70 kV/cm, indicating less trapping and de-trapping effects. Clearly, the sole impact of self-heating cannot be observed, and device comparisons are complicated because the extent to which trapping effects hide self-heating effects varies between technologies.

3.2 Trap-Effects Suppression in IV Measurements

Normally, an IV characterization of field-effect transistors is performed by sweeping V_{ds} and V_{gs} according to the settings selected by the operator. For an I_{ds}-V_{ds} characterization, V_{ds} is usually swept from a low-to-high value while V_{gs} is kept constant. The V_{ds} sweep is then repeated at a different V_{gs}, which is either increasing or decreasing. The characteristics obtained using this methodology (Fig. 3.1b, increasing V_{gs}), are evidently heavily dependent on the maximum V_{ds}, and deteriorate with increasing $V_{\mathrm{ds,max}}$. The deterioration is caused by the trapping effects, which are primarily induced and exacerbated by high electric fields. Thus, to avoid the deterioration of the characteristic, the bias points at high V_{ds} should be measured at the end of the sweep, and the peak electric field at preceding measurement points should ideally be lower or equal. To achieve this, a method is needed to quantify the strength of electric field as a function of bias. For this purpose, the drain-gate voltage (V_{dg}) can be used since the peak drain-gate electric field and extension of the field into the buffer increases when V_{ds} increases and/or V_{gs} decreases [25, 26]. This relationship is utilized in paper [A] to rearrange the gate and drain bias points so that the peak drain-gate E-field is predominantly increasing throughout the measurement. The ordering of the bias points is performed by first calculating V_{dg} using the voltage sweep settings, and subsequently sorting the bias points so that V_{dg} strictly increases. An example for the I_{ds}-V_{ds} characterization is presented in Fig. 3.2a, where V_{dg} for the standard methods (increasing and decreasing V_{gs}) as well as for the proposed method are shown. Clearly, V_{dg} repeatably changes from a low to a high value in a sawtooth shape for the standard methods while it increases monotonically in the case of the proposed method.

In paper [A], the methodology was evaluated on two commercially available AlGaN/GaN-on-SiC HEMT technologies. Examples of the I_{ds}-V_{ds} characteristics obtained using the proposed method and the standard methods are presented in Fig. 3.2b, where a lower knee current and the kink effect can be seen in the characteristics resulting from the standard methods. At $V_{\mathrm{gs,max}}$, the increasing V_{gs} characteristic shows the largest deterioration due to the preceding sweeps starting at $V_{\mathrm{gs,min}}$. On the contrary, the decreasing V_{gs} characteristic shows the smallest deterioration at $V_{\mathrm{gs,max}}$ since it is the first V_{gs} that is measured in this case. The IV characteristics of the proposed method show no obvious kink effect/trap-related deterioration.

The impact of trapping and de-trapping on the IV characteristics depends

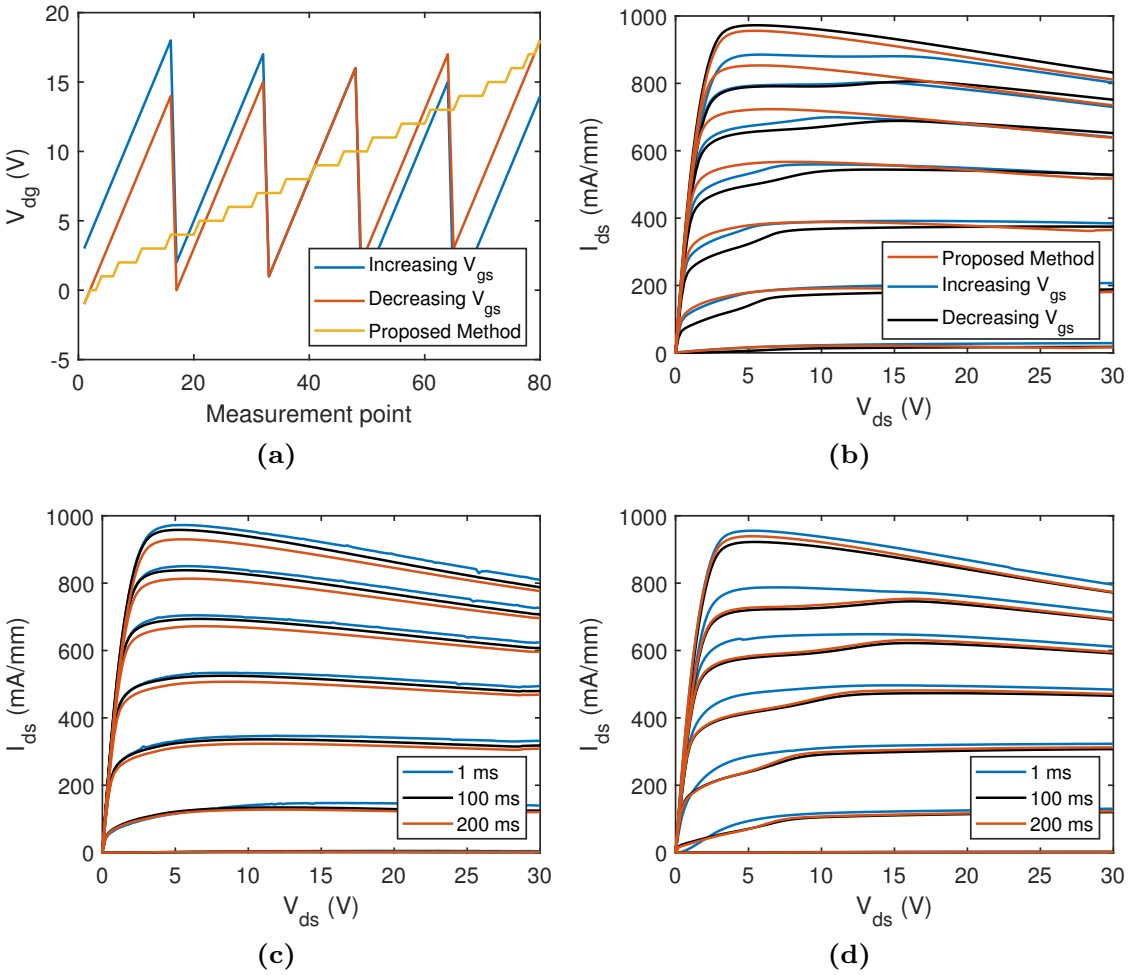


Figure 3.2

Figure 3.3: **(a)**: drain-gate voltages in different I_{ds}-V_{ds} characterizations. **(b)**: I_{ds}-V_{ds} characteristics measured with the proposed method, increasing V_{gs} method, and decreasing V_{gs} method. **(c)-(d)**: I_{ds}-V_{ds} characteristics obtained using different measurement delay times. **(c)** shows characteristics obtained using the proposed method and **(d)** shows characteristics obtained using the decreasing V_{gs} method.

on the timing of the measurement due to the time constants associated with the trap states. Thus, trap-related effects in IV characteristics can be investigated by varying the time settings of the source measurement unit (SMU). In paper A, the sensitivity of the characteristics to the timing was investigated by varying the delay time (t_{md}) between the output of the bias and the measurement start at each bias point. The results for the proposed method and the standard method (decreasing V_{gs}) are shown in shown in Fig. 3.2c and Fig. 3.2d, respectively. Evidently, the characteristics obtained using the proposed method show a smaller dependence on t_{md} compared to the standard method, indicating a smaller influence of traps. It can be further noted that a fast sweep with the standard method yields a characteristic seemingly devoid of trapping effects, partly because a possible kink is spread out over a larger voltage range.

Due to the self-heating, a current reduction, which increases with increasing t_{md} and/or V_{gs} is expected. This can be seen in the results of the proposed method (Fig. 3.2c) but not consistently in the case of the standard method. This suggests that the proposed method provides more accurate information

regarding the impact and time dependence of the self-heating in the HEMT. It can be further concluded that the proposed method yields an IV characteristic that is more independent of the time settings of the measurement.

3.3 Reliable Thermal Resistance Extraction

Thermal characterization techniques that rely on electric measurements exploit the self-heating in the device to determine key thermal properties such as the thermal resistance. These techniques (section 4.1) assume that the temperature behavior of the current is set by self-heating, which makes the validity of this assumption crucial to obtain accurate results. However, for many GaN-based devices, it is evident (section 3.1) that this assumption is not always true due to the charging and discharging of traps. As a result, the thermal analysis can yield inaccurate results that can be misleading. Furthermore, since technologies are affected by trapping to a varying extent, it is difficult to compare the results of the thermal analysis due to the variation of the accuracy.

The self-heating must be enhanced and trapping effects must be suppressed to enable an accurate thermal analysis. Thus, n_s should ideally be stable and independent of the lateral E-field and T_c. The trap-related current modulation increases when the peak E-field increases, and the obvious way to reduce the E-field is to reduce the applied voltage. However, a reduction of the voltage also decreases the dissipated power, leading to decreased self-heating. Another way to reduce the electric field is to increase the contact separation. To understand the relationship between the different parameters, the power dissipation in a gateless device (section 2.1) at low voltages can be examined, which is given by the following expression:

$$P = qn_\mathrm{s}\mu W\frac{V^2}{L}, \tag{3.1}$$

where V is the voltage and L is the contact separation, and W is the device width. In this case the E-field can be approximated as V/L. Thus, (3.1) implies that to keep P as high as possible, it is better to reduce the E-field by increasing the contact separation ($P \propto 1/L$) instead of decreasing the voltage ($P \propto V^2$) [27]. Obviously, layout requirements such as a minimum L severely limits the kind of device that can be evaluated, which reduces the usefulness of the approach. Furthermore, the desired device type is likely not available on new wafers, and the necessary design can be difficult to determine since it depends on possibly unknown trap characteristics of the technology. A solution to this is to utilize gateless devices in TLM structures, which are ubiquitous in PCM areas and feature an array of devices with different L. Therefore, a device from the TLM structure that meets the thermal measurement requirements is likely available. It should be emphasized that the proposed approach limits the layout of the device to enable a more accurate thermal evaluation, which makes it suitable to use for comparisons of the thermal performance of e.g. different epitaxial designs. The suggested approach was therefore used in paper [B] to compare the thermal resistances of GaN devices featuring different substrate suppliers and buffers thicknesses.

To test the proposed idea, measurements of the power dissipation in gateless devices with different contact separation were performed in paper [B], and the

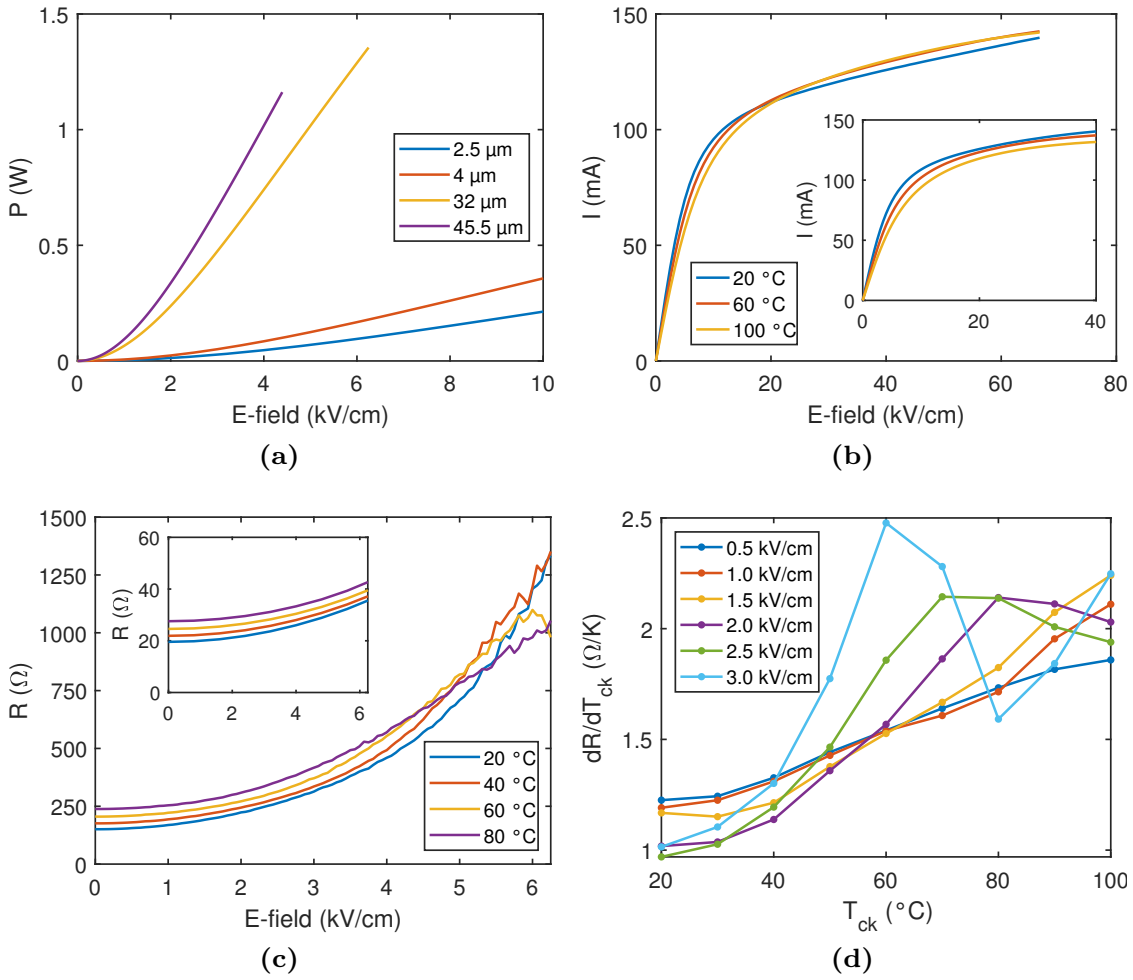


Figure 3.4: **(a)**: power dissipation versus E-field for gateless devices with different contact separation. **(b)**: current versus E-field at different chuck temperatures for a gateless device with 3 µm (main figure) and 5 µm (inset) contact separation. **(c)**: differential resistance versus E-field for a gateless device with 32 µm (main figure) and 2.5 µm (inset) contact separation. **(d)**: temperature derivative of the differential resistance versus chuck temperature at different bias voltages for a gateless device with 32 µm contact separation.

results are shown versus the E-field in Fig. 3.4a. At a given E-field, it can be seen that the power dissipation increases with increasing contact separation, as implied by (3.1), and it can be further noted that the difference in power dissipation between the devices increases with increasing E-field. To examine the effects of a larger L on trap-related effects, the IV characteristics at different T_{ck} can be inspected, which are shown in Fig. 3.4b for devices with $L = 3\,\mu\mathrm{m}$ (main figure) and $5\,\mu\mathrm{m}$ (inset). For this sample, it can be seen that the temperature coefficient at e.g. $40\,\mathrm{kV/cm}$ changes from positive (main figure) to negative (inset), which confirms that the trap-related effects are decreased when L is increased. In paper [B], devices with 30 to 32 µm contact separation were chosen based on the requirements of the thermal analysis and availability of similar devices on multiple engineering samples.

To further analyze the influence of trapping and self-heating in the devices, and to determine the range of bias voltages where the thermal analysis can be performed, the differential resistance ($R = dV/dI$) obtained from the IV measurements was utilized in paper [B]. Increased channel temperature is

expected to increase R, which therefore can be used to quantify the self-heating in different devices. Fig 3.4c shows R for a device with $L = 32\,\mu m$ (main figure) and $2.5\,\mu m$ (inset), and it can be seen at e.g. $4\,kV/cm$ that R has increased approximately a factor 3.1 for the $32\,\mu m$ device compared to a factor 1.3 for the $2.5\,\mu m$ device (inset). This strongly suggest the self-heating is significantly higher in the device with a longer contact separation.

Conversely, a decreasing or unchanged R at higher temperatures is an indication of electron trapping [28], which can be used to identify the maximum bias voltage suitable for thermal analysis. The $32\,\mu m$ device exhibits a positive temperature coefficient up to approximately $4.5\,kV/cm$ (Fig. 3.4c), suggesting self-heating is dominating up to this field level. However, trapping still affect R below $4.5\,kV/cm$, which can be seen by examining the temperature derivative dR/dT_{ck} in Fig. 3.4d. Although dR/dT_{ck} remains positive up to $3\,kV/cm$, a decrease is seen at higher temperatures, which is attributed to de-trapping, and the decrease occurs at lower T_{ck} for higher field levels. Thus, at e.g. $70\,°C$, the thermal analysis of this device should be performed up to approximately 8 V ($2.5\,kV/cm$), and a slightly higher voltage can be used at lower chuck temperatures. The subsequent step is to extract the thermal resistance at the selected bias voltages, and there are several electrical methods available for this purpose (section 4.1). In paper [B], R_{th} was extracted using the electrical method presented in [29]. The main advantage with this method is that the extraction is made at a single independent bias condition, which can be used to inspect R_{th} versus bias voltage, gain insight of the of the extraction, and limit the extraction to the valid bias voltage range. A detailed description of the extraction of R_{th} for N-port devices is provided in [29]. In this section, a qualitative derivation is presented for the case of a gateless device (1-port). To obtain the thermal resistance, the coupled electrothermal system needs to be solved, which consists of the following equations.

$$0 = f\left(i(t), v(t), T_{\mathrm{c}}(t)\right) \tag{3.2}$$

$$p(t) = i(t)v(t) \tag{3.3}$$

$$T_{\mathrm{c}}(t) = p(t) * h_{\mathrm{th}}(t) + T_{\mathrm{ck}}, \tag{3.4}$$

where f is the electric function of the device that describes the port voltage ($v(t)$) and current ($i(t)$). The function is dependent on the device temperature (T_c), which can be determined with the linear thermal system model (3.4), where the temperature is set by the instantaneous power dissipation ($p(t)$), thermal impulse response ($h_{\mathrm{th}}(t)$), and chuck temperature (T_{ck}). In [29], the electrothermal system is analyzed using a small signal approximation around an equilibrium state. This allows to derive expressions of the admittance parameters of the device as a function of the thermal transfer function and thermal (current) coefficient. In this case, the input admittance can be shown to be

$$Y_{\mathrm{in}}^{\mathrm{e}} = \frac{Y_{\mathrm{in}}^{\mathrm{i}} + Z_{\mathrm{th}}(\omega) I_{\mathrm{q}} \alpha}{1 - Z_{\mathrm{th}}(\omega) V_{\mathrm{q}} \alpha}, \tag{3.5}$$

where $Z_{\mathrm{th}}(\omega)$, is the thermal impedance α is the thermal coefficient, V_{q} is the bias voltage, and I_{q} is the bias current. $Y_{\mathrm{in}}^{\mathrm{e}}$ and $Y_{\mathrm{in}}^{\mathrm{i}}$ are the device input admittance with and without the influence of self-heating, respectively. For

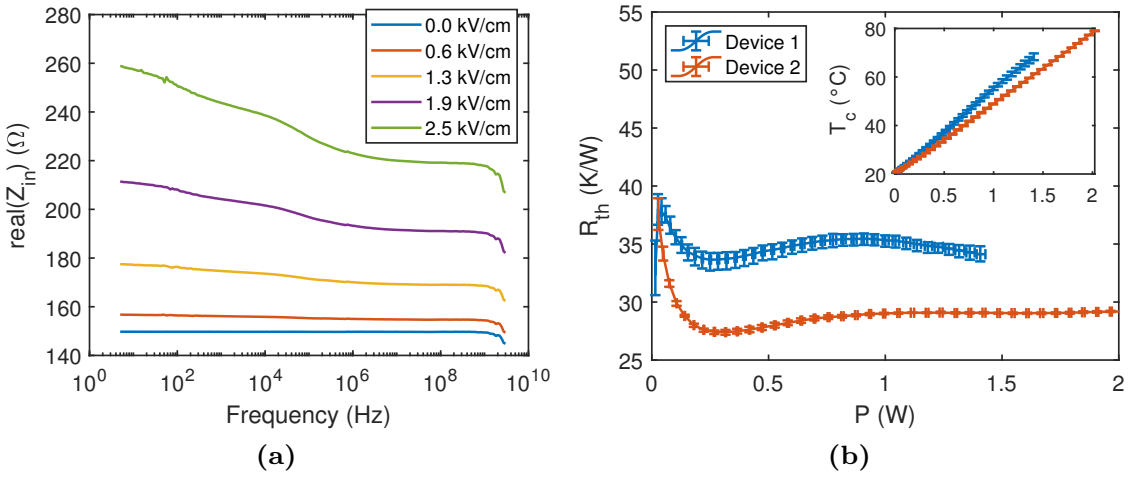


Figure 3.5: **(a)**: real part of the input impedance versus frequency at 0 to 8 V for a gateless device with 32 µm contact separation. **(b)**: thermal resistance versus power dissipation for two different GaN technologies. The inset shows the average channel temperature.

static voltages and currents, the thermal coefficient can be shown to be

$$\alpha = \frac{dI/dT_{\mathrm{ck}}}{R_{\mathrm{th}} V_{\mathrm{q}} dI/dT_{\mathrm{ck}} + 1}, \tag{3.6}$$

where dI/dT_{ck} is the current derivative with respect to ambient temperature (chuck temperature). Equation (3.5) and (3.6) can be solved for R_{th} at static signal conditions where $Z_{\mathrm{th}}(0) = R_{\mathrm{th}}$. The resulting expression for the thermal resistance is

$$R_{\mathrm{th}} = \frac{Y_{\mathrm{in}}^{\mathrm{e}} - Y_{\mathrm{in}}^{\mathrm{i}}}{dI/dT_{\mathrm{ck}}(I_{\mathrm{q}} + V_{\mathrm{q}} Y_{\mathrm{in}}^{\mathrm{i}})}. \tag{3.7}$$

As expected, the expression shows that the thermal resistance is zero when no self-heating occurs ($Y_{\mathrm{in}}^{\mathrm{e}} = Y_{\mathrm{in}}^{\mathrm{i}}$). It can be further noted that a positive dI/dT_{ck} would lead to a negative R_{th} (since $Y_{\mathrm{in}}^{\mathrm{e}} < Y_{\mathrm{in}}^{\mathrm{i}}$), showing how the effects of trapping can cause erroneous results. $Y_{\mathrm{in}}^{\mathrm{e}}$ can be obtained from DC measurements since $Y_{\mathrm{in}}^{\mathrm{e}} = dI(V_{\mathrm{q}})/dV$, and the derivative dI/dT_{ck} is obtained from DC measurements at different chuck temperatures. To reduce the impact of measurement noise, $Y_{\mathrm{in}}^{\mathrm{e}}$ can be estimated using a DC model extracted from the measurement data, as shown in paper [B].

It can be noted in (3.5) that $Y_{\mathrm{in}}^{\mathrm{e}} = Y_{\mathrm{in}}^{\mathrm{i}}$ when $Z_{\mathrm{th}} = 0$ (no self-heating occurs). The thermal impedance generally exhibits a low-pass frequency characteristic, and Z_{th} therefore becomes zero at higher frequencies, usually above 100 MHz. Thus, $Y_{\mathrm{in}}^{\mathrm{i}}$ can be determined using S-parameter measurements above the thermal response. Fig. 3.5a shows the real part of the input impedance (Z_{in}) obtained from S-parameters measurements from 5 Hz to 3 GHz. The self-heating increases the input resistance significantly at low frequencies, and larger impact can be seen at higher bias voltages due to the higher power dissipation. From approximately 100 to 900 MHz, $\mathrm{Re}(Z_{\mathrm{in}})$ is constant, suggesting $Z_{\mathrm{th}}(\omega) = 0$ in this region, which allows to extract $Y_{\mathrm{in}}^{\mathrm{i}}$. The parasitics of the device are small enough to have negligible influence on the measurement result at MHz frequencies. However, at higher frequencies, the parasitics cause Z_{in} to decrease, as seen at 1 to 3 GHz.

Two examples of the thermal resistance obtained by performing the outlined steps are shown in Fig. 3.5b, where R_{th} is shown as a function of the dissipated power. At low P (0 to 0.15 W), the self-heating in the device is small, causing a large uncertainty (large error bars), which results in R_{th} initially decreasing versus P. Above 0.25 W, sufficient self-heating occurs to enable a more accurate extraction, resulting in an approximately constant R_{th} versus P. This is reasonable since the temperature rise (inset Fig. 3.5b) is not high enough to cause significant changes of the thermal properties of the device. It can be noted that the device corresponding to the blue curve exhibits a decreasing R_{th} above 0.9 W, which is attributed to trapping since the corresponding bias points are in the voltage region where trapping effects could be observed in the DC characteristics. A comparison of the thermal resistance of the two devices can be made at e.g. 0.75 W, where trap-related effects on the extraction is negligible for both devices. A thermal evaluation of devices with different buffer and substrate thickness was performed in paper [B], which is discussed in section 4.2.

Chapter 4

Thermal Characterization and Management

Thermal characterization is an integral part in the thermal optimization of GaN circuits and devices. At higher frequencies, the thermal challenges become more difficult due to the miniaturization of MMICs and the need to down-scale devices (to improve high frequency performance). The reduced distances increases the lateral heat coupling between circuits and components, and such thermal properties therefore needs to be accurately measured to enable improved thermal optimization and assessments. However, contemporary thermal evaluation methods are not always suitable for e.g. lateral heat spread characterizations. Optical methods suffer from transparency effects and subsurface reflections causing depth averaging and uncertainty of the measurement location. Furthermore, optical methods require optical access, and more reliable methods such as Raman spectroscopy are narrow view and not practical for measurements over large areas. Thus, there is a lack of methods to characterize heat spread properties under application-relevant conditions, such as when MMICs are packaged.

The combination of high power and a small area for heat removal leads to high operating temperatures, which reduces the lifetime and performance of circuits. Although the lifetime inevitably decreases at higher temperatures, the electric performance loss can be mitigated by controlling other performance-influencing factors such as the bias voltage. However, supply modulation techniques are usually limited to gate bias control, and on-chip performance loss compensation circuits often feature a simpler design that aims to maintain e.g. a constant bias current versus increasing temperature. To counteract the thermal degradation of several RF performance parameters simultaneously, it may not be sufficient to control only the gate bias. Techniques are needed that can predict the thermal behavior of the power, gain, linearity, and noise, and utilize their dependencies on both the gate and drain bias to mitigate the thermal performance loss.

This chapter introduces studies that address thermal challenges regarding thermal characterization and management of GaN-based devices. Initially, different thermal characterization methods are discussed, and the method proposed in chapter 3 is used to demonstrate thermal influence of buffer and

substrate properties. Subsequently, a method to characterize the lateral thermal coupling in GaN circuits using a thermal sensor is introduced, which enables the use of standard equipment to measure horizontal heat spread. Furthermore, a biasing technique for a GaN MMIC is introduced, where behavioral models of the RF performance as a function of bias and temperature are extracted, which are used to predict the necessary bias control to mitigate thermal performance degradation.

4.1 Temperature Measurement Methods

There are numerous techniques to estimate the channel temperature, and these methods generally fall into three categories: electrical, physical, and optical. Depending on the properties and capabilities of the methods, transient or steady-state temperature characteristics can be obtained either directly or through $Z_{\mathrm{th}}/R_{\mathrm{th}}$. This section presents a brief review of established methods, covering their strengths and the challenges associated with measuring GaN-based devices.

Optical Methods

Despite the challenges with optical temperature measurements of GaN devices, these methods are often preferred for standard as well as detailed thermal evaluations [30–32] of bare die GaN HEMTs. Although the accuracy can vary, the methods offer direct measurement capability without the need to modify or physically contact the DUT, and the methods are considered suitable for devices affected by trapping.

Infrared Radiation

In IR thermography, the intensity of the thermal radiation emitted by an object is used to estimate its temperature. Real bodies do not exhibit perfect absorption and emission and the frequency-dependent emissivity (ε) of the (grey) body is decisive for the emitted radiation. In IR measurements, the signal is collected by an optical system, including IR optics and an IR sensitive detector array. By measuring the IR intensity from the circuit at a known temperature, the emissivity at each pixel of the IR camera can be obtained, which can then be used to compute the temperature of a powered device.

The energy impinging on a material must either pass through, be absorbed, or be reflected. In the case of good absorbers, all emitted light originates from thermal radiation and the temperature accuracy can approach mK. Metals tend to be very reflective and may exhibit $\varepsilon < 0.1$. In this case, a large part of the measured signal originates from reflected light, and the instrument mostly measures the ambient temperature or system noise level. The emissivity of semiconductors can vary in the range between 0.3 and 0.8. To obtain the temperature of low-emissivity materials, the temperature has to be raised substantially above the background temperature, which might not be possible for high-power devices. The wide bandgap of semiconductors such as GaN leads to a high transmissivity at IR wavelengths for such materials. Therefore, IR emission from deep below the surface can reach the IR detector, and gold

metallization on the backside can reflect more radiation. This leads to an averaging of the temperature in the vertical dimension, and it becomes difficult to determine what the temperature provided IR thermography represents. Absolute temperature uncertainty increases with temperature and can reach 20 to 50 °C for temperatures higher than 400 °C [32]. Coating the device with nontransparent material improves the accuracy, however, this method risks causing surface contamination/damage and does not guarantee a correct temperature observation. Additionally, the wavelength-related spatial resolution (around 1.9 µm) is not always sufficient for small devices, leading to lateral averaging. The main advantage of IR imaging is the capability to provide large area temperature mapping with reasonable spatial and temporal (3 µs) resolution.

Raman Spectroscopy

In Raman spectroscopy, the temperature is determined using the temperature dependence of phonon frequencies (lattice vibrations). The method involves focusing a laser onto a sample with an objective lens and passing the scattered light through a Rayleigh filter onto a spectrograph. A small fraction of light in a material undergo inelastic scattering, where the wavelength of scattered photons is shifted, which can provide information about phonons in the material. Any change in temperature leads to a change in phonon frequency, and the temperature in a powered device at localized regions can be determined by first determining the phonon frequency shift versus temperature in a calibration procedure.

Materials may exhibit several specific vibrational modes, and while the GaN Raman spectrum exhibits two strong phonon modes, contact metals do not exhibit easily accessible lines in their Raman spectrum. The accuracy of Raman measurements depends on the smallest frequency change of a given phonon mode that can be distinguished in the spectrum. A temperature accuracy around 4 % of the temperature rise can typically be achieved, and the accuracy inherently increases with temperature [32]. The linewidth of the Raman peak also defines the resolution, and the resolution for SiC is roughly 2–3 times better compared to GaN. A challenge when using Raman spectroscopy to measure the temperature in GaN devices is the phonon frequency shift due to non-thermally related factors, including piezoelectric strain caused by an applied electric field, and elastic strain resulting from the CTE mismatch between different layers. The total change in phonon frequency is therefore often separated into two parts, one related to the change in lattice temperature in a strain-free bulk material, and the other related to change induced by mechanical strain. To assess the effects of piezoelectric strain, HEMT pinch-off measurements are utilized, where the field is present and the power dissipation is negligible.

The advantages of Raman spectroscopy include the capability to measure the temperature of semiconductor materials a few microns below the semiconductor surface with high spatial resolution (approximately 0.4 µm laser spot size), and less lateral averaging compared to IR. The method is therefore considered suitable for precise single point temperature measurements in the HEMT channel.

Thermoreflectance

The thermoreflectance (TR) measurement technique exploits the temperature dependence of a material's reflectivity to determine its temperature. The reflectivity of a material depends on its temperature-dependent refractive index, and a first order approximation of the reflectivity-temperature relationship is $\Delta R/R = C_\mathrm{t}\Delta T$, where R is the reflectivity, T is the temperature, and C_t is the TR coefficient. In thermoreflectance imaging, a sample is illuminated using light sources that emit wavelengths typically ranging from 365 to 780 nm, and images are detected using a PIN diode array camera or a special high frame rate intensified charge coupled device (CCD) [33]. A pixel-by-pixel calibration of the TR coefficient enables to determine the temperature at targeted locations using the intensity of the reflected light.

The temperature sensitivity of the reflectivity (C_t) depends on the wavelength, ambient temperature, material, surface characteristics, and used material processing techniques. Dielectric coatings and passivation layers change the reflective properties and C_t needs to be determined at the measurement temperature at each surface to maximize measurement accuracy. To maximize the temperature resolution, the wavelength is usually selected to maximize C_t, although the wavelength also determines the spatial resolution. The possibility to use short wavelengths enables to achieve a diffraction limited resolution around 0.2-0.3 µmm for wavelengths between 365 to 780 nm. Most systems also offer high temporal (0.8 ns) resolution, and the temperature resolution ($< 0.5\,^\circ$C) is generally limited by the quantization threshold of the camera in CCD based systems [33]. For GaN devices, the transmission through the GaN and SiC can cause thin-film interference effects that convolute the TR signal, which increases uncertainty in vertical measurements. This can be mitigated by using UV radiation around 365 nm, which results in a clearer reflection on the top surface for GaN on SiC [34].

The strengths of TR include its capability to measure the surface temperature of semiconductors and metals with high spatial and temporal resolution, enabling fast transients measurements of temperature gradients on small surface microscopic regions such as the gate. Furthermore, TR does not require specific sample heating and can be done at room temperature or even at cryogenic temperatures.

Physical Methods

Physical methods use physical contact to the device or material to measure their temperature. Several such techniques exist [35], most of which are not applicable to small devices like RF GaN HEMTs. Physically integrated sensors such as micro resistance thermometer detectors (µRTDs) [36] are the best alternative for GaN devices. In this case, the sensor is located in the vicinity or inside the active region of the device, and the temperature is determined using temperature-dependent electric characteristics of the sensor (e.g. its resistance).

Integrated sensors face a number of challenges that need to be considered in their design and operation. The sensor needs to be non-invasive, meaning it should be able to operate without degrading the performance of the HEMT/circuit. Furthermore, the sensor itself should not affect the temper-

ature, meaning both the dissipated power in active sensors and the sensor size must be minimized. A small sensor is also needed to increase its spatial resolution and to be able to place the sensor as close as possible to hot spots. Furthermore, the sensor should ideally be compatible and manufacturable with the technology used for the DUT/MMIC. The temperature resolution depends on the sensor temperature characteristics and measurement equipment, and the sensor needs to be designed so it can detect small temperature changes using standard equipment.

Presumably, all requirements on the sensor can likely not be met simultaneously since the sensor for example becomes more invasive if it is placed closer to hot spots. However despite these challenges, thermal sensors offer several advantages to other techniques, including temperature monitoring of packaged end-applications circuits and low cost. Therefore, thermal sensors remain popular and state of the art sensors can be found in e.g. [37], where a resistive nickel temperature sensor was integrated next to the gate on the drain side of an RF HEMT. In paper [C], a small thermal sensor is proposed, which is well-suited for temperature measurements of GaN MMICs. The sensor exploits the temperature dependence of the current in a 2DEG, and the sensing element (thermometer) is thus the channel in the GaN layer. The measurement location is therefore inside the epitaxial structure in contrast to e.g. µRTDs, where the temperature of the sensor metal on the surface is measured. The proposed sensor is therefore suitable to use for studies of the thermal coupling between GaN channels (section 4.3).

The IV characteristics of a 2x15 µm sensor at different chuck temperatures are shown in Fig. 4.1a. Clearly, the current temperature sensitivity increases versus bias voltage up to around 1.5 V. However, a low bias voltage is needed to avoid the effects of self-heating and trapping (chapter 3). The pulsed IV measurement in Fig. 4.1b shows the impact of self-heating on the sensor current. The self-heating increases with increasing pulse width, and it can be seen that the self-heating is minimal up to 1.5 V. However, studies show that the current starts to decrease due to self-heating at 3-20 ns [38] at higher power levels. Shorter pulse widths are thus needed to observe the full impact of self-heating, and bias voltages lower than 1.5 V are therefore preferable. At a low bias, the self-heating is negligible and the sensor temperature is thus equal to T_{ck}, which allows to determine the sensor temperature using the current. To do this, the sensor current needs to be calibrated against a model, and the following model is proposed in paper [C].

$$I(T_{\mathrm{ck}}, V) = (a_1 + a_2 T_{\mathrm{ck}}) \tanh(V(b_1 + b_2 T_{\mathrm{ck}})) + V(c_1 + c_2 T_{\mathrm{ck}}), \tag{4.1}$$

where a-$c_{1\text{-}2}$ are fitting parameters. The model can predict the sensor behavior at low and high V and it is valid over a wide range of temperatures (inset in Fig. 4.1a). In practice, an accurate model is often only needed at a single V_{b}. In this case, simpler models such as polynomial expressions can be used, although such models are less accurate in extrapolated temperature regions compared to the proposed model.

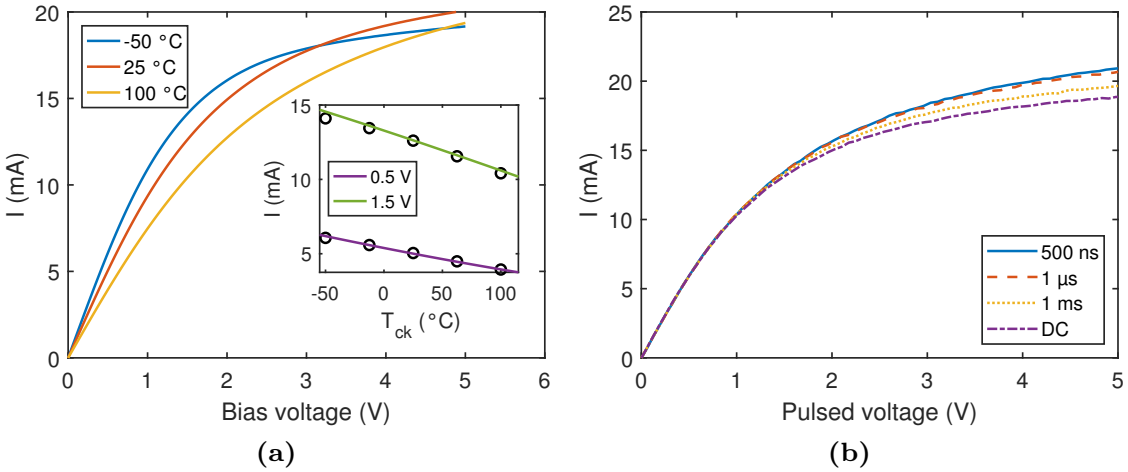


Figure 4.1: **(a)**: IV characteristics of the thermal sensor measured at -50 °C to 100 °C. Inset: model (-) and measurement (o) versus T_{ck} at different bias voltages. **(b)**: PIV characteristics of the thermal sensor measured with different pulse widths.

Electrical Methods

Electrical methods exploit temperature-dependent electric parameters of the device to determine its temperature characteristics. Usually, R_{th} is determined and used to calculate the average T_{c} at steady state conditions using the dissipated power. Techniques featuring AC signal analysis such as 3ω-based methods [39] can be used to determine Z_{th}, which allows for a transient thermal analysis of the device. An inherent property of electrical methods is the averaging of the temperature according to the size of the used thermometer (e.g. channel). Another weakness is their vulnerability to distortion due to trapping (chapter 3), which makes the characterization of GaN-based devices particularly challenging. There are numerous electric-based methods to determine $R_{\mathrm{th}}/Z_{\mathrm{th}}$ of GaN HEMTs [40–42]. Several electrical parameters can be utilized for this purpose, including the threshold voltage, Schottky diode current [43], gate resistance [44], and drain current [40]. In this section, common techniques and methods that address the measurement challenges due to trapping are briefly reviewed.

Pulsed IV Techniques

R_{th} can be determined using pulsed IV measurements as described in [41, 42], where the temperature dependence of the on-resistance is utilized. First, a look-up table of R_{on} versus T_{c} is created by measuring R_{on} at different chuck temperatures ($T_{\mathrm{ck}} = T_{\mathrm{c}}$). Next, R_{on} is measured at different quiescent bias points, which correspond to increasing power dissipation levels. Subsequently, the R_{on} versus P_{d} and T_{c} characteristics can be used to obtain a T_{c} versus P_{d} curve, where R_{th} can be extracted from the slope.

As discussed in [42], the method is highly dependent on the sub-microsecond pulses to limit the cool-down during the R_{on} measurements after a high power bias. Essentially, T_{c} must remain constant during the pulse, but PIV systems cannot always provide sufficiently short pulses, which can lead to underestimations of R_{th}. Extraction error due to trapping is also discussed in [42], and

based on tests on stressed and fresh devices, the influence of trapping on the obtained R_{th} is concluded to be minimal. However, this result depends on the particular device under test and trapping thus remains a potential source of error in the extraction.

3ω and GRT Methods

The 3ω method [45] was originally developed to determine the thermal conductivity of dielectric solids. A metal film on top of a sample is used as both heater and thermometer. The radial flow of heat from the metal film causes a resistance oscillation at (2ω), which produces a small voltage oscillation across the line at 3ω. This AC voltage is measured using lock-in amplifiers and can be used to calculate the thermal conductivity. The method has been modified in [39] so it can be used to determine thermal resistance of GaN HEMTs. In this case, the HEMT is operated in the linear region and the channel is used as thermometer. The DUT is placed in a Wheatstone bridge to be able to detect the 3ω signal, which is roughly 90 dB lower than the fundamental. The 3$^{\text{rd}}$ harmonic voltage can be expressed in terms of Z_{th}, the fundamental voltage and current magnitudes, as well as on-resistance properties. This allows to determine Z_{th} based on measurements of the 3$^{\text{rd}}$ harmonic.

The challenges with this technique are discussed in [46] and involve the impact of parasitics as well as the temperature coefficients of the bridge components. Although the Wheatstone bridge and lock-in amplifiers can be practically inconvenient, the method requires no modifications of the HEMT itself, which is an advantage compared to other methods. Furthermore, the method features low voltage amplitudes and zero bias voltage, which mitigates errors in the results due to trapping.

In gate resistance thermometry (GRT), the temperature dependence of the gate metal is used to estimate the temperature in the underlying channel [44,47]. A special HEMT is fabricated, where additional pads and access lines are added, which can be used to measure the voltage over the gate finger. First, the end-to-end resistance of the gate finger is measured versus T_{ck} while the HEMT is in a pinch-off condition. The data is then used to extract a model of the resistance versus gate temperature, which can be used to convert gate resistances at different bias conditions to the actual temperatures of the gate. In addition, it has been shown that frequency-resolved GRT can be used to extract the thermal impedance, which enables transient thermal analysis with high resolution (sub-100 ns) [48]. This is done by injecting a sinusoidal signal into the channel, which causes a temperature variation that is determined using gate resistance measurements. The thermal impedance can then be determined in the frequency domain as the ratio of the temperature variation over the dissipated power.

Several measurement challenges exist in GRT, where errors can be caused by e.g. leakage current in the probe and drain-gate leakage. Furthermore, the instruments need high sensitivity and low noise to measure a small voltages over the gate finger, and the frequency resolved GRT requires the use of additional correction methods and lock-in amplifiers. Nevertheless, in terms of trap-related distortion, GRT is advantageous since the gate metal is used as thermometer, which is not affected by trapping. This is achieved at the

cost of a measurement location slightly offset from the channel, and special layout design modifications. The method proposed in paper [B] also requires layout modifications to improve accuracy, although the channel is maintained as measurement location.

4.2 Example of Thermal Evaluation

Thermal management entails removing waste heat using remote or integrated cooling methods, where the device is passively or actively cooled. The total R_{th} is set by the thermal resistances in the GaN-die, heat spreader, package, and interface regions. The main difference between different cooling approaches is which one of the different thermal resistances that is lowered. Passive remote cooling is the traditional heat management approach, where the die is attached to and cooled by a heat-spreader and package with thermal interface materials (TIMs). Diamond composite materials are often used for the heat spreader to obtain high thermal conductivity and a low coefficient of thermal expansion (CTE), which ideally should be matched to adjacent materials to avoid cracking. Additional factors to consider are the thermal properties of the TIMs and thermal boundary resistances, which depend on e.g. surface roughness. Efforts are also made to develop active cooling approaches. Initially, the focus has been to explore microfluidic cooling by integrating microchannels into the heat-spreader [49]. This type of cooling faces unique challenges, and is usually not implemented near the channel.

Passive integrated cooling methods are implemented close to the channel. Such methods include the use of high thermal conductivity substrates, thermal optimization of device epitaxy, increased gate pitch, thermal via holes, and top side cooling approaches. High thermal conductivity substrates such as SiC (500 W/mK) are predominantly used for GaN HEMTs, although substrates made using chemical vapor deposition of diamond (2000 W/mK) are also emerging. Near-channel cooling is limited by thermal boundary resistances, such as the TBR caused by the nucleation layer [16]. Furthermore, differences in CTEs must be considered, and heat removal must be achieved without negatively affecting the device's electrical performance. In paper [B], the outlined R_{th} extraction method (chapter 3.3) was used to perform a thermal evaluation of devices with different buffer and substrate thickness. The thermal resistances of the devices are show in Fig. 4.2, where M1-M2 feature a 100 µm SiC substrate and M3-M4 feature a 500 µm SiC substrate. Evidently, a thicker substrate results in a lower R_{th}, and this is primarily due to increased horizontal heat spread in a thicker substrate, which increases the effective area of the heat source.

However, the substrate thickness also influences the cut-off frequency of higher order propagation modes, which can distort signals at microwave frequencies. Additionally, the characteristic impedance depends on the substrate thickness-to-line-width ratio, and the thickness needs to be set so that e.g. a 50 Ωline can be designed with a reasonable line width. These requirements generally leads to a need to reduce the thickness down to around 100 µm. Thus, a trade-off must be made between thermal and high frequency optimization to achieve high power at high frequency.

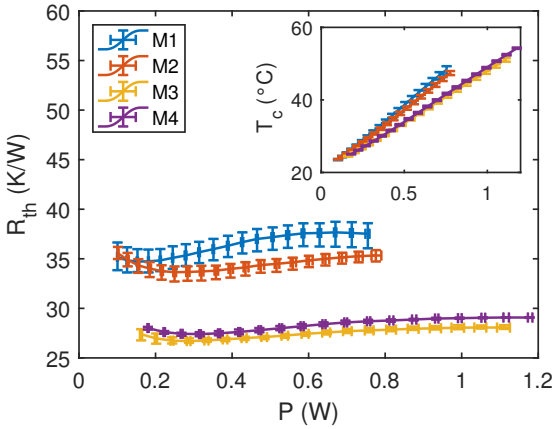


Figure 4.2: Thermal resistance versus power dissipation for different GaN technologies. The devices are gateless with 32 µm contact separation. M1-2 feature 100 µm thick substrates from different suppliers. M3-4 feature 500 µm thick substrates and have different buffer thickness. The inset shows the average channel temperature.

The difference between M1 and M2 is the supplier of the substrate, and the small observed difference is attributed to differences in crystal quality. M3 features a thin GaN buffer (250 nm) and M4 has a more common thickness around 1.7 µm. Although, the substrate suppliers are also different in these cases, the results suggest the influence of the buffer thickness on the thermal performance is minimal, which can be explained by the thermal simulations in [50], where small differences are seen if the nucleation-related TBR is small. It is further concluded that R_{th} increases for a very thin buffers, and the optimal thickness ranges from 200 nm to 2 µm depending on the TBR value. In general, the R_{th} values are also highly affected by the test rig and depend on if the samples are e.g. glued, screwed, or are placed directly on the chuck. Soldering the samples to a baseplate carrier may reduce the measured R_{th} by up to 40 % [42].

4.3 Thermal Coupling Characterization Method

Increased power density in the devices as well as the miniaturization of circuits at high frequencies naturally leads to a larger impact of thermal effects. An example of the miniaturization can be seen in integrated active antenna systems, where densely packed high power microwave transceiver front-ends are separated by half the wavelength. Thus, at higher frequencies the thermal (and electrical) coupling increases, and the operating temperature at the center array elements is significantly higher compared to the perimeter elements [51]. Naturally, thermal coupling also occurs on a device level, as demonstrated with simulations of an AlGaN/GaN powerbar in [52]. In this case, finite element-based simulations combined with electrical network simulations show how an individual cell heats up its neighbouring cells, and the temperature increase for adjacent and distant cells ranges from 5 to 15 °C. It can be concluded that methods are needed to characterize the thermal coupling to be able to assess heat-spreading properties in different devices and circuits. Electrical methods are an attractive alternative to optical methods since they enable the use of commonly available (and cheaper) lab equipment, and offer the possibility to evaluate packaged

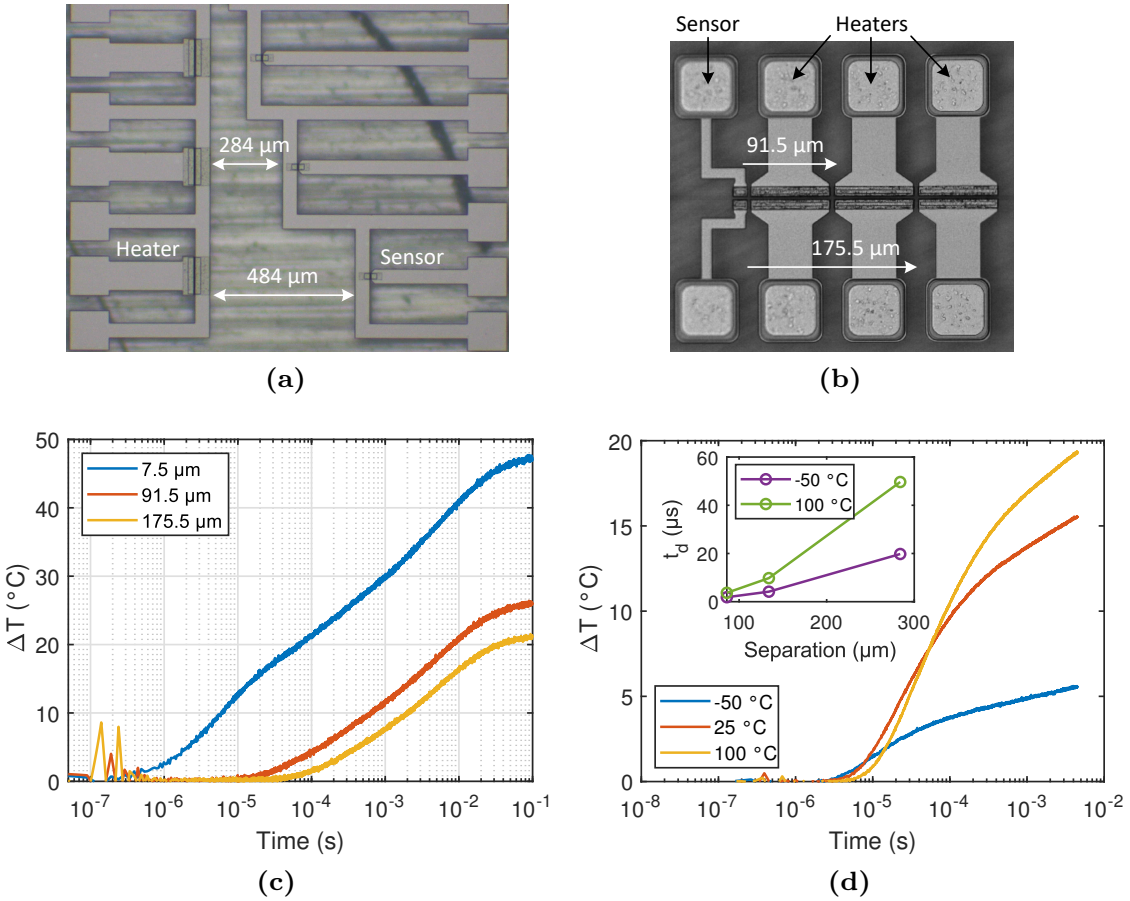


Figure 4.3: **(a)-(b)**: test structures for lateral thermal coupling characterization featuring heating elements and thermal sensors with different separation. **(c)**: transient temperature increase at the different heater-sensor separations shown in **(b)**. **(d)**: Transient temperature increase at different chuck temperatures, measured at a fixed distance of 86 µm using the structure in **(a)**. The inset shows the propagation delay versus separation at different chuck temperatures.

devices.

In paper [C], a method to evaluate lateral thermal coupling through electrical measurements on a dedicated test structure is proposed. The test structure is designed using the thermal sensor described in section 4.1 and heat sources in the form of larger gateless devices. A large and a more recently designed compact version of the structure are shown in Fig. 4.3a and Fig. 4.3b, respectively. The structures are comprised of heaters and sensors with separations ranging from a few µm up to hundreds of µm. This allows to measure the thermal coupling over distances equivalent to gate finger separations as well as between transistor cells. The structure enables to evaluate the thermal coupling by measuring the transient temperature at different distances from the heat source. This is done by applying a voltage step to the heater while simultaneously measuring the current in the sensor using an oscilloscope. The sensor temperature response is subsequently determined using the current-temperature model of the sensor (section 4.1).

Examples of the transient temperature response in the sensor due to the coupling of heat from heat sources at different distances are shown in Fig. 4.3c (measured on the structure shown in Fig. 4.3b). As expected, the temperature

decreases with increasing separation due to the heat spreading from the source in all directions corresponding to the lower half of a sphere. Furthermore, the shape of the response is different for the short distances compared to the longer separations, suggesting a different number of time constant are involved at different separations. Additionally, a time delay in the sensor response can be observed, which increases with increasing distance. To assess the properties of the thermal coupling at different operating temperatures, the transient measurement can be performed at different T_{ck}. This is shown in Fig. 4.3d, where the temperature increase (measured on the structure shown in Fig. 4.3a) at a fixed distance is presented. The thermal coupling is seen to be significantly higher at higher T_{ck}, and this is primarily attributed to a higher thermal diffusivity in the SiC and GaN layers at lower temperatures [53], which causes heat to spread through a larger volume. As a result, the temperature at a fixed distance from the heat source is reduced. An empirical model consisting of exponential terms can be used to determine the number of thermal time constants present in the transient characteristic. The following empirical model is proposed in paper [C]

$$I(t) = I_0 + \sigma(t - t_{\mathrm{d}}) \sum_{\mathrm{n}=1}^{3} A_{\mathrm{n}}(e^{-(t-t_{\mathrm{d}})/\tau_{\mathrm{n}}} - 1), \tag{4.2}$$

where

$$\sigma(t - t_{\mathrm{d}}) = \begin{cases} 0, & t - t_{\mathrm{d}} < 0 \\ 1, & t - t_{\mathrm{d}} \geq 0 \end{cases}, \tag{4.3}$$

A_{n} is the amplitude coefficient, τ_{n} is the time constant, and t_{d} is a propagation delay parameter. The inset in Fig. 4.3d shows that the propagation delay increases with increasing separation as expected, and it can be further noted that t_{d} decreases with decreasing T_{ck}, which confirms that the heat diffuses faster at lower operating temperatures.

The proposed methodology can be utilized in several different situations. In [54], the proposed sensor and measurements are used for noninvasive thermal characterization and monitoring of packaged and bare-die GaN MMICs. An electrothermal model in the form of multiple RC networks is derived and implemented in CAD software, and the model can be used to estimate the temperature in the active MMIC elements from a remote location on the die. The model can be extracted using the time constants in the thermal response (provided by (4.2)) and by fitting the simulation to the measured data.

The thermal coupling measurement method can also be utilized in numerical thermal modeling where the simulation environment needs to be calibrated against measured data. This is not trivial since several parameters with complex thermal influence need to be determined, and multiple possible parameter value combinations create large uncertainty. In [b], a method for calibrating the FEM model is demonstrated, where the lateral thermal coupling measurements enable to differentiate the thermal influence of the epitaxial layers, substrate, and die-attach layer. This allows to separately determine correct model parameter values, which greatly facilitates calibrating a model against measured data.

In [c], the methodology is used to investigate the role of thermal coupling in the dynamic self-heating of GaN MMIC power amplifiers. It is concluded that the thermal coupling exhibits a low-pass-filtered response, where the magnitude

and cutoff frequency decrease with increasing separation from the heat source. It is further noted that thermal coupling must be considered to predict the thermal response below 10 kHz.

4.4 Biasing to Mitigate Thermal Degradation

MMICs must meet strict performance requirements to ensure reliable functionality in their intended applications. However, the operating temperature of the circuit varies depending on ambient conditions and the output power drive level. This creates an undesirable variation of the RF characteristics, which can lead to fluctuations in application performance. Several techniques have consequently been developed to compensate/mitigate the thermal degradation in the device. The methods involve analog on-chip compensation circuits as well as digital off-chip regulators. For CMOS RF amplifiers, methods involving analog adaptive bias are used, including zero-temperature coefficient biasing, constant-transconductance biasing, and proportional-to-absolute temperature biasing [55, 56]. Furthermore, temperature compensation circuits based on diodes and current mirrors have been designed for GaAs MMICs to mitigate temperature-related reduction of the gain [57, 58].

However, several RF performance parameters such as efficiency and linearity cannot be extensively controlled using only the gate bias or bias current. The drain bias is therefore also controlled in more advanced supply modulation techniques such as envelope tracking, where the bias is controlled to ensure amplifiers always operate at maximum efficiency. Power amplifiers are typically biased to output the maximum possible RF power. However, when the amplifier is backed-off from peak output power, most of the power provided by the bias supply is converted into heat, resulting in low efficiency. This can be understood from the bias points in Fig. 4.4a. At maximum output power, the load line at B2 swings from the maximum to the minimum V_{ds} and the RF-to-DC power ratio $P_{\mathrm{out}}/P_{\mathrm{dc}}$ is maximized at the bias point. If the RF power decreases, the efficiency decreases since the transistor consumes the same amount of DC

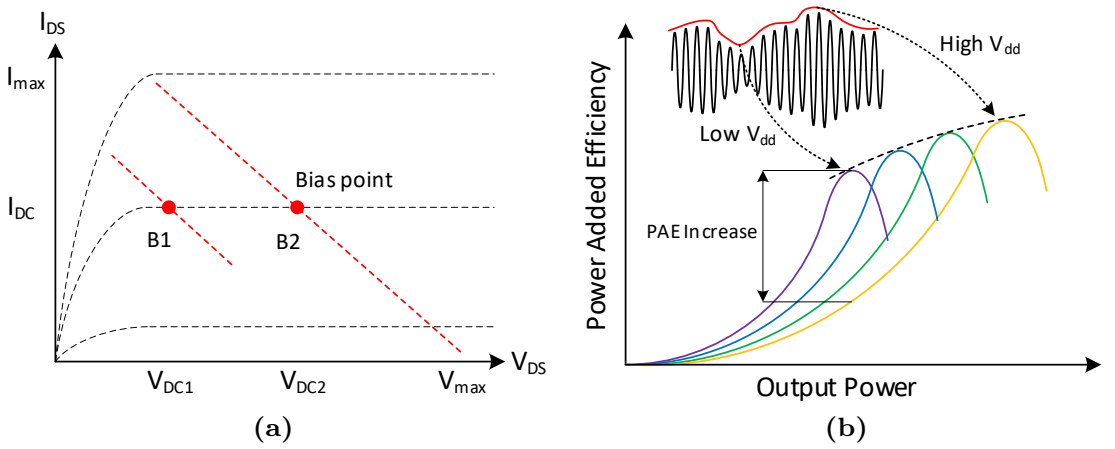


Figure 4.4: Principle of envelope tracking. **(a)**: transistor output characteristics and bias points enabling a small (B1) and large (B2) voltage swing. **(b)**: power added efficiency versus RF output power for different V_{ds}.

power. This can be avoided by reducing V_{ds} (and hence P_{dc}) so that only enough power is supplied to allow for the current load line swing, as shown at the bias point B1 in Fig. 4.4a. Fig. 4.4b shows the power-added efficiency versus RF output power at different V_{ds}. When the signal has a high peak-to-average power ratio and thus varying envelope (inset in Fig. 4.4b), the power amplifier is occasionally forced to operate with less efficiency if the drain voltage is kept fixed. In envelope tracking, V_{ds} is dynamically adjusted according to the envelope as the RF signal varies, ensuring that peak efficiency is maintained. As a result, the waste heat is reduced, which improves the circuit lifetime. However, the bias dependencies of properties such as linearity and gain are different compared to e.g. the efficiency. For example, it is well-know that the device becomes less linear at lower V_{ds}, meaning envelope tracking may degrade linearity although the temperature is reduced. Therefore, models of all main RF properties as a functions of bias and temperature are needed to see if and how adaptive biasing can be used to mitigate degradation of several RF performance parameters simultaneously.

Performance loss Compensation Biasing

In paper [D], an extensive characterization of a commercial 2-6 GHz GaN-on-SiC MMIC LNA (Fig. 2.2b) suitable for wireless communication and aerospace applications was carried out. The gain, output third order intercept point (OIP3), 1 dB compression point (P1dB) and noise figure (NF) were measured as functions of (V_{gs},V_{ds}), and T_{ck}. At a fixed frequency and temperature, the MMIC RF characteristics can be visualized as surfaces as functions of V_{gs} and V_{ds} as shown in Fig. 4.5b. Clearly, all parameters are fairly sensible to changes in the bias voltages, and the gain exhibits a strong dependence on V_{ds} whereas

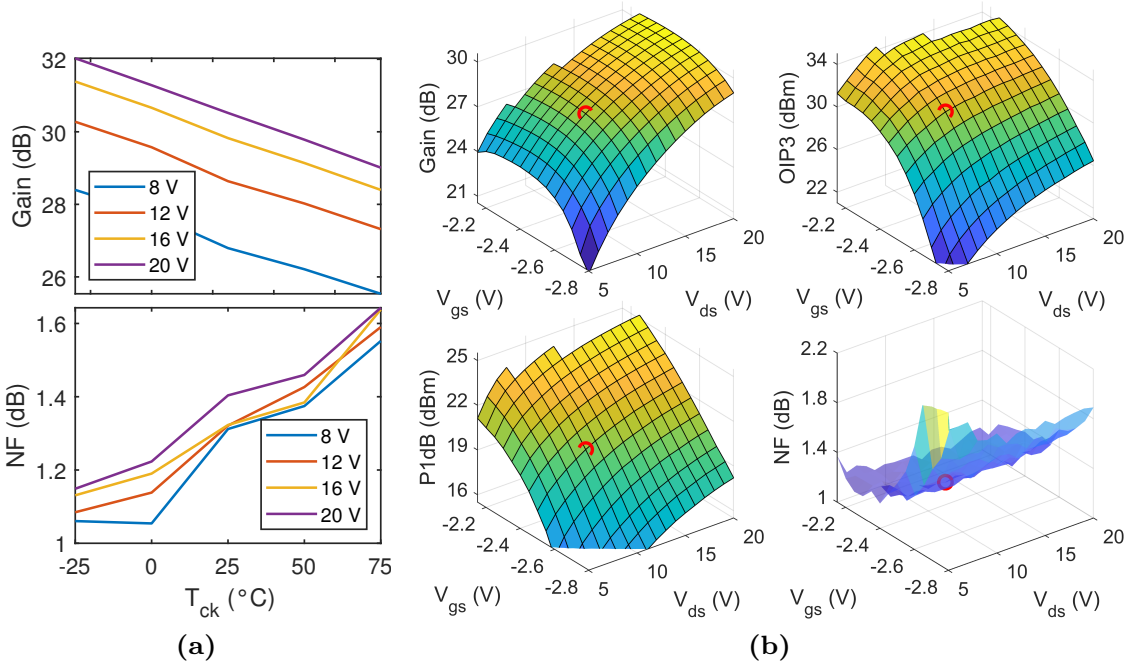


Figure 4.5: (a): Gain and NF versus chuck temperature for different drain-source voltages. **(b)**: bias voltage dependencies of the gain, OIP3, P1dB, and NF. The red circle marks the recommended bias point for the LNA.

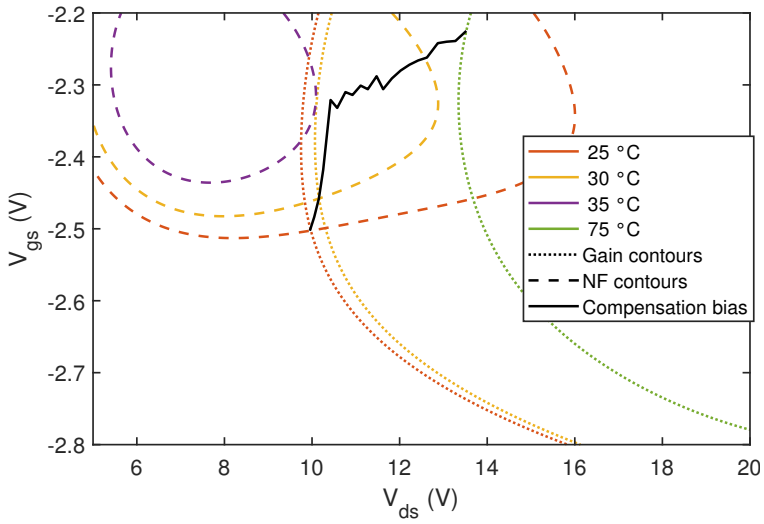


Figure 4.6: Gain and NF contours (28 dB & 1.8 dB) at temperatures from 25 °C to 75 °C. The black curve shows a biasing versus temperature for the LNA that compensates for thermal degradation of the gain and NF.

the OIP3, P1dB, and NF depend strongly on V_{gs}. The bias dependence of the NF is consistent with the bias-dependent white noise models for GaN HEMTs presented in [59], which predict increasing effective noise temperatures with increasing V_{ds} and decreasing $I_{\mathrm{ds}}/V_{\mathrm{gs}}$. The red circle in Fig. 4.5b indicates the recommended bias point, and it is clear that the bias can be used to improve all RF performance parameters. Fig. 4.5a shows how the NF and gain degrade at higher chip temperatures. The thermal noise power is proportional to temperature, and increased losses in the circuit degrades the NF further. The gain is sensitive to imperfect matching, and the mismatching increases at higher temperatures since the S-parameters of the HEMTs are changed. Although higher drain voltages can be seen to increase the gain notably, the increase can be seen to diminish at higher V_{ds}, which is caused by the higher DC power and consequent larger self-heating.

To determine the necessary biasing to counteract the thermal degradation of the RF characteristics, models of the characteristics as well as estimations of the operating temperature of the MMIC during operation are needed. Behavioral models were therefore fitted to the measured RF characteristics, and the models were used to analyze the bias and temperature behavior of multiple RF parameters simultaneously. This can be done using contour lines as shown in, Fig. 4.6, where gain and NF contours are shown at different T_{ck}. Evidently, the gain and NF contours intersect at temperatures up to 30 °C, which makes it possible to bias the MMIC to maintain the gain and NF. However, at higher temperatures the gain contour moves towards higher V_{ds} while the NF contour move towards lower V_{ds}. Thus, trade-offs must be made in the optimization of different RF performance parameters, and it can be further noted that no NF contour exist at 75 °C, meaning the NF compensation possibilities are limited. In Fig. 4.6, a curve representing the bias voltages versus increasing T_{ck} is indicated, which ensures a temperature invariant gain and as low NF as possible. This is achieved by selecting the bias voltages corresponding to the intersection of the gain and NF contour at each temperature, and when no intersection exist, the bias point on the gain contour corresponding to the

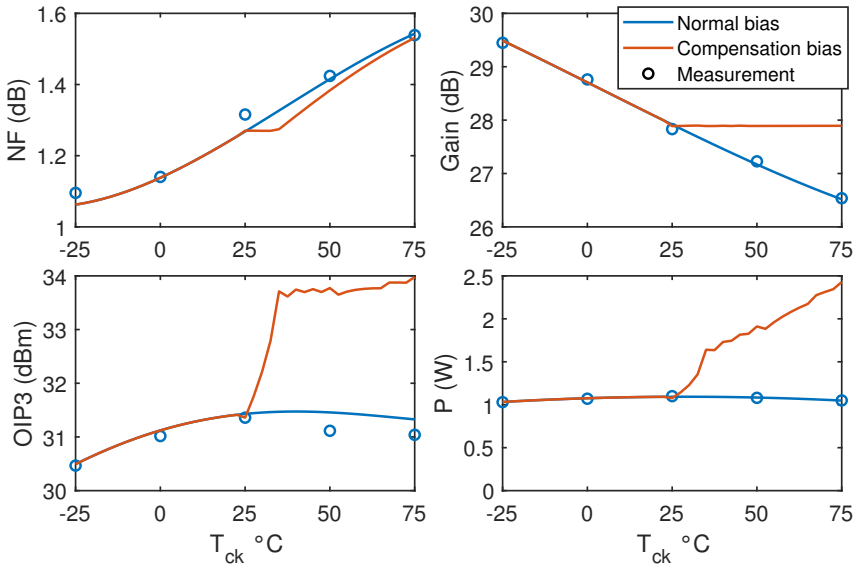


Figure 4.7: DC power and RF performance parameters versus temperature for a fixed recommended bias and temperature compensation bias. The compensation bias is performed to maintain a constant gain above 25 °C while keeping the NF as low as possible.

lowest NF is selected.

The temperature dependence of the RF characteristics resulting from the temperature compensation bias as well as a normal constant bias are shown in Fig. 4.7. The compensation biasing starts at 25 °C, above which the gain remains constant. The NF is only constant for roughly 10 °C, after which a zero gain temperature coefficient is prioritized. It can be seen that the compensation bias improves the linearity but the power consumption is also seen to increase with T_{ck}, which leads to a higher channel temperature. Despite this, a constant gain can be achieved since the gain increases more with increasing V_{ds} than it decreases due to the ensuing increase of T_{c}. However, the higher T_{c} decreases the lifetime of the circuit, which is the main drawback of the suggested approach. On the other hand, it would be possible to control the bias so the dissipated power increase is limited while maintaining a constant gain, although this would lead to reduced linearity and noise performance.

Chapter 5

Breakdown Characterizations

As the heat removal techniques are improved, it becomes possible to increase the device power density by increasing the breakdown voltage (BV) and/or current density. Increased breakdown voltage is achieved through advancements in material science and device design, including improvements in field plate (FP) and epitaxial design. The evaluation of novel high voltage designs is primarily based on DC breakdown measurements. However, the DC breakdown voltage may not represent the actual voltage capability of the device during large-signal operation, where the maximum voltage is only applied for a short time. This is indicated by the results of pulsed measurements on GaN power HEMTs, where the BV is observed to increase with shorter pulse widths [60]. However, the characterization of dynamic breakdown properties of GaN HEMTs is not trivial since it requires the use of non-standard methods such as waveform [61] and circuit-based [62] measurement techniques.

In addition, despite a large number of publications, there is no general agreement on the definition of breakdown. Usually the breakdown under pinch-off conditions is characterized by the sudden increase of the drain current, and the associated bias voltage is referred to as the breakdown voltage. Another way to define breakdown is to identify the bias condition (at a certain V_{gs}), where a burnout of the device is triggered. Although this definition is the most precise, it is also undesirably destructive for the DUT. Another approach is to define the breakdown at a certain current level such as 1 mA/mm. However, different leakage currents may contribute significantly to the increase of current at high drain voltages, and the total current leakage depends on device design and temperature. As a result, BV estimations based on a fixed current density criterion can be misinterpreted and misleading.

In this chapter, GaN HEMT breakdown measurements and characteristics are examined. Initially, possible causes for the breakdown are briefly discussed and an approach for DC breakdown characterizations is outlined, which ensures the measurement is not limited by leakage. Furthermore, methods to measure breakdown under dynamic signal conditions are demonstrated, and the different results are compared and discussed.

Breakdown Mechanisms

Several breakdown mechanisms have been proposed to cause the off-state breakdown in AlGaN/GaN HEMTs, and a comprehensive description of different mechanisms is provided in [11]. In this section, mechanisms relevant for microwave GaN HEMTs are briefly discussed followed by a simulation analysis of the DC breakdown, as described in paper [E].

The breakdown of microwave devices is suggested to to be caused by different mechanism, including punch-through effects, impact ionization, as well as other mechanisms related to the gate [62–64]. Punch through is an increase in I_{ds} due to poor confinement of charge at the AlGaN/GaN interface, which results in poor gate modulation capability. This breakdown predominantly occurs in short gate-length HEMTs [63]. Thermal runaway is a rapid temperature increase due to positive temperature feedback, which can be caused by the positive temperature coefficient of e.g. gate leakage currents [65]. Above a certain power density threshold in the gate surface leakage, surface heating exceeds cooling, leading to a positive temperature feedback and subsequent breakdown [66]. A current conduction mechanism involving electron hopping along surface states between the gate and drain has been proposed as an explanation for this type of breakdown. The gate breakdown has also been suggested to be caused by degradation related to crystallographic defect formation, and gate metal degradation due to electromigration forming local interruptions of the Schottky contact [11]. It is further suggested that the high electric field at the drain edge of the gate causes mechanical strain, and degradation occurs when a critical elastic energy is reached. Another gate-related breakdown mechanism is impact ionization related to Auger generation [11]. In this case, electrons penetrating the barrier possess energies significantly higher than the GaN conduction band. Such electrons can transfer their energy to electrons in the valence band, which can create additional electron-hole pairs.

Impact ionization is assumed to be one of the primary reasons for the breakdown in GaN HEMTs. It refers to the generation of free charge carriers due to collisions between free carriers and atoms. In a high electric field, an electron can gain sufficient energy so it can break a covalent bond when colliding with another crystal atom. The accelerated electron must gain at least an energy equal to the bandgap to break the bond, which is equivalent to exciting the electron to the conduction band. The result of this process is the creation of a new electron-hole pair. Impact ionization can cause avalanche current multiplication, where newly generated free carrier create additional free electron-hole pairs. The breakdown-associated impact ionization occurs at critical electric fields, and it can occur at different locations in the device depending on material properties as well as where electric fields and leakage currents are high.

Ultimately, the cause of the breakdown depends on e.g. device geometries, epitaxial design, and surface passivation. In paper [E], Technology Computer-Aided Design (TCAD) simulations were used to identify and study possible reasons for the breakdown in a typical microwave GaN HEMT. Although the analysis is limited by the physics included in the simulation, it can provide valuable information about what occurs inside the device during the breakdown.

The device was simulated at a pinch-off condition where V_{ds} was increased

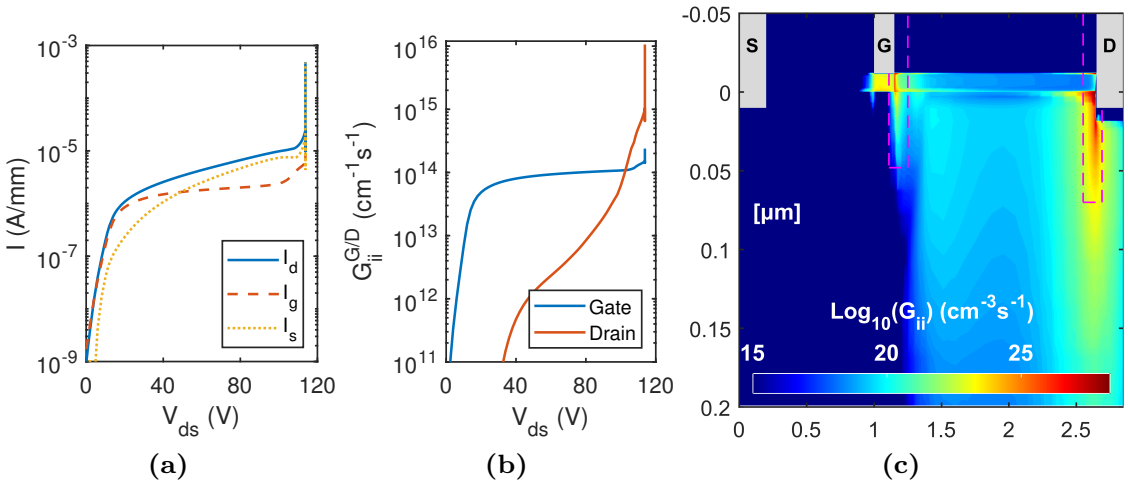


Figure 5.1: GaN HEMT off-state breakdown simulation. **(a)**: simulated currents versus drain-source voltage. **(b)**: total carrier generation rate due to impact ionization at the gate and drain contacts, obtained by integrating the generation rate in **(c)** over the areas enclosed by the dashed lines. **(c)** shows the carrier generation rate at the drain-source breakdown voltage (113 V).

until the BV was reached, as shown in Fig. 5.1a. Punch-through effects contribute to a gradual increase of the drain current, which can be seen in I_s and I_d at 30 to 100 V. The impact ionization causes a large current increase at 113 V, which coincides with a high carrier generation rate at the drain contact, as seen in Fig. 5.1c. The total generation rate (obtained by integration) versus V_{ds} at the gate contact (G_{ii}^{G}) and drain contact (G_{ii}^{D}), are shown in Fig. 5.1b, where an abrupt increase is seen for G_{ii}^{D} at the BV. The maximum carrier generation rate per unit volume and the maximum E-field are significantly higher at the gate compared to the drain. Despite this, the breakdown is driven by impact ionization in the buffer at the drain, which creates an avalanche current flowing into the source. This simulation analysis is a useful tool for identifying possible explanations for real breakdown measurement.

5.1 DC Breakdown Measurements

DC breakdown measurements are the standard measurements used to obtain the breakdown voltage characteristics of a device. The three-terminal measurement methods include current- or voltage-controlled IV sweeps as well as constant current injection techniques, and the different methods are often supplemental to each other. Furthermore, although two-terminal measurements yield different results compared to the three-terminal configuration, these can be used to study specific breakdown properties between two terminals, as demonstrated in paper [E].

In real devices, complex leakage mechanisms exist, which may contribute significantly to an increase in I_{ds} at high drain voltages in the off-state. The initial step in a DC breakdown characterization is therefore to determine the current leakage levels in the HEMT as a function of voltage and temperature. For this purpose, the current-controlled DC breakdown method [67, 68], where the current is swept at a fixed V_{gs} can be used. Fig. 5.2a shows three I_d-V_{ds} characteristics, which were measured consecutively. At lower V_{ds} (up to ≈30 V),

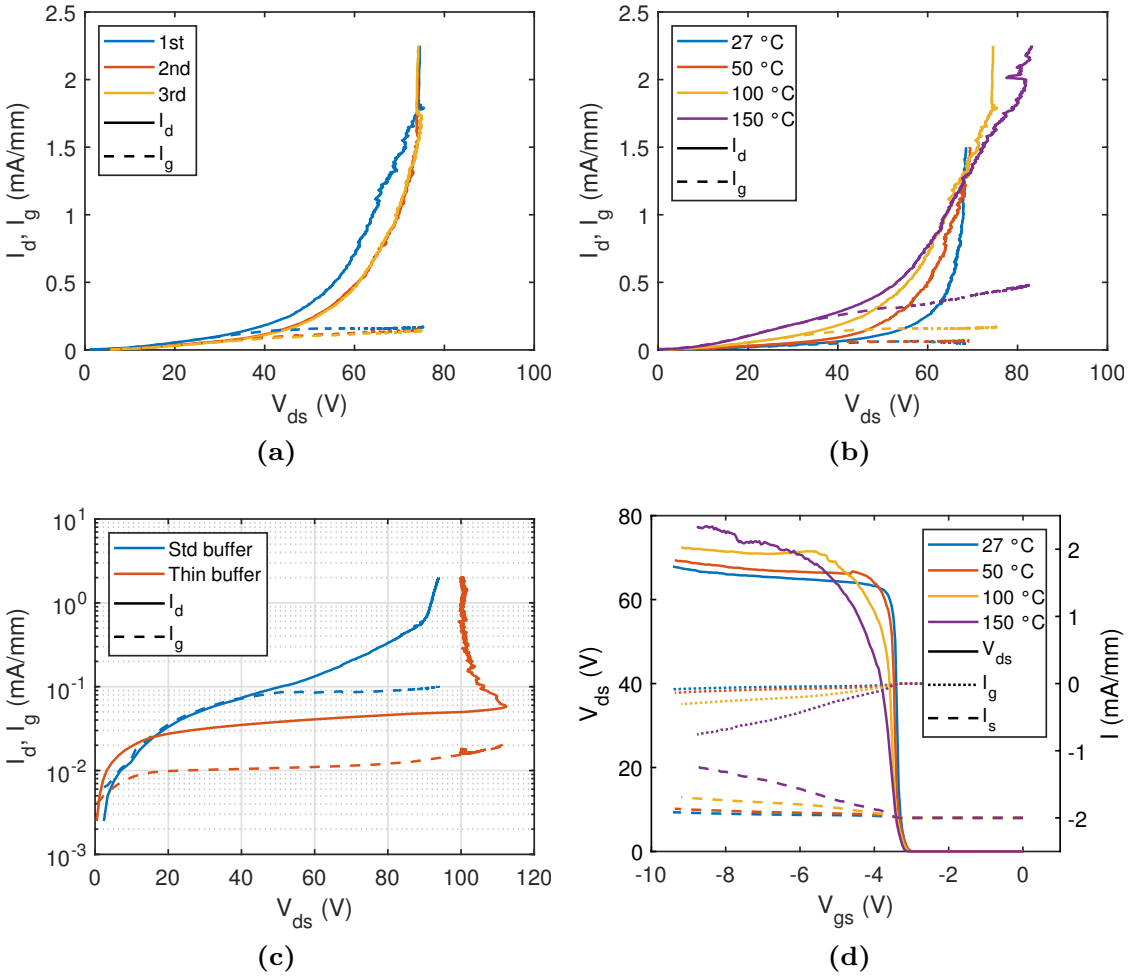


Figure 5.2: Three-terminal off-state breakdown characteristics. **(a)**: three I_d-V_{ds} characteristics measured consecutively. **(b)**: I_d-V_{ds} characteristics measured at different chuck temperatures. **(c)**: I_d-V_{ds} characteristics of GaN HEMTs with a thin and standard buffer thickness. **(d)**: results of breakdown measurements performed with the drain current injection technique at different temperatures.

I_d is comprised of a resistive drain-gate current leakage. However, above $\approx$ 40 V, I_d increases much quicker due to a current component that flows into the source, which is ascribed to punch-through effects. BV_{ds} is often characterized by a steep current increase [64, 68], and although this can be seen around 74 V $= BV_{ds}$, the exact BV is not entirely obvious in Fig. 5.2a. The first curve is not identical to the 2nd and 3rd curves due to trap-related memory effects, which mostly affect leakage and punch-through currents. Thus, the overlap of the curves at 74 V indicates that the voltage is set by breakdown current and that the BV measurement is highly repeatable. It can be further concluded that leakage and punch-through currents can cause significant increase in I_d at drain-source voltages lower than BV_{ds}. Fig. 5.2b shows the I_d-V_{ds} characteristics at temperatures ranging from 27 to 150 °C. At e.g. 65 V, the current increases versus T_{ck} up to 1 mA/mm, meaning the breakdown can only be measured at current levels higher than 1 mA/mm at 150 °C. Naturally, the leakage characteristics depend on the device technology, as can be seen in Fig. 5.2c, where the I_d-V_{ds} characteristics of two different devices are shown. For the thin buffer (TB) device, the leakage is up to ten times lower and the leakage increase versus V_{ds} is significantly smaller compared to the standard buffer

device. Furthermore, the shape of the curve at the BV is clearly different. In contrast to the standard buffer, the TB device exhibits an abrupt current increase and abrupt voltage reduction due to the protection resistor (R_{pd}) on the drain. R_{pd} reduces V_{ds} when the current rapidly increases, which inhibits the breakdown process and limits the joule heating. R_{pd} must be high enough to reduce V_{ds} sufficiently, and small enough to be negligible compared to the off-state output resistance of the device. The appropriate R_{pd} value therefore depends on the HEMT (e.g. the gate periphery) and measurement conditions such as temperature. The effectiveness of R_{pd} also depends on the mechanism causing the breakdown. Thus, it is not straightforward to determine the necessary R_{pd}, and iterations are often needed. In the case of impact ionization, a voltage drop between 100 to 500 mV for a current increase around 0.5 mA/mm is often needed to ensure the device is protected. In Fig. 5.2c it can be noted that the TB device exhibits a breakdown at (112 V, 0.06 mA/mm), where R_{pd} causes a large voltage drop and a negative differential resistance. In this case, extracting the BV at higher current levels would lead to an underestimation of the BV, which is one drawback of using a protection resistor. Another drawback is that a negative resistance can be caused by measurement noise, which depends on e.g. the sweep step. In [68], logarithmic I_{d} sweeps were used and the BV is defined as the first radical variation in the slope of the IV curve. Although larger current steps can facilitate detecting the BV, it reduces the resolution and can induce large breakdown currents before the measurement is stopped.

Drain-Current Injection Technique

The HEMT breakdown depends on the voltage applied to all three terminals, and the drain-current injection technique [69] was used in paper [E] to study the BV dependence on V_{gs}. In this measurement, V_{gs} is swept while a constant I_{d} is forced. The current value should be selected to ensure the measurement is not limited by leakage, and the I_{d}-V_{ds} characteristics were used in paper [E] to determine an appropriate value. Examples of the characteristics obtained using the current injection method are shown in Fig. 5.2d. The threshold region starts at approximately -3 V, where the drain-source resistance increases rapidly with decreasing V_{gs}, which forces an increased V_{ds}. In the pinch-off region ($V_{\mathrm{gs}} \leq$ -4 V), I_{d} is comprised of leakage, punch-through and breakdown currents. At high pinch-off voltages, the punch-through current and its temperature derivative are high due to a small depletion region. As V_{gs} decreases, the punch-through current decreases, and at sufficiently low pinch-off voltages, V_{ds} is forced to increase so a breakdown current is induced, which enables to extract $BV_{\mathrm{ds}}(V_{\mathrm{gs}})$. Thus, I_{d} is mainly set by punch-through current at high pinch-off voltages, which leads a negative $dV_{\mathrm{ds}}/dT_{\mathrm{ck}}$ as seen at e.g. -4 V in Fig. 5.2d. Furthermore, the V_{gs} below which BV_{ds} can be extracted decreases with increasing T_{ck} since the punch-through current increases significantly at higher temperatures. As a result, the BV is not obtained at all temperatures at high pinch-off voltages, and this can only be solved by increasing I_{d}. However, this risks destroying the device at low pinch-off voltages, and this trade-off is an inherent limitation of the current injection technique.

In the breakdown region ($V_{\mathrm{gs}} \leq$ -6 V), I_{d} is seen to primarily flow into the

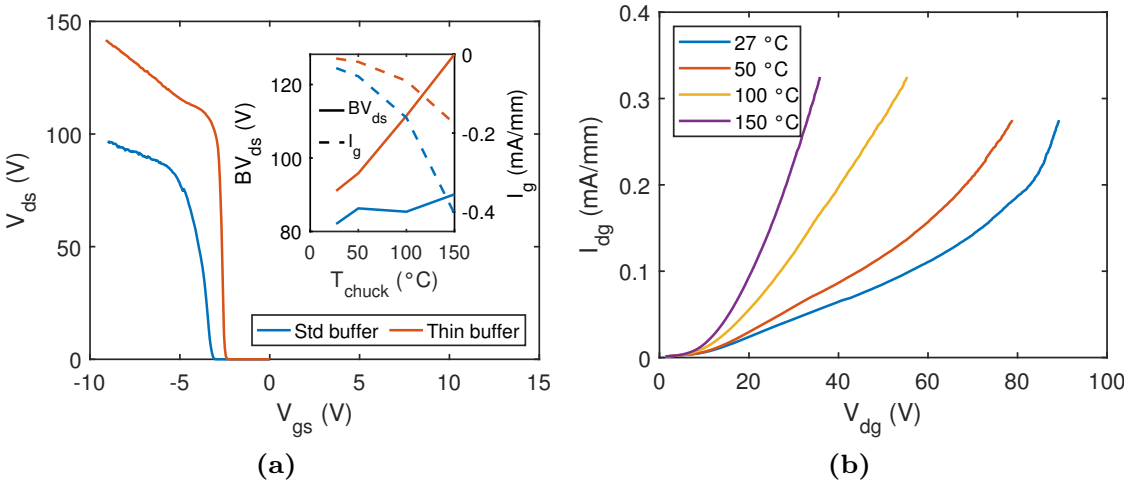


Figure 5.3: (a): gate-source voltage dependence and temperature dependence (inset) of the breakdown voltage for GaN HEMTs with a thin and standard buffer thickness. **(b)**: drain-gate current versus drain-gate voltage at different chuck temperatures.

source, indicating a breakdown in the buffer [70]. Furthermore, the temperature dependence of the BV shows a positive temperature coefficient, which suggests the breakdown is caused by impact ionization [64]. These results are in line with the TCAD simulation.

The field plate and epitaxial design are continuously developed to increase the device breakdown performance. Fig. 5.3a shows HEMTs featuring source-connected field plates and different buffer designs. The FP increases the BV by approximately 20 V for the standard device (Fig. 5.2d compared to Fig. 5.3a). Moreover, the BV of the thin buffer device is around 40 V higher compared to the standard device (Fig. 5.3a). This can be explained by the lower current leakage in the TB device (Fig. 5.2c), which inhibits avalanche current generation. The lower leakage is primarily a result of a better charge carrier confinement as well as a reduced current conduction area due to the thinner buffer. The leakage level also influence the slope of $BV_{\mathrm{ds}}(T_{\mathrm{ck}})$, shown in the inset of Fig. 5.3a. For the thin buffer device, the BV is predominately set by an avalanche current, which causes the BV to increase with temperature. In contrast, I_{d} for the standard device contains large buffer and gate leakage components, which cause the BV to decrease with temperature. This causes the slope of $BV_{\mathrm{ds}}(T_{\mathrm{ck}})$ to be smaller compared to the thin buffer, as seen in the inset of Fig. 5.3a. It can be further noted that BV_{ds} slowly increases with decreasing V_{gs}, which is a known property of a buffer breakdown [71]. The reason is that a lower V_{gs} extends the depletion region, which pushes the leakage path deeper into the buffer [70]. As a result, the drain-source resistance is increased, and a higher voltage is consequently needed to drive the same current. For the thin buffer device, the depletion region removes a larger part of the total buffer leakage, leading to a stronger dependency on V_{gs} compared to the standard device, as seen in Fig. 5.3a.

Gate Breakdown Characterization

As V_{gs} is decreased in breakdown measurements, the buffer leakage is reduced while V_{dg} increases, which eventually triggers a drain-gate breakdown. This is

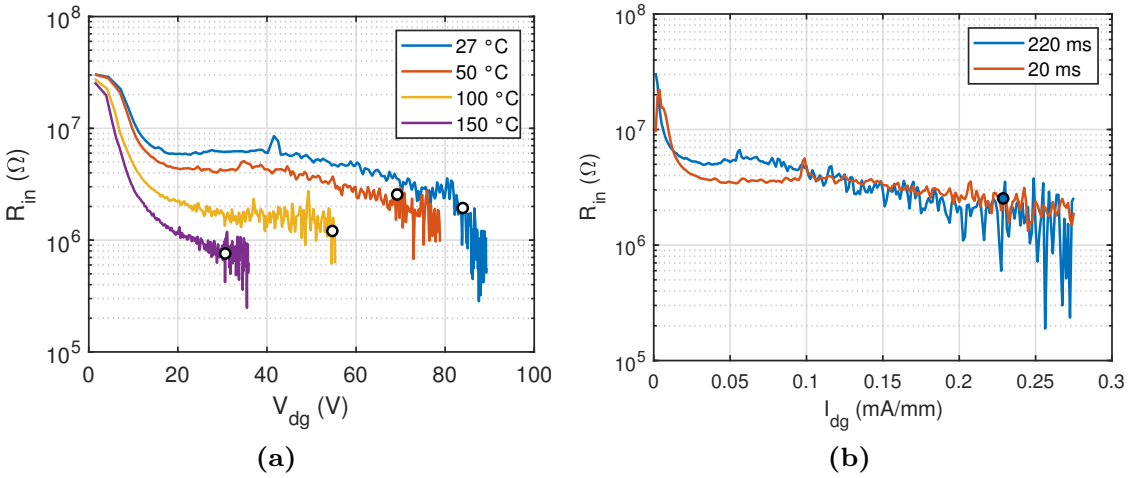


Figure 5.4: **(a)**: differential gate input resistance versus drain-gate voltage at different chuck temperatures. The circle markers indicate the first voltage, where a change in the resistance by more than 60 % occurs. **(b)**: results of differential input resistance measurements with different measurement times.

not seen in Fig. 5.3a because the gate can be destroyed by the the high injection current, which is selected to avoid leakage limitations at high pinch-off voltages. The gate breakdown was therefore studied in paper [E] using current controlled two-terminal measurements. Fig. 5.3b shows the reverse bias IV characteristics of the gate diode at different T_{ck}. Evidently, I_{d} does not increase rapidly at a discrete BV, in contrast to the three terminal characteristics. However, it was concluded that V_{dg} exhibits instability near the BV, which can be observed in the differential input resistance (R_{in}) of the gate diode, shown in Fig. 5.4a. The instability increases with V_{dg}, and the circle marker indicates a change in R_{in} by more than 60 %, which was used to define the BV. The BV is seen to decrease with increasing temperature, which indicates that the gate breakdown could be caused by the thermal runaway mechanism [66]. It was further noted that the drain-gate breakdown is very sensitive to the measurement time, which can be observed in Fig. 5.4b, where the instability in R_{in} is much larger with a longer measurement time. In conclusion, the outlined approach enables multiple non-destructive measurements, which facilitates studying the properties of the gate breakdown.

5.2 Dynamic Breakdown Measurements

In power applications, the HEMTs are often operated as switches and are driven with pulsed signals at kHz frequencies. Furthermore, in microwave applications, the HEMTs are often operated as amplifiers and are driven with modulated RF signals. Thus, the breakdown should ideally be measured under similar conditions. Despite this, dynamic breakdown characterization remains unpopular partly because it requires non-standard measurement methods. GaN-based devices put additional demands on measurement hardware due to the need of high voltage at high frequency. In paper [E], a procedure to perform pulsed breakdown measurements is proposed and a practical method for RF breakdown characterizations based on time domain measurements is suggested.

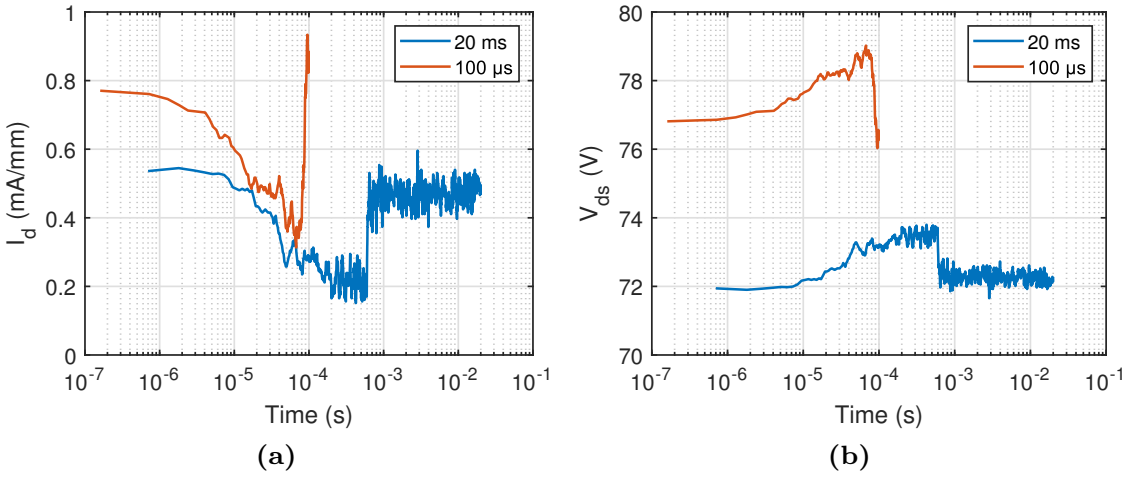


Figure 5.5: **(a)**: drain current pulse profiles obtained from pulsed breakdown measurements with two different pulse widths. **(b)** shows the corresponding drain-source voltage pulse profiles.

Pulsed Breakdown Characterization

There are different methods to perform pulsed breakdown characterizations [11], including techniques based on transmission line pulse circuits, SPDT switch pulse circuits, BJT avalanche pulse circuits, unclamped inductive switching (UIS) circuits, and dedicated off-shelf PIV systems. In transmission line pulse circuits, the line behaves like an ideal square-wave voltage pulse generator [72], where the amplitude is controlled by the charging voltage and the pulse width is set by the length of the line. This allows generating sub-microsecond pulses with short rise time, which was used in e.g. [73] to study the dependence of the breakdown on the slew rate of the stimulus. In a UIS test, the device is first turned on to charge a loop inductor on the output, and when the device is turned off the energy stored in the inductor triggers a high voltage overshoot. The amplitude and pulse period of this resonance can be tuned by the inductor value, charging time, and an additional capacitor in parallel [62]. This technique was used in [60] to measure the breakdown in GaN power HEMTs with different pulse widths, which revealed a dynamic behavior in the BV. In paper [E], pulsed breakdown measurements were performed using a dedicated PIV system, allowing flexible control of the timing and amplitudes of the pulses. The pulsed V_{ds} amplitude was incremented while the HEMT was biased in the pinch-off region, and a pulse profile measurement was performed at each amplitude. Fig. 5.5a shows the I_{d} pulse profiles obtained from pulsed breakdown measurements using two different pulse widths. Initially, a decrease of the current is seen due to the charging of the device output capacitor. The current subsequently becomes temporarily constant before a rapid increase is seen, which was used as an indicator that the BV is reached. To study the effects of the timing on the breakdown, pulse widths ranging from 10 µs to 20 ms were evaluated. Fig. 5.5b shows the V_{ds} corresponding to I_{d} in Fig. 5.5a, and it can be seen that the BV is higher for a shorter pulse width.

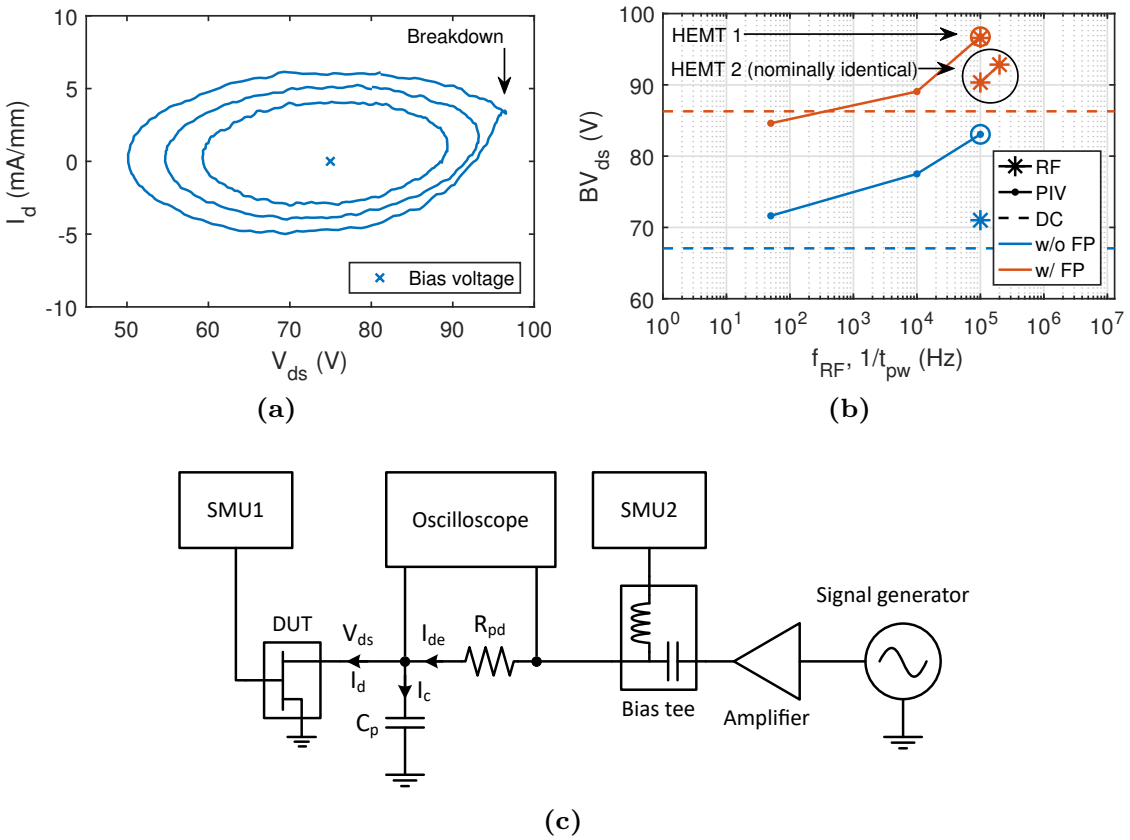


Figure 5.6: **(a)**: time-varying drain current versus drain-source voltage for different RF amplitudes. **(b)**: comparisons of static and dynamic drain-source breakdown voltages of devices with and without FP. The arrows show RF breakdown voltages of two nominally identical HEMTs. The circle markers indicate that the measurement reached the maximum voltage limit set for the sweep and the breakdown voltage was not detected. t_{pw} is the pulse width in the PIV measurement and f_{RF} is the CW frequency in the RF measurement. **(c)**: RF breakdown measurement setup.

RF Breakdown Characterization & Breakdown Comparisons

The value of RF breakdown characterization has been discussed at an early stage [74]. Despite this, there is a lack of measurement-based studies of the RF breakdown characteristics of microwave GaN HEMTs. However, the RF breakdown has been the subject of a number of studies for GaAs FETs, including [61] where the RF breakdown voltage is shown to be higher than the DC equivalent, and [75], where high breakdown currents are observed to flow for a short time. In these cases, the RF breakdown characterization is performed using a special waveform probing technique [61] and a nonlinear network measurement system [75]. To measure the off-state RF breakdown of GaN HEMTs, the characterization needs to be performed with a large RF swing on the drain side under pinch-off conditions. In paper [E], RF breakdown measurements were performed using the custom made setup in Fig. 5.6c. The setup allows for large signal injections on the drain, and it is based on an oscilloscope. This enables direct voltage waveform measurements as well as current waveform measurements via the voltage over R_{pd} in Fig. 5.6c. The value of R_{pd} needs to be chosen based on a trade-off between impedance mismatch, adequate protection, and current resolution. The voltage probe and the cable connected to the drain add a parasitic capacitance (approximately

10 pF), which causes a reactive current that needs to be de-embedded from the measured I_{d}. Furthermore, to maintain the pinch-off condition, the drain bias voltage needs to be set higher than the amplitude of the RF signal.

In paper [E], measurements were performed at 100 and 200 kHz on GaN HEMTs with and without source-connected field plates. The breakdown voltage is determined by incrementing the RF power while monitoring the I_{d} versus V_{ds} waveform, and stopping the amplitude sweep when the signs of breakdown are detected. Fig. 5.6a shows the time-varying I_{d} versus V_{ds}, where the waveforms correspond to the lowest, middle, and maximum amplitude levels in a sweep. The waveform exhibits an elliptic shape (up to half the amplitude sweep) due to a reactive current component in I_{d}. At the maximum amplitude, the current is no longer completely sinusoidal since it consists of a breakdown current in addition to leakage and punch-through currents. As a result, a local current peak tends to form at $V_{\mathrm{ds,max}}$, and a voltage drop is seen (due to R_{pd}) at the lower part around $V_{\mathrm{ds,max}}$.

Comparisons of BV_{ds} values obtained from DC, PIV, and RF breakdown measurements on different devices are shown in Fig. 5.6b, where the pulsed BV_{ds} is shown versus the inverse of the pulse width, the RF BV_{ds} is shown versus CW frequency, and the DC values are shown as dashed horizontal lines. The RF BV_{ds} at 100 kHz is presented for two nominally identical devices (HEMT 1 & 2), showing a variation of 7 V due to non-uniformities between devices. Despite the variation, an overall trend can be inferred that BV_{ds} increases with increasing frequency, and the RF/PIV BV_{ds} can be up to 10 V higher than the DC breakdown voltage, as seen for the device with FP. The cause of the static-dynamic BV_{ds} difference is discussed in paper [E], and it is mainly attributed to acceptor-like buffer traps [60] introduced by the Fe doping in the buffer.

However, it is clear that the comparisons in Fig. 5.6b suffer from the BV variation between nominally identical HEMTs, which is on the same order as the static-dynamic BV differences. Breakdown measurements are performed on multiple nominally identical devices due to the limitations and trade-offs made for the protection, as well as the inherent lack of avalanche capability in GaN HEMTs [9]. In the case of the PIV measurement, R_{pd} increases the pulse rise time, and it is not obvious how R_{pd} should be determined when the breakdown occurs at voltages high above the DC breakdown voltage. Ideally, the breakdown characterizations should be performed on the same device up to GHz frequencies (RF measurement). However, the necessary trade-offs for the protection (e.g. reflections) increase the chances of a catastrophic device failure at higher frequency. A possible solution could be to add a large inductance in series on the drain to limit the maximum possible current increase at the BV. This would also allow to reduce the series resistance. Furthermore, instead of a CW measurement, a transient measurement could be performed with a finite signal length, which possibly would allow to detect the breakdown and stop the measurement at an earlier stage. In this scenario, the frequency limiting factors are the bandwidth of the voltage probes and the self-resonance frequency of the inductor.

Chapter 6

Conclusions and Future Work

Measurement methodology is a crucial subject to study because of the need to obtain reliable information about various properties of components. New semiconductor technologies create new measurement-challenges, and methods must therefore continuously be developed and adapted. The demands of existing applications require efforts to improve power density, efficiency, and linearity coupled with efforts to improve the cooling of GaN devices. In this context, characterization techniques play a key role since measurements are used to examine the effects of alterations to the device design. It is therefore imperative that methods are available that can capture the multifaceted characteristics of GaN devices accurately. The presented methods in this thesis provide solutions to problems faced in the characterization of GaN-based devices and circuits.

The method in paper [A] enables to obtain the I_{ds}-V_{ds} characteristics of devices with and without trap-related memory effects, enabling to analyze trapping and heating effects separately. This could facilitate the extraction of large signal models since these are generally not designed to model complex trap-related memory effects in the IV data. The proposed method makes it possible to extract trap-related model parameters separately using IV data with and without memory effects. The usefulness of this method in the extraction of small signal models from multi-bias S-parameters is also of interest to explore. The method could also be useful in PIV measurements, where it would ensure only the effects of the quiescent pulse settings are studied in e.g. current collapse measurements. Future studies could focus on these ideas, as well as evaluating the method on a broader range of GaN HEMTs.

The method in paper [B] addresses the problem of trap-distortion in electric-based thermal evaluation of semiconductor technologies. Verifying thermal evaluations and comparing results obtained using different temperature measurement methods is not trivial. The proposed method contains extraction steps that can be used to validate the result, removing the trap-related uncertainty, which facilitates comparisons of different devices. This can be utilized in e.g. the evaluation of packages, where the trapping characteristics of enclosed devices can change due to piezoelectric strain induced on their surface.

Paper [C], introduces a method to electrically characterize the lateral heat

spread. The used sensor is suitable for integration into GaN MMICs, and the method enables to measure lateral thermal coupling in MMICs using commonly available lab equipment. The evaluation of the methodology shows that thermal coupling increases with operating temperature, and the number of time constants involved in the coupling transient decreases with increasing separation. Thus, lowering the overall temperature of the die helps to disperse heat from hot-spots, and coupling over large distances is mainly determined by the substrate, as seen in [b]. The need to measure the heat coupling in circuits will presumably increase due to the miniaturization of circuits at high frequencies. Additional possibilities enabled by this method are demonstrated in [b], [c], and [54]. Future additional work could be to connect the time constants to physical properties of the material layers in the device. Furthermore, the lateral thermal coupling in different types of packages is also of interest to study and compare.

The biasing technique in paper [D] shows that a constant gain versus increasing temperature can be achieved using the V_{gs} and V_{ds} dependencies of the RF performance. The compensation biasing also significantly increases OIP3, which can be utilized at high input powers to minimize the nonlinear distortion in the circuit. This can improve the signal-to-noise and distortion ratio, as demonstrated in paper [a]. Although a dynamic drain bias is complex to implement in real applications, it is necessary in order to compensate for thermal degradation of e.g. the gain. However, the performance loss compensation generally comes at the cost of increased power dissipation. Future work could include real time tests of the suggested algorithm as well as simulations where the power dissipation is regulated.

Paper [E] highlights many challenges with GaN HEMT breakdown measurements. It is clear that the device's leakage characteristics need to be considered in DC breakdown measurements to ensure reliable BV estimates are obtained. Furthermore, the proposed methods for RF and pulsed breakdown characterization enable to measure the breakdown under more application-relevant conditions, and the waveform analysis is key to determine the BV in these measurements. The comparisons show an increasing breakdown voltage with increasing frequency, which provides a certain voltage margin when amplifiers are designed using the DC BV. Ideally, the RF breakdown measurement method should allow for non-destructive measurements over a wide frequency range. This requires further improvements of the protection circuitry and adjustments to the proposed setup, as discussed in section 5.2. Furthermore, the dynamic BV characteristic could be different if the device breakdown is driven by a breakdown of the gate. Experiments at higher temperatures are therefore of interest since the gate BV is seen to exhibit a negative temperature coefficient.

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