Evaluation of the Self-Interference Cancellation Limits of Full-Duplex Antenna Arrays Using Zynq UltraScale+ RF System-On-Chip Board

Evaluation of the Self-Interference Cancellation Limits of Full-Duplex Antenna Arrays Using Zynq UltraScale+ RF System-On-Chip Board

1st Mustafa Ayebe
Electrical Engineering Department (E2)
Chalmers University of Technology
Göteborg, Sweden
ayebe@chalmers.se

2th Rob Maaskant
Electrical Engineering Department (E2)
Chalmers University of Technology
Göteborg, Sweden
rob.maaskant@chalmers.se

3nd Johan Malmström
Surveillance
SAAB
Järfälla, Sweden
johan.malmstrom@saabgroup.com

4rd Sten E. Gunnarson
Surveillance
SAAB
Järfälla, Sweden
sten.gunnarsson@saabgroup.com

5th Henrik Holter
Hardware Research
Ericsson AB
Stockholm, Sweden
henrik.holter@ericsson.com

6th Marianna Ivashina
Electrical Engineering Department (E2)
Chalmers University of Technology
Göteborg, Sweden
marianna.ivashina@chalmers.se

***Abstract*—We present a procedure and experimental setup using a state-of-the-art commercial RF system-on-chip (RFSoC) to evaluate self-interference cancellation in full-duplex array antennas. Our focus is on assessing the capacity of the system's interference cancellation abilities, namely how effectively the technology can perform nulling in the presence of hardware imperfections and practical testing conditions. This step is crucial for evaluating complex array transceivers that comprise multiple non-linear components, such as power- and low-noise amplifiers, and that require advanced beamforming strategies to maximize antenna gain, effective radiated power, receiving sensitivity, etc, while canceling self-interference. Our initial experimental setup includes a 1×5 Vivaldi antenna array operating in the $3-6$ GHz band, connected to the digital transceiver system on the RFSoC board. We introduce a calibration procedure to compensate for DAC-induced errors and synchronize the transmit channels during measurements. This calibration procedure shows a cancellation limit of up to 63 dB.**

***Index Terms*—In-band full-duplex, Self-Interference, Calibration, RFSoC**

I. Introduction

In-band full-duplex (IBFD) architectures enable simultaneous transmission and reception of signals at the same frequency, representing a significant advancement in wireless communications. This approach has the potential to theoretically double spectral efficiency and increase the data rate of wireless communication systems as well as improve sensitivity in e.g., radar and Electronic Warfare applications [1].

However, there are several challenges in the practical implementation of cost-effective and compact full-duplex transceivers. The most significant obstacle is known as self-interference (SI), which arises because the transmitter and receiver either share the same antennas or have closely spaced antennas [2]. Employing digital domain methods in multiple-input multiple-output configurations can mitigate SI and prevent saturation of receiver (RX) low noise amplifiers. Sufficient isolation between distinct transmitter (TX) and RX antenna arrays, even in closely spaced antenna arrays, enables simultaneous transmission and reception within the same frequency band for an IBFD system. For instance, in [3], a TX beamforming technique was introduced, which finds the TX excitation vector maximizing the realized array antenna gain in a specific direction while guaranteeing the per-element or total coupled TX-to-RX self-interference power below a maximum threshold level.

To implement and ultimately demonstrate the beamforming method suggested in [3], we employ the Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit. This evaluation kit combines analog-to-digital converters (ADCs), digital-to-analog converters (DACs), programmable logic, and digital signal processing (DSP) cores into one chip. This integration enables the creation of highly flexible and configurable software-defined radio systems capable of performing real-time RF processing tasks [4]. Using this board, we can execute complex algorithms for self-interference mitigation and synchronization, allowing us to examine the concept of full-duplex communication systems. This paper focuses on evaluating the RFSoC board in its inherent capability to achieve SI cancellation, which is a more extreme type of beamforming than the one proposed in [3], but a useful test case to examine the capabilities and limitations of this board.

In principle, achieving perfect cancellation of SI in the receiver is theoretically possible when the non-wanted leakage between the transmitting and receiving paths is perfectly known by the RFSoC. However, practical limitations arise if the channel is non-stationary as in most sensing and communication applications. Furthermore, non-linear DAC effects of the transmitter components can complicate channel

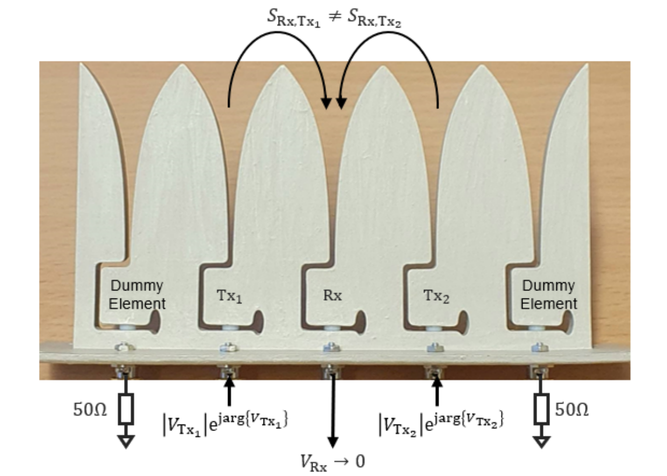


Fig. 1. Antenna array and excitation configuration used for evaluating the SI cancellation performance with the RFSoC.

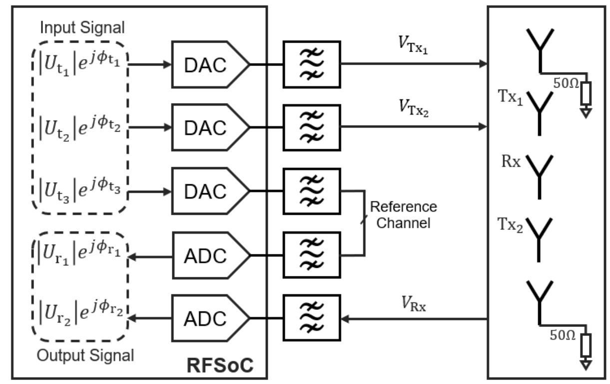


Fig. 2. Block diagram of transceiver and antenna array used for signal calibration and digital beamforming.

estimation [5], [6]. On-the-fly phase and amplitude calibration is therefore essential for effectively using digital beamforming, in particular the ability to cancel SI.

The rest of the paper is organized as follows: Section II presents the SI cancellation configuration, whereas Section III formulates the calibration process. Section IV presents the experimental setup and measurement results, followed by conclusions in Section V.

II. SI Cancellation Configuration

In [5], a near-field cancellation duplexing system is demonstrated, employing synchronized transceivers with symmetrically arranged monopole antenna elements and a digital backend for phase and amplitude control. By adjusting the excitation weights across multiple transmit elements, the coupled interference at the receiver elements provides up to 50 dB additional isolation compared to the largest TX-RX coupling.

Building upon the principles proposed in [5], our objective is to showcase a 1×5 Vivaldi antenna array configuration [*cf.* Fig. 1] in conjunction with digital transceivers implemented on the RFSoC. This array is fabricated using 3D-printed materials and coated with a conductive layer of silver [7]. Operating within the frequency range of 3 to 6 GHz, the central element functions as the receiving antenna, whereas the two adjacent elements serve as transmitting antennas, as indicated in Fig. 1. The edge (dummy) elements are matched, i.e. terminated with a 50 Ω load.

Here, the time-domain Continuous Waveforms (CW) of the two transmitting elements can be manipulated in phase and magnitude to minimize the coupling signal at the receiving antenna, in terms of the frequency-domain incident ($V_{\mathrm{Tx}_{1,2}}$) and reflected (V_{Rx}) complex voltage wave amplitudes, i.e.,

$$V_{\mathrm{Rx}} = S_{\mathrm{Rx,Tx_1}} V_{\mathrm{Tx_1}} + S_{\mathrm{Rx,Tx_2}} V_{\mathrm{Tx_2}} \to 0 \tag{1}$$

III. Calibration and Nulling Procedure

Regarding Eq. (1), one can achieve perfect nulling of the received signal V_{Rx} if both the channel paths $S_{\mathrm{Rx,Tx_1}}$ and $S_{\mathrm{Rx,Tx_2}}$ are perfectly known and if $V_{\mathrm{Tx_1}}$ and $V_{\mathrm{Tx_2}}$ can be realized without errors. Amplitude and phase errors are introduced by DACs, filters, cables, and antenna coupling. We will compensate for these errors using a calibration procedure as shown by the block diagram in Fig. 2. To this end, three digital CW signals are converted into analog signals using phase-synchronized DACs and subsequently filtered through bandpass filters (BPFs). One of these signals ($U_{\mathrm{t_3}} = |U_{\mathrm{t_3}}|e^{j\phi_{\mathrm{t_3}}}$) is used as a reference signal as detailed below, while the remaining two ($U_{\mathrm{t_1}}, U_{\mathrm{t_2}}$) are exciting the two transmitting antennas. The received signal V_{Rx} also passes through a BPF and an ADC to yield $U_{\mathrm{r_2}}$ in the digital domain. Additionally, the received reference signal bypasses the antenna and is directly connected to a BPF and an ADC to result in $U_{\mathrm{r_1}}$.

When both Tx_1 and the reference channel are equally excited, i.e., $U_{\mathrm{t_1}} = U_{\mathrm{t_3}}$, while $U_{\mathrm{t_2}} = 0$, the calibrated signal for Tx_1 is expressed as:

$$C_1 = \left.\frac{U_{\mathrm{r_2}}}{U_{\mathrm{r_1}}}\right|_{U_{\mathrm{t_1}} = U_{\mathrm{t_3}}, U_{\mathrm{t_2}} = 0} \tag{2}$$

Similarly, when Tx_2 and the reference channel are excited,

$$C_2 = \left.\frac{U_{\mathrm{r_2}}}{U_{\mathrm{r_1}}}\right|_{U_{\mathrm{t_2}} = U_{\mathrm{t_3}}, U_{\mathrm{t_1}} = 0} \tag{3}$$

Therefore, C_1 and C_2 are the amplitudes and phases of the two transmitting signals relative to the reference signal at the output. SI cancellation is now achieved by choosing

$$U_{\mathrm{t_1}} = C_1 e^{j0} \tag{4a}$$
$$U_{\mathrm{t_2}} = C_2 e^{j\pi} \tag{4b}$$

IV. Experimental Setup and Measurement Results

A. Experimental Setup

The experimental setup utilized for validating the proposed methodology is illustrated in Fig. 3, employing the Zynq UltraScale+ RFSoC ZCU216 Evaluation Kit, one of the latest software-defined radio boards [4]. The Xilinx chip incorporates an array of 16 DACs (14-bit) and 16 ADCs (14-bit), with a maximum supported DAC sampling rate of 9.85 GSPS

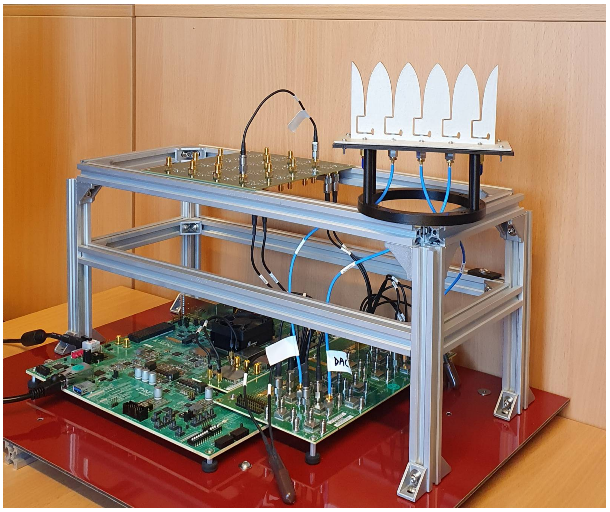


Fig. 3. Experimental setup in an office environment.

and 2.5 GSPS for the ADCs. All 16 DACs (and 16 ADCs) are divided into four tiles, each comprising 4 DACs (4 ADCs) and one phased locked loop.

In our work, the MATLAB environment is used to control the board and to generate the transmitting time-domain waveforms at 3 and 3.3 GHz, similar to Xilinx's System Generator design tool. Additionally, the Fast Fourier Transform is used to post-process the received time-domain data for frequency-domain presentation. The hardware setup incorporates baluns, each with a frequency range from 3 to 6 GHz.

B. Measurement Results

The transmitted signals cannot exceed 1 V in magnitude, hence, we need to set either U_{t_1} or U_{t_2} equal to 1 V, depending upon which one is larger, to maximize power excitation. That is, if $C_1 \geq C_2$, then we can calculate Eq. (4) inversely proportional to C_1 to obtain

$$U_{t_1} = \frac{C_2}{C_1} e^{j\pi} \tag{5a}$$

$$U_{t_2} = 1 \tag{5b}$$

else, we recalculate Eq. (4) inversely proportional to $C_2 e^{j\pi}$ to get

$$U_{t_1} = 1 \tag{6a}$$

$$U_{t_2} = \frac{C_1}{C_2} e^{-j\pi} \tag{6b}$$

Fig. 4 illustrates the interference that is received at the receiving port (V_{Rx}) from the strongest coupled transmitting antenna channel, emitting a CW tone with an amplitude of 1 V and a phase of 0° at 3 and 3.3 GHz. The observed spurious emissions at other frequencies are generated by the data conversion process, primarily due to spurious distortion caused by non-linearities in the data converter. After executing the calibration script only once, the isolation measurement is repeated 200 times. The additional average isolation achieved

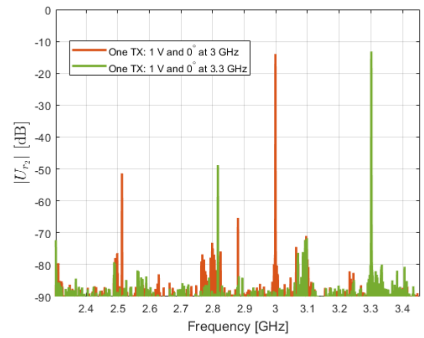


Fig. 4. The central receiver element measured signal from a single adjacent transmitter with 1 V amplitude and 0° phase.

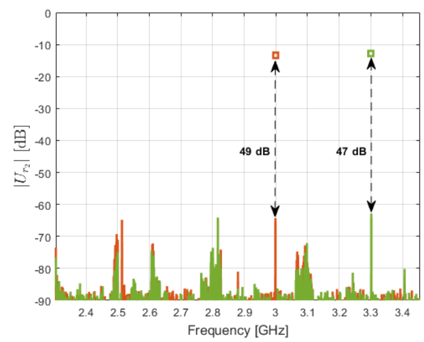
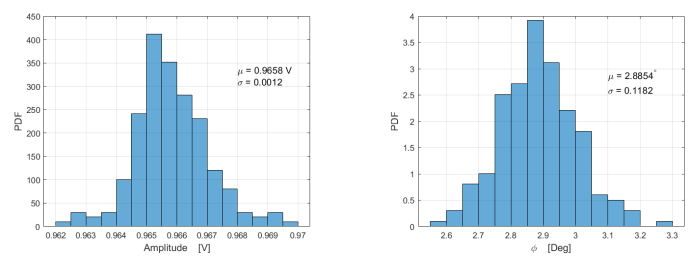


Fig. 5. By employing the calibration for cancellation at 3 and 3.3 GHz, the interference is mitigated.



(a) (b)

Fig. 6. A pdf function of: (a) $|U_{t_1}|$; (b) ϕ_{t_1} at 3 GHz

over these 200 measurements is $47 - 49$ dB, as depicted in Fig. 5.

To further improve isolation, enhancing the estimation accuracy of C_1 and C_2 is critical. This is achieved by re-evaluating Eq. (2) and (3) also for 200 calibration measurements and use the mean-value estimations $\widehat{C}_1$ and $\widehat{C}_2$ in (5) and (6) instead.

For instance, Fig. 6 illustrates the probability density function (pdf) of $|U_{t_1}|$ and ϕ_{t_1} for Eq. (6) at 3 GHz. In this example, the standard deviations of amplitude and phase are 0.0012 V and $0.1182°$, respectively.

Fig. 7 presents the coupled interference signal $|U_{t_2}|$ into the central receiver element from two transmitting antennas when operating in SI cancellation mode using estimated values for $\widehat{C}_1$ and $\widehat{C}_2$. A significant isolation improvement up to 63 and

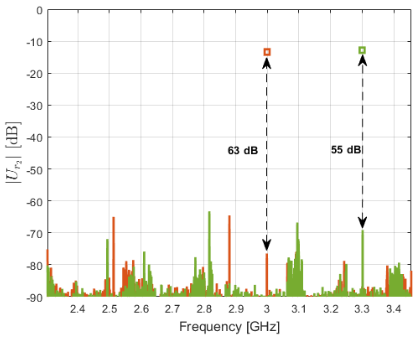


Fig. 7. By employing the expected amplitude and phase values for cancellation at 3 and 3.3 GHz, the interference is effectively mitigated.

55 dB is seen at 3 and 3.3 GHz, respectively.

V. Conclusion

Self-interference in full-duplex array antennas can be effectively analyzed using a commercially available state-of-the-art RFSoC board. This analysis requires an accurate calibration procedure to compensate for the hardware-induced errors between multiple channels on the board and to synchronize transmit channels during measurements. We have proposed a calibration procedure that uses one of the RFSoC channels as as a Tx-Rx reference channel and that is combined with a nulling algorithm to evaluate self-interference. This procedure has been demonstrated through a small-scale experimental setup employing a linear array of five strongly coupled tapered slot (Vivaldi) antenna elements connected to the RFSoC digital transceiver. The achieved self-interference cancellation (measured by the TX-RX coupling level) has been improved from $10-12$ dB to 63 dB, i.e. by 50 dB, by utilizing a calibrated pair of transmit channels.

Future work will focus on characterizing large-scale full-duplex array antenna systems with integrated active electronic components and evaluating advanced beamforming algorithms that trade-off self-interference with other critical metrics such as effective isotropic power, gain, etc.

Acknowledgment

This research has been carried out in Vinnova Competence Centre WiTECH (Wireless Technologies at Chalmers) in the DIGIARRAY project financed by Ericsson, SAAB, Satcube, and Chalmers.

References

[1] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan and R. Wichman, ”In-Band Full-Duplex Wireless: Challenges and Opportunities,” in IEEE Journal on Selected Areas in Communications, vol. 32, no. 9, pp. 1637-1652, Sept. 2014.

[2] K. E. Kolodziej, B. T. Perry and J. S. Herd, ”In-Band Full-Duplex Technology: Techniques and Systems Survey,” in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, pp. 3025-3041, July 2019.

[3] M. Ayebe, J. Malmström, S.E. Gunnarson, H. Holter, M. Ivashina, C. Bencivenni, and R. Maaskant, ”Systematic Self-Interference Mitigation In Full Duplex Antenna Arrays Via Transmit Beamforming,” 2023 International Conference on Electromagnetics in Advanced Applications (ICEAA), Venice, Italy, 2023, pp. 158-163, doi: 10.1109/ICEAA57318.2023.10297706.

[4] AMD Xilinx, “Zynq UltraScale+ RFSoC RF Data Converter v2.6 Gen 1/2/3/DFE”, October 21, 2022. [Online]. Available: https://docs.amd.com/r/en-US/pg269-rf-data-converter

[5] T. Snow, C. Fulton and W. J. Chappell, ”Transmit–Receive Duplexing Using Digital Beamforming System to Cancel Self-Interference,” in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 12, pp. 3494-3503, Dec. 2011, doi: 10.1109/TMTT.2011.2172625.

[6] J. I. Choi, M. Jain, K. Srinivasan, P. Levis, and S. Katti, “Achieving single channel, full duplex wireless communication,” in Proc. Mobile Computing Wireless Commun. Int. Conf., Sep. 2010, pp. 20–24.

[7] M. Ayebe, R. Maaskant, J. Malmström, S.E. Gunnarson, H. Holter, and M. Ivashina ”3D-printed Silver-coated Vivaldi Array With Integrated Coaxial Probe Feeding,” 2024 IEEE USNC-URSI Radio Science Meeting, Florence, Italy, 2024.