Thesis for The Degree of Licentiate of Engineering

Efficient MMIC Power Amplifier Implementations for Applications Beyond 100 GHz

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To my family

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Abstract

The rapid increase in worldwide wireless data traffic underscores the need for advancements in wireless communication infrastructure. Millimeter Wave (mm-wave) frequencies provide abundant and less crowded spectrum resources for these networks. However, designing energy-efficient Power Amplifiers (PAs) at these frequencies remains a challenge due to increased power losses and the performance limitations of transistors.

In this thesis, we present the design and implementation of energy-efficient PAs for mm-wave frequencies using a commercial 0.1 µm GaAs pHEMT process, specifically targeting telecommunications bands between 100 GHz to 114 GHz. Starting from fundamental PA design principles, various power-combining techniques were investigated. A balanced PA demonstrating competitive performance relative to state-of-the-art designs was developed, achieving 24.1 dBm saturated output power, 18.2 dB gain, and 11.9 % power-added efficiency. Additionally, a non-uniform distributed power amplifier employing multi-branch combining was designed, exhibiting a small-signal gain exceeding 20 dB from 107 GHz to beyond 116 GHz.

To further enhance performance, a dynamic gate biasing technique was introduced and initially validated on an 80 GHz PA, improving average energy efficiency at the spectral emission mask limit from 4.9 % to 7.4 % and increasing average RF output power by 1.7 dBm, surpassing traditional digital pre-distortion techniques. A novel integrated dynamic gate bias circuit was subsequently implemented in a single Monolithic Microwave Integrated Circuit (MMIC), dynamically adjusting gate voltage based on instantaneous input power. Quasi-static simulations confirmed significant improvements, increasing maximum RF output power from 19.14 dBm to 20.81 dBm for a 4QAM signal and improving energy efficiency from 10.2 % to 12.5 %. These findings demonstrate the effectiveness of dynamic gate biasing in optimizing efficiency and output power in advanced mm-wave PAs.

Overall, this work demonstrates the potential of MMIC implementations using 0.1 µm GaAs pHEMT technology for energy-efficient PA design in mm-wave applications. These findings support the development of high-performance PAs for modern wireless systems, particularly those operating with signals that exhibit a large dynamic range.

Keywords Millimeter-wave, Power Amplifier, GaAs, Power Combining, Gate Modulation, Energy Efficiency,

List of Publications

Appended publications

This thesis is based on the following publications:

[**Paper A**] **G. Kaval**, G. Lasser, M. Gavell, C. Fager, *"A Balanced 100-114 GHz Millimeter-Wave GaAs MMIC Power Amplifier with High Gain"* *Submitted to IEEE Microwave and Wireless Technology Letters.*

[**Paper B**] **G. Kaval**, G. Lasser, M. Gavell, C. Fager, *"A 100-114 GHz GaAs MMIC Power Amplifier With Fully Integrated Dynamic Gate Bias Control for Linearization and Efficiency Enhancement"*
19th European Microwave Integrated Circuits Conference (EuMIC), Paris, France, 2024.

[**Paper C**] **G. Kaval**, G. Lasser, M. Gavell, C. Fager, *"Enhancement of Power-Added Efficiency in GaAs Power Amplifiers by Dynamic Gate Biasing"*
International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), Aveiro, Portugal, 2023.

[**Paper D**] **G. Kaval**, G. Lasser, M. Gavell, C. Fager, *"Multi-Stage Gate Modulation of E-Band MMIC Power Amplifier for Efficiency Improvement"* *International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), Cardiff, United Kingdom, 2022.*

Other publications

The following publications were published during my PhD studies, or are currently in submission/under revision. However, they are not appended to this thesis, due to contents overlapping that of appended publications or contents not related to the thesis.

[**a**] K. Ryynänen, K. Stadius, J. Bergman, **G. Kaval**, G. Lasser, V. Vassilev, C. Fager, J. Ryynänen, *"A Wideband 60–100 GHz GaAs Low-Noise Amplifier as a Pre-Amplifier to a CMOS Receiver"*
31st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Nancy, France, 2024.

Abbreviations

AWG Arbitrary Waveform Generator.
BEOL Back End of Line.
CMOS Complementary Metal–Oxide–Semiconductor.
CW Continuous Wave.
DPD Digital Predistortion.
DUT Device Under Test.
EM Electromagnetics.
FWA Fixed Wireless Access.
HBT Hetero-junction Bipolar Transistor.
HEMT High Electron Mobility Transistor.
IQ In-phase Quadrature.
LO Local Oscillator.
MAG Maximum Available Gain.
mHEMT Metamorphic High Electron Mobility Transistor.
mm-Wave Millimeter Wave.
MMIC Monolithic Microwave Integrated Circuit.
NDPA Nonuniform Distributed Power Amplifier.
PA Power Amplifier.
PAE Power Added Efficiency.
PAPR Peak-to-Average Power Ratio.
PET Power Envelope Tracking.
pHEMT Pseudomorphic High Electron Mobility Transistor.
QAM Quadrature Amplitude Modulation.
RRC Root Raised Cosine.
SLC Single-Layer Capacitor.
SMD Surface-Mount Device.
SNR Signal to Noise Ratio.
VNA Vector Network Analyzer.

Contents

Chapter 1

Introduction

1.1 Motivation

The volume of data generated, captured, copied, or consumed in 2023 is estimated to be 123 ZB, with projections indicating it will reach 394 ZB by 2028 [1]. Companies worldwide provide a wide range of services by utilizing, processing, storing, or leveraging this data to generate new data. Examples of such services include remote computing, cloud storage, smart wearable devices, shared mobility solutions, and smart home and city applications—all of which are enabled by—and dependent on—the effective circulation of data. As a consequence, global mobile data traffic has experienced rapid growth in parallel with the increasing volume of worldwide data creation, as illustrated in Figure 1.1. Mobile data traffic, including Fixed Wireless Access (FWA) traffic, has doubled from 2018 to 2024, reaching 165.7 EB/month. This figure is projected to double again by 2028, reaching 345.7 EB/month [2]. Moreover, as of 2024, the number of internet users has reached 5.5 billion, accounting for 68% of the global population [3].

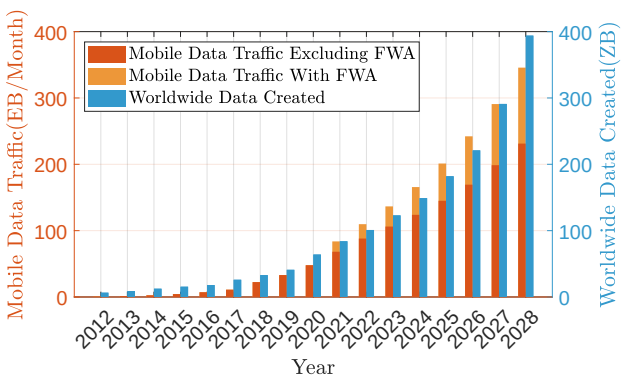


Figure 1.1: The volume of data generated, captured, copied, or consumed [1], alongside total global mobile data traffic with and without FWA traffic [2].

As a result of the growing global mobile data traffic, increasingly stringent data rate and capacity requirements for future telecommunications infrastructures are anticipated [4]. The use of mm-wave frequencies (30 GHz to 300 GHz) presents several advantages for both backhaul transport links and access points (base stations) [5–7] to address these demands. First, this frequency range offers an abundance of relatively underutilized, wideband frequency resources [8]. Additionally, the short wavelengths of mm-wave frequencies enable the development of compact components such as circuits and antennas, facilitating the design of highly directive and steerable beamforming antennas [9]. Although atmospheric attenuation increases with frequency which limits the maximum transmission range, it provides an advantage when combined with directed beams for point-to-point applications by reducing interference between transceivers and enabling efficient frequency reuse [10].

As shown in Shannon's equation in (1.1), the capacity of a network is limited by the Signal to Noise Ratio (SNR), such that the maximum link capacity (C) in bits per second is given by:

$$C = \mathrm{BW} \cdot \log_2(1 + \mathrm{SNR}), \tag{1.1}$$

where BW is the bandwidth of the channel in hertz [11]. For a generic wireless telecommunications system, illustrated in Figure 1.2 the expression for SNR can be written as below following the Friis' equation [12]:

$$\mathrm{SNR} = \frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}}} = \frac{P_{\mathrm{TX}} \cdot G_{\mathrm{TX}} \cdot G_{\mathrm{RX}}}{k_{\mathrm{B}}T \cdot F_{\mathrm{RX}} \cdot \mathrm{BW}_{\mathrm{RF}}} \cdot \left(\frac{c}{4\pi d f_0}\right)^2 \tag{1.2}$$

where P_{TX} is the RF transmit power, G_{TX} and G_{RX} are the antenna gains of the transmitter and receiver, respectively. $k_{\mathrm{B}}T$ is the product of Boltzmann's constant and the temperature, F_{RX} is the noise factor of the receiver, and $\mathrm{BW}_{\mathrm{RF}}$ is the RF bandwidth of the receiver. c is the speed of light, d is the distance between the transmitter and receiver antennas, and f_0 is the center frequency. The combination of (1.1) and (1.2) shows that to achieve high-capacity and long coverage range wireless communication links at high RF frequencies, possible improvements in system components include increasing transmit power, using antennas with higher gain, or employing a receiver with a lower noise factor.

In this thesis, we focus on PAs, which generate the RF power for transmission. RF power generation is achieved through the consumption of DC power, making PAs the most energy-consuming components in a transmitter. Designing energy-efficient PAs that meet system requirements presents numerous challenges, which are summarized in the following section.

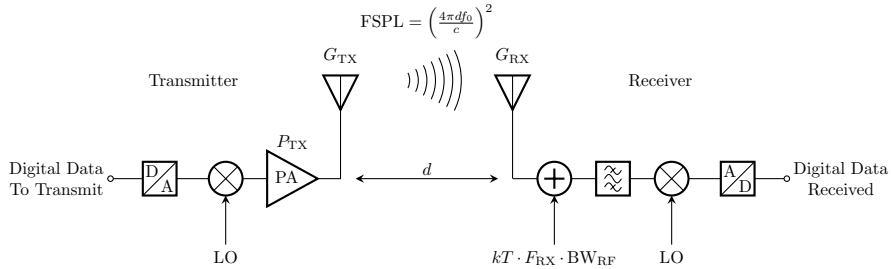


Figure 1.2: A generic wireless telecommunication system.

1.2 Challenges of Energy-Efficient mm-wave PAs

PAs designed for mm-wave frequencies are commonly fabricated using MMIC technologies, where transistors and passive components are integrated onto a single semiconductor substrate. However, as the operating frequency increases, transistors exhibit reduced gain, RF output power, and energy efficiency. Additionally, their parasitic components—such as input and output capacitances—become more significant with frequency, further complicating the design of energy-efficient PAs with high RF output power.

Semiconductor technologies with a transition frequency (f_T) capable of providing high gain at mm-wave frequencies require devices with small physical dimensions, yielding reduced parasitic capacitive effects. However, this also lowers the breakdown voltage and such the operational voltage, which limits maximum RF power and necessitates power combining of multiple transistors [13]. Additionally, passive components—such as interconnections, combiners, splitters, and transmission lines—exhibit increased losses at higher frequencies, further complicating efforts to optimize both output power and energy efficiency. Consequently, as design frequencies increase, the maximum output power, energy efficiency, and gain of amplifiers reported in the literature tend to decrease [14].

Furthermore, mm-wave PAs are desired to support large continuous bandwidths in the mm-wave frequency range [15, 16]. A major limitation for wideband PAs is the large impedance transformation ratio between the low impedance of transistors caused by low operating voltage, high current and large parasitic effects and the standardized 50 Ω MMIC interfaces.

Moreover, in modern wireless communication systems, complex modulation schemes are employed to maximize channel capacity [17]. These schemes require the system, including the PA, to operate with RF signals exhibiting high Peak-to-Average Power Ratio (PAPR) values. This implies that high energy efficiency and gain at peak output power alone do not fully describe the performance of the amplifier. The flatness of gain and energy efficiency within a specific dynamic range are also important factors in determining the overall energy efficiency and linearity of the amplifier in a telecommunications system.

Commercial wireless communication systems must adhere to international standards regulating spectral emissions caused by nonlinear distortion [18].

To meet these requirements, PAs are typically operated at backed-off power levels, which enhance linearity. However, operating at reduced power levels often reduces energy efficiency [19].

Energy-efficient PA topologies, such as outphasing, Doherty, and sequential PAs, are challenging to implement at mm-wave frequencies due to the significant parasitic effects of transistors. Furthermore, these energy-efficient PA topologies often degrade the linearity of the amplifier.

In conclusion, designing energy-efficient PAs for mm-wave frequencies presents significant challenges spanning from the inherent limitations of MMIC technologies to the demands of modern wireless communication systems. Addressing these interconnected challenges is representing an interesting research area for both the academia and industry, necessitating innovative designs to balance performance trade-offs in next-generation networks.

1.3 Thesis Scope and Outline

In this thesis, we present our circuit implementations , proposing innovative solutions to some of the main challenges summarized above. In this work, the design frequency range was selected as 100 to 114 GHz. This range encompasses three spectrum slots allocated for fixed radio links, each offering more than 2.25 GHz of bandwidth [15, 16]. The suitability of this frequency range for wireless telecommunication links was demonstrated practically in [20].

In Chapter 2, the general steps for designing mm-wave MMIC PAs within this frequency band are presented. We begin by reviewing the available semiconductor processes for this frequency range and describing the key aspects of the 0.1 µm GaAs Pseudomorphic High Electron Mobility Transistor (pHEMT) technology that motivate its selection. Next, we outline the theoretical foundations and practical steps involved in designing a mm-wave amplifier. Finally, the chapter concludes with a discussion on the preparation of MMICs for measurements and commonly employed PA characterization methods.

Chapter 3 examines the commonly used MMIC power combining techniques to realize high RF output power in mm-wave PAs. It covers tee junctions, distributed combiners, directional couplers, and stacked amplifiers, analyzing their effectiveness and limitations at mm-wave frequencies.

Chapter 4 presents our manufactured PA designs with different power combining methods operating in the 100 to 114 GHz frequency range, along with their measurement results. The chapter consists of a balanced amplifier and a non-uniformly distributed PA, both manufactured in a 0.1 µm GaAs pHEMT process.

Chapter 5 introduces dynamic gate biasing to enhance PA efficiency and linearity when operating with modulated signals and spectral emission constraints. Starting with presenting the current status in the literature. Then, a dual-input PA behavioral model is presented, along with the optimization goals and algorithms, which allows us to study dynamic gate profiles. In the chapter, the simulated results are verified with a dedicated measurement setup. Finally, the MMIC-integrated dynamic gate bias amplifier design is presented.

Chapter 6 concludes the thesis, summarizing key findings on energy-efficient mm-wave PAs design and proposing future research directions to further address performance challenges in next-generation wireless systems.

Chapter 2

Theory, Design and Characterization of mm-wave MMIC PAs

In this chapter, the general PA concepts are presented, focusing on theory, design and characterization aspects relevant for mm-wave applications. This will form the basis for the following chapters. In Section 2.1, we present commonly used semiconductor technologies for mm-wave MMIC PA design and present our motivation for choosing the GaAs pHEMT process for designs operating above 100 GHz. In Section 2.2, the theoretical fundamentals of PA design—including transistor operation, optimum load conditions, and matching networks—are explained. Stability analysis and bias networks are discussed in Section 2.3. Throughout the theoretical discussion, realistic examples from the selected GaAs pHEMT process are provided. Finally, the general steps for measurements and measurement methods used for the characterization of PAs are described in Section 2.4; these procedures have been employed to obtain the results presented in subsequent chapters.

2.1 Available Semiconductor Technologies

Numerous PAs have been reported in the literature, implemented using various semiconductor technologies. Complementary Metal–Oxide–Semiconductor (CMOS) technology has been widely adopted for mm-wave PA design, including applications beyond 100 GHz [21–23], due to several advantages. One of its most significant benefits is its high level of integration and advanced Back End of Line (BEOL) compared to other technologies. This facilitates the integration of high-performance analog components alongside the PA itself [24], as well as mixed-signal and digital circuitry [25, 26].

SiGe BiCMOS technology combines the benefits of CMOS technology with Hetero-junction Bipolar Transistors (HBTs), albeit often employing greater gate lengths [27]. The high gain, lower noise, and moderate power of bipolar

transistors, along with the possibility of integrating digital or mixed-signal circuits, make it an attractive option for transmitters and receivers [28, 29]. Therefore, various PAs have also been reported in this technology [30–32]. While silicon technologies can yield a low unit cost when production volume is high, their initial cost is higher than that of III–V technologies; furthermore, they often cannot reach the RF output power levels achieved by III–V High Electron Mobility Transistors (HEMTs) technologies [13].

GaN HEMT, with its wide bandgap and favorable carrier transport properties, is another strong candidate for mm-wave applications. The high breakdown electric field of GaN allows transistors to support very large voltage swings, enabling high RF output power and energy efficiency [33–35] as well as reasonably good noise performance [36–38]. Despite being a highly competitive choice, its maturity lags behind that of GaAs pHEMT and silicon processes. Challenges related to heat dissipation and material growth on Si or SiC substrates persist [13]. Despite providing the highest output power compared to other processes up to the 100 GHz range, its RF output power trending line shows a steeper decline [14], thereby diminishing its main attractiveness above 100 GHz.

At the upper frequency edge of the mm-wave spectrum, InP HBTs or HEMTs are among the most significant options, owing to their exceptional transport properties [39–44]. However, InP processes are expensive and involve fragile, small wafers [13]. As a result, the availability of InP products in the market is limited.

For our targeted frequency band 100 to 114 GHz GaAs pHEMT process appears as one of the most ideal option. GaAs have a greater band gap than silicon and InP. Its already high carrier mobility utilised effectively in GaAs pHEMTs [45, 46] and Metamorphic High Electron Mobility Transistors (mHEMTs) [47, 48] processes to allow mm-wave PAs to be designed. Commercial foundries such as Win Semiconductors offer GaAs processes at a reasonable cost and with exceptionally high yield. Despite its limited BEOL options, GaAs pHEMT processs provide an ideal trade-off between cost, yield, and circuit performance [13, 14] for medium to low-volume applications.

The circuits presented in this thesis are fabricated on 150 mm GaAs wafers using the WIN Semiconductors PP10-20 pHEMT platform. At its core, this technology features a 0.1 µm-gate D-mode transistor with a cutoff frequency (f_T) of 160 GHz, qualified for 4 V operation. This platform provides two interconnect metal layers with air-bridge crossovers, monolithic PN diodes for on-chip ESD protection, precision thin-film resistors, MIM capacitors, and through-wafer vias for low-inductance ground connections. Additionally, it supports fabrication with through-chip RF transitions. This technology allowed us to implementations of the circuits that will be presented in the following chapters.

2.2 Fundamentals of mm-wave Transistor Amplifiers

This section summarizes the fundamental background and steps involved in designing mm-wave PAs. Whenever possible, the theoretical principles are illustrated and compared to simulated results obtained from a $4 \times 25\,\mu m$ transistor belonging to the WIN semiconductors PP10-20 GaAs pHEMT process described in the previous section.

There are two primary ways in which transistors are utilized to generate RF power amplification: as switches or as transconductance amplifiers. While switched-mode amplifiers offer significant advantages, particularly in efficiency, their implementation requires precise harmonic termination conditions and switching frequencies that scale with the operating frequency. These requirements become impractical when the harmonics of interest exceed the rated operating frequency range of the selected semiconductor technology. For example, for a design frequency of 100 GHz, the PP10-20 process may be unsuitable, as its 160 GHz f_T is lower than the frequencies of the harmonics. Therefore, in this thesis, our focus is on transconductance amplifiers. Figure 2.1 illustrates a generic ideal transconductance amplifier in common source configuration. The circuit consists of a transistor Q_1 biased with DC gate (V_{GG}) and drain (V_{DD}) voltages to establish a quiescent current, I_{DD}. The output of the amplifier is terminated with a load impedance, Z_{load}.

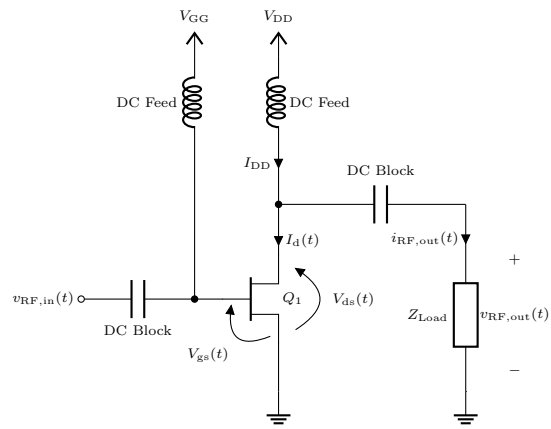


Figure 2.1: A simple transconductance amplifer in common source configuration.

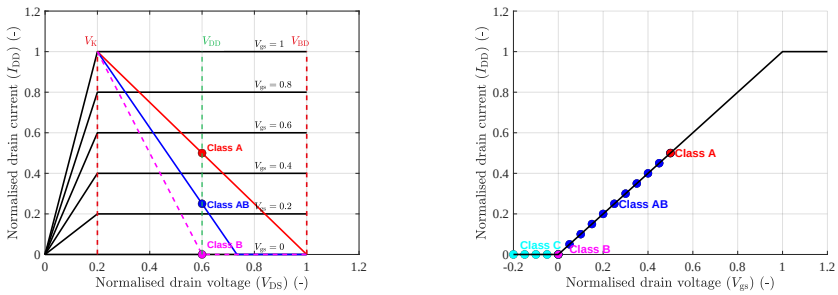
The DC blocking capacitors are designed to act as RF short circuits, allowing the passage of RF signals while blocking DC components. Conversely, the DC feed elements provide high impedance at RF frequencies, isolating the RF signals while permitting the passage of DC voltages and currents.

The gate-to-source voltage, $V_{gs}(t)$, is formed by the superposition of the RF input signal, $v_{RF,in}(t)$, and the DC gate bias, V_{GG}. This signal modulates the drain current, $I_d(t)$. The RF-varying component of $I_d(t)$ flows through the branch connected to Z_{load}, generating an RF output current, i_{out}, in the

opposite direction. Consequently, an output voltage, $v_{\mathrm{RF,out}}$, develops across the load impedance. The real power delivered to the load by sinusoidal signals with a period of T can be calculated as:

$$P = \frac{1}{T}\int_0^T v_{\mathrm{RF,out}}(t) \cdot i_{\mathrm{RF,out}}(t)\mathrm{d}t. \tag{2.1}$$

The bias voltages and load of a PA are adjusted to maximize the swings of i_{out} and v_{out}, thereby maximizing P_{out}. However, these characteristics are inherently constrained by the physical properties of the transistor. Figure 2.2 shows the idealized IV response of an arbitrary FET device. The figure illustrates the Class-A load line for this ideal transistor, which maximizes the voltage swing from the knee voltage, V_{K}, to the breakdown voltage, V_{BD}. Similarly, the full current range of the transistor is utilized to achieve the maximum possible output power. The load line is determined by the quiescent point, which is set by the bias condition and the load connected to the transistor's output.



(a) **(b)**

Figure 2.2: Drain current versus drain bias voltage for various gate bias points (a), and drain current versus gate bias voltage for a single drain bias point (b), for a hypothetical ideal transistor.

Another important aspect of the amplifier is power consumption, which is a primary factor in determining its energy efficiency. The drain efficiency of an amplifier can be calculated as:

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}}, \tag{2.2}$$

where P_{dc} is the DC power supplied to the PA.

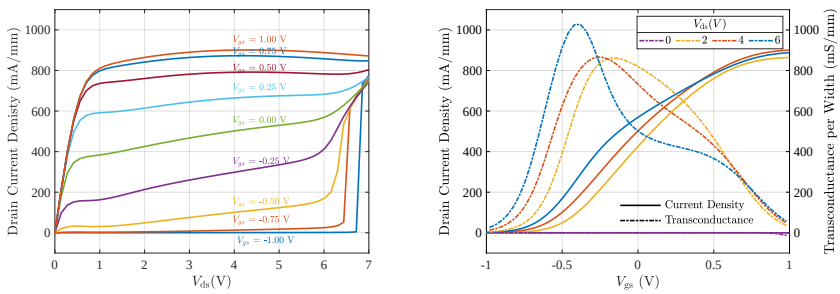
To evaluate the power added by the amplifier while excluding the RF input power (P_{in}) to the PA, the Power Added Efficiency (PAE) is calculated as:

$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}}. \tag{2.3}$$

To improve energy efficiency by reducing P_{dc}, the quiescent bias can be adjusted so that the amplifier draws less current and consumes less power. However, under such conditions, the transistor conducts only during a certain

portion of the input sinusoid's period. The fraction of the signal cycle during which the transistor conducts current is known as the conduction angle (θ_c). The load lines for reduced conduction angle configurations—such as Class-AB ($\pi < \theta_c < 2\pi$), Class-B ($\theta_c = \pi$), and Class-C ($\theta_c < \pi$)—are illustrated in Figure 2.2. The reduced conduction angle increases energy efficiency at the expense of gain and linearity of the amplifier [19]. Depending on the application, different operating modes may be more ideal. Furthermore, the bias point can be dynamically adjusted depending on the instantaneous drive level of the amplifier, as presented in Chapter 5.

Although load-line analysis provides an insightful theoretical foundation for understanding amplifier operation, it becomes less effective as the design frequency increases. When designing a high-frequency amplifier, parasitic effects significantly influence the voltage and current waveforms. Furthermore, as illustrated in Figure 2.3(a), parameters such as breakdown voltage, knee voltage, and threshold voltage can become ambiguous in real transistors designed for high-frequency operation. Additionally, the nonlinear relationship between V_{gs} and I_{ds} further complicates analytical modeling. For illustration, Figure 2.3(b) depicts the small-signal transconductance (g_m) of a transistor in the PP10-20 pHEMT, scaled to its width, under various biasing conditions. The bell-shaped g_m curve, introduces additional considerations when selecting the bias point.



(a) **(b)**

Figure 2.3: IV curve simulations (a), and drain current density versus gate bias voltage for various drain bias points (b), for the GaAs pHEMT transistor.

To analyze the performance of a device in the presence of significant parasitic effects, an empirical method is often preferred. Load-pull analysis addresses this need by identifying the optimal load impedance and, in some cases, the appropriate bias point for the amplifier to meet design goals. This method involves systematically varying the load impedance presented to the device while measuring key metrics such as output power, efficiency, and gain. Load-pull analysis can be conducted through both measurements and simulations, provided that a reliable large-signal model of the device is available. It not only determines the optimal load impedance for a specific performance metric but also characterizes performance variations under different load conditions. This approach enables designers to effectively balance various performance trade-offs to achieve the overall design objective.

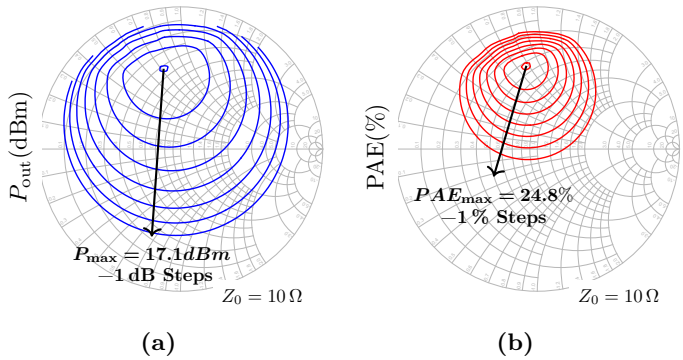


Figure 2.4: Load-pull data showing output power (a) and PAE (b) at 110 GHz for a $4 \times 25\,\mu m$ GaAs pHEMT transistor biased at a drain current density of 300 mA/mm.

To illustrate, Figure 2.4 shows the locations of the load impedances presented to the amplifier that yield various RF output power and PAE values for a $4 \times 25\,\mu m$ GaAs pHEMT transistor. In this specific example, the optimal load impedances for output power and efficiency are relatively close to each other; however, they can also be farther apart depending on the technology and frequency range. By analyzing the contour plots, trade-offs between different performance metrics can be accurately assessed, and a load impedance that satisfies the design goals can be selected.

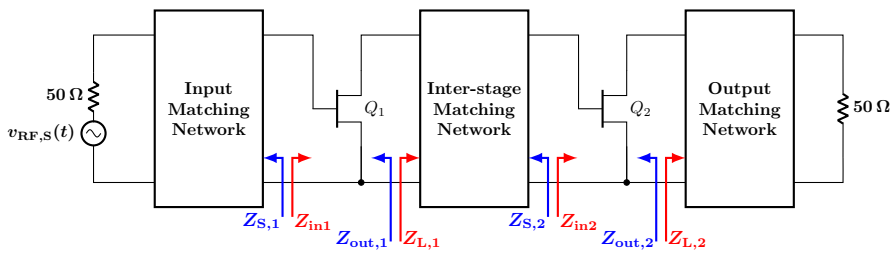


Figure 2.5: A generic multi-stage amplifier.

Unlike the idealized scenario depicted in Figure 2.1, in practical designs, the load termination is not a design parameter. Instead, it is dictated by the system impedance (commonly 50 Ω) or the optimal impedance of subsequent stages. Matching networks are an essential part of PA design and are used to transform these predetermined impedances into the impedance that maximizes performance at the transistor's interface. For example, the output matching network in Figure 2.5 converts the 50 Ω output interface impedance into a load impedance for Q_2 ($Z_{L,2}$), where $Z_{L,2}$ is determined by the load-pull simulations described above. Similarly, the inter-stage matching network transforms the input impedance of Q_2 ($Z_{in,2}$) into the optimal load for Q_1 ($Z_{L,1}$). Due to parasitic coupling between the gate and drain of transistors at mm-wave frequencies, the input impedances $Z_{in,1}$ and $Z_{in,2}$ in the figure depend on the

load impedances presented at the output of the transistors. Therefore, the design procedure typically starts with the output stage and progresses toward the input, ensuring that each individual transistor is presented with its optimum source ($Z_{S,1}$, $Z_{S,2}$) and load impedances.

To achieve greater RF output power, transistors are selected to have a greater total width (periphery) than those in the previous stages. Periphery can be increased by widening individual transistors. However, choosing excessively large transistors results in significant heat generation, higher current flowing through ground vias, and increased distributed effects. When increasing the gate width is not possible, the periphery can be expanded by using multi-finger transistors or employing multiple transistors. However, efficiently combining power from multiple transistors with minimal loss is another critical aspect of the design, which is discussed in Chapter 3.

2.3 Stability and Bias Networks

The bias network implementations in Figure 2.6 are an important part of the PA design and are closely linked to the circuit's stability. For this reason, stability and bias networks are discussed together in this section. These networks are commonly implemented either by a capacitor, as shown in Figure 2.6(a), or as an open-circuited quarter-wave long stub, as shown in Figure 2.6(b). Ideally, these elements isolate RF signals from the DC network while retaining the DC bias voltage. Due to the larger area requirements of the stub implementation, the capacitor-based approach is generally preferred. However, in III-V processes, the capacitor implementation often employs an air bridge to access the capacitor and a via to connect to the ground. The capacitor value, C_b, must be carefully selected to resonate with the parasitic inductances of the air bridge (L_{Bridge}) and the ground via (L_{via}) to achieve an ideal RF short. Connecting these elements to the circuit via an additional quarter-wave transformer creates a high impedance to RF signals at the interface, thereby effectively minimizing the RF power delivered to the bias network while still allowing the delivery of DC power.

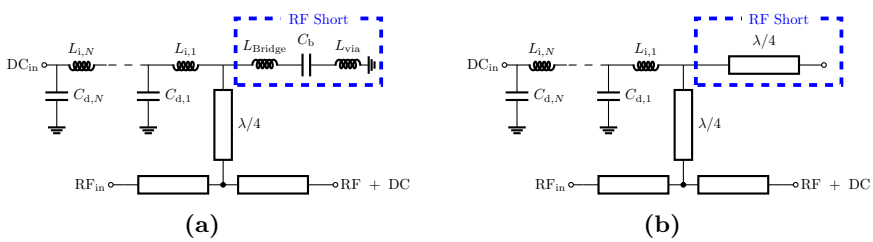


Figure 2.6: DC bias network implementation: (a) with a capacitor, (b) with a quarter-wave transformer.

Amplifier stability refers to an amplifier's ability to operate without producing unwanted oscillations. Such oscillations occur when the overall loop gain and phase conditions allow a feedback signal to reinforce itself, creating a

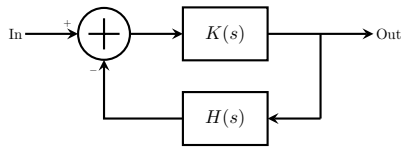


Figure 2.7: A generic linear feed back system.

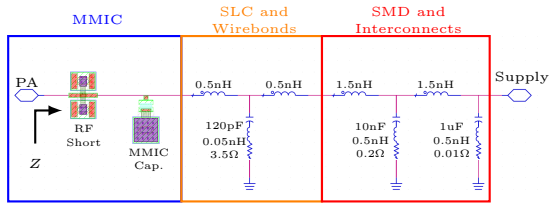
self-sustaining oscillatory condition. Feedback paths may arise from reflected signals, coupling between different conductors, or even intentionally introduced feedback for specific circuit functionalities. Figure 2.7 shows a generic feedback topology of a system with an open-loop gain of $K(s)$, where s represents the complex angular frequency. The output of the system is coupled back to its input through a feedback path with a gain of $H(s)$, forming an overall closed-loop transfer function, $T(s)$, given by

$$T(s) = \frac{K(s)}{1 - K(s)H(s)}. \tag{2.4}$$

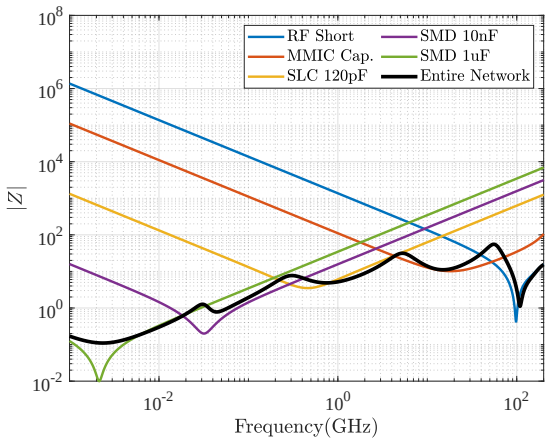
Oscillations occur at any node of the circuit if the denominator in (2.4) has zeros, or equivalently, when $T(s)$ has a pair of poles in the right half-plane. To avoid this issue, it is crucial to ensure that the transistors used in the design exhibit a reflection coefficient with a magnitude less than unity for any passive load and source termination condition; this property is referred to as unconditional stability. Common methods for assessing unconditional stability include Rollet's stability criterion [49] and the geometrically derived stability test [50]. If unconditional stability cannot be achieved, the transistor's gain can be reduced by incorporating resistive networks at the amplifier's input or output. When designing multistage or multi-branch amplifiers, combinations of metal interconnects, parasitic coupling between them, and reflections can form feedback loops that lead to instability. In such cases, two-port stability analysis methods may fail to detect unstable loops formed between different branches or stages, as they measure only the signals at the input and output of the amplifier. To accurately capture instabilities, signals between active and nonreciprocal devices must be accessed with minimal disturbance to circuit operation. Various probing methods have been proposed in the literature [51, 52] and are integrated into circuit simulators to monitor these intermediate interfaces. Once these interfaces have been probed, the absence of right-half-plane poles in the closed-loop system can be verified using visualization techniques such as Nyquist contours [49, 53].

The Maximum Available Gain (MAG) of transistors commonly decreases with increasing frequency. This can lead to the amplification of unwanted signals and potentially cause instability. At these frequencies, bias networks play a crucial role in ensuring stability by providing a low-impedance path that effectively attenuates parasitic signals. Moreover, when a signal with finite bandwidth is applied to a transistor, nonlinear processes generate power components spanning from DC to integer multiples of the bandwidth. If this power is not attenuated through the bias networks, it can modulate the

amplifier output, leading to waveform distortion.



(a)



(b)

Figure 2.8: (a) Schematic of a modeled practical implementation of a bias network. (b) Magnitude of impedance versus frequency for the Electromagnetics (EM) simulated components and the external capacitors, where the inductances from preceding elements are included in their response.

To achieve attenuation through bias networks, a series of decoupling capacitors—placed after the RF short circuit shown in Figure 2.6—are used, denoted as $C_{\mathrm{d},n}$, where $n \in 1, 2, \ldots, N$. These capacitors are designed to filter undesired signals from DC to arbitrarily high frequencies, where the signals are naturally dissipated by loss. Smaller capacitors, effective at filtering high-frequency signals, are placed closer to the interface, while larger capacitors, which target lower frequencies, are positioned farther from the circuit or even outside the MMIC. However, placing capacitors at greater distances introduces larger parasitic inductances, denoted as $L_{\mathrm{i},n}$ in the Figure 2.6, due to physical layout constraints. Therefore, the capacitor values and their placement must be carefully optimized.

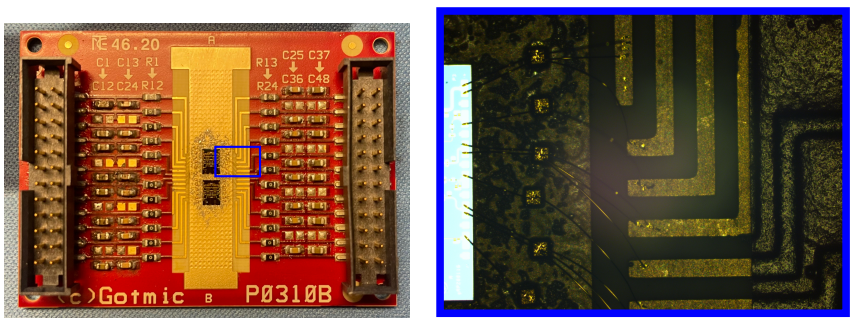
Figure 2.8(a) shows a model of a DC bias network based on electromagnetic (EM) simulations of MMIC elements and measurements of the external bias network. From left to right, the figure includes an RF short structure, an on-chip

shunt bias capacitor with 10 Ω resistor, a Single-Layer Capacitor (SLC) capacitor with its parasitic model, inductances modeling the wirebond connections, and two Surface-Mount Device (SMD) capacitors with their parasitic models and inductances representing PCB interconnections. Figure 2.8(b) shows the magnitude of the impedance versus frequency for the EM components and the external capacitors, with the inductances from preceding elements added to each response. The figure illustrates that each component has a limited frequency range over which it can effectively provide low impedance, and only their combined operation ensures a low impedance from DC to the operating frequency.

2.4 Characterization of mm-wave PAs

After the design process, PAs are measured to verify their performance. To illustrate, Figure 2.9 shows an MMIC mounted on a test structure. In this design, the backside of the MMIC serves as the ground conductor. Therefore, the MMIC is mounted on a metal surface using an electrically and thermally conductive epoxy to ensure low-impedance grounding and efficient heat dissipation. The figure also shows capacitors with increasing sizes mounted on the PCB due to the reasons explained in the previous section.

Interfacing the MMIC PA with RF probes is a common method for evaluating its performance. For measurements—where probes are unsuitable or when assessing the performance of packaged PAs—the RF interfaces of the amplifier are wire-bonded to structurs that couple RF power to a coaxial or waveguide interface. However, this approach introduces some additional loss.



(a) **(b)**

Figure 2.9: a) A test structure for a mm-wave PA. b) A zoomed-in view of the blue rectangle showing single-layer capacitors and wire bonds.

Measuring scattering parameters (S-parameters) against frequency is a standard measurement step for microwave components. Figure 2.10(a) shows a measurement setup utilizing a Vector Network Analyzer (VNA). Excluding the driver amplifier in the figure, the setup is used for the small-signal characterization of the amplifiers presented in later chapters. The frequency range of the VNA can be extended to cover the desired frequency range—75 to 115 GHz in

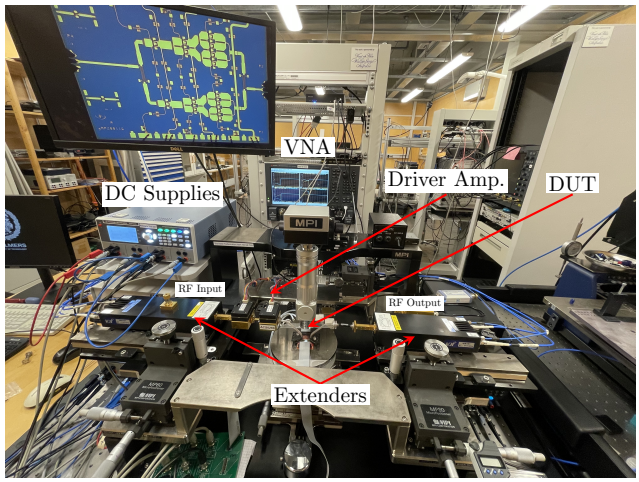
this specific case. The RF input and output of the MMIC are interfaced with RF probes.

Continuous Wave (CW) large-signal measurements involve characterizing the amplifier at various RF input levels. The measurement setup shown in Figure 2.10(a) can also be used for CW power sweeps. In this case, the VNA extender at the input side serves as an RF power source, while the extender at the output captures the output power. The power readings of these extenders are calibrated using power meters. To supply sufficient RF power to saturate the PA, driver amplifiers are utilized. Sweeping the RF input power to the PA while measuring the output power and energy consumption allows for the characterization of important PA parameters, such as energy efficiency and saturation curves.

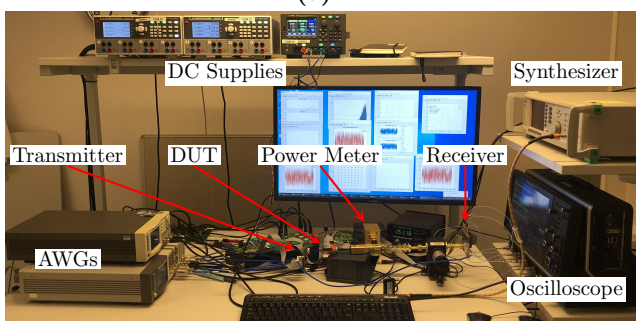
Multitone measurements, including two-tone tests, are useful for gaining deeper insight into PA behavior when operating in systems driven by signals with a specific bandwidth. These measurements involve applying two or more sinusoidal input signals (tones) at different frequencies. The frequency separation between these tones is much smaller than their absolute frequencies. Due to the nonlinear operation of transistors, these signals mix and generate inter-modulation distortion. These products can be observed as spectral regrowth and in-band distortions when the output waveform of the PA is measured.

In Figure 2.10(b), a modulated signal measurement setup is presented. This setup simulates a real data transmission scenario to validate the findings that will be further discussed in Chapter 5. One of the Arbitrary Waveform Generator (AWG)s generates the complex baseband signal with In-phase Quadrature (IQ) components, each assigned to one of the output channels of the AWG. The transmitter upconverts the signal to the RF frequency by mixing it with the Local Oscillator (LO) signal supplied by the synthesizer. The resulting RF signal drives the PA, and its RF output power is measured using a power meter.

The output waveform is downconverted by the receiver using the identical LO signal. The resulting complex baseband IQ components are recorded with an oscilloscope. By digitally processing the waveform, system-level information related to the PA, such as the output spectrum and constellation diagram, are obtained.



(a)



(b)

Figure 2.10: (a) A measurement setup utilizing a VNA with frequency extenders to measure scattering parameters and dynamic response. (b) A modulated signal measurement setup utilizing an AWG, transmitter, receiver, and oscilloscope.

Chapter 3

MMIC Power Combining Methods

Load-pull simulations presented in Section 2.2 revealed that a 4×25 μm transistor in the PP10-20 pHEMT technology achieves a maximum RF output power of 17 dBm at 110 GHz. The optimum load impedance of this transistor is $4.0 + j4.6$ Ω. To attain an output power of 1 W, 20 such transistors must be combined. Integrating 20 transistors within a two-metal-layer process necessitates combiner networks that exhibit the lowest possible insertion loss to maintain energy efficiency, which will be discussed in this chapter. Furthermore, transforming this low impedance to the standard system impedance of $50\,\Omega$ introduces significant bandwidth limitations due to the constrained quality factor of on-chip matching networks. Therefore, in this chapter, we describe commonly used combiner networks suitable for realizing high-power mm-wave PAs in III–V technologies. Some of the combiner networks are applied in the MMIC PA designs presented in Chapter 4.

3.1 Tee Junctions

Connecting two or more conductors to a central node is one of the simplest yet most widely used power-combining methods in MMIC design. This technique is applied across various design scales, from transistor-level multi-finger configurations to the output combiner of the overall PA [42, 48, 54].

Figure 3.1 presents a multi-port tee combining structure for real input and output load impedances. By adjusting the characteristic impedance of the lines, this structure can function not only as a power combiner but also as an impedance-matching network with the help of impedance transformers at the input branches or output branch. The transmission lines are designed to be quarter-wavelength long for real input and output loads. However, their lengths can be adjusted to compensate for or realize the imaginary components of the input or output impedances.

As discussed in the previous chapter, active devices operating in different

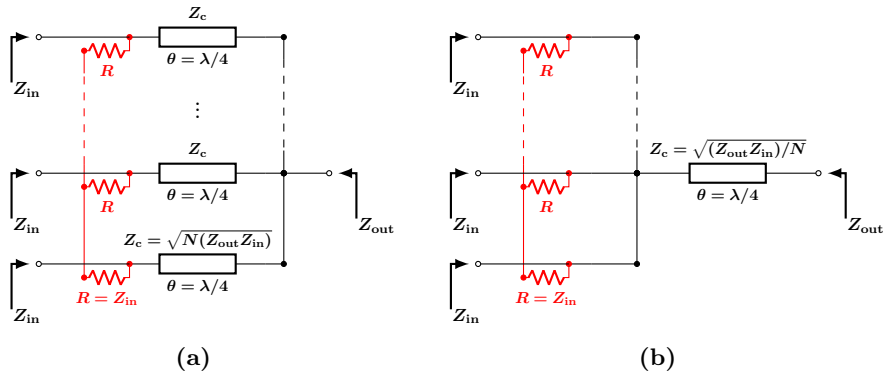


Figure 3.1: Impedance-transforming tee junctions, where transformers are implemented in individual branches (a) and in the combined branch (b) for real Z_{in} and Z_{out}. Optional isolation resistors are shown in red.

branches can form feedback paths, potentially leading to odd-mode oscillations. To mitigate these oscillations and dissipate the resulting unwanted power, a resistive network—shown in red in Figure 3.1—is often required between the branches. This resistive network improves isolation between input ports and dissipates odd-mode excitations. For cases where oscillations occur out of band, the impedance values of the network may differ from those analyzed at the operating frequency. Therefore, the resistor value that yields the best isolation may also differ.

Ideally, the resistive network does not affect the operation of the combiner when all ports are evenly driven. However, at high frequencies, the distributed effects arising from the physical dimensions of the resistor can introduce loading effects on the branches. To achieve maximum isolation without degrading the combiner network's performance, the resistors should be implemented with minimal physical dimensions, including interconnections [55].

In practice, implementing this topology with more than two branches in a layout requires extra phase compensation due to unequal distances between the input and output ports. Another approach to combining multiple branches is cascading multiple tee junctions. However, both options result in extra losses and increased chip area due to the extra interconnects.

3.2 Distributed Combiners

Considering the layout limitations mentioned above, tee junctions can be impractical for combining more than two branches. In such cases, instead of combining power at a centralized node, integrating power continuously along the propagation path can be advantageous. Figure 3.2 illustrates a generic N-branch distributed power combining topology, along with a simplified transistor model used for analysis in this section. Under ideal conditions—neglecting the parasitic output capacitances of the transistors, $C_{\text{p},n}$ (where $n \in 1, 2, \ldots, N$)—the RF

branch currents (represented as phasors, I_n) provided by the current sources are summed over the load admittance, Y_L. Simultaneously, the magnitude of the RF voltage drop across each transistor, denoted as V_{ds}, remains identical for all branches. To achieve this condition, the characteristic admittance of the transmission lines must satisfy the constraint presented in (3.1).

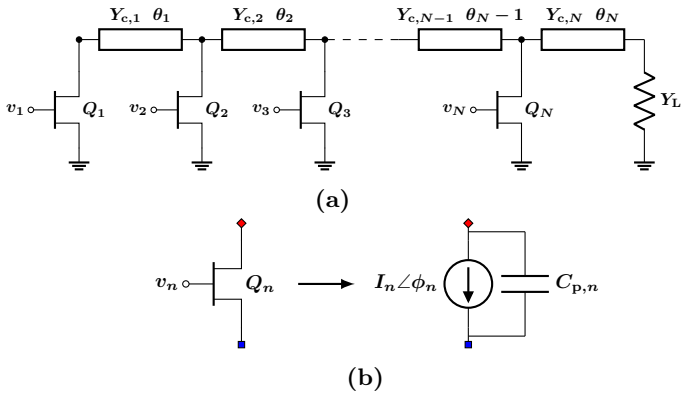


Figure 3.2: a) A generic distributed combining structure. b) Simplified equivalent circuit model of the transistors.

$$\begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{bmatrix} = \left(\begin{bmatrix} Y_{\text{c},1} \\ Y_{\text{c},2} \\ \vdots \\ Y_{\text{c},N} \end{bmatrix} - \begin{bmatrix} 0 \\ Y_{\text{c},1} \\ \vdots \\ Y_{\text{c},N-1} \end{bmatrix} \right) V_{\text{ds}} \tag{3.1}$$

$$\phi_{n+1} = \sum_{m=1}^{n} \theta_m, \tag{3.2}$$

By setting the drain current phase of the first transistor as a reference (i.e., $\phi_1 = 0°$) and adjusting the drain current phases of the remaining transistors to compensate for the electrical lengths of the preceding transmission lines, we ensure that the currents are summed in phase and constructively, maximizing power-combining efficiency. Furthermore, by setting the admittance difference in (3.1) to achieve the optimum admittance—i.e., yielding the maximum RF output power for the transistors—the maximum possible RF output power from each individual transistor is efficiently delivered to the load.

As shown in [56], different transistor sizing and transmission line impedance configurations yield a variety of PA topologies, including load-modulated, sequential, and traveling-wave amplifiers. Load-modulated and sequential amplifier designs are primarily aimed at improving back-off efficiency. However, at mm-wave frequencies, transistors in the off state exhibit significant parasitic capacitance ($C_{\text{p},n}$). Therefore, PAs in these configurations are limited [17, 57, 58], especially in III-V processes [59–61].

Nonuniform Distributed Power Amplifier s (NDPAs) with tapered-width drain-line sections are another implementation that utilizes this combiner

network. In this approach, following (3.1), the characteristic impedance of the transmission lines after each combined branch is reduced to facilitate the combination of identical transistors or PA branches. Various implementations of NDPAs have been reported in the literature [62–64]. Ideally, all power propagates to the load at the drain line, eliminating the need for a termination resistor at the drain node of the first transistor used in uniform distributed power amplifiers [65–67].

Nonuniform configurations allow the combination of multiple transistor peripheries with a single conductor, provided that the characteristic impedance or transistor sizes are practical for implementation. The layout consists of a single continuous metal structure, making it relatively simple to implement. However, unlike the tee junction case, there is no symmetry between branches due to phase differences. This makes the use of an odd-mode resistor impractical and requires an input splitter network that feeds the branches with the desired phase difference.

3.3 Directional Couplers

For the combiners mentioned in Sections 3.1 and 3.2, the reflected power from the output load propagates back to the input terminals of the combiner. Directional couplers, on the other hand, leverage the phase difference between input signals and incorporate an additional isolation terminal, enabling the separation of incident and reflected power to different ports. When the network is fed from its input port, the signal is split with a 90° phase difference, causing any reflected signal to combine either constructively or destructively at different ports.

In balanced amplifiers, 90° hybrid couplers are among the most commonly used configurations. These couplers evenly split the input signal between the output ports, introducing a 90° phase difference between them. The key advantage of this arrangement is that reflected signals add constructively at the isolation port—allowing them to be dissipated—while they add destructively at the input port, thereby minimizing return loss at the port.

Branch-line couplers [68–70], shown in Figure 3.3(a), and coupled-line couplers, shown in Figure 3.3(b), are among the most commonly used implementations. However, branch-line couplers are less preferred than coupled-line couplers for MMIC designs at mm-wave frequencies. This is because they require larger area, transmission lines in this configuration are prone to parasitic coupling, and the areas enclosed by metal layers are not suitable for manufacturing.

The details of coupled-line couplers are well studied in the literature [71]. To achieve an even split, the coupling factor, (k), must satisfy the condition

$$k = \frac{Z_{\mathrm{c,e}} - Z_{\mathrm{c,o}}}{Z_{\mathrm{c,e}} + Z_{\mathrm{c,o}}} \approx \frac{1}{\sqrt{2}}, \tag{3.3}$$

where $Z_{\mathrm{c,e}}$ and $Z_{\mathrm{c,o}}$ are the even-mode and odd-mode characteristic impedances of the coupled lines, respectively. However, this coupling level is often difficult

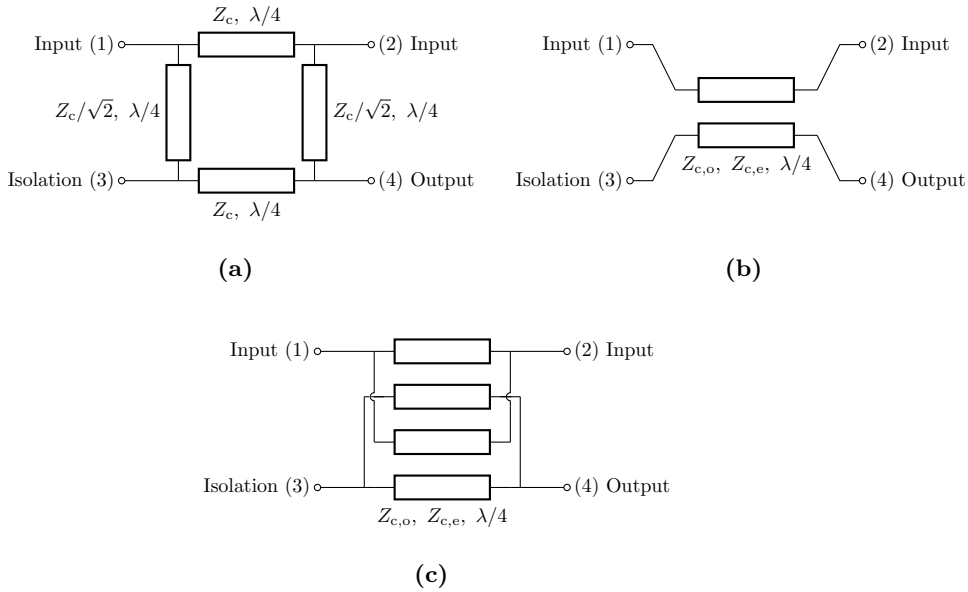


Figure 3.3: Schematics of (a) A Branch-line coupler, (b) Coupled line coupler and (c) a Lange coupler

to achieve with edge-coupled lines. Furthermore, typically in many III-V processes, there are not enough suitable metal interconnect layers to implement broadside-coupled lines, as described in [47]. A more commonly employed approach for achieving greater coupling is the use of Lange couplers, as shown in Figure 3.3(c) [61, 72]. Lange coupler designs interdigitate the coupled-line sections, enabling tighter coupling between the lines.

Despite their relatively complex layout, many III-V processes provide metal layers with sufficient manufacturing tolerances to implement directional couplers. Due to their isolation properties and improvements in matching, they are widely preferred by MMIC designers.

3.4 Stacked Amplifiers

Power-combining methods discussed until now produce an output impedance that is either lower than or equal to the impedance observed at their input ports. Voltage-summing amplifiers are particularly important, as they not only combine power levels but also increase the output impedance [73]. This characteristic is especially crucial for mm-wave applications, as it helps to address the challenge posed by the low optimum output impedance of PAs.

A commonly adopted configuration for summing voltages using transistors is the stacked amplifier configuration, as shown in Figure 3.4. Stacked amplifiers consist of two or more common-source transistors sharing the same drain current and operating in series, such that their V_{DS} voltages are summed. The

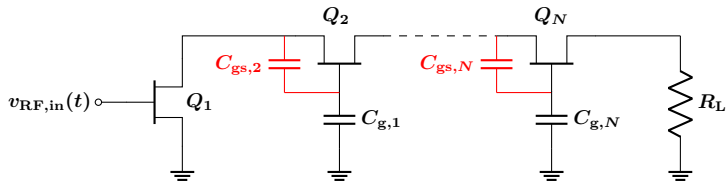


Figure 3.4: A generic stacked amplifier structure.

drain current generated by the first transistor as a result of the input drive, $v_{\text{in}}(t)$, charges both the parasitic gate-to-source capacitance, $C_{\text{gs},n}$, and an externally added gate capacitor, $C_{\text{g},n}$. With the help of additional matching networks between transistors and by adjusting $C_{\text{g},n}$, both transistors can be operated to deliver maximum output power [74, 75]. Since there is no phase difference between the input and output of the stacked transistors, the voltages sum up while the drain current remains constant.

The stacked topology has been utilized to achieve broadband designs in [76] and [77], achieving frequency ranges of 65 GHz to 125 GHz and 200 GHz to 255 GHz, respectively. In [46], the stacked topology enabled the achievement of a high power density.

Stacked amplifiers offer various benefits; however, their implementation is more challenging compared to other power-combining techniques. Key challenges include ensuring the stability of transistors in the cascode structure [78], evenly distributing the voltage swing across the transistors, and the availability of accurate models for transistors whose sourvce is npot coonected to gorong.

Chapter 4

MMIC PAs Operating Over 100 GHz

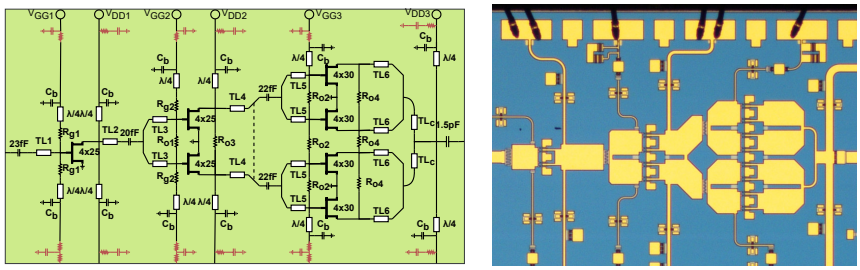
In this section, we present the PA designs that utilize the theoretical background and measurement methods discussed so far. First, we demonstrate the results of a balanced amplifier designed using the 0.1 µm GaAs process. Second, we present an NDPA and its associated combiner, also implemented in the same process.

4.1 A MMIC Balanced Amplifier

In [Paper A], a balanced amplifier consisting of two identical PA branches was designed for the frequency range of 100 GHz to 114 GHz. Figure 4.1 illustrates both the schematic and layout implementations of the identical branches. The optimum load and the corresponding conjugate source impedance for the transistors were determined by load-pull analysis across the frequency range, as shown in Figure 4.2. The lines $Z_{\mathrm{L,P_{out}}}$ and $Z_{\mathrm{L,PAE}}$ represent the load impedances that maximize peak RF output power and power-added efficiency, respectively. Meanwhile, $Z_{\mathrm{L,Gain}}$ corresponds to the load impedance for simultaneous conjugate matching of the amplifier, maximizing small signal gain. The same notation is used for the corresponding source impedances, $Z_{\mathrm{S,P_{out}}}$, $Z_{\mathrm{S,PAE}}$, and $Z_{\mathrm{S,Gain}}$.

The input output and interstage matching networks were implemented using transmission lines and interdigital capacitors to present the optimum load to each transistor. The specific values of the transmission lines used in Figure 4.1(b) can be found in [Paper A].

The output stage of the individual branches is designed as an impedance-transforming tee junction, incorporating isolation resistors, $R_{\mathrm{o},n}$ (where $n \in 1, 2, 3, 4$), to suppress odd-mode oscillations. The two PA branches are then combined using Lange couplers, as illustrated in Figure 4.3(a).



(a) **(b)**

Figure 4.1: ((a) Schematic implementation of a singe branch of a mm-wave PA .(b) Manufactured layout implementation of the schematic.

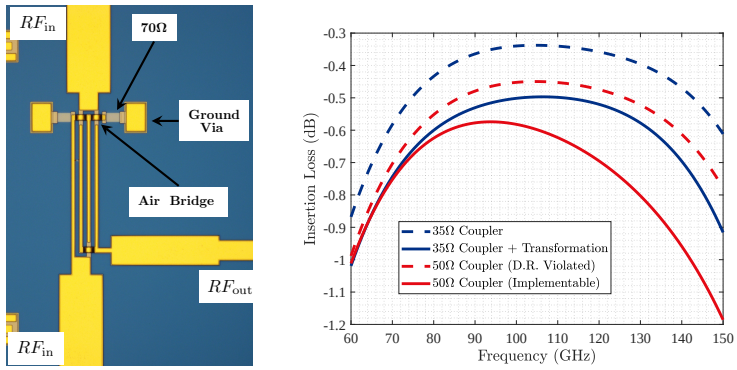
(a) **(b)**

Figure 4.2: Source and load termination impedance yielding maximum RF output power, PAE, and small signal gain for (a) 4×25 μm transistors and (b) 4×30 μm transistors, biased at 300 mA/mm, over the 100 GHz to 115 GHz range. Circular markers indicate the lower edge of the frequency range.

The Lange coupler design with a port impedance of 50 Ω, matching the standard input and output impedance of the MMIC, requires excessively thin coupled lines. This violates the design rules and introduces additional conductor losses, as shown in Figure 4.6(b). Using the thinnest possible lines that doesn't violate design rules results in degraded coupler performance. Therefore, Lange couplers are realized with 35 Ω port impedances. This design, which includes a quarter-wavelength transformer to match the coupler to the input and output impedance of the MMIC, yields lower insertion loss compared to the suboptimal 50 Ω implementation, as also demonstrated in Figure 4.3(b).

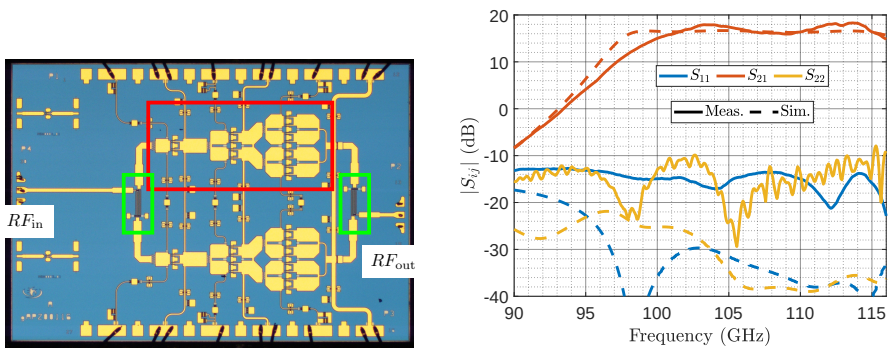
The overall PA design is presented in Figure 4.4(a). The small-signal performance of the amplifier, shown in Figure 4.4(b), indicates that the PA provides more than 15 dB of gain over the frequency range from 100 GHz to 114 GHz. The input and output reflection coefficients remain below −10 dB, owing to the use of directional couplers. However, the deviation between the simulated and measured reflection coefficients suggests limited directivity in

the coupler design, as well as non-ideal characteristics of the probe pads.



(a) **(b)**

Figure 4.3: a) Layout of a 35 Ω Lange coupler designed in the 0.1 µm GaAs process. b)Simulated insertion loss for various Lange coupler designs



(a) **(b)**

Figure 4.4: Photograph of the 3.4 × 2.4 mm MMIC PA designed in the 0.1 µm GaAs process. The red square highlights an individual PA branch, green squares indicate Lange couplers. (b) Small signal measurement and simulations of the PA

The overall design shown in Figure 4.5, achieves RF output power levels between 20.3 dBm and 24.2 dBm over the frequency range from 100 GHz to 114 GHz, with a peak efficiency ranging from 5.3 % to 11.9 %. These results provide competitive performance compared to other GaAs MMIC PAs reported in the literature.

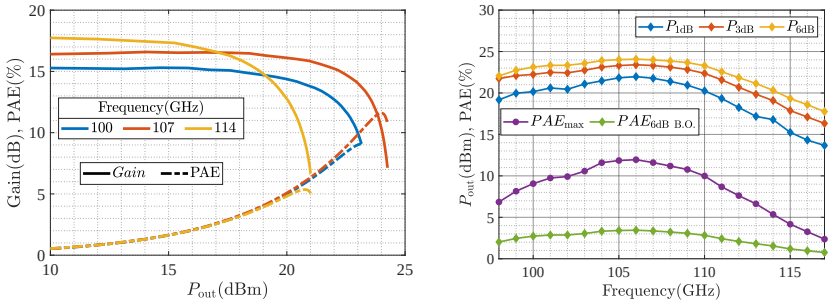


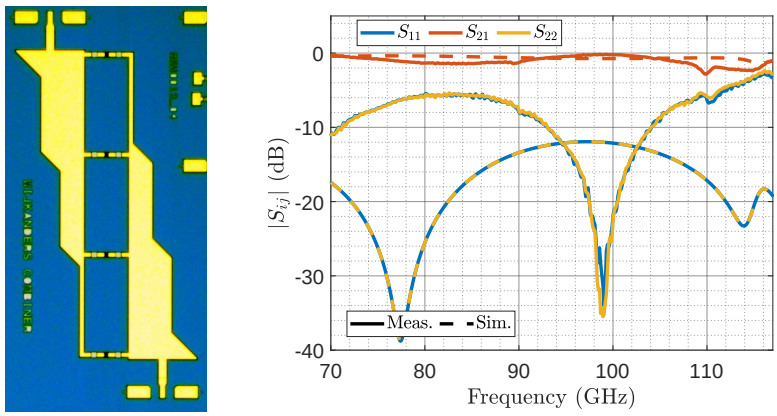
Figure 4.5: (a) Gain compression curves of the balanced PA. (b) Output power at 1, 3, and 6 dB gain compression, peak PAE, and PAE at 6 dB back-off against frequency.

4.2 A Non-Uniform Distributed MMIC Power Amplifier

We utilized the distributed power combining method to combine multiple PA branches. According to the theory described in in section 3.2 the combiner is designed avoid dynamically varying the operating point or load condition of the branches in this configuration. Therefore, this implementation realizes a NDPA, similar to works reported in [62, 64].

To combine four identical PA branches, the admittance of the lines is set to $Y_{c,n} = n/75\ \mho$, following (3.1). Ultimately, the characteristic impedances of the microstrip transmission lines span from 18.75 Ω to 75 Ω, utilizing the full practically implementable impedance range of the technology. The power-handling limitations of the lines prevent the implementation of transmission lines with a characteristic impedance greater than 75 Ω. Achieving characteristic impedances lower than 18.75 Ω requires excessively wide microstrip lines, exceeding 240 µm. The electrical length of the transmission line sections is set to $\theta = 120°$ at the center frequency of 107 GHz. To ensure phase consistency, as described in (3.2), an identical network is also used as a power splitter.

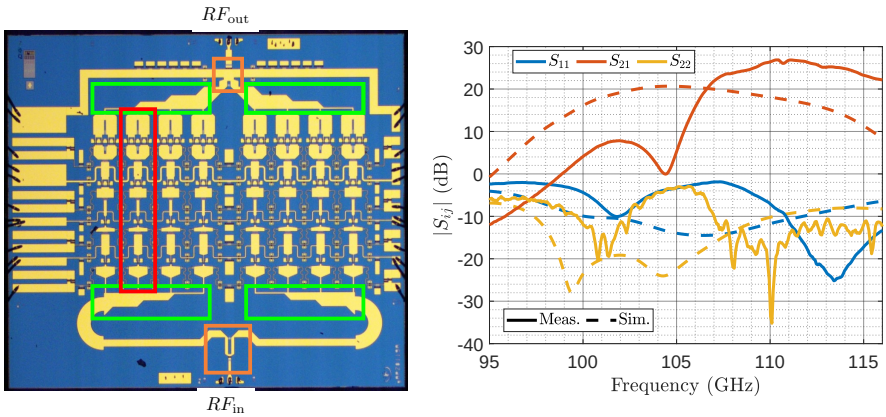
Figure 4.6(b) presents the S-parameters of the network designed to combine four PA branches, targeting an operating frequency range of 100 GHz to 114 GHz. The measurement results indicate that the back-to-back combiner yields an insertion loss of less than 1.5 dB over the 70 GHz to 108 GHz frequency range. However, compared to EM simulations, the measured return loss is higher, suggesting discrepancies between the simulated and fabricated structures. A dip in the design frequency range limits the optimal performance of the structure over 110 GHz. Nevertheless, despite this dip, the insertion loss of the back-to-back structure remains below 2 dB up to 120 GHz. The network offers an additional benefit of having the output port located at the side, which provides a significant advantage in because this configuration allows two of these structures to be combined with a minimal amount of additional transmission



(a) **(b)**

Figure 4.6: (a) Photograph of distributed combiner network in back to back configuration designed in the 0.1 µm GaAs process. (b) Scattering parameters of the back-to-back distributed combiners and splitters for 18.75 Ω termination at both ports.

lines, simplifying the overall integration. Figure 4.7(a) demonstrates a PA design that utilizes this structure, combining two of them using an isolated tee junction.



(a) **(b)**

Figure 4.7: (a) Chip photograph of an NDPA designed in the 0.1 µm GaAs process. The red square highlights an individual PA branch, green squares indicate distributed combiners and splitters for four PA branches, and orange squares represent isolated tee-type power combiners. (b) the small signal response of the NDPA

The structure enables the combination of eight PA branches within the MMIC. The small-signal performance of the PA is shown in Figure 4.7(b), exhibiting a small-signal gain of more than 20 dB from 107 to over 116 GHz.

However, a significant discrepancy was observed between simulated and measured results, leading to poor large-signal performance both in small and large signal. To address this issue, improved device models and additional design iterations are planned. We aim to address these limitation in future iterations.

4.3 Discussion and Comparison

The presented balanced amplifier IN [Paper A] achieves a performance level that is competitive with other GaAs PAs reported in the literature. Table 4.1 summarizes PAs manufactured using GaAs processes, and Figure 4.8 shows the saturated output power of amplifiers fabricated in various semiconductor technologies. Achieving higher output power typically requires additional combining networks or wider transistors, which results in lower energy efficiency and gain. However, Table 4.1 shows that our design achieves the highest gain per stage—except for one reference that utilizes a cascode configuration. Additionally, our design provides one of the highest RF output power levels compared to other works. These findings demonstrate that we have successfully implemented low-loss and accurate matching networks, ensuring stable operation for the balanced amplifier.

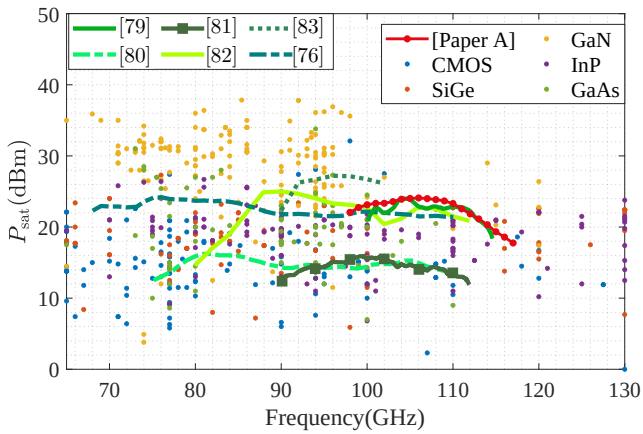


Figure 4.8: State of the Art power amplifiers manufactured in different material technologies [14].

Neither design achieves a competitive bandwidth compared to other works in the literature. The main limitation is the restricted bandwidth of the matching networks—particularly those connecting the output of the PA to the 50 Ω interface of the MMIC due to the extensive impedance transformation ratio. By sacrificing output power, energy efficiency, and gain, PAs with greater bandwidth can be achieved. However, our designs specifically target communication bands within the 100 GHz to 114 GHz frequency range.

Table 4.1: Comparison with other GaAs works in the literature covering or close to the frequency range of 100 GHz to 114 GHz.

Ref.	Freq.	Gain(dB)	$P_{\mathrm{dc,q}}$	P_{sat}	PAE	Size	G/Stage (dB)
[79]	100-113	4-7	-	22-24	-	2.3×1.6	2-3.5
[80]	75-110	15-19	0.41	14.5	9.6	2.7×1.9	3.75-4.75
[81]	90-112	22	-	15.2	3.5	1.5×0.8	7.3(Cascode)
[82]	85-116	20.5	-	22.5	4	2.8×3.0	4.1
[83]	92-102	27	3.00	27	12.5	3.0×3.0	5.4
[76]	65-125	16.8	2.15	22.5	7.6	1.3×2.8	4.2 (Stacked)
This Work	100-114	15.2-18.2	1.87	20.3-24.1	11.9-5.3	2.6×2.4 **	5.1-6.1

* Freq. is in GHz; $P_{\mathrm{dc,q}}$ denotes the quiescent DC power consumption (in W); P_{sat} is saturated RF output power in dBm; PAE is in %; Size is in mm×mm; Gain/Stage is the gain per stage (in dB).

** The long transmission line at the input of the PA used to fit the PA to the reticle plan was de-embedded to accurately report the PA size.

Chapter 5

Dynamic Gate Biasing

In Chapter 1, it was mentioned that PAs operating in modern radio equipments amplify modulated signals with large peak-to-average power ratios (PAPR). The transmitted signal must comply with regulatory spectral emission masks [18]. As a result, PAs are typically operated in a back-off region, where amplification is more linear but at the cost of lower energy efficiency. Various efficient power amplifier topologies, such as load- or supply-modulated PAs, have been proposed to address this trade-off [84–87]. However, implementations at mm-wave frequencies remain limited due to additional design challenges, including the significance of parasitic effects. Furthermore, these topologies often compromise amplifier linearity, necessitating an additional linearization stage to fully exploit their benefits while meeting spectral emission requirements.

Dynamic gate biasing, as illustrated in Figure 5.1, is a method in which one or more gate bias voltages of the amplifier are not fixed but instead follow a pattern, derived from the instantaneous RF input power to the amplifier. In Figure 5.1, V_{Bias} represents the static drain bias and the static gate bias applied to those stages that are not dynamically gate-biased.

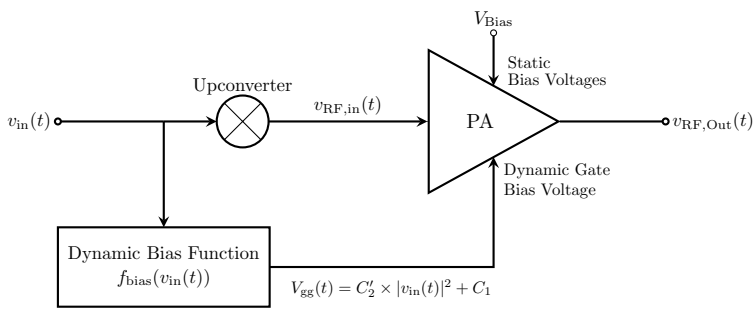


Figure 5.1: Block diagram of the dynamic gate bias power amplifier. V_{Bias} represents the static drain and gate biases applied to the stages that are not dynamically gate-biased.

This chapter is organized as follows. In Section 5.1 we present the other dynamic gate biasing works in the literature. In Section 5.2, we first present the behavioral modeling method utilized in [Papers C-D], which allows us to predict the modulated signal behavior from static CW measurements. Then, in Section 5.3, we describe the optimization goals and limitations to select the best dynamic gate bias function for the [Papers B-D], along with the simulated results that we acquired. The construction of a dedicated measurement setup to verify these results and the subsequent verification process are explained in Section 5.4. Finally, the MMIC integration of the overall study is described in Section 5.5.

5.1 Literature Survey

Dynamic gate biasing has emerged as a powerful technique to enhance the performance of RF and mm-wave PAs, particularly in terms of efficiency and linearity. This method was initially theoretically proposed to improve efficiency for an idealized FET with a linear drain current–gate bias voltage relationship [88]. The combination of dynamic drain and gate bias to improve efficiency was further theoretically elaborated in [89] and experimentally demonstrated in [90]. In [91], an integrated adaptive bias circuit was employed in a GaAs HBT circuit to improve efficiency as well as to enhance the adjacent channel leakage ratio. In [92], the drain efficiency of a PA increased from 1.5% to 6.7% for a code-division multiple-access application while maintaining linearity. A 10 dB reduction in third-order intermodulation product levels was achieved in [93]. Integrated gate modulation for CMOS field-effect transistor amplifiers was realized in [94, 95], enabling linear operation. The phase linearization effect of gate modulation was demonstrated in [96] for GaN power amplifiers, achieving a reduction in adjacent channel leakage by 5.6 to 7.7 dB. Moreover, simultaneous amplitude and phase linearization was achieved by modulating multiple stages of a GaN PA [97]. Gate modulation has also been implemented in some load-modulated PAs to further enhance their performance. For example in [57, 98], dynamic gate-biased active load-modulated amplifiers were reported.

5.2 Dual Input PA Behavioral Modeling

The greatest complexity gap between dynamic gate biasing and analog pre-distortion lies in how the RF nonlinearities of the Device Under Test (DUT) are addressed. In analog pre-distortion, these nonlinearities are compensated for in the RF path. Conversely, dynamic gate biasing modulates the RF response of the amplifier via an external control voltage, necessitating an additional mapping between the gate bias voltage and the complex gain response of the PA. Furthermore, dynamic gate biasing also modulates the energy consumption of the amplifier, which should also be included in the model. In this section, we present a simple, memory-less dual-input model for PAs that maps both the baseband-equivalent RF input voltage and the dynamic gate bias voltage to the baseband-equivalent complex RF output voltage and the energy consumption

of the PA. The model is used to predict the performance of the PA driven by modulated signals and dynamic gate bias profiles using the quasi-static simulations described in the next section.

To accomplish this, a CW RF input signal is swept at the Device Under Test (DUT) to create a data set for modeling. At each RF input power level, the complex large signal gain, DC power consumption, and phase difference between the input and output are recorded. This procedure is repeated for various gate bias voltages, thereby covering the entire range of voltages that will be supplied to the PA during modulated signal operations.

The RF signal supplied to the PA can be written as

$$v_{\mathrm{RF,in}}(t) = A_{\mathrm{in}}(t)\cos\Big(\omega_c t + \phi_{\mathrm{in}}(t)\Big), \tag{5.1}$$

where $A_{\mathrm{in}}(t)$ and $\phi_{\mathrm{in}}(t)$ represent the amplitude and phase modulations of the signal, respectively. The complex baseband equivalent of this signal is given by

$$v_{\mathrm{in}}(t) = A_{\mathrm{in}}(t)e^{j\phi_{\mathrm{in}}(t)},$$

and a similar representation applies to the output voltage:

$$v_{\mathrm{out}}(t) = A_{\mathrm{out}}(t)e^{j\phi_{\mathrm{out}}(t)}.$$

For a specific gate bias voltage, the output voltage of the PA can be estimated as a function of the input voltage using an odd-order polynomial expansion as follows:

$$v_{\mathrm{out}}(v_{\mathrm{in}}) = \sum_{p=0}^{P} a_p v_{\mathrm{in}}|v_{\mathrm{in}}|^{2p}$$

where a_p are the complex polynomial coefficients, p denotes the polynomial index related to the input signal, and P is the number of polynomial terms.

To incorporate variations in complex gain, and power consumption resulting from the dynamic gate bias voltage (V_{gg}), we employ a polynomial model that accounts for the cross-product terms of the polynomial expansion for both the gate bias voltage and the baseband-equivalent complex input signal. The model is given by

$$v_{\mathrm{out}}(v_{\mathrm{in}}, v_{\mathrm{gg}}) = \sum_{q=0}^{Q}\sum_{p=0}^{P} \beta_{p,q} V_{\mathrm{gg}}^{q} v_{\mathrm{in}}|v_{\mathrm{in}}|^{2p} \tag{5.2}$$

where $\beta_{p,q}$ represents the complex polynomial coefficients, p is the index associated with the input signal, and q is the index associated with the gate bias voltage.

Similarly, the DC power consumption can be modeled by including both odd- and even-order polynomial terms of the magnitude of v_{in} as

$$P_{\mathrm{dc}}(v_{\mathrm{in}}, V_{\mathrm{gg}}) = \sum_{l=0}^{L}\sum_{k=0}^{K} c_{k,l} V_{\mathrm{gg}}^{l}|v_{\mathrm{in}}|^{k} \tag{5.3}$$

where P_{dc} is the DC power consumption of the PA in watts, $c_{k,l}$ represents the real polynomial coefficients for estimating the DC power consumption, k is the index associated with the input signal, and l is the index associated with the gate bias voltage.

Equivalently, (5.2) can be written in matrix form as:

$$\mathbf{v}\mathrm{out} = \mathbf{X}(v_{\mathrm{in}}, V_{\mathrm{gg}})\boldsymbol{\beta} \tag{5.4}$$

where the columns of $\mathbf{X}(v_{\mathrm{in}}, V_{\mathrm{gg}})$ represent the individual polynomial basis functions derived from (5.2), and each row contains the evaluated polynomial expansion terms corresponding to a specific pair of input values $(V_{\mathrm{in}}, V_{\mathrm{gg}})$. Here, $\boldsymbol{\beta}$ is a column vector containing the complex polynomial coefficients $\beta_{m,n}$:

$$\boldsymbol{\beta} = \begin{bmatrix} \beta_{0,0} & \beta_{0,1} & \dots & \beta_{0,Q} & \beta_{1,0} & \beta_{1,1} & \dots & \beta_{P,Q} \end{bmatrix}^T$$

Similarly, $\mathbf{V}$out is a column vector containing the output voltage responses corresponding to the different $(v_{\mathrm{in}}, V_{\mathrm{gg}})$ pairs.

To estimate $\boldsymbol{\beta}$, a least-squares estimation is performed as follows:

$$\widetilde{\boldsymbol{\beta}} = \left(\mathbf{X}^{\mathrm{H}}\mathbf{X}\right)^{-1}\mathbf{X}^{\mathrm{H}}\mathbf{v}_{\mathrm{out}}, \tag{5.5}$$

where $\mathbf{X}^{\mathrm{H}}$ denotes the Hermitian transpose of $\mathbf{X}$, and $\widetilde{\boldsymbol{\beta}}$ represents the estimated polynomial coefficient vector. Similar procedures can be applied to determine the model coefficients for P_{dc}. By utilizing the polynomial coefficient vectors $\boldsymbol{\beta}$ for the output voltage and $\boldsymbol{c}$ for the DC power consumption, one can estimate the power consumption, the complex output voltage, and consequently the gain of the amplifier for all $(v_{\mathrm{in}}, V_{\mathrm{gg}})$ pairs. Figure 5.2 demonstrates good agreement between the modulated and CW measurements of the PA, as well as with the model derived from the CW measurements. In this particular instance, the model employs four coefficient terms for v_{in} and three terms for V_{gg} (i.e., $P = 4$, $Q = 3$ in (5.2)).

5.3 Optimum Dynamic Gate Bias Trajectories

To optimize the dynamic gate bias voltage, the function f_{bias} maps the complex baseband voltage $v_{\mathrm{in}}(t)$ to the real dynamic gate signal, such that $V_{\mathrm{gg}}(t) = f_{\mathrm{bias}}(v_{\mathrm{in}}(t))$. also shown in figure 5.1 The expression for f_{bias} varies depending on the specific use case and optimization goal. Therefore, in this section, we describe our optimization objectives and define f_{bias} accordingly.

In our initial study [Paper D], we constructed f_{bias} by generating a look-up table from the V_{gg} and v_{in} pairs that yielded the maximum PAE for each output power level achievable by the PA. This approach ensured the most efficient operation of the PA across its dynamic range during CW operation. However, this method was impractical for telecommunications applications due to two main limitations. First, the look-up table required fitting to an excessively high-order polynomial, making it difficult to effectively drive the gate bias terminal of the amplifier, as the gate drive signal's bandwidth increases with the

Figure 5.2: Gain of an E-Band amplifier operating at 80 GHz. Measurements were performed using CW signals, a 62.5 MHz QAM16 signal, and a model based on the CW measurements.

order of f_{bias}. Second, the resulting gate drive caused significantly nonlinear amplification. The PA driven with such dynamic gate bias profiles fail to comply with spectral emission requirements without additional linearization. Therefore, in [Paper C], we aimed to find band-limited dynamic gate bias profiles that improve the energy efficiency of the amplifier without requiring additional linearization.

The bandwidth of the dynamic gate bias signal can be limited using the Power Envelope Tracking (PET) method described in [99]. If f_{bias} is selected such that it consists solely of even-order powers of the magnitude of $V_{\text{in}}(t)$, then the resulting real signal exhibits a bandwidth of $BW \times n$, where n is the greatest even power and BW is the bandwidth of the complex baseband input signal. In this work, we utilized only the second-order term to minimize the bandwidth at the gate terminal of the amplifier. In other words, we select

$$V_{\text{gg}}(t) = C_2'|v_{\text{in}}(t)|^2 + C_1. \tag{5.6}$$

Assuming a real constant input impedance, this equation can be rewritten in terms of the instantaneous RF power, $P_{\text{inst}}(t)$, by modifying the coefficient as follows:

$$V_{\text{gg}}(t) = C_2 P_{\text{inst}}(t) + C_1. \tag{5.7}$$

In (5.7), $V_{\text{gg}}(t)$ tracks the instantaneous power with a slope of C_2 and an offset of C_1, thereby providing a linear mapping between the instantaneous RF power and the dynamic gate bias voltage. Consequently, the problem simplifies to finding the most suitable pair of C_1 and C_2 for data transmission. To achieve this, we incorporated the European spectral emission mask requirements as outlined in ETSI EN 302 217-2 [18]. We identify the optimal pair of C_1 and C_2 that maximizes the performance figures of the PA at the maximum drive

level where the output spectrum still complies with the spectral emission mask requiremetn.

Shown in Figure 5.3, a fixed stream of bits is modulated using a Quadrature Amplitude Modulation (QAM) constellation with a modulation order M and filtered with a Root Raised Cosine (RRC) filter having a roll-off factor $\alpha_{\mathrm{RRC}} = 0.25$. The coefficients C_1 and C_2 are set for testing, and $V_{\mathrm{gg}}(t)$ is calculated accordingly. The modulated signal is generated, and the corresponding power $\overline{P_{\mathrm{out}}}$ is determined. The modulated and filtered waveform, as well as $V_{\mathrm{gg}}(t)$, are scaled such that the resulting average output power of the DUT becomes $\overline{P_{\mathrm{out}}}$ when the DUT is driven with these signals. The DUT or its behavioral model is then driven with the modulated signal and the corresponding dynamic gate bias, after which the output spectrum of the DUT is captured. If the output spectrum exceeds the spectral emission mask, the drive level is reduced; otherwise, it is increased. This process is repeated until the maximum drive level at which the DUT still complies with the spectral emission mask requirements is reached. At that drive level, the performance metrics of the amplifier, such as the average RF output power ($\overline{P_{\mathrm{out}}}$) and the average power-added efficiency ($\overline{\mathrm{PAE}}$), are evaluated. The input to the behavioral models described is the complex baseband equivalent of the RF input; therefore, the modulated and filtered waveform can be directly fed into the model. However, in experiments with actual mm-wave PAs, the filtered and modulated waveform is upconverted to RF frequencies before being delivered to the DUT. Following this algorithm with behavioral models of the PA yields quasi-static simulations, as these models are based on CW measurements and do not capture dynamic nonlinear effects.

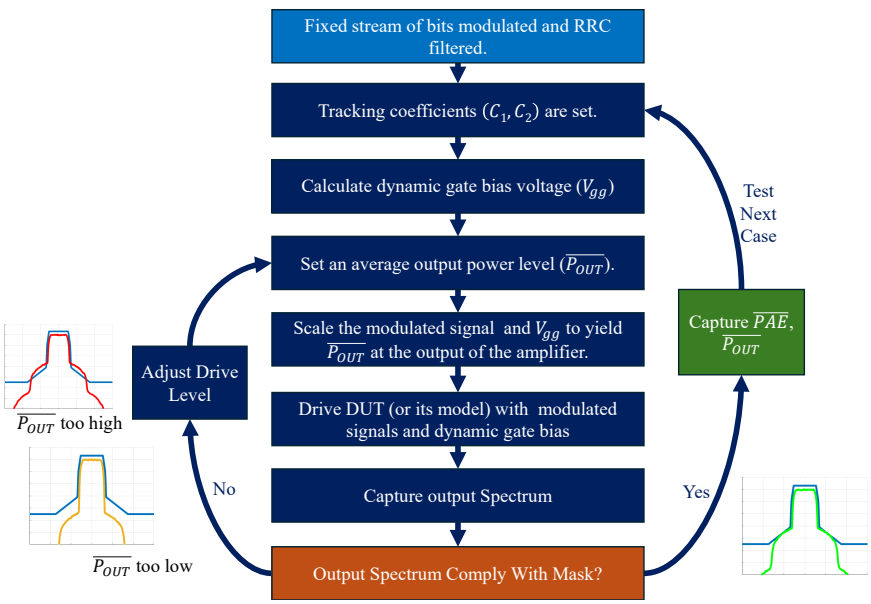


Figure 5.3: Test algorithm for determining the optimum dynamic gate bias coefficients for a specific modulation format and its associated mask.

(a) **(b)**

Figure 5.4: (a) RF output power at the spectrum emission mask limit for various dynamic bias coefficients. (b) Energy efficiency at the spectrum emission mask limit for various dynamic bias coefficients.

In [Paper C], we first used the modeled PA to determine the optimal coefficients C_1 and C_2, and then observed the improvement they yielded. To calculate $P_{\text{inst}}(t)$ in (5.7) , we first computed the instantaneous input power to the PA as

$$P_{\text{in}}(t) = \frac{|v_{\text{in}}(t)|^2}{2Z_0},$$

and then scaled it by the average gain of the amplifier to define $P_{\text{inst}}(t) = P_{\text{in}}(t)\,\overline{\text{Gain}}$. In this equation, $P_{\text{inst}}(t)$ represents the hypothetical linear instantaneous output power of the amplifier. This approach enables us to compare different cases and devices with varying gains and to implement a Digital Predistortion (DPD) on the system, as will be presented in the next section.

Figure 5.4 presents the results obtained using the modeled PA for a modulated signal with a QAM16 constellation. Considering that the $C_1 = 0$ line corresponds to a static bias, Figure 5.4(a) shows that certain dynamic gate bias profiles yield higher RF output power at the spectral emission mask limit compared to the static case. Moreover, a similar trend is observed for energy efficiency. These findings suggest that dynamically gate-biased mm-wave PAs can operate with improved performance under spectral mask requirements. The promising simulation results are further validated in a measurement setup that emulates a realistic data transmission scenario, as described in the following section.

5.4 Modulated Signal Test-Bed for Millimeter-Wave PAs

To validate the results obtained in the previous section, an experimental setup mimicking a realistic E-Band transmitter was constructed using commercial backhaul components, as shown in Figure 5.5. The setup consists of an Arbitrary Waveform Generator (AWG) to generate the baseband signal in IQ components. The IQ signal is then upconverted to RF using a up converting

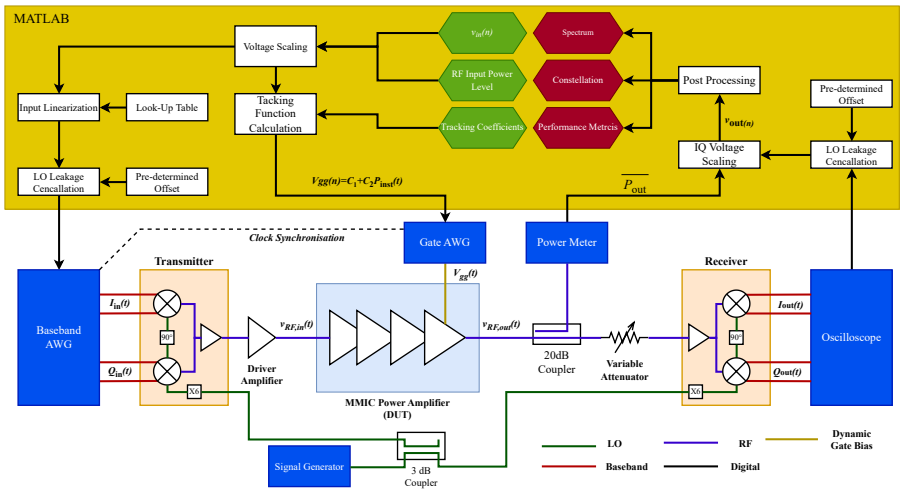


Figure 5.5: Block diagram of the modulated signal measurement setup.

transmitter (TX) that incorporates an internal LO multiplier of six times. We set the RF carrier frequency to 80 GHz for this work due to the availability of the components. An amplifier is inserted between the TX and the DUT MMIC to allow it to reach compression the DUT while keeping the TX operating linearly. The gate bias terminal at the final stage of the DUT MMIC is connected to another AWG, which is clock-synchronized and generates the dynamic gate bias signal. The delays between the AWGs are adjusted to ensure that the signals from both units reach the DUT simultaneously.

To capture the time-domain IQ signal, a downconverting receiver (RX) is used at the output of the DUT. The RX is fed by the same LO source used for the TX. The IQ readings from the RX are then scaled to the output level of the DUT using average power measurements from a power meter. Consequently, the baseband equivalent time-domain complex output of the DUT PA, denoted as $v_{\text{out}}(t)$, is constructed. This signal is subsequently used to calculate the constellation, spectrum, and performance metrics such as $\overline{PAE}$ with the help of power consumption information collected from the DC supplies (which are not shown in the figure).

Nonidealities, such as LO leakage at the TX and RX, are compensated for using look-up tables obtained during characterization steps prior to the actual measurements. Similarly, an additional linearization block is implemented at the input to improve the linearity of the TX and driver using third-order linearization terms.

These steps allowed us to linearly drive a mm-wave PA with a modulated signal, as well as to drive its last stage gate terminal with a dynamic gate bias that tracks the instantaneous power. The algorithm portrayed in Figure 5.3 is repeated in the measurement setup using a 16QAM modulation scheme and, as shown in Figure 5.6, we achieved very similar results to those obtained via simulations presented in the previous section. Both the measurements and

(a) **(b)**

Figure 5.6: (a) Measured RF output power at the spectrum emission mask limit for various dynamic bias coefficients. (b) Measured Energy efficiency at the spectrum emission mask limit for various dynamic bias coefficients.

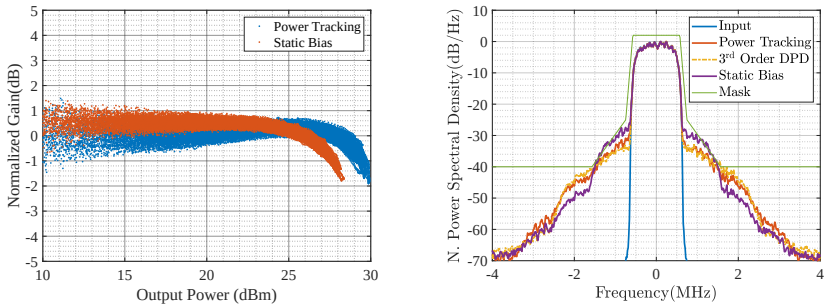
simulations agree that the optimal drive profile for PAs is not a static bias but rather a dynamic gate bias.

Table 5.1 shows the average energy efficiency, output power, and gain of the amplifier at the level where the output spectrum reaches the spectral emission mask limit. The linear power tracking approach yielded improved average energy efficiency and output power compared to the static bias cases—even those that provided the best output power and energy efficiency among the static bias scenarios. In addition, to compare linear power tracking with another linearization method, we re-measured the static bias case that produced the highest RF output power using a third-order DPD. The measurements indicate that dynamic gate biasing outperformed that case as well in terms of average output power and energy efficiency. However, linear power tracking does sacrifice some average gain compared to the static bias case that yielded the highest RF output power with and without DPD.

Table 5.1: Measurement results at spectrum emission mask limit

	C_1	C_2	$\overline{PAE}$(%)	$\overline{P_{\text{out}}}$(dBm)	$\overline{\text{Gain}}$ (dB)
Best $\overline{P_{\text{out}}}$ Static	-0.53	0	4.8	24.1	14.0
Best $\overline{PAE}$ Static	-0.84	0	4.9	23.4	12.1
Linear Power Tracking	-0.78	0.38	7.4	25.8	13.2
3^{rd} Order DPD	-0.53	0	5.5	24.8	13.3

Figure 5.7(a) shows the AM-AM response of the linear PET PA as well as that of the PA statically biased at the gate bias voltage that yields the maximum RF output power. The figure shows that the linear PET case exhibits an expanding gain characteristic at low output power levels, which is expected since the gate bias voltage is low. In this region, the PA consumes less power compared to the statically biased case. However, the figure also shows that the



(a) **(b)**

Figure 5.7: (a) Comparison of measured AM-AM responses for linear PET gate-biased and static gate-biased amplifiers. (b) Output spectrum of the amplifier at an output power level of 25.2 dBm.

linear PET PA compresses at higher output power levels. In summary, the PA operates more efficiently at low drive levels but only reaches an operating region that yields greater output power when the drive level is high.

Figure 5.7(b) shows the output spectrum of the static bias case that yields the highest RF output power, both with and without DPD, as well as that of the linear PET gate-biased amplifier. The figure shows that the linear PET suppresses the undesired third order intermodulation products similarly to DPD. These results demonstrate that dynamic gate-biased amplifiers have a strong capability to improve both output power and energy efficiency while effectively suppressing undesired third order intermodulation distortion, similar to the performance achieved with DPD.

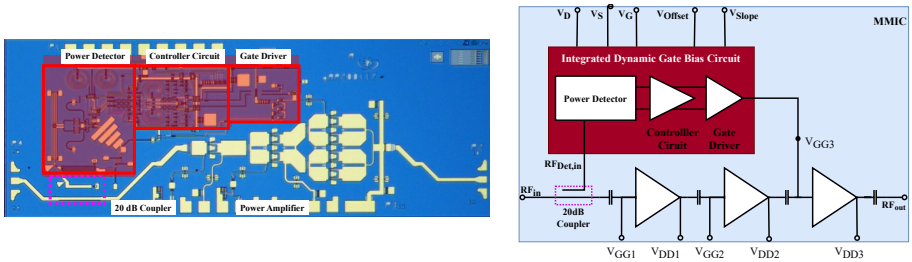
5.5 MMIC Integration of Dynamic Gate Biasing

One of the most impractical and costly aspects of the study described above is the need to use an additional AWG and synchronize it with the other one. To overcome this issue, and motivated by the promising results obtained, we next integrated this idea into a single MMIC described in [Paper B]. Figure 5.8 shows the layout and block diagram of the implementation.

To generate the $P_{\text{inst}}(t)$ term in (5.7), we utilized a power detector whose output is proportional to the instantaneous input power to the PA. The instantaneous power is obtained using a single-balanced differential mixer that self-mixes the RF input signal with itself. The RF input signal is given in (5.1). The ideal second-order mixing process for that signal can be expressed as

$$v^2_{\text{RF,in}}(t) = \frac{A^2_{\text{in}}(t)}{2}\Big[1 + \cos\big(2\big(\omega_c t + \phi_{\text{in}}(t)\big)\big)\Big].$$

In the output of the detector, the cosine term is not observed as it is a high-frequency component that is filtered out in the MMIC. Consequently, the



(a) **(b)**

Figure 5.8: (a) Chip photograph (b) block diagram of the dynamic gate biased PA .

output of the power detector is proportional to the square of the amplitude, which in turn is proportional to the instantaneous power:

$$v_{\mathrm{Det,out}}(t) \propto A_{\mathrm{in}}^2(t) \propto P_{\mathrm{inst}}(t).$$

The instantaneous power to the PA is probed using a 20 dB coupler, as shown in Figure 5.8.

To have control over C_1 and C_2 (i.e., the offset and slope with respect to the instantaneous power in (5.7)), the output of the detector is connected to a differential variable gain amplifier with common-mode voltage controls, as shown in Figure 5.9(a). The V_{Slope} control adjusts the slope term by modifying the gain of the variable gain amplifier, and V_{Offset} controls the common-mode voltage level of the variable gain amplifier, which translates into an offset voltage.

Finally, the generated and shaped control signal is delivered to the gate bias terminal of the main amplifier, which is capacitively loaded and constitutes the main limiting factor. The total capacitive loading at the gate bias terminal was measured to be 1.5 pF. We implemented a common-drain driver stage with 2×40 μm transistors and a bias current density of 145 mA/mm, as shown in Figure 5.9(b). This configuration sets the impedance seen from the amplifier's gate bias terminal to $1/g_m = 19.2\ \Omega$. This setting yields a theoretical 3 dB bandwidth of 5.5 GHz.

Both the simulations and measurements agree that the power detector, controller circuit, and gate driver consume a total of 349 mW of energy. This value is distributed among the detector, controller, and gate driver as 56 mW, 189 mW, and 104 mW, respectively.

Figure 5.10 shows the gate bias voltage realized at the final-stage gate bias terminal of the amplifier. The gate bias voltage was measured by sweeping the RF input power to the amplifier and capturing the drain current of the last stage. The collected current was then mapped to the corresponding gate bias voltage. The results demonstrate that the control voltage effectively adjusts both the slope of the gate bias voltage relative to the RF input power and the offset. Furthermore, the figure also shows the linear relationship between

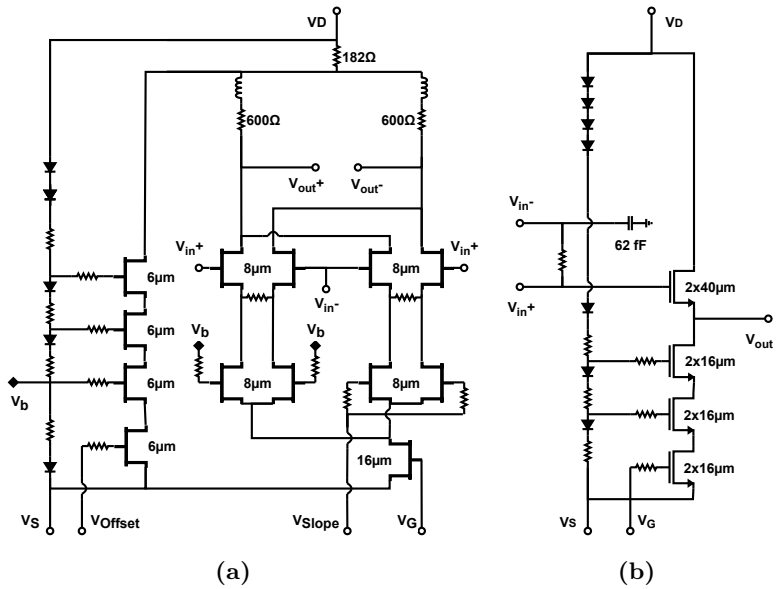


Figure 5.9: Schematic representation of (a) controller circuit and (b) gate driver.

the RF input power and the gate bias voltage. In other words, the gate bias voltage of the final stage of this amplifier tracks the instantaneous input power of the other PA.

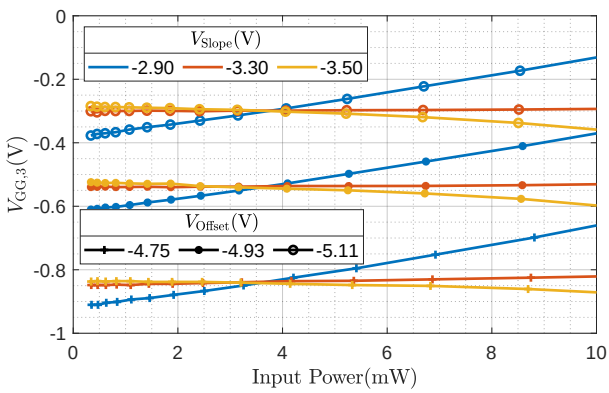
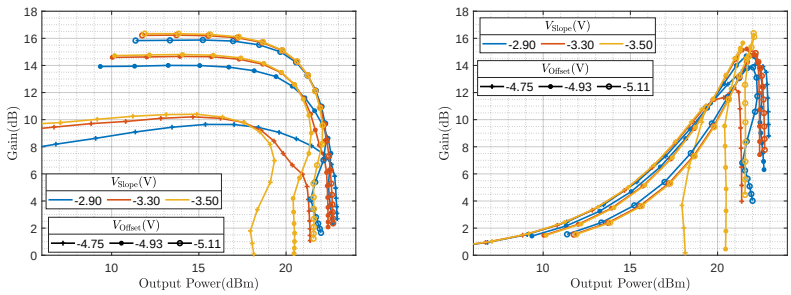


Figure 5.10: Measured dynamic gate bias voltages for different V_{Slope} and V_{Offset} settings against RF input power.

Figure 5.11 shows the gain and energy efficiency of the amplifier for various V_{Slope} and V_{Offset} settings. Figure 5.11(a) demonstrates that V_{Offset} successfully modulates the gain level of the amplifier. For example, when $V_{\mathrm{Offset}} = -4.75\mathrm{V}$, the amplifier exhibits expanding gain curves, which implies class-C operation, whereas when $V_{\mathrm{Offset}} = -5.11\mathrm{V}$, the gain is higher and non-expanding, in-

dicating class A-AB operation. This demonstrates that the V_{Offset} setting can effectively modulate the amplifier's operating point. Moreover, while $V_{\text{Slope}} = -2.90\text{V}$ expands and boosts the output power level at compression, $V_{\text{Slope}} = -3.50\text{V}$ decreases the output compression point. In parallel, this setting also modulates the power consumption of the amplifier, which is reflected in its energy efficiency, as shown in Figure 5.11.



(a) **(b)**

Figure 5.11: (a) Gain and (b) energy efficiency of the amplifier for various V_{Slope} and V_{Offset} settings.

To demonstrate the effectiveness of the implementation, a set of behavioral models of the measured amplifier was created for various V_{Slope} and V_{Offset} settings. The models were tested using the algorithm shown in Figure 5.3; however, instead of evaluating the polynomial coefficients C_1 and C_2, the corresponding voltages V_{Offset} and V_{Slope} were examined. The tests were repeated for various QAM signals with different numbers of symbols, yielding different PAPR values.

The results are compiled in Table 5.2. The table separately shows the PAE of the dynamic bias configuration expressed both as the overall efficiency, ($\overline{PAE_S}$), which includes the power consumption of the additional circuits other than the PA, and as the efficiency of the PA only, ($\overline{PAE_{PA}}$). The table indicates that, especially for lower modulation orders such as 4QAM and 16QAM, the average RF output power at the spectrum emission mask limit is increased by 1.6 dB and 0.4 dB, respectively, and the energy efficiency of the PA is also increased by up to 22% for these modulation orders. With increasing modulation orders, we observed less improvements. The comparison of the output spectra for dynamic and static bias conditions at identical RF output power levels is presented in Figure 5.12. The figure clearly illustrates that the static bias condition violates the spectral emission mask requirements, whereas the dynamic bias condition remains compliant. This demonstrates that dynamic gate biasing effectively reduces spectral regrowth. This improvement highlights the advantage of dynamically adjusting gate bias voltages in response to instantaneous input power, thereby ensuring compliance with spectral emission standards without sacrificing output power performance. This observation also aligns with the experiments done using the E-band amplifier presented in te previous section.

Although the integration manages to improve the energy efficiency and RF

Table 5.2: Performance parameters at spectrum emission mask limit of the integrated dynamic gate-biased PA for various dynamic bias settings.

		Dynamic Bias					Static Bias		
	PAPR	V_{Offset}	V_{Slope}	$\overline{PAE_S}$	$\overline{PAE_{PA}}$	$\overline{P_{out}}$	V_{GG3}	$\overline{PAE}$	$\overline{P_{out}}$
4QAM	4.9	-4.75	-2.90	8.54	12.53	20.81	-0.44	10.23	19.14
16QAM	7.3	-4.84	-2.90	4.71	7.52	17.06	-0.44	6.16	16.63
64QAM	7.6	-4.98	-2.93	3.14	4.74	15.47	-0.51	4.39	15.45
256QAM	7.9	-5.07	-3.05	2.27	3.21	14.54	-0.31	3.09	14.30

PAPR is in dB; V_{Offset},V_{Slope}, V_{GG3} in V; $\overline{PAE_S}$, $\overline{PAE_{PA}}$ in % ; $\overline{P_{out}}$ in dBm;

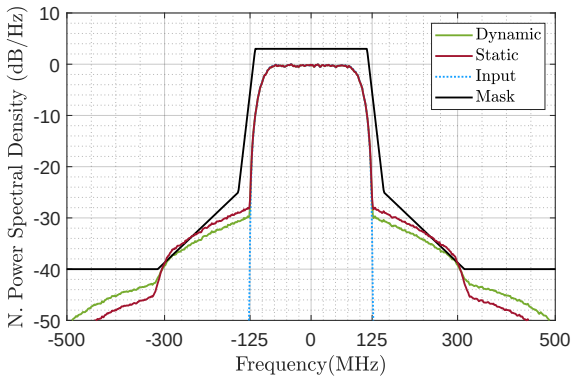


Figure 5.12: Output spectrum of the integrated dynamic gate-biased PA for the best dynamic bias and static bias cases at an average RF output power level of 17.1 dBm for both cases. The figure is constructed using quasi-static simulations for 16QAM , based on CW measurements of the integrated dynamic gate-biased PA.

output power of the PA (excluding the power consumption of the linearizer) at spectral emission mask limit, the overall power consumption increases. This can be addressed by simplifying the power detector or by using an amplifier with a greater output periphery, where the overall detector power consumption contribution decreases. Overall, we present the first integration of a dynamic gate-biased amplifier in an III-V pHEMT process operating at over 100 GHz.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis focused on the design and implementation of energy-efficient PAs for mm-wave frequencies, specifically targeting the 100 GHz to 114 GHz frequency range. The motivation behind this work stems from the increasing demand for high-data-rate wireless communication systems, which necessitate efficient RF power generation at high frequencies. The work presented in this thesis addresses the challenges outlined in the introduction: achieving high-power, energy-efficient, and linear PAs operating beyond 100 GHz.

One of the achievements of this thesis is the development of a balanced PA using a commercial 0.1 µm GaAs pHEMT process. Measurements demonstrate that the design exhibits competitive performance relative to state-of-the-art designs. This amplifier achieves a favorable combination of peak efficiency, gain, and saturated output power, enabled by low-loss power combiners and optimized matching networks. Exploring the potential of commercial semiconductor technologies with affordable costs for the telecommunications market is important to accelerate their deployment.

To extend these achievements, an NDPA was implemented using the same process. While this design exhibited reasonably high gain, the skew in frequency resulted in an overall amplifier performance that did not meet expectations. These deviations highlight the challenges of accurately modeling device behavior beyond 100 GHz, reinforcing the need for improved transistor models tailored for high-frequency operation.

Additionally, this work explored the potential of dynamic gate biasing as a means to enhance the energy efficiency and linearity of PAs. Experimental validation on an 80 GHz PA demonstrated improvements in both energy efficiency and linearity, outperforming a DPD implementation with the same number of coefficients. This demonstrates the effectiveness of dynamic gate biasing as both a linearization and energy efficiency enhancement technique.

Furthermore, a circuit implementation of dynamic gate biasing was integrated with a PA and manufactured using the 0.1 µm GaAs pHEMT process. The design highlights opportunities for integrated implementations within the GaAs pHEMT process, showcasing its potential for advanced PA architectures.

Overall, this thesis contributes to addressing the challenges of energy-efficient power amplification for mm-wave applications by demonstrating innovative MMIC PA implementations. In addition, some of the implementations in this thesis introduce techniques to improve PA performance when operating with telecommunication signals characterized by large PAPR. These findings contribute to the advancement of modern telecommunication systems by enhancing efficiency, linearity, and overall PA performance.

6.2 Future Work

Building upon the findings of this thesis, several promising research directions can be explored to further improve the performance of mm-wave PAs.

One key research direction is the efficient combination of multiple amplifier branches. The existing balanced amplifier employs an output periphery of 960 µm. Extending this using an NDPA structure could enable an increased output periphery of 2400 µm, providing RF output power beyond 1 W in simulations. Addressing the discrepancies between simulations and measurements in power combiner networks and improving transistor models is crucial for achieving this performance in practice. Therefore, iterating this design with more accurate transistor models and enhanced EM simulations for passive components represents a promising future direction.

To improve bandwidth and reduce the physical dimensions of amplifiers while maintaining the same output power, stacked amplifier architectures offer a viable solution by increasing output impedance and energy density. Investigating the limitations and potential advantages of this structure for the 0.1 µm GaAs pHEMT process at frequencies beyond 100 GHz, as well as integrating it with other power-combining methods, represents another important area for future research.

Another promising direction is the development of a dynamic gate bias circuit with higher-order power tracking capability beyond a purely linear term. By incorporating higher-order tracking, the energy efficiency and linearity improvements observed for lower-order modulation formats such as 4QAM and 16QAM could also be extended to higher-order formats like 64QAM and 256QAM. Investigating whether this approach effectively mitigates the degradation in efficiency and linearity at higher modulation orders is an important research avenue. Additionally, simplifying the power detector architecture could lead to PA designs with both reduced energy consumption and improved linearity.

Finally, leveraging the experience gained from dynamically adjusting the operating point of the amplifier, future research could explore the design of sequential amplifiers with dynamically biased auxiliary branches. The auxiliary branch could be selectively activated or deactivated based on the instantaneous

input power to the amplifier. This approach has the potential to enhance the amplifier's back-off efficiency, thereby achieving better average energy efficiency when driven by telecommunication signals.

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